Complete 10-Bit and 12-Bit, 25 MHz CCD Signal Processors

Data Sheet **AD9943/AD9944**

FEATURES

25 MSPS correlated double sampler (CDS)
6 dB to 40 dB 10-bit variable gain amplifier (VGA)
Low noise optical black clamp circuit
Preblanking function
10-bit (AD9943), 12-bit (AD9944) 25 MSPS A/D converter
No missing codes guaranteed
3-wire serial digital interface
3 V single-supply operation
Space-saving 32-lead 5 mm × 5 mm LFCSP package

APPLICATIONS

Digital still cameras
Digital video camcorders
PC cameras
Portable CCD imaging devices
CCTV cameras

GENERAL DESCRIPTION

The AD9943/AD9944 are complete analog signal processors for CCD applications. They feature a 25 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The signal chain for the AD9943/AD9944 consists of a correlated double sampler (CDS), a digitally controlled variable gain amplifier (VGA), and a black level clamp. The AD9943 offers 10-bit ADC resolution, while the AD9944 contains a true 12-bit ADC.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input clock polarity, and power-down modes. The AD9943/AD9944 operate from a single 3 V power supply, typically dissipate 79 mW, and are packaged in space-saving 32-lead LFCSP packages.

FUNCTIONAL BLOCK DIAGRAM

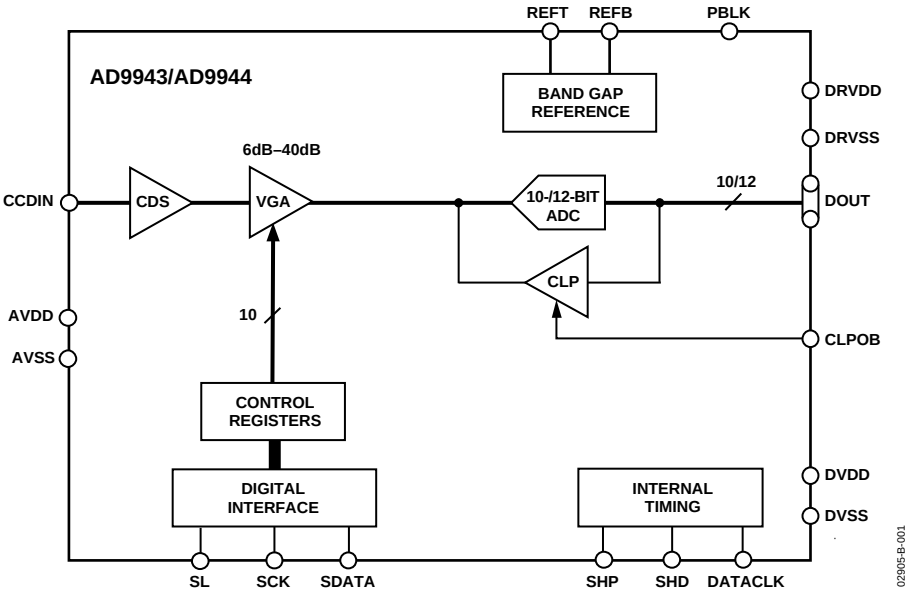


Figure 1. Functional Block Diagram

Rev. C
Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2004–2014 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

3/14—Rev. B to Rev. C

Added Exposed Pad Notation, Figure 2 and Table 6 ... 7
Added Exposed Pad Notation, Figure 3 and Table 7 ... 8
Changes to Figure 17 ... 17
Changes to Figure 18 ... 18
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

5/04—Data Sheet Changed from Rev. A to Rev. B

Updated Format ... Universal
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

5/03—Data Sheet changed from Rev. 0 to Rev. A

Added AD9944 ... Universal
Changes to Features Section ... 1
Updated Ordering Guide ... 5
Replaced TPC 3 ... 9
Added Figure 12 ... 15
Updated Outline Dimensions ... 16

SPECIFICATIONS

GENERAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3 V, f_{SAMP} = 25 MHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−20		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE				
Analog, Digital, Digital Driver	2.7		3.6	V
POWER CONSUMPTION				
Normal Operation		79		mW
Power-Down Mode		150		µW
MAXIMUM CLOCK RATE	25			MHz

DIGITAL SPECIFICATIONS

DRVDD = DVDD = 2.7 V, C_L = 20 pF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I_{OH} = 2 mA	V_{OH}	2.2			V
Low Level Output Voltage, I_{OL} = 2 mA	V_{OL}			0.5	V

AD9943 SYSTEM SPECIFICATIONS

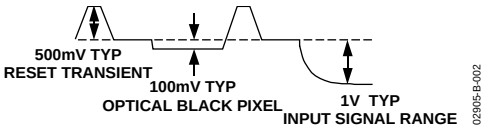
T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3 V, f_{SAMP} = 25 MHz, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions
CDS					
Maximum Input Range before Saturation[1]		1.0		V p-p	
Allowable CCD Reset Transient[1]		500		mV	See input waveform in footnote.
Maximum CCD Black Pixel Amplitude[1]		100		mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Minimum Gain		5.3		dB	See Figure 13 for VGA gain curve.
Maximum Gain	40	41.5		dB	See Variable Gain Amplifier section for VGA gain equation.
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC output.
Minimum Clamp Level		0		LSB	
Maximum Clamp Level		63.75		LSB	

Parameter	Min	Typ	Max	Unit	Conditions
A/D CONVERTER					
Resolution	10			Bits	
Differential Nonlinearity (DNL)		±0.3		LSB	
No Missing Codes		Guaranteed			
Data Output Coding		Straight binary			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
SYSTEM PERFORMANCE					Specifications include entire signal chain.
Gain Range					
Low Gain (VGA Code = 0)		5.3		dB	
Maximum Gain (VGA Code = 1023)	40	41.5		dB	
Gain Accuracy		±1		dB	
Peak Nonlinearity 500 mV Input Signal		0.1		%	12 dB gain applied.
Total Output Noise		0.3		LSB rms	AC grounded input, 6 dB gain applied.
Power Supply Rejection (PSR)		50		dB	Measured with step change on supply.

[1] Input signal characteristics defined as follows:



AD9944 SYSTEM SPECIFICATIONS

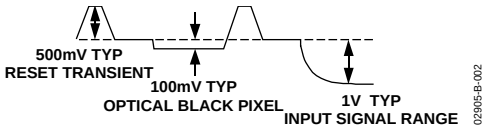
T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3 V, f_{SAMP} = 25 MHz, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Conditions
CDS					
Maximum Input Range before Saturation[1]		1.0		V p-p	
Allowable CCD Reset Transient[1]		500		mV	See input waveform in footnote.
Maximum CCD Black Pixel Amplitude[1]		100		mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Minimum Gain		5.3		dB	See Figure 13 for VGA gain curve.
Maximum Gain	40	41.5		dB	See Variable Gain Amplifier section for VGA gain equation.
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC output.
Minimum Clamp Level		0		LSB	
Maximum Clamp Level		255		LSB	
A/D CONVERTER					
Resolution	12			Bits	
Differential Nonlinearity (DNL)		±0.4		LSB	
No Missing Codes		Guaranteed			
Data Output Coding		Straight binary			
Full-Scale Input Voltage		2.0		V	

Parameter	Min	Typ	Max	Unit	Conditions
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
SYSTEM PERFORMANCE					Specifications include entire signal chain.
Gain Range					
Low Gain (VGA Code = 0)		5.3		dB	
Maximum Gain (VGA Code = 1023)	40	41.5		dB	
Gain Accuracy		±1		dB	
Peak Nonlinearity 500 mV Input Signal		0.1		%	12 dB gain applied.
Total Output Noise		0.9		LSB rms	AC grounded input, 6 dB gain applied.
Power Supply Rejection (PSR)		50		dB	Measured with step change on supply.

[1] Input signal characteristics defined as follows:



TIMING SPECIFICATIONS

C_L = 20 pF, f_{SAMP} = 25 MHz. See CCD-mode timing in Figure 14 and Figure 15, and serial timing in Figure 10 and Figure 11.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SAMPLE CLOCKS					
DATACLK, SHP, SHD Clock Period	t_{CONV}	40			ns
DATACLK High/Low Pulse Width	t_{ADC}	16	20		ns
SHP Pulse Width	t_{SHP}		10		ns
SHD Pulse Width	t_{SHD}		10		ns
CLPOB Pulse Width[1]	t_{COB}	2	20		Pixels
SHP Rising Edge to SHD Falling Edge	t_{S1}		10		ns
SHP Rising Edge to SHD Rising Edge	t_{S2}	16	20		ns
Internal Clock Delay	t_{ID}		3.0		ns
DATA OUTPUTS					
Output Delay	t_{OD}		9.5		ns
Pipeline Delay			9		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns

[1] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter (With Respect To)	Min	Max	Unit
AVDD (AVSS)	−0.3	+3.9	V
DVDD (DVSS)	−0.3	+3.9	V
DRVDD (DRVSS)	−0.3	+3.9	V
Digital Outputs (DRVSS)	−0.3	DRVDD + 0.3	V
SHP, SHD, DATACLK (DVSS)	−0.3	DVDD + 0.3	V
CLPOB, PBLK (DVSS)	−0.3	DVDD + 0.3	V
SCK, SL, SDATA DVSS (AVSS)	−0.3	DVDD + 0.3	V
REFT, REFB, CCDIN	−0.3	AVDD + 0.3	V
Junction Temperature		150	°C
Lead Temperature (10 sec)		300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

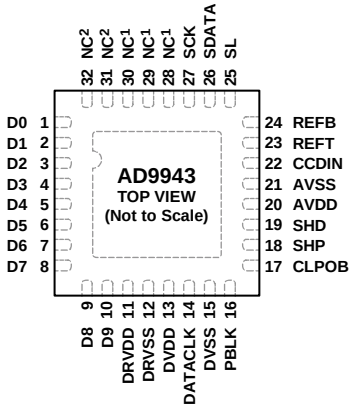
THERMAL RESISTANCE

The thermal resistance of a 32-lead LFCSP package (with the exposed bottom pad soldered to the board GND) is θ_{JA} = 27.7°C/W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



[1]NC = NO CONNECT. INTERNALLY PULLED DOWN. FLOAT OR CONNECT TO GND.
[2]NC = NO CONNECT. INTERNALLY NOT CONNECTED.

NOTES
1. SOLDER THE EXPOSED PAD TO THE GROUND PLANE OF THE PCB.

02905-003

Figure 2. AD9943 Pin Configuration

Table 6. AD9943 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1 to 10	D0 to D9	DO	Digital Data Outputs.
11	DRVDD	P	Digital Output Driver Supply.
12	DRVSS	P	Digital Output Driver Ground.
13	DVDD	P	Digital Supply.
14	DATACLK	DI	Digital Data Output Latch Clock.
15	DVSS	P	Digital Supply Ground.
16	PBLK	DI	Preblanking Clock Input.
17	CLPOB	DI	Black Level Clamp Clock Input.
18	SHP	DI	CDS Sampling Clock for CCD Reference Level.
19	SHD	DI	CDS Sampling Clock for CCD Data Level.
20	AVDD	P	Analog Supply.
21	AVSS	P	Analog Ground.
22	CCDIN	AI	Analog Input for CCD Signal.
23	REFT	AO	A/D Converter Top Reference Voltage Decoupling.
24	REFB	AO	A/D Converter Bottom Reference Voltage Decoupling.
25	SL	DI	Serial Digital Interface Load Pulse.
26	SDATA	DI	Serial Digital Interface Data Input.
27	SCK	DI	Serial Digital Interface Clock Input.
28 to 30	NC	NC	Internally pulled down. Float or connect to GND.
31 to 32	NC	NC	Internally not connected.
	EPAD		Exposed Pad. Solder the exposed pad to the ground plane of the PCB.

[1] Type: AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power, and NC = no connect.

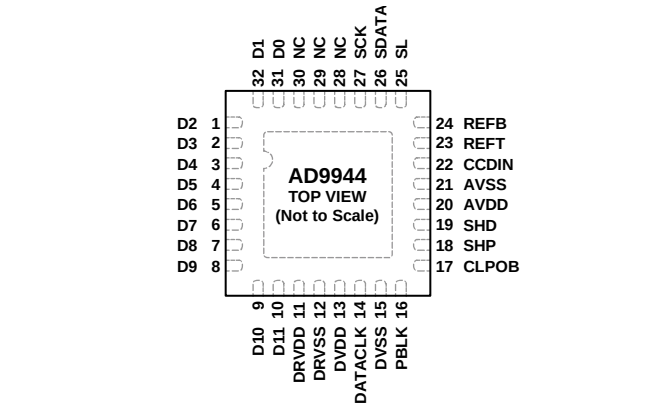


Figure 3. AD9944 Pin Configuration

Table 7. AD9944 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1 to 10	D2 to D11	DO	Digital Data Outputs.
11	DRVDD	P	Digital Output Driver Supply.
12	DRVSS	P	Digital Output Driver Ground.
13	DVDD	P	Digital Supply.
14	DATACLK	DI	Digital Data Output Latch Clock.
15	DVSS	P	Digital Supply Ground.
16	PBLK	DI	Preblanking Clock Input.
17	CLPOB	DI	Black Level Clamp Clock Input.
18	SHP	DI	CDS Sampling Clock for CCD Reference Level.
19	SHD	DI	CDS Sampling Clock for CCD Data Level.
20	AVDD	P	Analog Supply.
21	AVSS	P	Analog Ground.
22	CCDIN	AI	Analog Input for CCD Signal.
23	REFT	AO	A/D Converter Top Reference Voltage Decoupling.
24	REFB	AO	A/D Converter Bottom Reference Voltage Decoupling.
25	SL	DI	Serial Digital Interface Load Pulse.
26	SDATA	DI	Serial Digital Interface Data Input.
27	SCK	DI	Serial Digital Interface Clock Input.
28 to 30	NC	NC	Internally pulled down. Float or connect to GND.
31	D0	DO	Digital Data Output.
32	D1	DO	Digital Data Output.
	EPAD		Exposed Pad. Solder the exposed pad to the ground plane of the PCB.

[1] Type: AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power, and NC = no connect.

TERMINOLOGY

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore every code must have a finite width. No missing codes guaranteed to 10-bit resolution indicates that all 1024 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full-signal chain specification, refers to the peak deviation of the output of the AD9943/AD9944 from a true straight line. The point used as zero scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

$$1\ \text{LSB} = \left(ADC\ Full\ Scale / 2^{N}\ codes\right)$$

where N is the bit resolution of the ADC. For example, 1 LSB of the AD9943 is 1.95 mV.

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. This represents a very high frequency disturbance on the AD9943/AD9944's power supply. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Internal Delay for SHP/SHD

The internal delay (also called aperture delay) is the time delay that occurs from the time a sampling edge is applied to the AD9943/AD9944 until the actual sample of the input signal is held. Both SHP and SHD sample the input signal during the transition from low to high, so the internal delay is measured from each clock's rising edge to the instant the actual internal sample is taken.

EQUIVALENT INPUT CIRCUITS

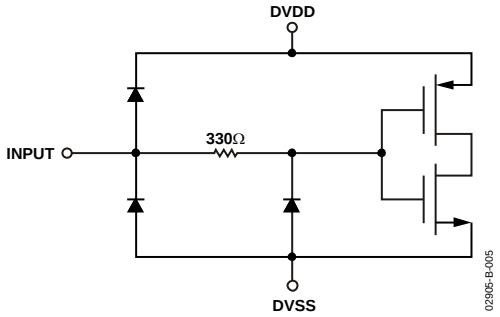


Figure 4. Digital Inputs—SHP, SHD, DATACLK, CLOB, PBLK, SCK, SL

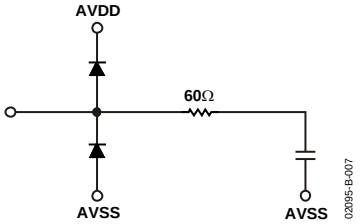


Figure 6. CCDIN (Pin 22)

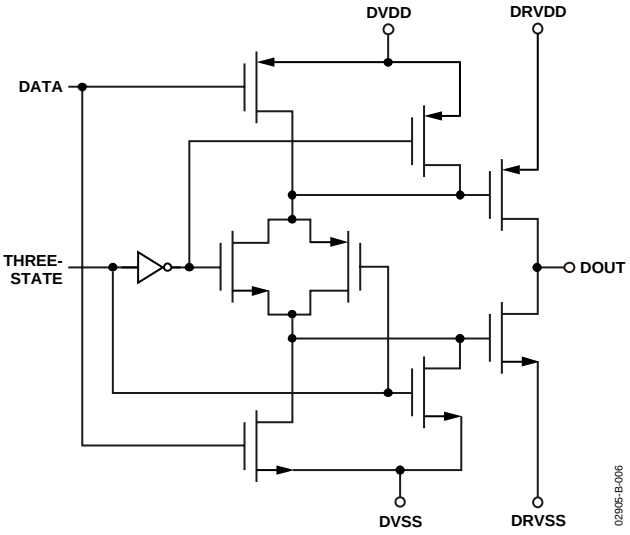


Figure 5. Data Outputs

TYPICAL PERFORMANCE CHARACTERISTICS

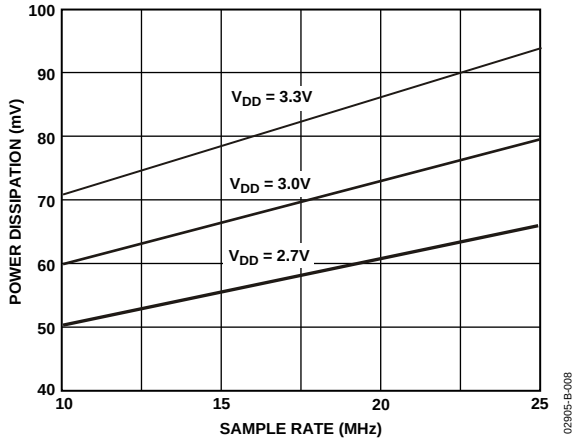


Figure 7. AD9943/AD9944 Power vs. Sample Rate

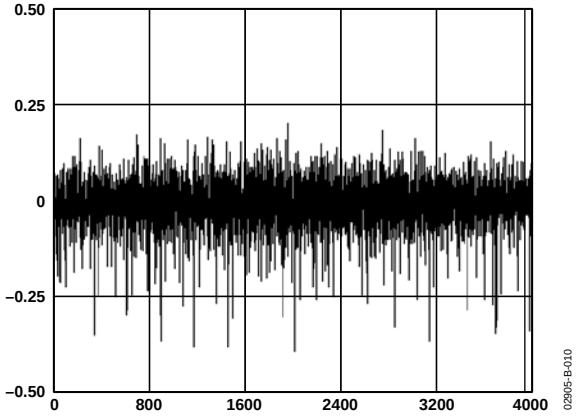


Figure 9. AD9944 Typical DNL Performance

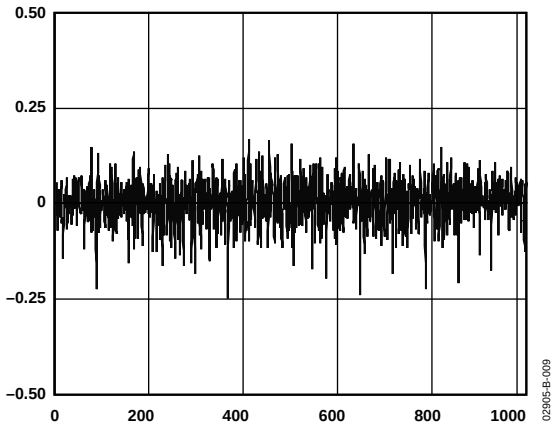


Figure 8. AD9943 Typical DNL Performance

INTERNAL REGISTER MAP

All register values default to 0x000 at power-up except clamp level, which defaults to 128 decimal (AD9943 = 32 LSB clamp level, and AD9944 = 128 LSB clamp level).

Table 8.

Register Name	Address Bits A2	A1	A0	Data Bits	Function
Operation	0	0	0	D0	Software Reset (0 = normal operation, 1 = reset all registers to default).
				D2, D1	Power-Down Modes (00 = normal power, 01 = standby, 10 = total shutdown).
				D3	OB Clamp Disable (0 = clamp on, 1 = clamp off).
				D5, D4	Test Mode. Should always be set to 00.
				D6	PBLK Blanking Level (0 = blank output to zero, 1 = blank to ob clamp level).
				D8, D7	Test Mode 1. Should always be set to 00.
				D11 to D9	Test Mode 2. Should always be set to 000.
Control	0	0	1	D0	SHP/SHD Input Polarity (0 = active low, 1 = active high).
				D1	DATACLK Input Polarity (0 = active low, 1 = active high).
				D2	CLPOB Input Polarity (0 = active low, 1 = active high).
				D3	PBLK Input Polarity (0 = active low, 1 = active high).
				D4	Three-State Data Outputs (0 = outputs active, 1 = outputs three-stated).
				D5	Data Output Latching (0 = latched by DATACLK, 1 = latch is transparent).
				D6	Data Output Coding (0 = binary output, 1 = gray code output).
				D11 to D7	Test Mode. Should always be set to 00000.
Clamp Level	0	1	0	D7 to D0	OB Clamp Level (AD9943: 0 = 0 LSB, 255 = 63.75 LSB, AD9944: 0 = 0 LSB, 255 = 255 LSB).
VGA Gain	0	1	1	D9 to D0	VGA Gain (0 = 6 dB, 1023 = 40 dB).

SERIAL INTERFACE

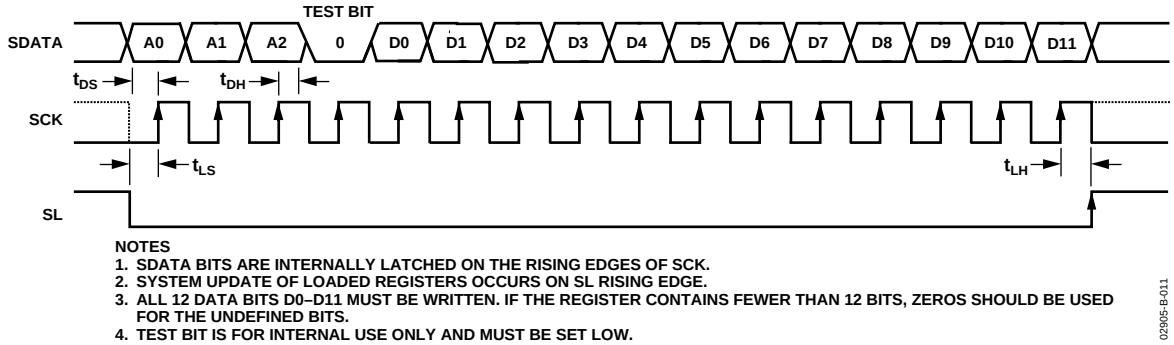


Figure 10. Serial Write Operation

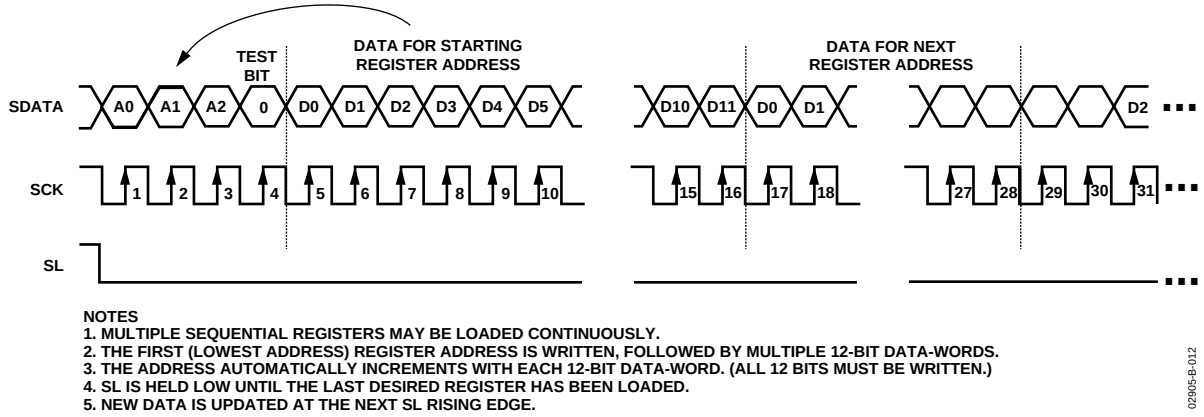


Figure 11. Continuous Serial Write Operation to All Registers

CIRCUIT DESCRIPTION AND OPERATION

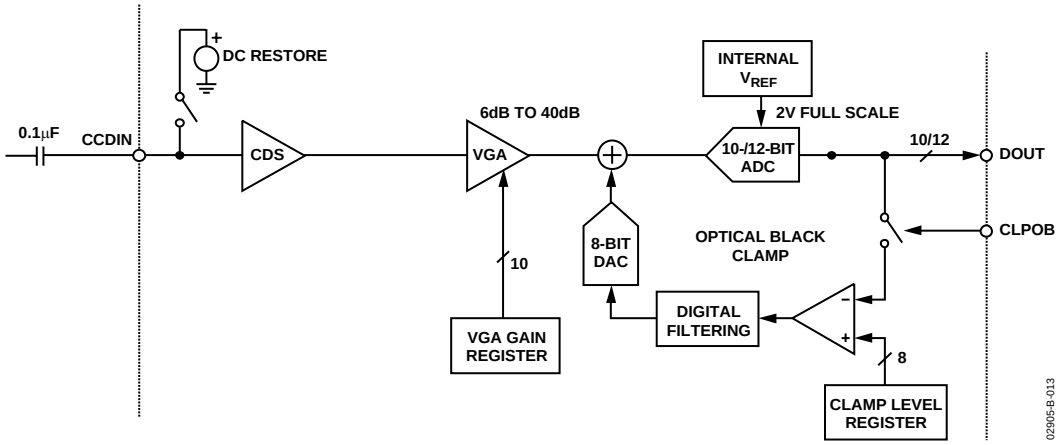


Figure 12. CCD Mode Block Diagram

The AD9943/AD9944 signal processing chain is shown in Figure 12. Each processing step is essential for achieving a high quality image from the raw CCD pixel data.

DC RESTORE

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V, which is compatible with the 3 V single supply of the AD9943/AD9944.

CORRELATED DOUBLE SAMPLER

The CDS circuit samples each CCD pixel twice to extract video information and reject low frequency noise. The timing shown in Figure 14 illustrates how the two CDS clocks, SHP and SHD, are used, respectively, to sample the reference level and data level of the CCD signal. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical for achieving the best performance from the CCD. An internal SHP/SHD delay (t_{ID}) of 3 ns is caused by internal propagation delays.

OPTICAL BLACK CLAMP

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with the fixed black level reference selected by the user in the clamp level register. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the post processing, the optical black clamping for the AD9943/AD9944 may be disabled using Bit D3 in the operation register. Refer to Table 8 and Figure 10 and Figure 11.

When the loop is disabled, the clamp level register may still be used to provide programmable offset adjustment. Horizontal timing is shown in Figure 15. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse be used during valid CCD dark pixels. The CLPOB pulse should be a minimum of 20 pixels wide to minimize clamp noise. Shorter pulse widths may be used, but clamp noise may increase and the loop's ability to track low frequency variations in the black level is reduced.

A/D CONVERTER

The ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range. The ADC uses a pipelined architecture with a 2 V full-scale input for low noise performance.

VARIABLE GAIN AMPLIFIER

The VGA stage provides a gain range of 6 dB to 40 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. A plot of the VGA gain curve is shown in Figure 13.

$$VGA\ Gain(\text{dB}) = (VGA\ Code \times 0.035\ \text{dB}) + 5.3\ \text{dB}$$

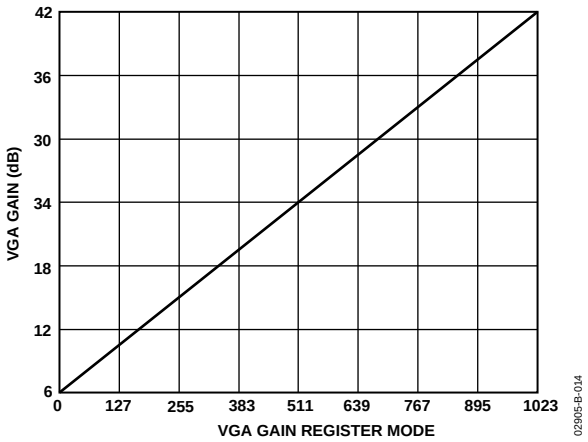


Figure 13. VGA Gain Curve

CCD MODE TIMING

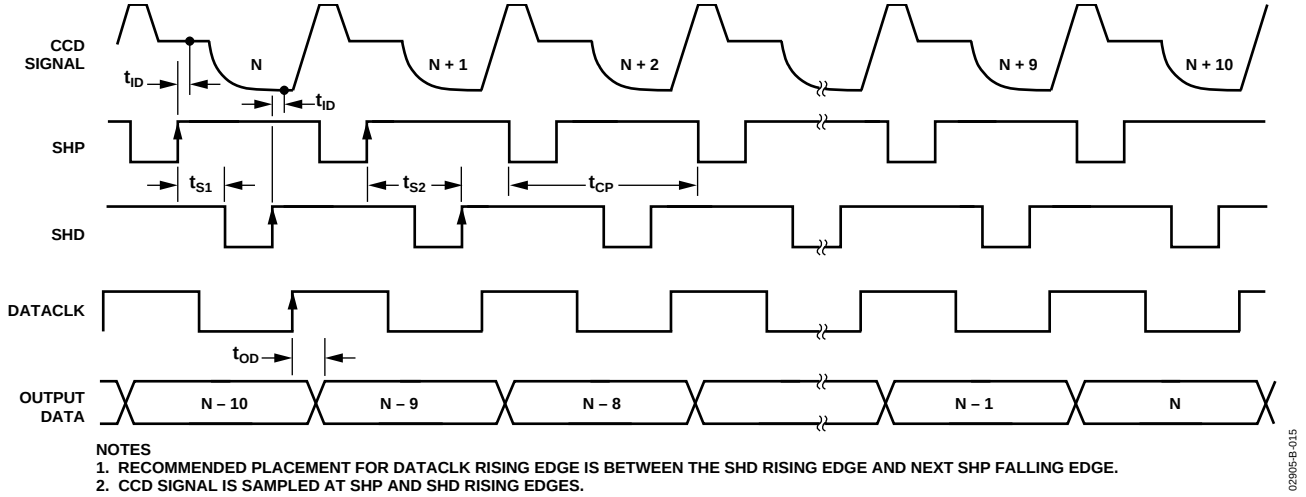


Figure 14. CCD Mode Timing

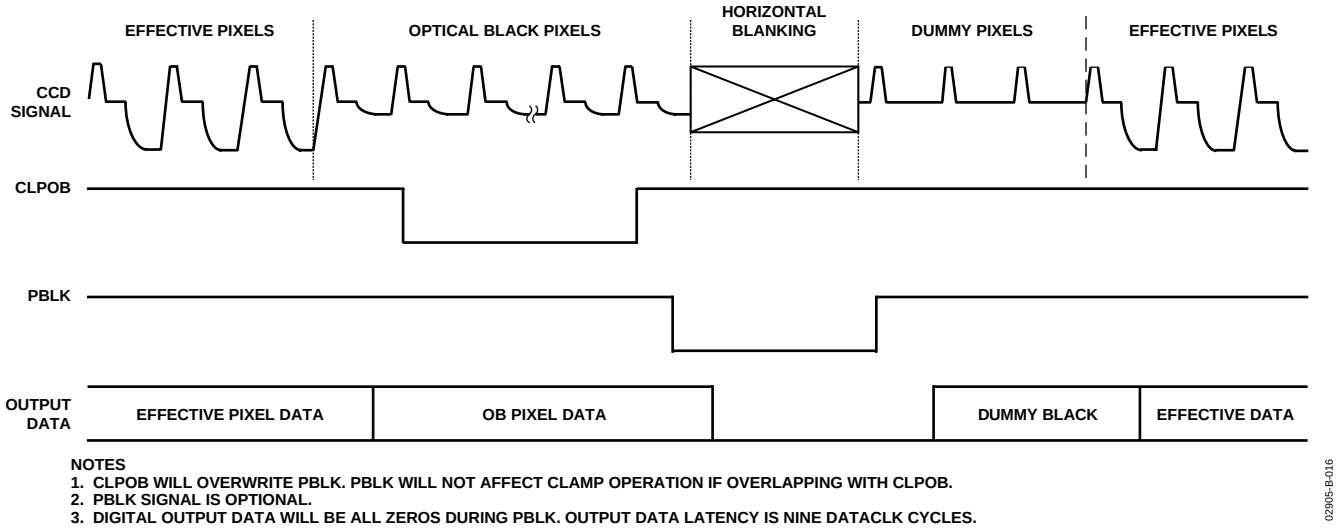


Figure 15. Typical CCD Mode Line Clamp Timing

APPLICATIONS INFORMATION

The AD9943/AD9944 are complete analog front end (AFE) products for digital still camera and camcorder applications. As shown in Figure 12, the CCD image (pixel) data is buffered and sent to the AD9943/AD9944 analog input through a series input capacitor. The AD9943/AD9944 perform the dc restoration, CDS, gain adjustment, black level correction, and analog-to-digital conversion. The AD9943/AD9944's digital output data is then processed by the image processing ASIC. The internal registers of the AD9943/AD9944—used to control gain, offset level, and other functions—are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE.

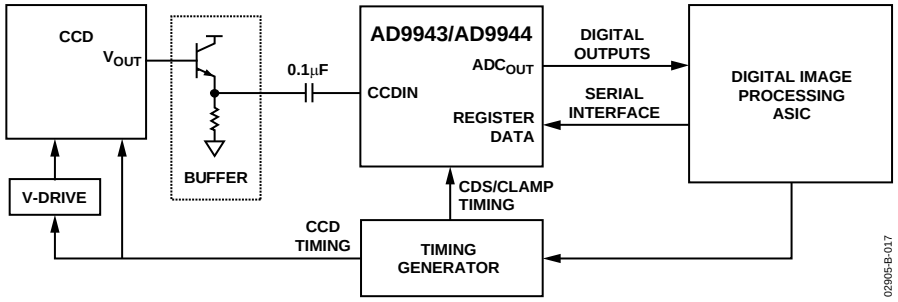


Figure 16. System Applications Diagram

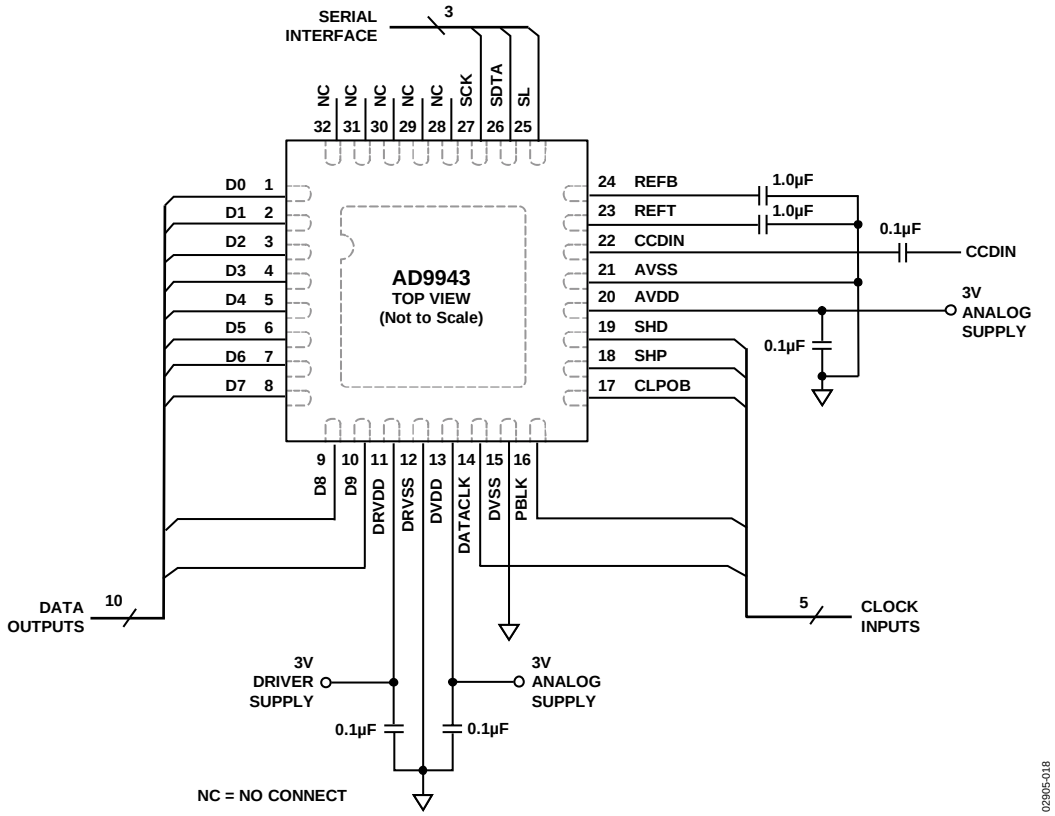


Figure 17. AD9943 Recommended Circuit Configuration for CCD Mode

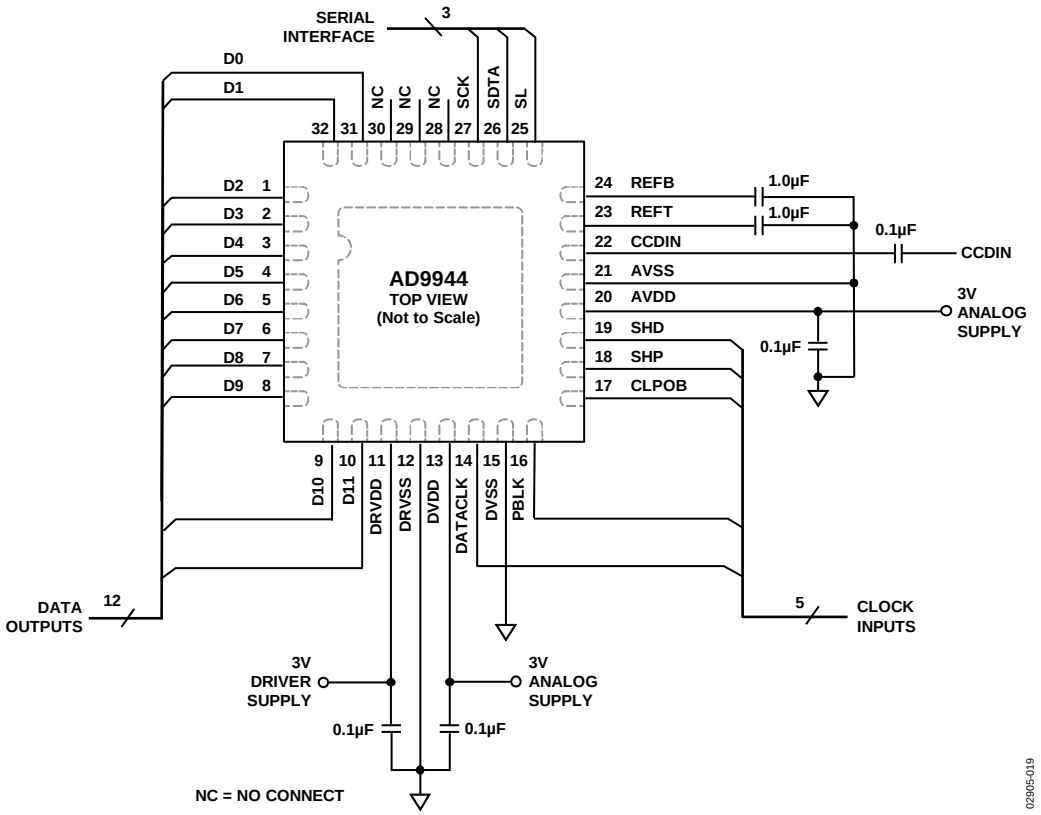


Figure 18. AD9944 Recommended Circuit Configuration for CCD Mode

INTERNAL POWER-ON RESET CIRCUITRY

After power-on, the AD9943/AD9944 automatically reset all internal registers and perform internal calibration procedures. This takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations may occur. However, serial register writes are ignored until the internal reset operation is completed.

GROUNDING AND DECOUPLING RECOMMENDATIONS

As shown in Figure 17 and Figure 18, a single ground plane is recommended for the AD9943/AD9944. This ground plane should be as continuous as possible. This ensures that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the AD9943 and AD9944, but a separate digital driver supply may be used for DRVDD (Pin 11). DRVDD should always be decoupled to DRVSS (Pin 12), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, and reducing digital power dissipation and potential noise coupling. If the digital outputs must drive a load larger than 20 pF, buffering is the recommended method to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help reduce noise.

Note: The exposed pad on the bottom of the AD9943/AD9944 should be soldered to the GND plane of the printed circuit board.

OUTLINE DIMENSIONS

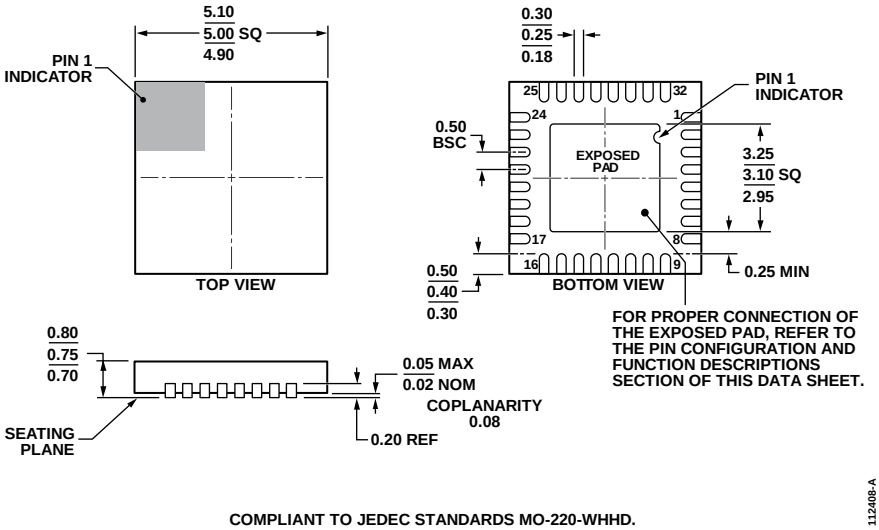


Figure 19. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9943KCPZ	−20°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP-WQ]	CP-32-7
AD9943KCPZRL	−20°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP-WQ]	CP-32-7
AD9944KCPZ	−20°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP-WQ]	CP-32-7
AD9944KCPZRL	−20°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP-WQ]	CP-32-7

[1] Z = RoHS Compliant Part.

NOTES

©2004–2014 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D02905-0-3/14(C)

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А