36Vin to 60Vin Cool-Power ZVS Buck Regulator & LED Driver

Description

The PI354X-00 is a family of high input voltage, wide input range DC-DC ZVS-Buck regulators integrating controller, power switches, and support components all within a high density System-in-Package (SiP). The integration of a high performance Zero-Voltage Switching (ZVS) topology, within the PI354X-00 series, increases point of load performance providing best in class power efficiency. The PI354X-00 requires only an external inductor, two voltage selection resistors and minimal capacitors to form a complete DC-DC switching mode buck regulator.

Device	Output Voltage		Iout Max
	Set	Range	
PI3542-00-LGIZ	2.5V	2.2V to 3.0V	10A
PI3543-00-LGIZ	3.3V	2.6V to 3.6V	10A
PI3545-00-LGIZ	5.0V	4.0V to 5.5V	10A
PI3546-00-LGIZ	12V	6.5V to 14V	9A

Table 1 *- PI354X-00 Portfolio.*

PI354X-00 Family can operate in constant voltage output for typical buck regulation applications in addition to constant current output for LED lighting and battery charging applications.

Features

- High Efficiency HV ZVS-Buck Topology
- Wide input voltage range of 36V to 60V
- Very-Fast transient response
- Constant voltage or constant current operation
- Constant current error amplifier and reference
- Power-up into pre-biased load
- Parallel capable with single wire current sharing
- Two phase interleaving
- Input Over/Under Voltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Over Temperature Protection (OTP)
- Fast and slow current limits
- Differential amplifier for output remote sensing
- User adjustable soft-start & tracking
- -40°C to 125°C operating range (T_J)

Applications

- HV to PoL Buck Regulator Applications
- Computing, Communications, Industrial, Automotive Equipment
- Constant current output operation:
  - LED Lighting
  - Battery Charging

Package Information

- 10mm x 10mm x 2.6mm LGA SiP

Contents

Order Information

Cool-Power	Output Range		Iout Max	Package	Transport Media
	Set	Range			
PI3542-00-LGIZ	2.5V	2.2V to 3.0V	10A	10mm x 10mm LGA	TRAY
PI3543-00-LGIZ	3.3V	2.6V to 3.6V	10A	10mm x 10mm LGA	TRAY
PI3545-00-LGIZ	5.0V	4.0V to 5.5V	10A	10mm x 10mm LGA	TRAY
PI3546-00-LGIZ	12V	6.5V to 14V	9A	10mm x 10mm LGA	TRAY

Thermal, Storage, and Handling Information

Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 125°C
Soldering Temperature for 20 seconds	245°C
MSL Rating	3

Absolute Maximum Ratings

VIN	-0.7V to 75V
VS1	-0.7 to 75V, -4V for 5ns
VOUT	-0.5V to 25V
SGND	100mA
TRK	-0.3V to 5.5V / 30mA
VDR, SYNCI, SYNCO, PWRGD, EN, LGH, COMP, EAO, EAIN, VDIFF, VSN, VSP, TESTx	-0.3V to 5.5V / 5mA

Notes: At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted.

Block Diagram

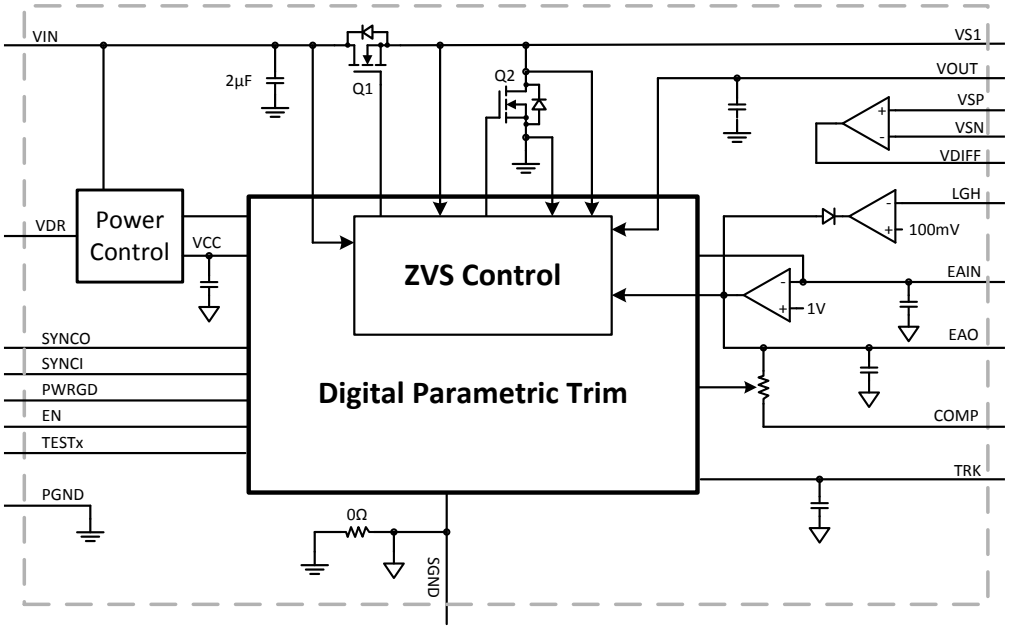
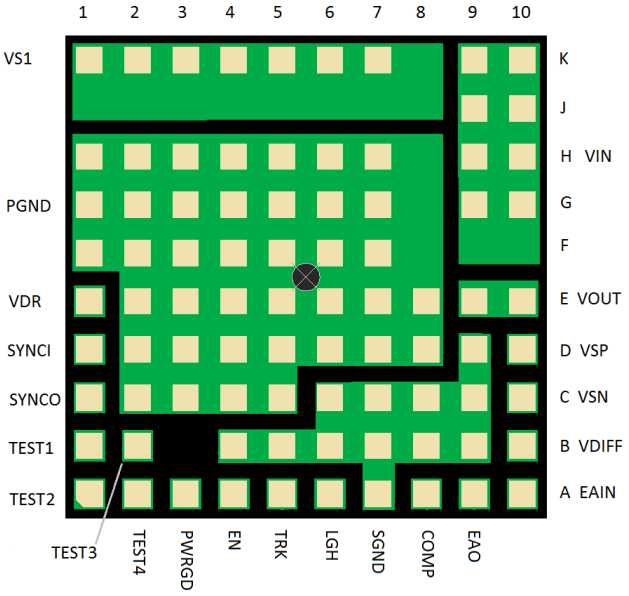


Figure 1: *Simplified Block Diagram*

Package Pin-Out



85 Pad LGA Sip (10mm x 10mm)

Block 1: VIN; K9-10, J9-10, H9-10, G9-10

Block 2: VS1; K1-7

Block 3: PGND; H1-7, G1-7,F1-7, E2-8, D2-8, C2-5

Block 4: SGND; D9, C6-9, B4-9, A7

Pin Description

Name	Location	I/O	Description
VS1	Block 2 (See Pkg Pin-Out dwg)	I/O	**Switching node:** and ZVS sense for power switches
VIN	Block 1	I	**Input voltage:** and sense for UVLO, OVLO and feed forward ramp.
VDR	1E	I/O	**Gate Driver Vcc** : Internally generated 5.1V. May be used as reference or low power bias supply for up to 2mA. Must be impedance limited by the user.
SYNCI	1D	I	**Synchronization input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use.
SYNCO	1C	O	**Synchronization output:** Outputs a high signal for ½ of the minimum period for synchronization of other regulators.
TESTx	1B, 1A, 2B, 2A	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
PWRGD	3A	O	**Power Good:** High impedance when regulator is operating and VOUT is in regulation. May also be used as "Parallel Good" – see applications section.
EN	4A	I	**Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; asserted low, regulator output disabled.
TRK	5A	I	**Soft-start and track input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start.
LGH	6A	I	**Lighting (LGH)/Constant Current (CC) Sense Input:** Input with a 100mV threshold. Used for lighting and constant current type applications.
COMP	8A	O	**Compensation Capacitor:** Connect capacitor for control loop dominant pole.
EAO	9A	O	**Error amp output:** External connection for additional compensation and current sharing.
EAIN	10A	I	**Error Amp Inverting Input:** Connection for the feedback divider tap.
VDIFF	10B	O	**Independent Amplifier Output:** If unused connect in unity gain with VSP connected to SGND.
VSN	10C	I	**Independent Amplifier Inverting Input**
VSP	10D	I	**Independent Amplifier Non-Inverting Input**
VOUT	9E, 10E	I/O	**Output voltage:** and sense for power switches and feed-forward ramp
SGND	Block 4	-	**Signal ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO communication returns. SGND and PGND are star connected within the regulator package.
PGND	Block3	-	**Power ground:** VIN and VOUT power returns

PI354x-00 Common Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, EN=High, V_{VDR} =5.1V +/- 2%, L1=340nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Differential Amp						
Open loop gain		96	120	140	dB	
Small signal gain-bandwidth		5	7	12	MHz	
Offset		-1	0.5	1	mV	
Common mode input range		-0.1		2.5	V	
Differential mode input range				2	V	
Input bias current		-1		1	uA	
Maximum Vout		V_{VDR} -0.2			V	I_{Diff} = -1mA
Minimum Vout				20	mV	
Capacitive load range for stability		0		50	pF	
Slew rate rising			11		V/µsec	
Slew rate falling			11		V/µsec	
Sink/source current		-1		1	mA	
Current Source Function (LGH)						
Reference		95	100	105	mV	
Input Offset			0.5		mV	
Gain-Bandwidth Product		3			MHz	
Internal feedback capacitance			20		pF	
Gain Amp						
Gain			10		V/V	
Intermediate reference			1		V	
Gain-Bandwidth Product		3			MHz	
Transconductance			1		mS	
Output current capability		1			mA	Sink current only
PGD						
PGD Rising Threshold	$V_{PG\_HI\%}$	79	85	91	% V_{OUT_DC}	Note 2.
PGD Falling Threshold	$V_{PG\_LO\%}$	77	83	89	% V_{OUT_DC}	Note 2.
PGD Output Low	V_{PG_SAT}			0.4	V	Sink = 4mA, Note 2.
PGD Sink Current	I_{PG_SAT}		4		mA	Note 2.

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
Note 4: Refer to Output Ripple plots.
Note 5: Refer to Load Current vs. Ambient Temperature curves.
Note 6: Refer to Switching Frequency vs. Load current curves.

PI3542-00 (2.5Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2%, L1=340nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	36	48	60	V	
Input Current	I_{IN_DC}		0.597		A	Vin = 48V, T_C = 25°C, Iout=10A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}		3.1	-	mA	Short at terminals
Input Quiescent Current	I_{Q_VIN}		1.27 2.42		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	0.985	1.00	1.015	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	2.2	2.5	3.0	V	Notes 2, 3.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 36V<Vin<60V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<10A
Output Voltage Ripple	V_{OUT_AC}		47		mVp-p	Iout=10A, Cout=6x100µF, 20MHz BW Note 4
Output Current	I_{OUT_DC}	0		10	A	Note 5.
Current Limit	I_{OUT_CL}	-	12	-	A	L1 = 340nH ±1%
Protection						
Input UVLO Start Threshold	V_{UVLO_START}	33.8	34.8	35.8	V	
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		0.9		V	
Input UVLO Response Time			1.25		usec	
Input OVLO Stop Threshold	V_{OVLO}	62	64.3	66.2	V	
Input OVLO Start Hysteresis	V_{OVLO_HYS}		1.3		V	
Input OVLO Response Time	t_f		1.25		usec	
Output Over Voltage Protection	V_{OVP}		20		%	Above Set V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}		130		°C	
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
Note 4: Refer to Output Ripple plots.
Note 5: Refer to Load Current vs. Ambient Temperature curves.
Note 6: Refer to Switching Frequency vs. Load current curves.

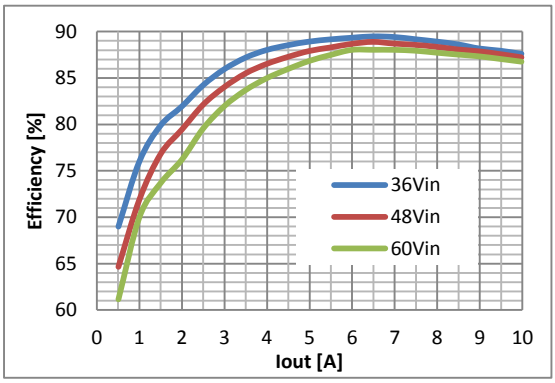
PI3542-00 (2.5Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2% , L1=340nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S	-	400	-	kHz	Note 6. 48Vin to 2.5Vout, 3A out, L1 = 340nH ±1%
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		V_{VDR} /2		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	V_{VDR} -0.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start, Tracking And Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}	0		1.08	V	
TRK Enable Threshold	V_{TRK_OV}	20	40	60	mV	
TRK to EAIN Offset	V_{EAIN_OV}	50	80	110	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		10		mA	V(TRK) = 0.5V
Soft-Start Time	t_{SS}	0.6	.94	1.6	ms	C_{TRK} = 0
Error Amplifier Trans-Conductance	GMeao		5.1		mS	Note 2.
PSM Skip Threshold	PSM_{SKIP}		0.8		V	Note 2.
Error Amplifier Output Impedance	Rout	1			MOhm	Note 2.
Internal Compensation Capacitor	Chf		56		pF	Note 2.
Internal Compensation Resistor	Rzi		5k		Ohm	Note 2.
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, no fault)	V_{EN_PU}		2		V	
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	

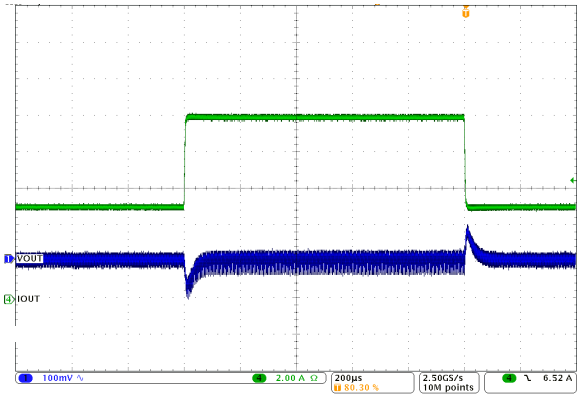
PI3542-00 (2.5 Vout) Electrical Characteristics

Efficiency at 25°C



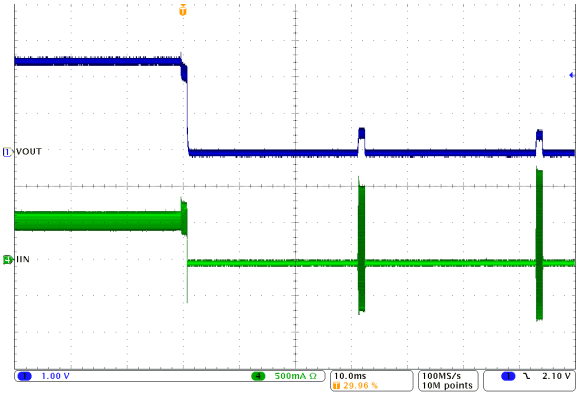
Regulator and inductor performance

Transient Response: 5A to 10A, at 1A/µs

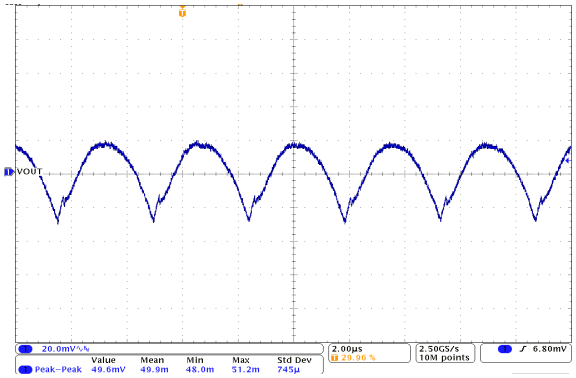


48Vin to 2.5Vout, Cout = 6 x 100µF Ceramic
Vout (Ch1) = 100mV/Div, Iout (Ch4) = 2A/Div, 200us/Div

Output Short Circuit @ Vin = 48V

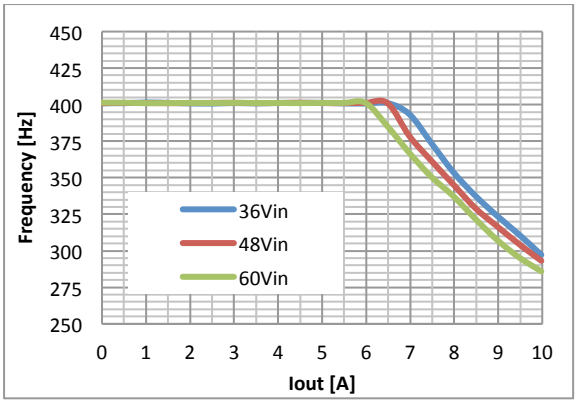


Output Ripple: 24Vin, 2.5Vout at 10A

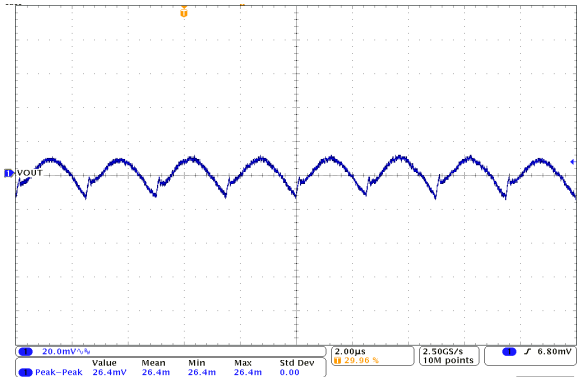


Vout = 20mV/Div, 2.0us/Div
Cout = 6 x 100µF Ceramic

Switching Frequency vs. Load Current



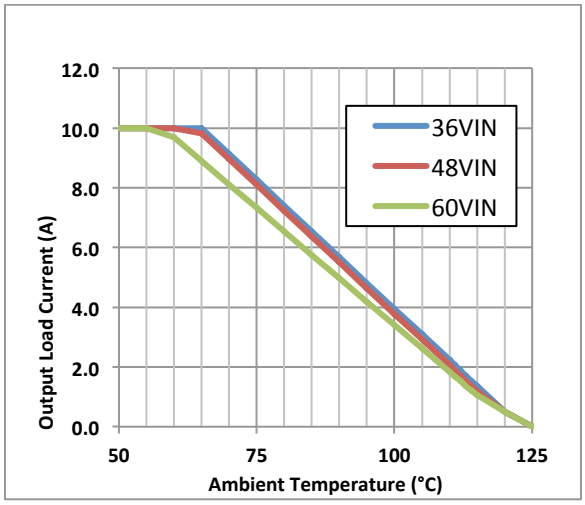
Output Ripple: 24Vin, 2.5Vout at 5A



Vout = 20mV/Div, 2.0us/Div
Cout = 6 x 100µF Ceramic

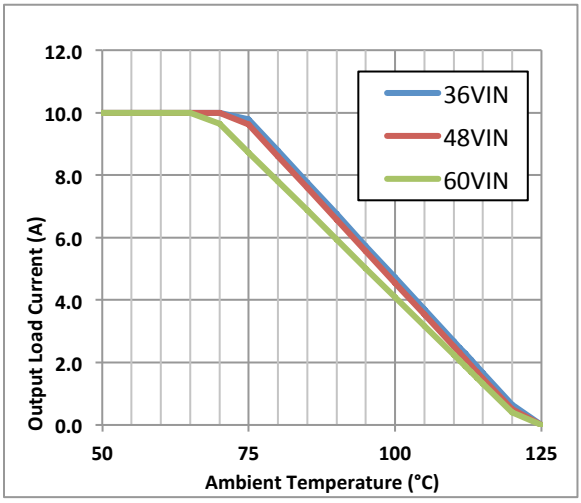
PI3542-00 (2.5 Vout) Electrical Characteristics

Load Current vs. Ambient Temperature, 0 LFM



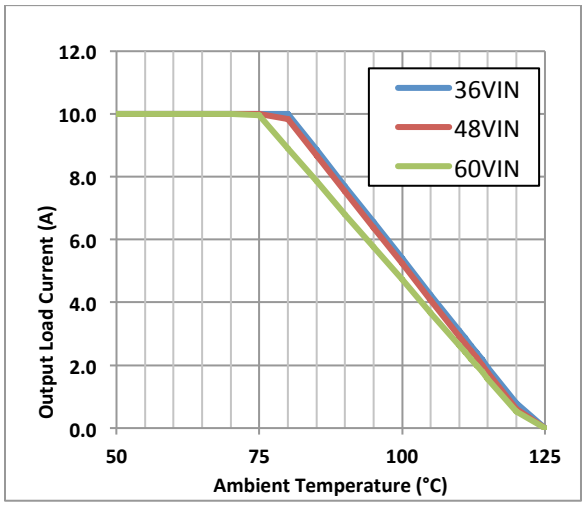
Regulator and inductor performance, full trim range

Load Current vs. Ambient Temperature, 200 LFM



Regulator and inductor performance, full trim range

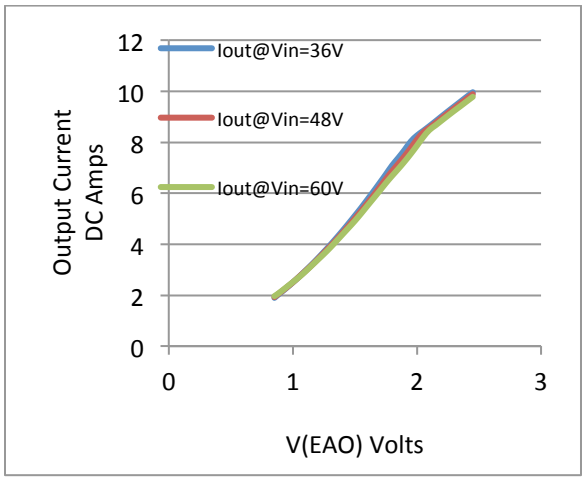
Load Current vs. Ambient Temperature, 400 LFM



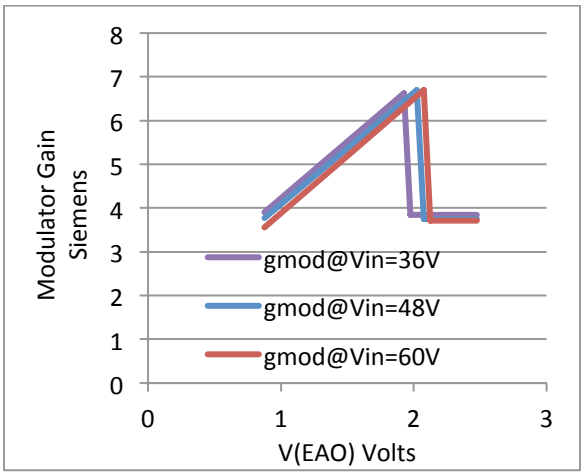
Regulator and inductor performance, full trim range

PI3542-00 (2.5 Vout) Electrical Characteristics

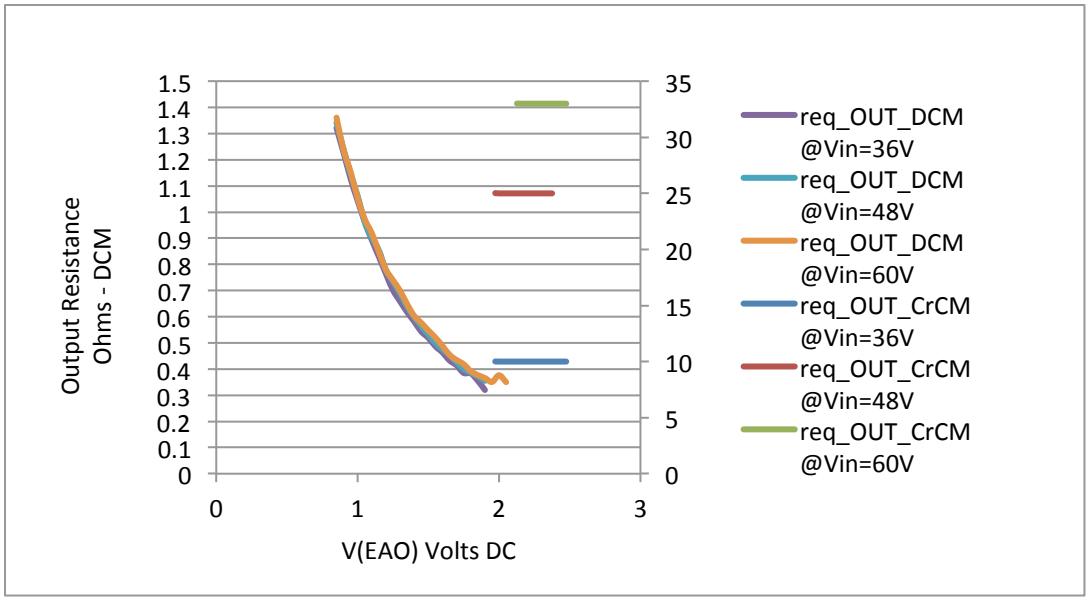
Output Current vs. Error Voltage V(EAO)



Modulator Gain vs. Error Voltage (VEAO)



Output Equivalent Resistance vs. Error Voltage V(EAO)



PI3543-00 (3.3 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2%, L1=420nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	36	48	60	V	
Input Current	I_{IN_DC}		0.762		A	Vin = 48V, T_C = 25°C, Iout=10A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}		3	-	mA	Short at terminals
Input Quiescent Current	I_{Q_VIN}		1.265 2.4		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	0.985	1.00	1.015	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	2.6	3.3	3.6	V	Notes 2, 3.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 36V<Vin<60V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<10A
Output Voltage Ripple	V_{OUT_AC}		62		mVp-p	Iout=10A, Cout=6x100µF, 20MHz BW Note 4
Output Current	I_{OUT_DC}	0		10	A	Note 5
Current Limit	I_{OUT_CL}	-	11.5	-	A	L1 = 420nH ±1%
Protection						
Input UVLO Start Threshold	V_{UVLO_START}	33.8	34.8	35.8	V	
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		0.9		V	
Input UVLO Response Time			1.25		usec	
Input OVLO Stop Threshold	V_{OVLO}	62	64.3	66.2	V	
Input OVLO Start Hysteresis	V_{OVLO_HYS}		1.3		V	
Input OVLO Response Time	t_f		1.25		usec	
Output Over Voltage Protection	V_{OVP}		20		%	Above Set V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}		130		°C	
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.

Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves

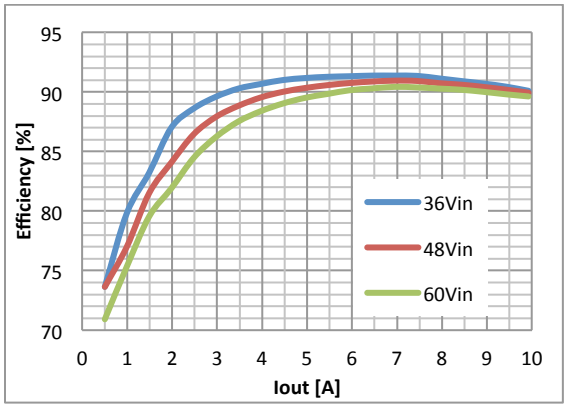
PI3543-00 (3.3 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2%, L1=420nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S	-	400	-	kHz	Note 6. 48Vin to 3.3Vout, 6A out, L1 = 420nH ±1%
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		V_{VDR} /2		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	V_{VDR} -0.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start, Tracking And Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}	0		1.08	V	
TRK Enable Threshold	V_{TRK_OV}	20	40	60	mV	
TRK to EAIN Offset	V_{EAIN_OV}	50	80	110	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		10		mA	V(TRK) = 0.5V
Soft-Start Time	t_{SS}	0.6	.94	1.6	ms	C_{TRK} = 0
Error Amplifier Trans-Conductance	GMeao		5.1		mS	Note 2.
PSM Skip Threshold	PSM_{SKIP}		0.8		V	Note 2.
Error Amplifier Output Impedance	Rout	1			MOhm	Note 2.
Internal Compensation Capacitor	Chf		56		pF	Note 2.
Internal Compensation Resistor	Rzi		6k		Ohm	Note 2.
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, no fault)	V_{EN_PU}		2		V	
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	

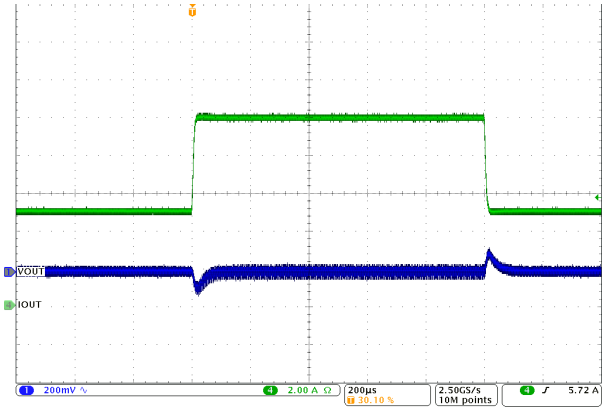
PI3543-00 (3.3 Vout) Electrical Characteristics

Efficiency at 25°C



Regulator and inductor performance

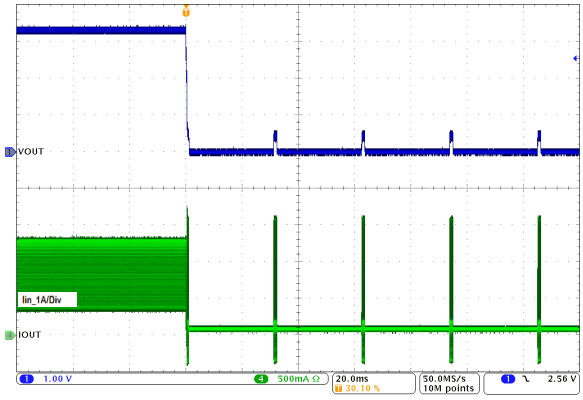
Transient Response: 5A to 10A, at 1A/µs



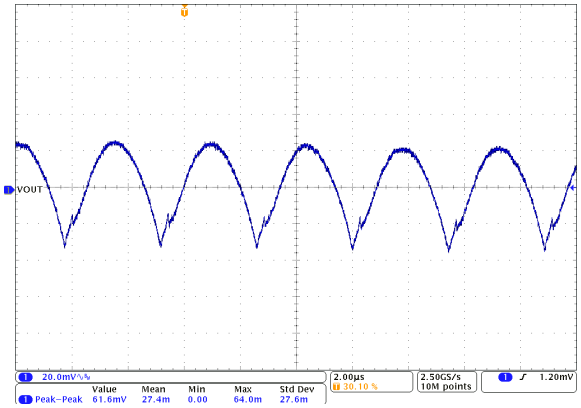
48Vin to 3.3Vout

Cout = 6 x 100µF Ceramic

Short Circuit 48Vin



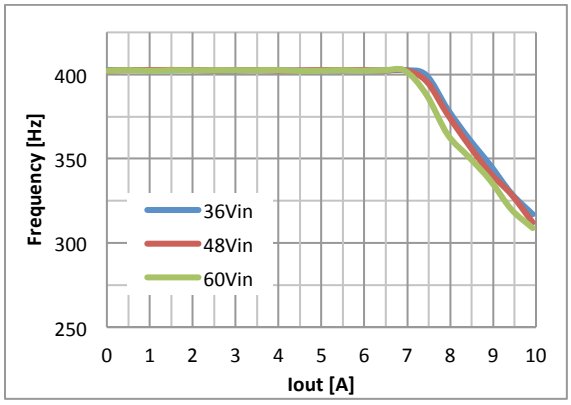
Output Ripple: 48Vin, 3.3Vout at 10A



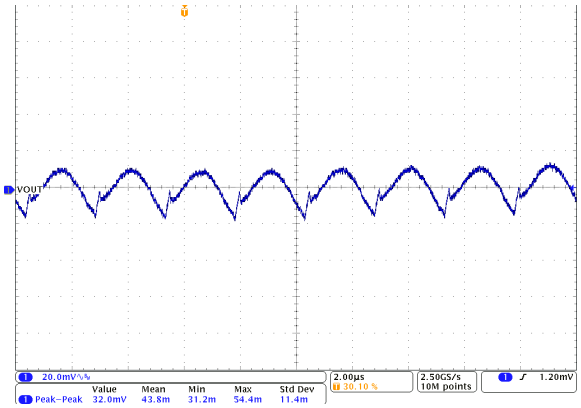
Vout = 20mV/Div, 2.0us/Div

Cout = 6 x 100µF Ceramic

Switching Frequency vs. Load Current



Output Ripple: 48Vin, 3.3Vout at 5A

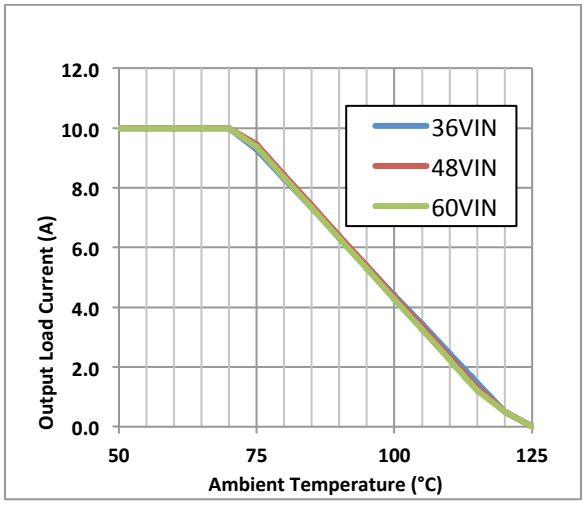


Vout = 20mV/Div, 2.0us/Div

Cout = 6 x 100µF Ceramic

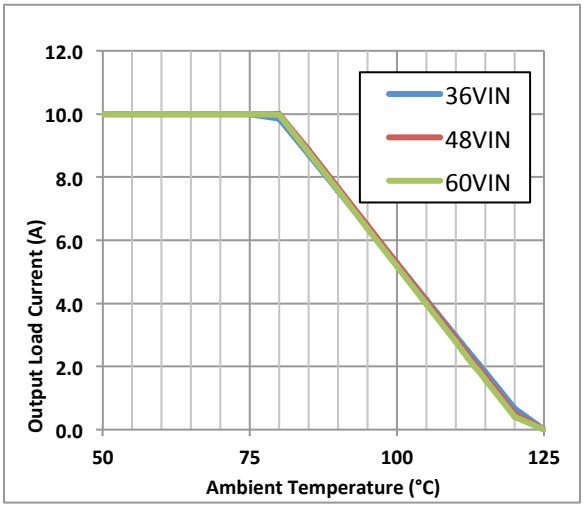
PI3543-00 (3.3 Vout) Electrical Characteristics

Load Current vs. Ambient Temperature, 0 LFM



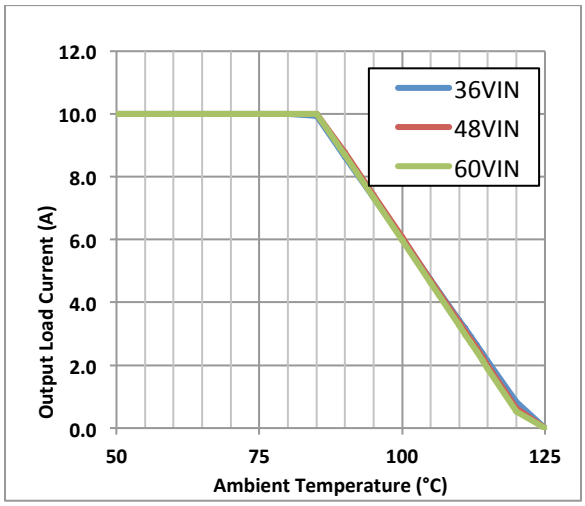
Regulator and inductor performance, full trim range

Load Current vs. Ambient Temperature, 200 LFM



Regulator and inductor performance, full trim range

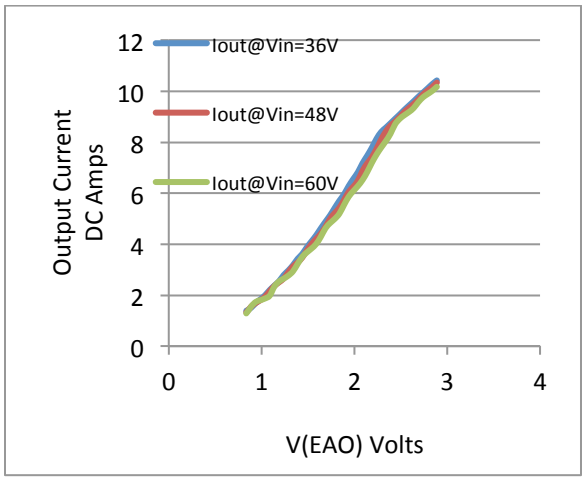
Load Current vs. Ambient Temperature, 400 LFM



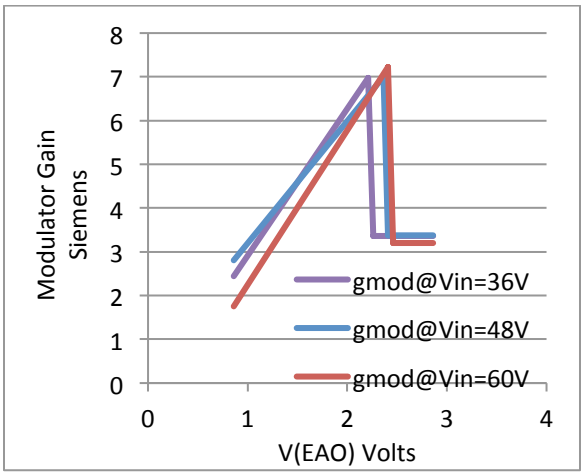
Regulator and inductor performance, full trim range

PI3543-00 (3.3 Vout) Electrical Characteristics

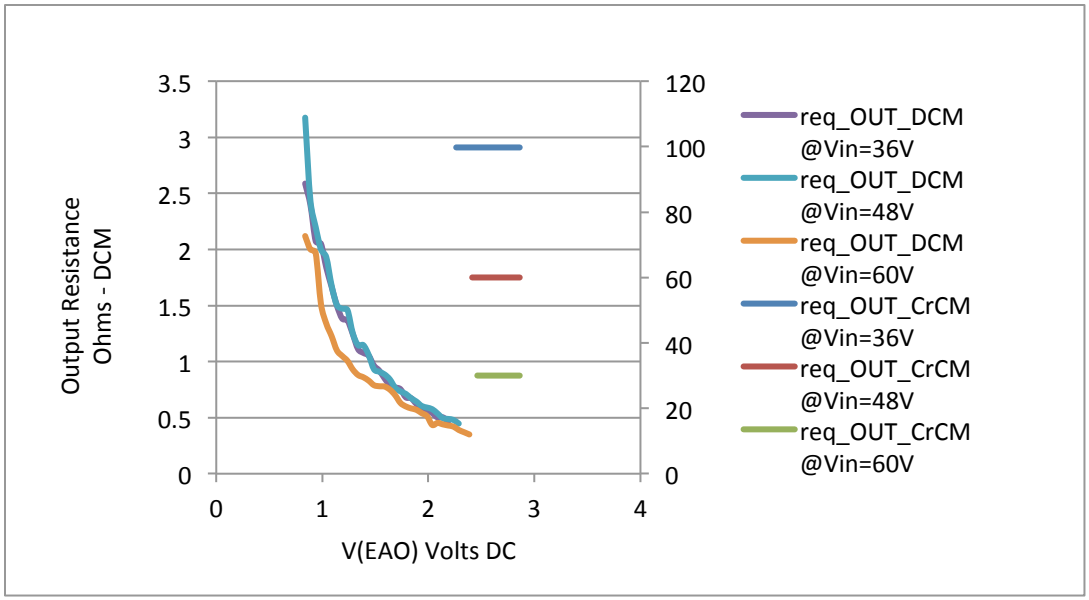
Output Current vs. Error Voltage V(EAO)



Modulator Gain vs. Error Voltage (VEAO)



Output Equivalent Resistance vs. Error Voltage V(EAO)



PI3545-00 (5.0 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2%, L1=420nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	36	48	60	V	
Input Current	I_{IN_DC}		1.126		A	Vin = 48V, T_C = 25°C, Iout=10A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}		3.2	-	mA	Short at terminals
Input Quiescent Current	I_{Q_VIN}		1.26 2.42		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	0.985	1.00	1.015	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	4.0	5.0	5.5	V	Notes 2, 3.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 36V<Vin<60V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<10A
Output Voltage Ripple	V_{OUT_AC}		62.4		mVp-p	Iout=10A, Cout=6x47µF, 20MHz BW Note 4
Output Current	I_{OUT_DC}	0		10	A	Note 5.
Current Limit	I_{OUT_CL}	-	12	-	A	L1 = 420nH ±1%
Protection						
Input UVLO Start Threshold	V_{UVLO_START}	33.8	34.8	35.8	V	
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		2.6		V	
Input UVLO Response Time			1.25		usec	
Input OVLO Stop Threshold	V_{OVLO}	62	64.3	66.2	V	
Input OVLO Start Hysteresis	V_{OVLO_HYS}		1.3		V	
Input OVLO Response Time	t_f		1.25		usec	
Output Over Voltage Protection	V_{OVP}		20		%	Above Set V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}		130		°C	
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.

Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

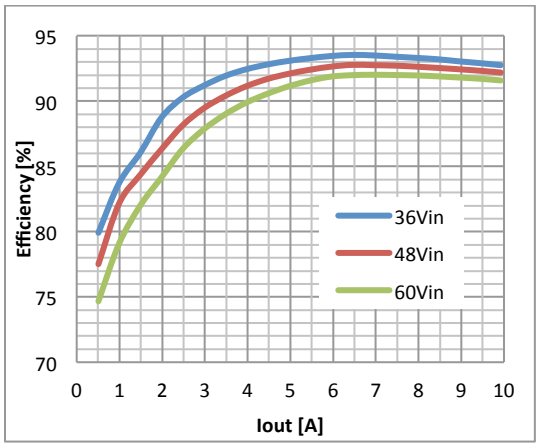
PI3545-00 (5.0 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2%, L1=400nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S	-	600	-	kHz	Note 6. 48Vin to 5Vout, 3A out, L1 = 420nH ±1%
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		V_{VDR} /2		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	V_{VDR} -0.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start, Tracking And Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}	0		1.08	V	
TRK Enable Threshold	V_{TRK_OV}	20	40	60	mV	
TRK to EAIN Offset	V_{EAIN_OV}	50	80	110	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		10		mA	V(TRK) =0.5V
Soft-Start Time	t_{SS}	0.6	.94	1.6	ms	C_{TRK} = 0
Error Amplifier Trans-Conductance	GMeao		5.1		mS	Note 2.
PSM Skip Threshold	PSM_{SKIP}		0.8		V	Note 2.
Error Amplifier Output Impedance	Rout	1			MOhm	Note 2.
Internal Compensation Capacitor	Chf		56		pF	Note 2.
Internal Compensation Resistor	Rzi		6k		Ohm	Note 2.
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, no fault)	V_{EN_PU}		2		V	
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	

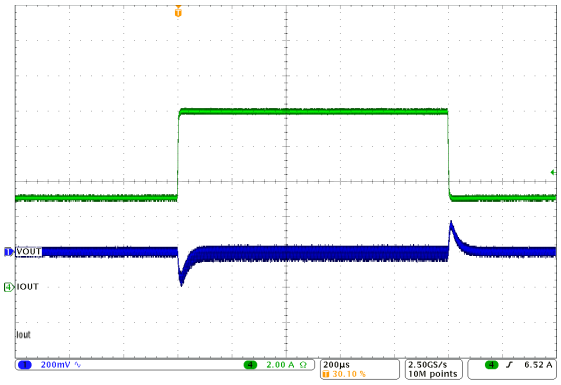
PI3545-00 (5.0 Vout) Electrical Characteristics

Efficiency at 25°C



Regulator and inductor performance

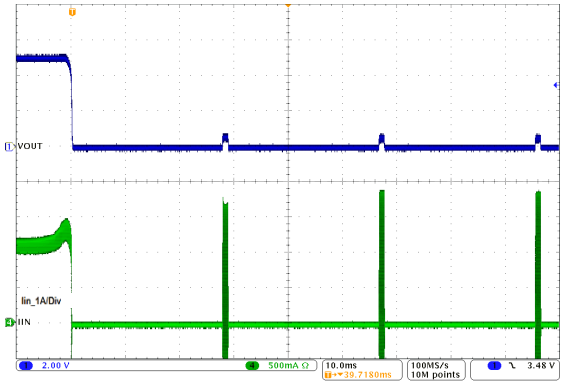
Transient Response: 5A to 10A, at 1A/µs



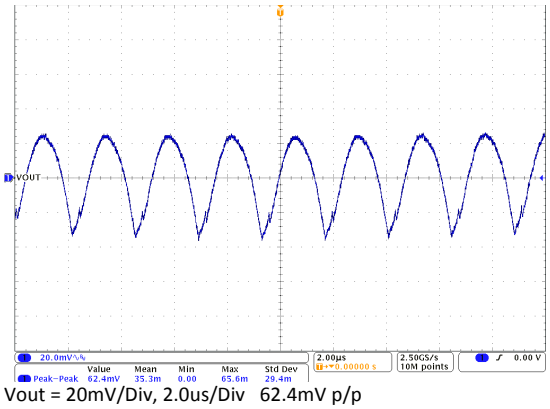
48Vin to 5.0Vout

Cout = 6 X 47uF Ceramic

Short Circuit Test 48Vin



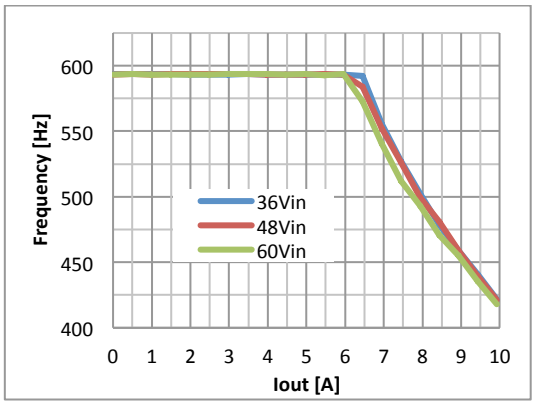
Output Ripple: 48Vin, 5.0Vout at 10A



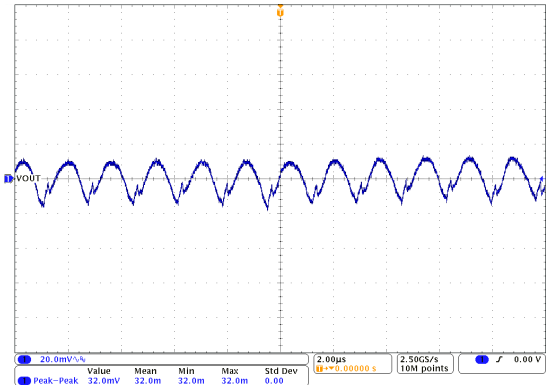
Vout = 20mV/Div, 2.0us/Div 62.4mV p/p

Cout = 6 x 47µF Ceramic

Switching Frequency vs. Load Current



Output Ripple: 24Vin, 5.0Vout at 5A

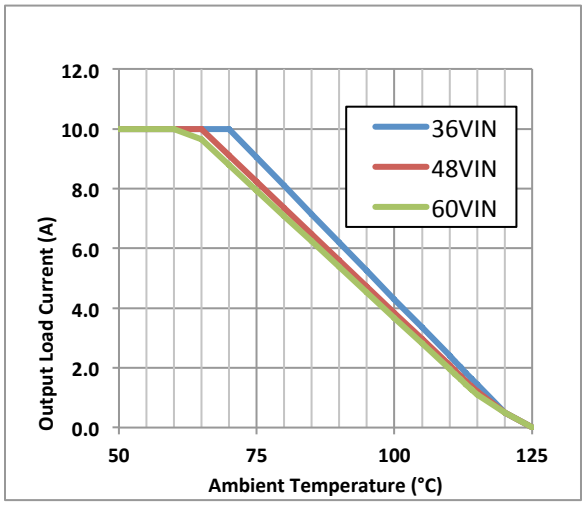


Vout = 20mV/Div, 2.0us/Div 32mV/p/p

Cout = 6 X 47uF Ceramic

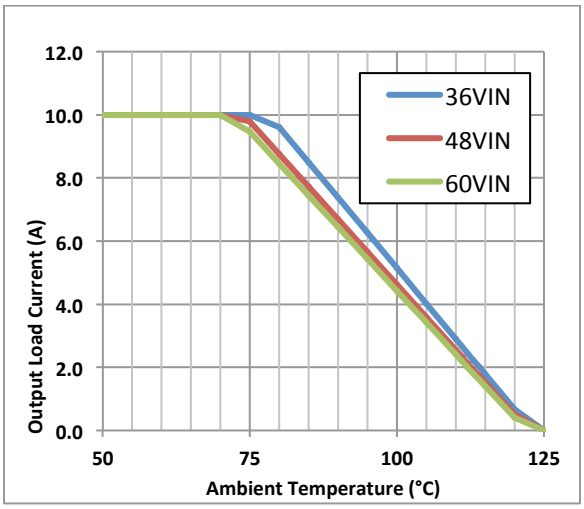
PI3545-00 (5.0 Vout) Electrical Characteristics

Load Current vs. Ambient Temperature, 0 LFM



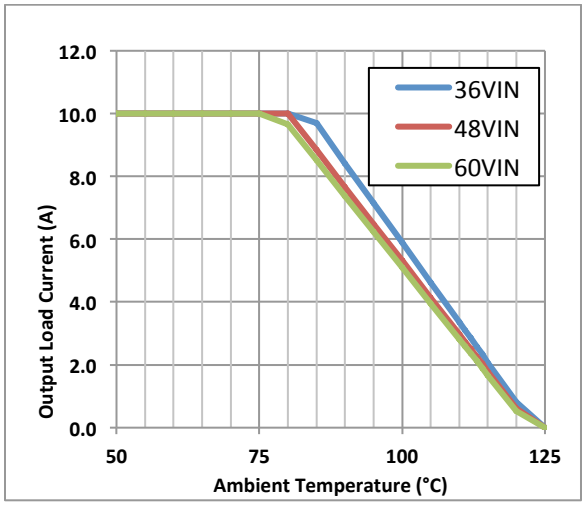
Regulator and inductor performance, full trim range

Load Current vs. Ambient Temperature, 200 LFM



Regulator and inductor performance, full trim range

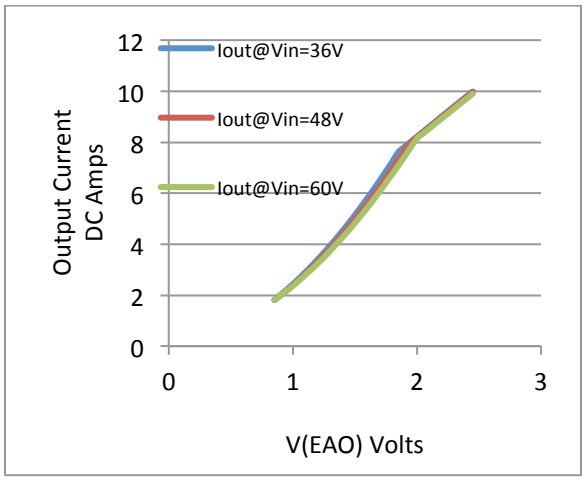
Load Current vs. Ambient Temperature, 400 LFM



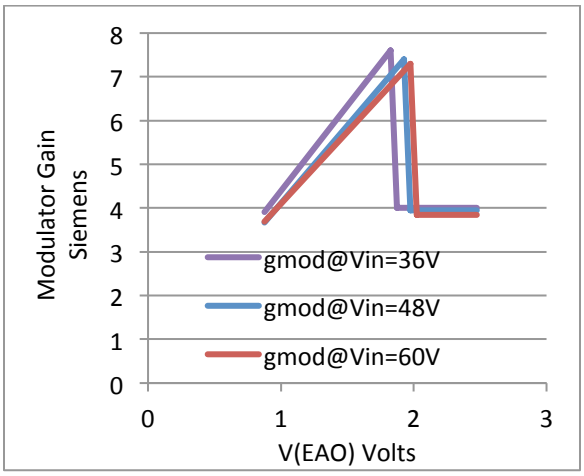
Regulator and inductor performance, full trim range

PI3545-00 (5.0 Vout) Electrical Characteristics

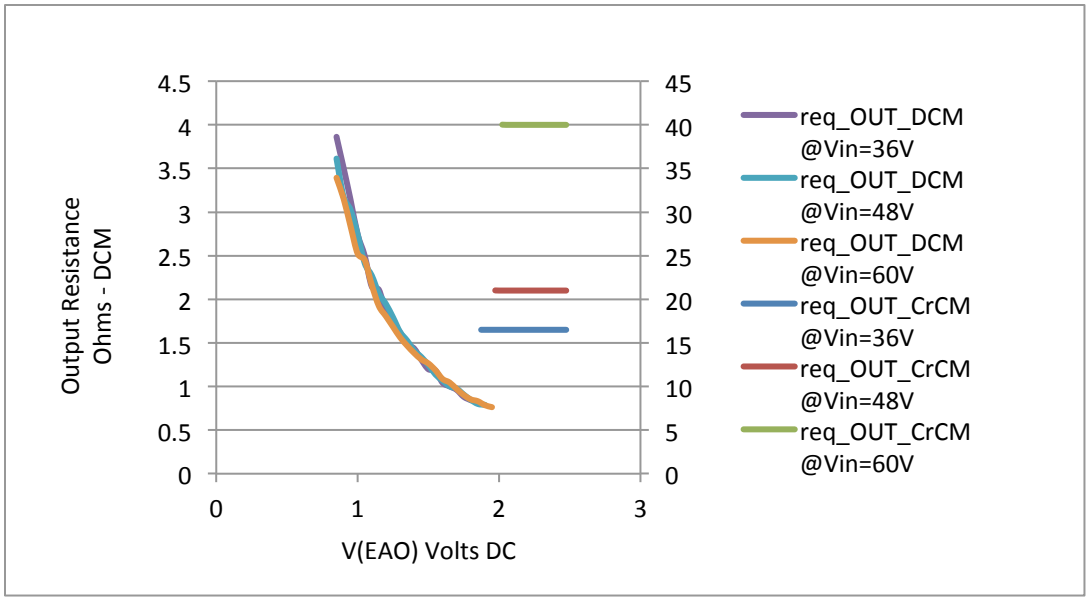
Output Current vs. Error Voltage V(EAO)



Modulator Gain vs. Error Voltage (VEAO)



Output Equivalent Resistance vs. Error Voltage V(EAO)



PI3546-00 (12.0 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2%, L1=900nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	36	48	60	V	
Input Current	I_{IN_DC}		2.33		A	Vin = 48V, T_C = 25°C, Iout=9A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}		3.3	-	mA	Short at terminals
Input Quiescent Current	I_{Q_VIN}		1.26 2.9		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	0.985	1.00	1.015	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	6.5	12	14	V	Notes 2, 3.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 36V<Vin<60V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<9A
Output Voltage Ripple	V_{OUT_AC}		114		mVp-p	Iout=9A, Cout=6x10µF, 20MHz BW Note 4
Output Current	I_{OUT_DC}	0		9	A	Note 5.
Current Limit	I_{OUT_CL}	-	10.5	-	A	L1 = 900nH ±1%
Protection						
Input UVLO Start Threshold	V_{UVLO_START}	33.8	34.8	35.8	V	
Input UVLO Stop Hysteresis	V_{UVLO_HYS}		2.6		V	
Input UVLO Response Time			1.25		usec	
Input OVLO Stop Threshold	V_{OVLO}	62	64.3	66.2	V	
Input OVLO Start Hysteresis	V_{OVLO_HYS}		1.3		V	
Input OVLO Response Time	t_f		1.25		usec	
Output Over Voltage Protection	V_{OVP}		20		%	Above Set V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}		130		°C	
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.

Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

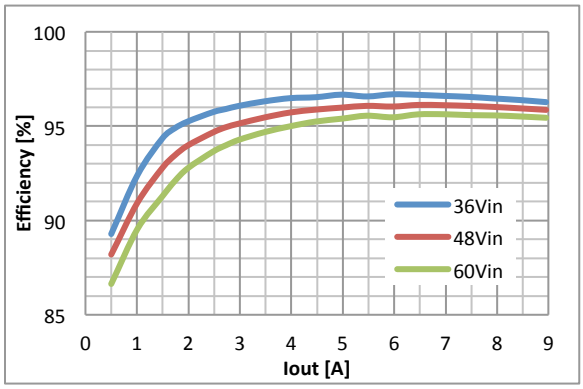
PI3546-00 (12.0 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =48V, V_{VDR} =5.1V +/- 2%, L1=900nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S	-	800	-	kHz	Note 6. 48Vin to 12Vout, 2A out, L1 = 900nH ±1%
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		V_{VDR} /2		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	V_{VDR} -0.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start, Tracking And Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}	0		1.08	V	
TRK Enable Threshold	V_{TRK_OV}	20	40	60	mV	
TRK to EAIN Offset	V_{EAIN_OV}	50	80	110	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		10		mA	V(TRK) = 0.5V
Soft-Start Time	t_{SS}	0.6	.94	1.6	ms	C_{TRK} = 0
Error Amplifier Trans-Conductance	GMeao		7.6		mS	Note 2.
PSM Skip Threshold	PSM_{SKIP}		0.8		V	Note 2.
Error Amplifier Output Impedance	Rout	1			MOhm	Note 2.
Internal Compensation Capacitor	Chf		56		pF	Note 2.
Internal Compensation Resistor	Rzi		5k		Ohm	Note 2.
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, no fault)	V_{EN_PU}		2		V	
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	

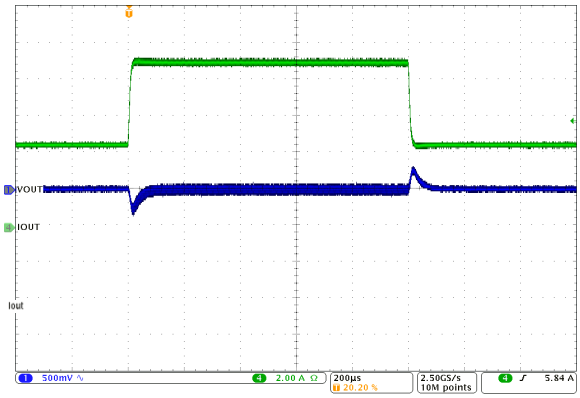
PI3546-00 (12.0 Vout) Electrical Characteristics

Efficiency at 25°



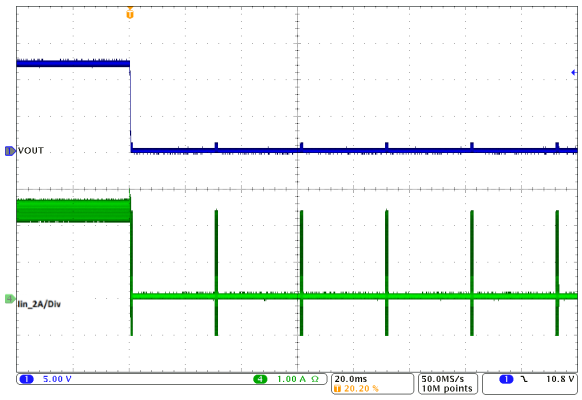
Regulator and inductor performance

Transient Response: 4.5A to 9A, at 1A/µs

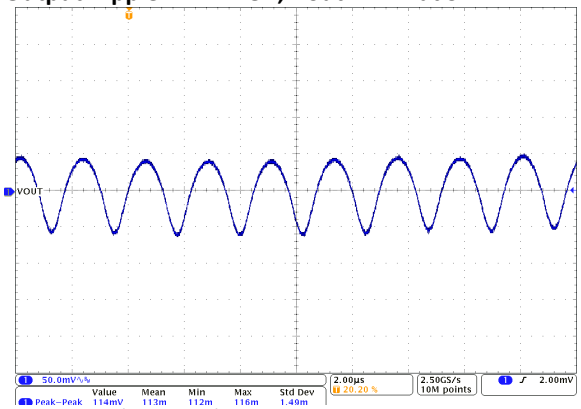


48Vin to 12.0Vout
Cout = 6 X 10uF Ceramic

Short Circuit Test

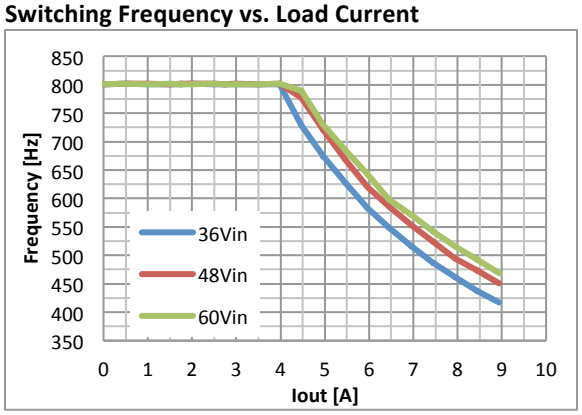


Output Ripple: Vin = 48V, Vout = 12V at 9A

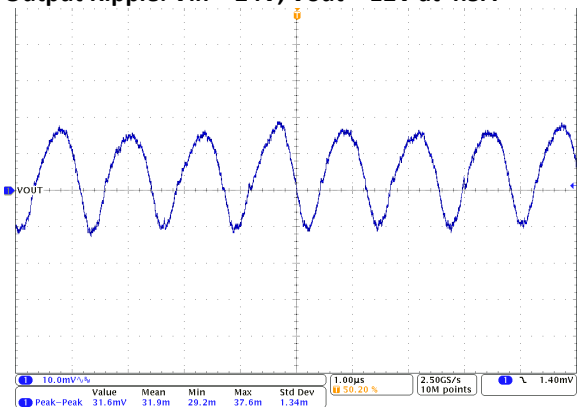


Vout = 50mV/Div, 2.0us/Div
Cout = 6 X 10uF Ceramic

Switching Frequency vs. Load Current



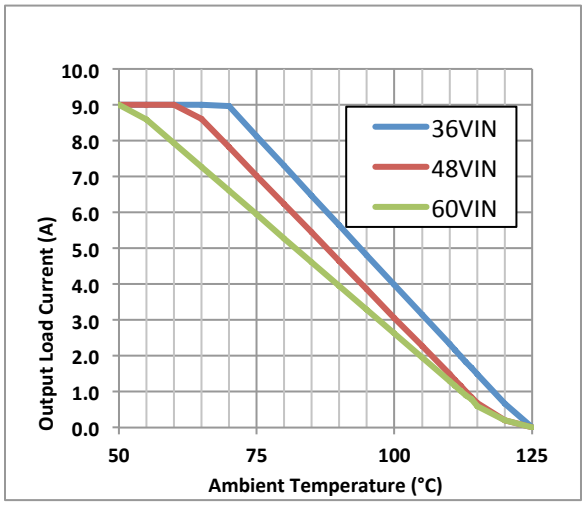
Output Ripple: Vin = 24V, Vout = 12V at 4.5A



Vout = 10mV/Div, 2.0us/Div
Cout = 6 X 10uF Ceramic

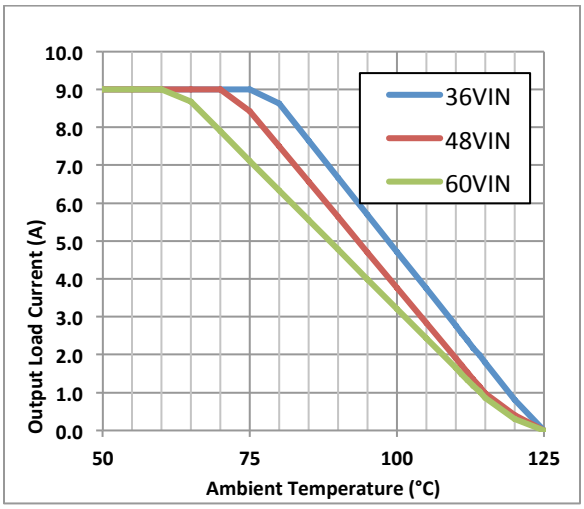
PI3546-00 (12.0 Vout) Electrical Characteristics

Load Current vs. Ambient Temperature, 0 LFM



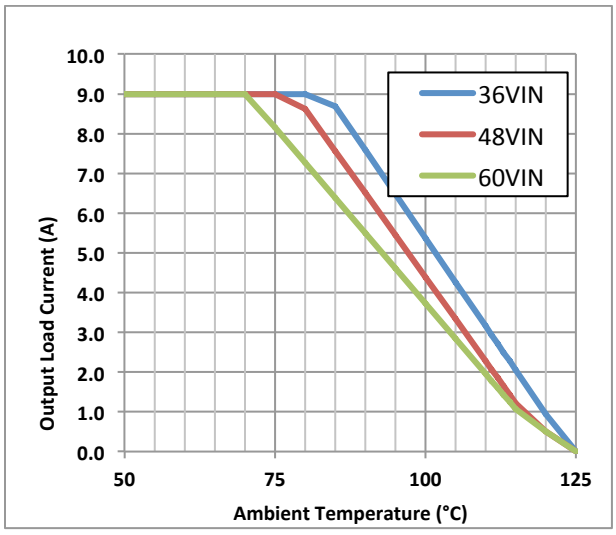
Regulator and inductor performance (6.5-12.0 Vout)

Load Current vs. Ambient Temperature, 200 LFM



Regulator and inductor performance (6.5-12.0 Vout)

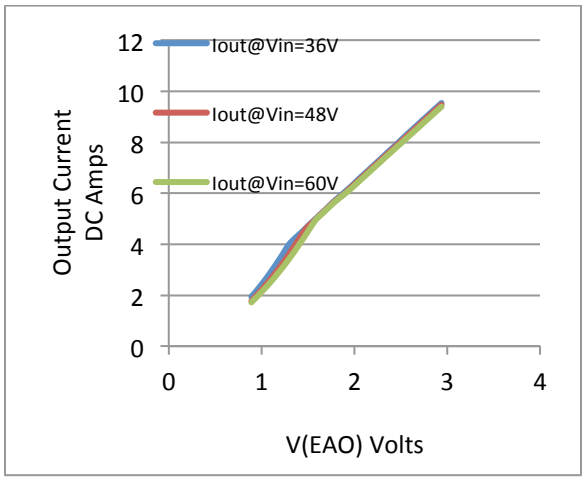
Load Current vs. Ambient Temperature, 400 LFM



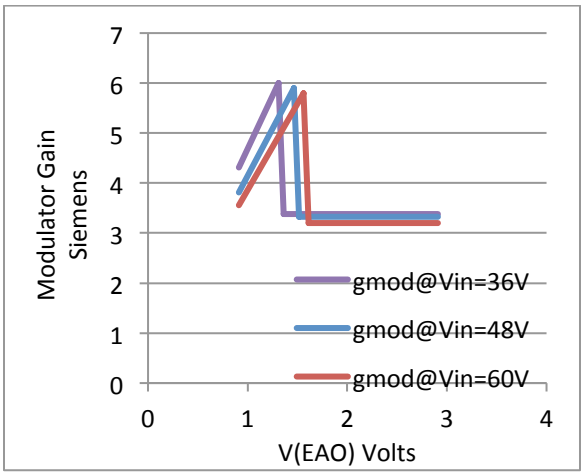
Regulator and inductor performance (6.5-12.0 Vout)

PI3546-00 (12.0 Vout) Electrical Characteristics

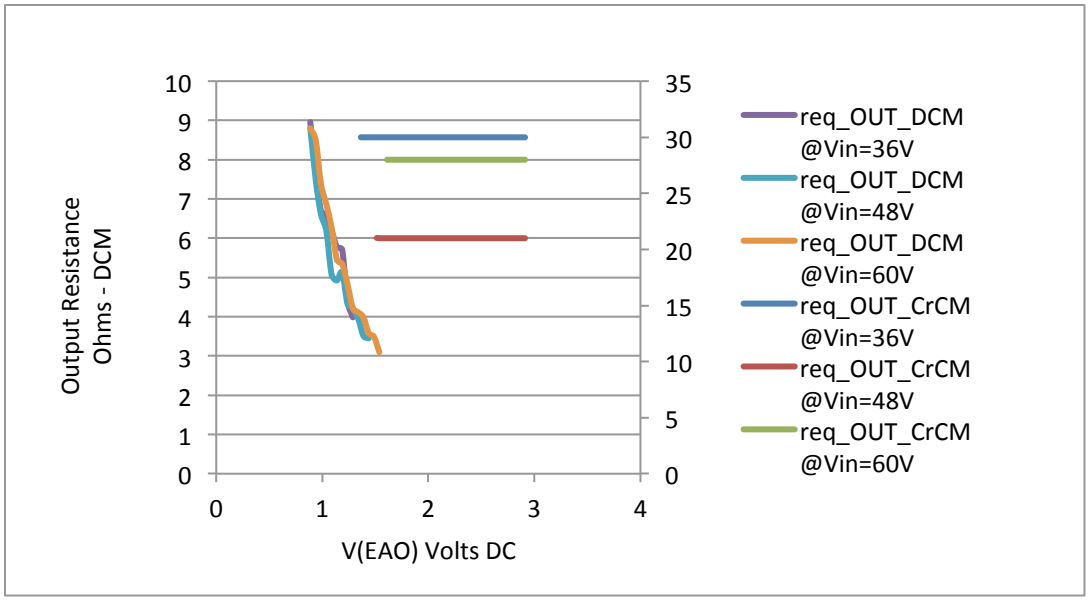
Output Current vs. Error Voltage V(EAO)



Modulator Gain vs. Error Voltage (VEAO)



Output Equivalent Resistance vs. Error Voltage V(EAO)



Functional Description

The PI354X-00 is a family of highly integrated ZVS-Buck regulators. The PI354X-00 has an output voltage that can be set within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 5).

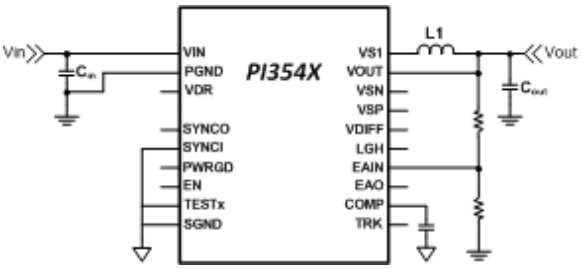


Figure 2 - *HV ZVS-Buck with required components*

For basic operation, Figure 2 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below 0.8 Vdc with respect to SGND will disable the regulator output.

Remote Sensing

If remote sensing is required, the PI354X-00 product family is equipped with an undedicated differential amplifier. This amplifier can allow full differential remote sense by configuring it as a differential follower and connecting the VDIFF pin to the EAIN pin.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (f_S). SYNCI pin, as determined by the main switching frequency f_s.

The PI354X-00 default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the interleaved paralleling of two PI354X-00 devices without the need for further user programming or external sync clock circuitry.

When using the internal oscillator, the SYNCO pin provides a 5V clock that can be used to sync other regulators. Therefore, one PI354X-00 can act as the lead regulator and have additional PI354X-00s running in parallel and synchronized.

Soft-Start

The PI354X-00 includes an internal soft-start capacitor to control the rate of rise of the output voltage. See the Electrical Characteristics Section for the default value. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, “Soft Start Adjustment and Track,” in the Applications Description section for more details.

Output Voltage Selection

The PI354X-00 output voltage can be selected by connecting a resistor from EAIN pin to SGND and a resistor from Vout to the EAIN pin as shown in Figure 2. Table 2 defines the allowable operational voltage ranges for the PI354X-00 family.

Device	Output Voltage	
	Nom.	Range
PI3542-00-LGIZ	2.5V	2.2V to 3.0V
PI3543-00-LGIZ	3.3V	2.6V to 3.6V
PI3545-00-LGIZ	5.0V	4.0V to 5.5V
PI3546-00-LGIZ	12V	6.5 to 14.0V

Table 2 - *PI354X-00 family output voltage ranges.*

Output Current Limit Protection

PI354X-00 has two methods implemented to protect from output short or over current condition.

Slow Current Limit protection: prevents the output from sourcing current higher than the regulator’s

maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024us, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI354X-00 monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to sudden low impedance short. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Input Under-Voltage Lockout

If VIN falls below the input Under Voltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI354X-00 will complete the current cycle and stop switching. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

Input Over Voltage Lockout

If VIN exceeds the input Over Voltage Lockout (OVLO) threshold (V_{OVLO}), while the controller is running, the PI354X-00 will complete the current cycle and stop switching. The system will soft start after the Fault Restart Delay once VIN recovers.

Output Over Voltage Protection

The PI354X-00 family is equipped with output Over Voltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle and stop switching. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Over Temperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Over Temperature Protection Threshold (OTP) is exceeded (T_{OTP}), the regulator will complete the current switching cycle, enter a low power mode and will soft-start when the internal temperature falls below Over-Temperature Restart Hysteresis (T_{OTP_HYS}).

Pulse Skip Mode (PSM)

PI354X-00 features a PSM to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

Variable Frequency Operation

Each PI354X-00 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 3), to operate at peak efficiency across line and load variations. At low line and high load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Parallel Operation

Paralleling modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple.

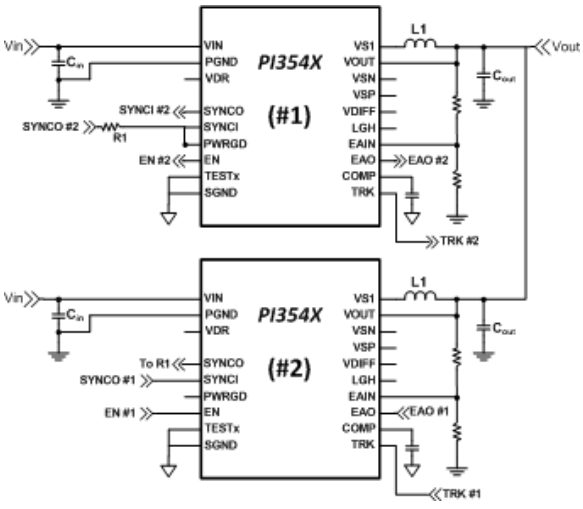


Figure 3 *- PI354X-00 parallel operation*

The PI354X-00 default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI354X-00 devices without the need for further user programming or external sync clock circuitry.

By connecting the EAO pins and SGND pins of each module together the units will share the current equally. When the TRK pins of each unit are connected together, the units will track each other during soft-start and all unit EN pins have to be released to allow the units to start (See Figure 3). Also, any fault event in any regulator will disable the other regulators. The two regulators will be out of phase with each other reducing output ripple (refer to Switching Frequency Synchronization).

To provide synchronization between regulators over the entire operational frequency range, the Power Good (PGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.4kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 3. In this configuration, at system soft-start, the PWRGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop startup synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust, on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop.

Application Description

Output Voltage Set Point

The PI354X-00 family of Buck Regulators utilize an internal 1V reference. The output voltage setting is accomplished using external resistors as shown in Figure 4. Select R2 to be at or around 1k for best noise immunity. Use equations (1) and (2) to determine the proper value based on the desired output voltage.

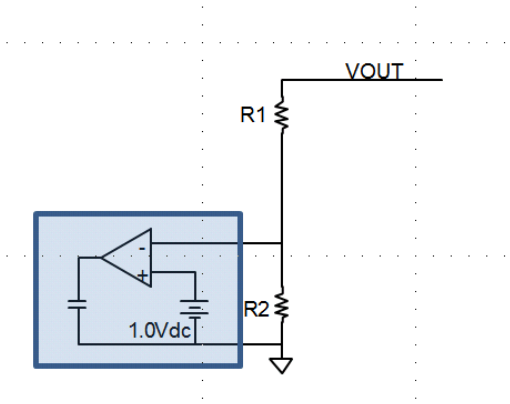


Figure 4 *-External resistor divider network*

$$Vout = Vref\ (1V) * \frac{(R1 + R2)}{R2} \qquad (1)$$

$$R1 = -R2 * \frac{(Vref(1V) - Vout)}{Vref} \qquad (2)$$

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal capacitor and a fixed charge current to provide a Soft-Start Time t_{SS} for all PI354X-00 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK} \times I_{TRK}) - 100x10^{-9},$$

Where, t_{TRK} is the soft-start time and I_{TRK} is a 50uA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at startup, simply connect all PI354X-00 device TRK pins together. This type of tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 5 (a)).

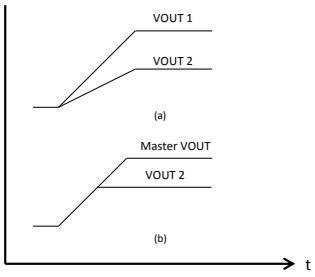


Figure 5 - *PI354X-00 tracking methods*

For Direct Tracking, choose the PI354X-00 with the highest output voltage as the master and connect the master to the TRK pin of the other PI354X-00 regulators through a divider (Figure 6) with the same ratio as the slave's feedback divider (see Table 4 for values).

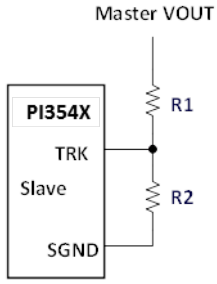


Figure 6 - *Voltage divider connections for direct tracking*

All connected PI354X-00 regulator soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 5 (b). All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI354X-00 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 3 details the specific inductor value and part number utilized for each PI354X-00.

Device	Inductor [nH]	Inductor Part Number	Manufacturer
PI3542-00	340	FPT1006-340-R	Eaton
PI3543-00	420	HCV1206-R42-R	Eaton
PI3545-00	420	HCV1206-R42-R	Eaton
PI3546-00	900	HCV1206-R90-R	Eaton

Table 3 - *PI354X-00 Inductor pairing*

Thermal De-rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the Picor regulator and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

Thermal measurements were made using a standard PI354X-00 Evaluation board which is 2.5x4 inches in area and uses 4-layer, 2oz copper. Thermal measurements were made on the three main power devices, the two internal MOSFETs and the external inductor, with air flows of 0, 200, and 400 LFM.

Small Signal Model - Constant Voltage Mode

The PI354X product family is a variable frequency CCM/DCM ZVS Buck Regulator. The small signal model for this powertrain is that of a voltage controlled current source which has a trans-conductance that varies depending on the operating mode. When the converter is operating at its normal frequency, it is in discontinuous mode. As the load increases to the point at which the boundary between discontinuous and continuous modes is reached, the powertrain changes frequency to remain in critical conduction mode. This mode of operation allows the PI354X product family to have a very simple compensation scheme, as the control to output transfer function always has a slope of -1. In addition, when critical conduction is reached, the voltage controlled current source becomes nearly ideal with a high output equivalent resistance.

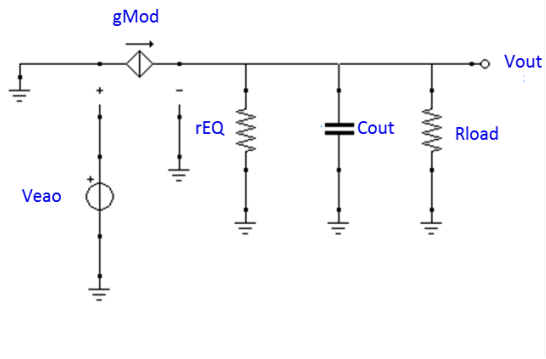


Figure 7 – *PI354X Small Signal Model Control-Output*

The control to output transfer function of the PI354X product family is defined as the gain from the output of the error amplifier , through the modulator and to the output voltage. The transfer function equation is shown in Equation (3), where gMOD is assumed to be 7S, rEQ = 0.4 Ohms, Cout = 600uF and Rload = 1 Ohm:

$$Gco(s) = \frac{gMOD}{\frac{1}{Rload} + \frac{1}{rEQ} + s(Cout)} \qquad (3)$$

The Control-Output transfer function (also known as the small signal modulator gain) has a single pole response determined by the parallel combination of Rload and rEQ and the output capacitor Cout. Equation (4) determines the frequency of the modulator pole:

$$Fpmod = \frac{1}{2 * \pi * \left(\frac{Rload * rEQ}{Rload + rEQ}\right) * Cout} \qquad (4)$$

Figure 8 depicts the small signal response of the modulator when perturbing EAO and measuring the differential gain and phase from EAO to Vout.

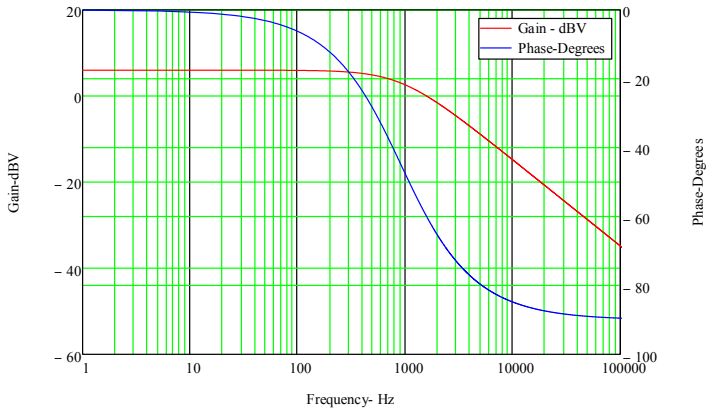


Figure 8 – *PI354X Control-Output Gain/Phase Example*

Error Amplifier

The small signal model of the error amplifier and compensator is shown in Figure 9. and the transfer function is shown in Equation 5, where in this example R1 = 2.3k, R2 = 1k, GMeao = 5.1mS, Chf=56pF, Ccomp = 4.7nF and Rzi = 5k. Here it is important to note that the only external component is Ccomp. The other components are internal to each specific model. See the data tables section “Soft Start, Tracking And Error Amplifier” for details.

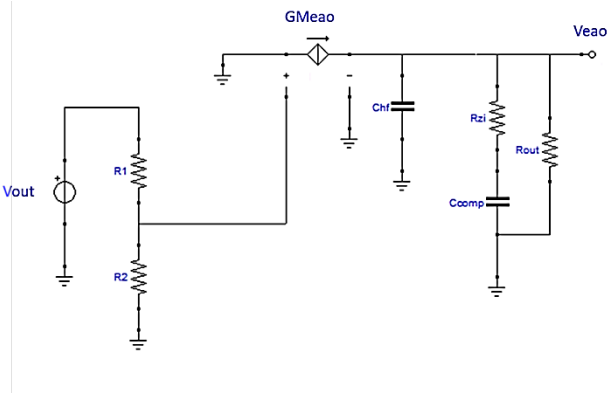


Figure 9 – *PI354X Error Amplifier Model*

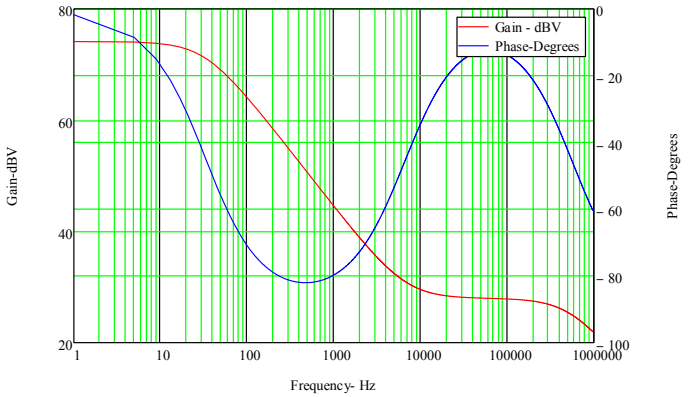


Figure 10 – *PI354X Input-Control Gain/Phase*

$$Ginctl(s) = GMeao * \frac{Rout + s(Rzi * Ccomp * Rout)}{1 + s * (Ccomp + Chf) + s^{2*}(Chf * Ccomp * Rzi)} * \frac{R2}{R1 + R2} \qquad (5)$$

The transfer function of the error amplifier and compensator (also known as the Input To Control transfer function) reveals the response of a Type II amplifier with a low frequency pole determined by Equation(6), a zero which sets the mid-band gain determined by Equation (7) and a high frequency pole determined by Equation (8). Figure 10 shows the calculated Input To Control transfer function. Multiplying Equation (3) by Equation (5) ; described by Equation (9), results in the total loop gain (also known as the Output To Input transfer function). A graph is shown in Figure 11. The strategy is to set the zero such that the mid-band gain allows a high crossover frequency while providing maximum phase boost at crossover, with proper gain and phase margin.

$$Fplf = \frac{1}{2 * \pi * (Rzi + Rout) * (Ccomp + Chf)} = 33Hz \qquad (6)$$

$$Fzmb = \frac{1}{2 * \pi * (Rzi // Rout) * Ccomp} = 6.8kHz \qquad (7)$$

$$Fphf = \frac{Chf + Ccomp}{2 * \pi * (Rzi // Rout) * Ccomp * Chf} = 580kHz \qquad (8)$$

$$Goutin(s) = Gco(s) * Ginctl(s) \qquad (9)$$

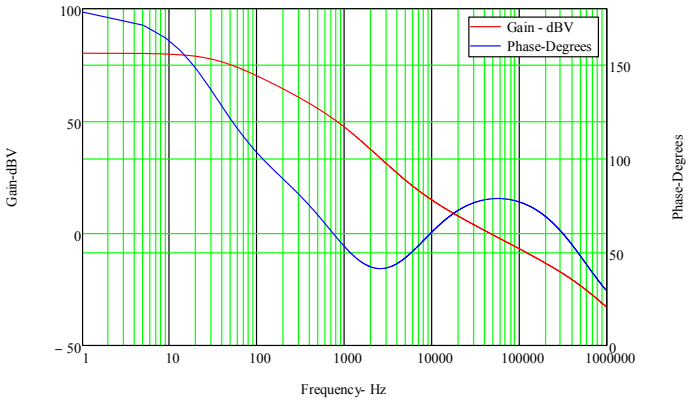


Figure 11 – *PI354X Output-Input Gain/Phase*

Lighting Mode (LGH)

The Lighting (LGH) mode allows the PI354X product family to be able to operate in constant current mode (CC) so that it can support a wide range of applications that require the ability to regulate current or voltage. Primary applications are LED lighting, battery / super-capacitor charging and high peak current pulse transient load applications. The PI354X product family can operate in dual modes, either as a constant voltage (CV) regulator or a constant current (CC) regulator. Both modes can be utilized in a single system. The PI354X family has a separate current amplifier, called LGH, and built in 100mV lighting reference that has its output connected to the EAO pin internally. If the current through an external shunt starts to develop 100mV at the LGH pin, the LGH amplifier will take over regulation by pulling down on the EAO output until the current is in regulation according to the designed shunt value. The LGH amplifier is a sink only TCA. It does not source current. In the event of an open LED string or open current signal, the voltage loop can be set to regulate the output voltage to a safe or desired value in CV mode.

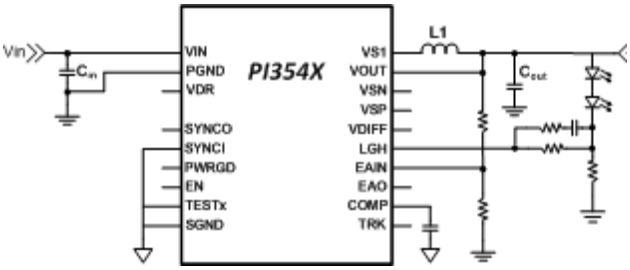


Figure 11 – *Lighting Configuration Using CC Mode*

When using the CC mode, it is important to set R1 and R2 appropriately to avoid voltage loop interaction with the current loop. In this case, the voltage setting at the EAIN pin should be set so that the error between it and the 1V reference is sufficient to force the EAO to be open loop and source current always. When not using the LGH amplifier, the LGH pin should be connected to SGND.

The LGH amplifier is able to sink more current than the error amplifier can source, thus avoiding arbitration issues when transitioning back and forth from LGH mode to voltage mode. The equation for setting the source current for EAO is shown in Equation (10).

$$Ieao = (Veain - Vref) * Gmea > 400uA \qquad (10)$$

LGH Amplifier Small Signal Model

A small signal model of the LGH amplifier is shown in Figure 11.

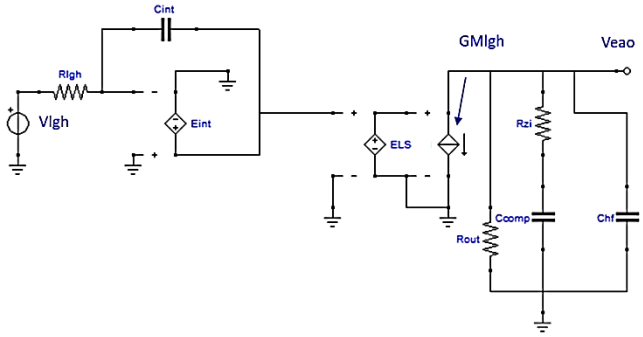


Figure 12 – *LGH Amplifier Small Signal Model*

The LGH amplifier consists of three distinct stages. The first is a wide bandwidth integrator stage, followed by a fixed gain level shift circuit. Finally, the level shift circuit drives a trans-conductance (TCA) amplifier with an open collector sink only output stage. Since the LGH output is internally connected to the output of the voltage error amplifier, the compensation components show up in the model and are used by both stages, depending on which one is in use. Only one stage should be in use at a time. When using LGH or if the LGH input rises above the internal reference, the voltage error amplifier acts as a 400uA current source pull up for the EAO pin.

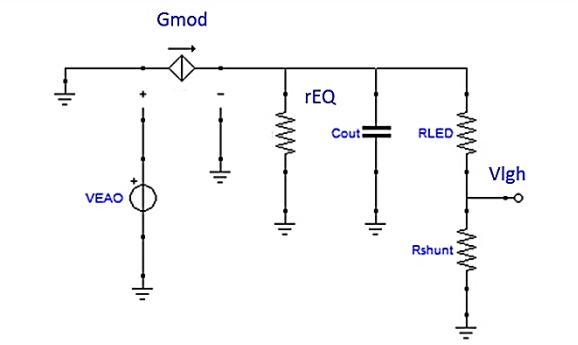


Figure 13 – *Lighting Application Modulator Gain Model*

Figure 13 shows a small signal model of the modulator gain when using the application circuit shown in Figure 11 with (2) 3.4V high current LED's in series. RLED is the series combination of the AC resistance of each LED, which is 0.2 Ohms. Rshunt is used to sense the current through the LED string. It has a value of 0.050 Ohms in this case. The other component values were defined earlier and remain the same values. Equation (11) defines the transfer function of the modulator and equation (12) defines the pole of transfer function. The transfer function of the LGH amplifier is defined in Equation 13. The open loop gain of Eint is 2500 and ELS = 4.4.

$$Gled(s) = gMOD * (rEQ * Rshunt)/((Rshunt + RLED + rEQ) + s(Cout * rEQ * RLED + Rshunt * rEQ * Cout)) \quad (11)$$

$$Fpled = \frac{1}{2 * \pi * ((RLED + Rshunt)//rEQ) * Cout} = 1.2kHz \quad (12)$$

$$Glgheao(s) = Eint(s) * ELS * GMlgh * \frac{Rout + s(Rzi * Ccomp * Rout)}{1 + s * (Ccomp + Chf) + s^{2*}(Chf * Ccomp * Rzi)} \quad (13)$$

Where:

$$Eint(s) = Eint * \frac{1}{1 + s * (Rlgh * Cint * Eint))} \quad (14)$$

The integrator pole is determined by the external input resistor Rlgh and the internal Cint, which is 20pF. Assuming Rlgh = 100k and Eint = 2500:

$$FpEint = \frac{1}{2 * \pi * (Rlght * Cint * Eint)} = 33Hz \quad (15)$$

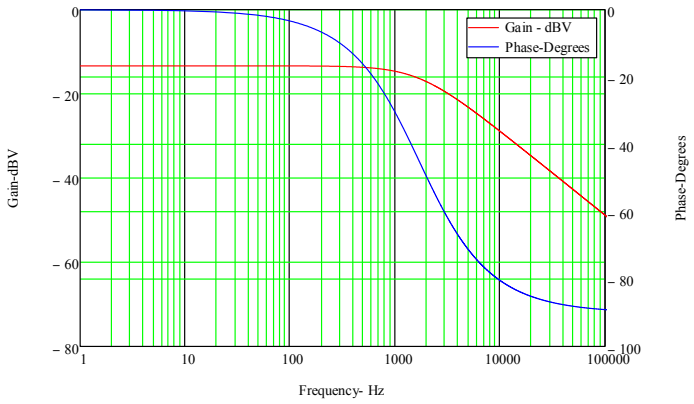


Figure 14 – *Gled(s) Gain/Phase Plot*

Figure 14 is the Bode plot of the Gled(s) transfer function, which in LGH mode is what needs to be compensated for by the LGH amplifier and compensator. This transfer function defines the gain and phase from the error amplifier output (EAO) to the current shunt Rshunt. Figure 17 is a plot of the transfer function Glgheao(s), which defines the gain and phase from the LGH pin (voltage across current sensing Rshunt) to EAO. As shown in Equation (13), the output is dependent on the integrator stage and the following trans-conductance stage. Figures 15 and 16 show the two individual sections that make up Equation (13) which produces Glgheao(s).

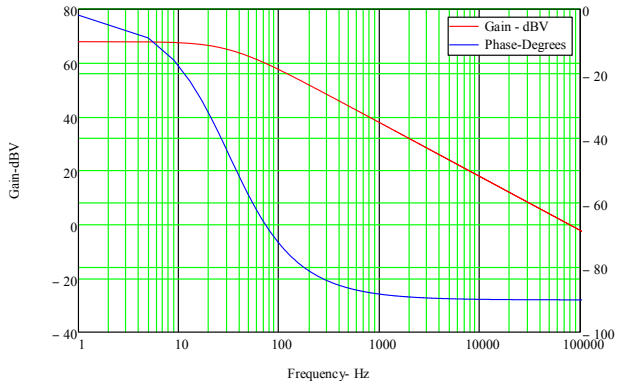


Figure 15 *– Eint(s) Gain/Phase Plot Rlgh = 100k*

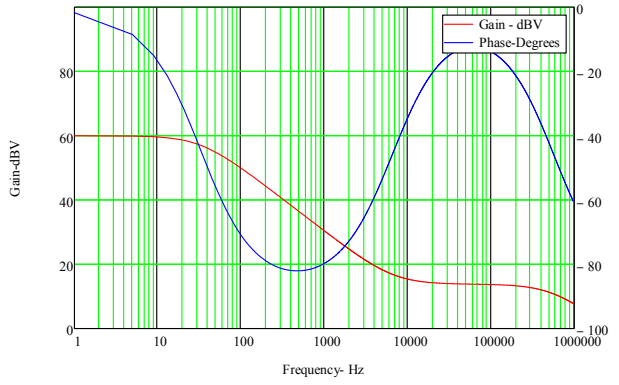


Figure 16 *– GMlgh(s) Gain/Phase Plot Voltage Loop Open*

The GMlgh(s) plot is from integrator to EAO with the voltage loop open and sourcing 400uA of current.

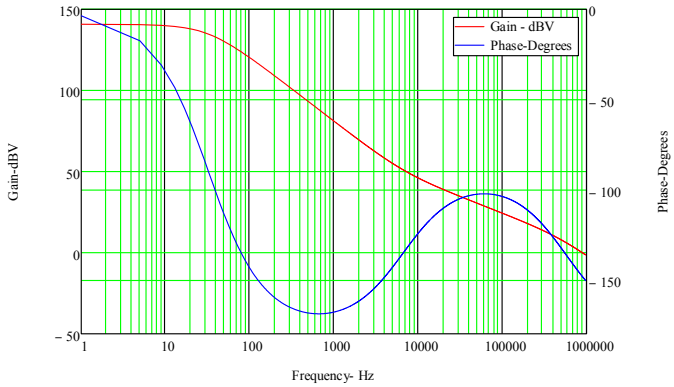


Figure 17 *– Glgheao(s) Gain/Phase Plot Rlgh = 100k*

When combining Figure 14 with Figure 17, it becomes clear that additional compensation is needed to have enough phase and gain margin like can be seen with the voltage loop plot. We can remedy that easily, by adding a series R-C in parallel with Rlgh as shown in the lighting application diagram in Figure 11. The capacitor will be chosen to work with Rlgh to add a zero approximately 1.2kHz before the zero provided by the GMlgh(s) transfer function (the trans-conductance stage of the LGH amplifier). This value will be chosen to be 270pF. The external added resistor will form a high frequency pole to roll the gain off at higher frequency. This pole will be set at approximately 120kHz so a common 4.99k resistor will be used. The resulting Bode plot with the new compensator of Glgheao(s) can be seen in Figure 18. Figure 19 shows the final Bode plot of the loop gain when using a lighting application with LED's operating in constant current mode. Note that it is very important to understand the AC resistance of the LED's that are being used. Please consult the LED manufacturer for details. For a series string, you should add the individual LED resistances and combine them into one lumped value to simplify the analysis.

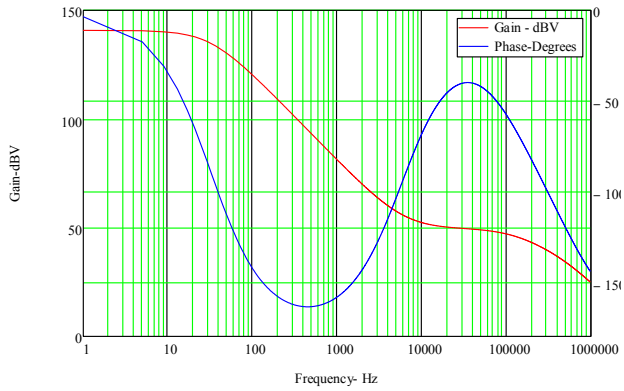


Figure 18 *– GMlgh(s) Gain/Phase Plot Compensated*

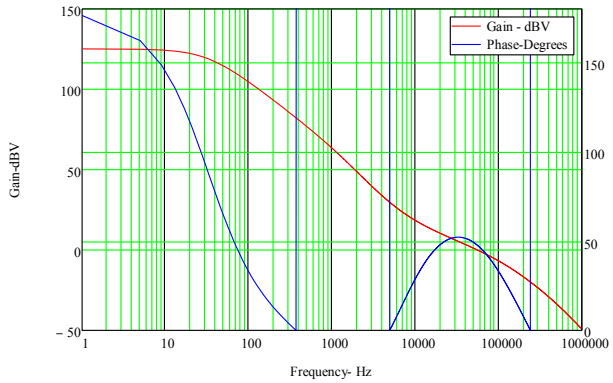


Figure 19 *– Lighting Application Loop Gain/Phase Plot*

Filter Considerations

The PI354X-00 requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI354X-00 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source. Table 4 shows the recommended input and output capacitors to be used for the PI354X-00 as well as per capacitor RMS ripple current and the input and output ripple voltages. Table 5 includes the recommended input and output ceramic capacitors.

It is very important to verify that the voltage supply source as well as the interconnecting lines are stable and do not oscillate.

Input Filter Case 1; Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e.: ceramic type):

The voltage source impedance can be modeled as a series R(line) L(line) circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be
verified:

$$R_{line} > \frac{L_{line}}{(Cin_{int} + Cin_{ext}) * |r\_EQin|} \qquad (16)$$

$$R_{line} \ll |r\_EQin| \qquad (17)$$

Where r_EQin can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation (17). However, R_{line} cannot be made arbitrarily low otherwise Equation (16) is violated and the system will show instability, due to an under-damped RLC input network.

Input Filter case 2; Inductive source and local, external input decoupling capacitance with significant RCIN_EXT ESR (i.e.: electrolytic type)

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor Lline. Notice that, the high performance ceramic capacitors CIN_INT within the PI354X-00 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$|r\_EQin| > R_{Cin_{ext}} \qquad (18)$$

$$\frac{L_{line}}{(Cin_{int} * R_{Cin_{ext}})} > |r\_EQin| \quad (19)$$

Equation (19) shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (CIN_EXT) – the system will be under-damped and may even become destabilized. As noted, an octave of design margin in satisfying Equation (18) should be considered the minimum.

When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

VDR Bias Regulator

The VDR internal bias regulator is a ZVS switching regulator that resides internal to the PI354X product family. It is intended strictly for use to power the internal controller and driver circuitry. The power capability of this regulator is sized only for the PI354X, with adequate reserve for the application it was intended for. It may be used for as a pull-up source for open collector applications and for other very low power use with the following restrictions:

1. No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation.
2. All loads must be locally de-coupled using a 0.1uF ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1k. which forms a loss pass filter and limits the total current to 5mA.

System Design Considerations

1. Inductive loads- As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI354X is recommended for these applications.
2. Low voltage operation – there is no isolation from an SELV power system. Powering low voltage loads from input voltages as high as 60V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS gating an external load switch is an example of such protection.
3. Use of Lighting Mode (LGH) as a battery charger is certainly very feasible. It is fashionable to design these chargers such that the battery is always connected to it. Since the Buck topology is not isolated, shorting the input terminals or capacitors of an unpowered regulator/charger could allow damaging current flow through the body diode of the high side MOSFET that would be unprotected by a conventional input fuse. It is recommended to connect the PI354X family to the battery using an active ORing device if LGH mode is used as a constant current battery charger. The same should be considered for super-capacitor applications as well.

Device	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} Ceramic X5R	C_{OUTPUT} Ceramic X5R	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mVpp)	Output Ripple (mVpp)	Transient Deviation (mVpk)	Recovery Time (µs)	Load Step (A) (Slew/µs)
PI3542	48	10	5x2.2µF 100V	6x100µF	0.7	1.32	416	47	-/+80	40	5 (1A/µs)
		5					220	22			
PI3543	48	10	5x2.2µF 100V	6x100µF	0.8	1.3	464	61.6	-/+90	40	5 (1A/µs)
		5					230	31			
PI3545	48	10	5x2.2µF 100V	6x47µF	.88	1.37	485	62	-/+150	40	5 (1A/µs)
		5					245	32			
PI3546	48	9	5x2.2µF 100V	6x10µF	1.12	1.26	880	114	-/+300	20	4.5 (1A/µs)
		4.5					125	33			

Table 4 - *Recommended input and output capacitance*

TDK PART NUMBER	DESCRIPTION	MURATA PART NUMBER	DESCRIPTION
C3225X7S1H1106M250AB	2.2uF 100V 1210 X7R	GRM31CR60J107ME39L	100uF 6.3V 1206 X7R
		GRM31CR61A476ME15L	47uF 10V 1206 X5R
C3225X7S1H106M250AB	10uF 50V 1210 X7R	GRM32ER61H106MA12	10uF 50V 1210 X7R

Table 5 *- Capacitor manufacturer part numbers*

Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI354X-00 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 20. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

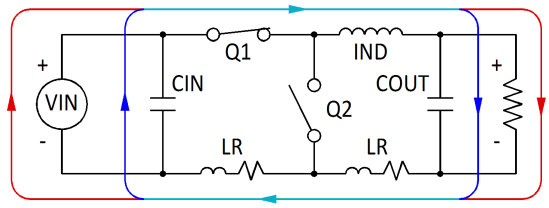


Figure 20 - *Typical Buck Converter*

The path between the COUT and CIN capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 21, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI354X-00 performance.

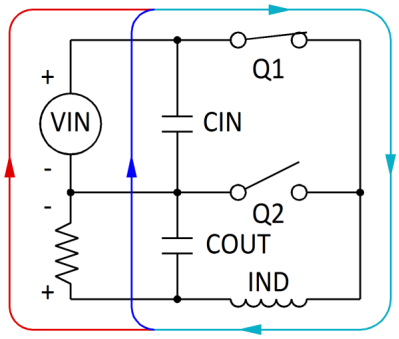


Figure 21 *- Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of CIN's current is used to satisfy the output load and to recharge the COUT capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the COUT capacitor as shown in Figure 22. During this period CIN is also being recharged by the VIN. Minimizing CIN loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the CIN loop and COUT loop is vital to minimize switching and GND noise.

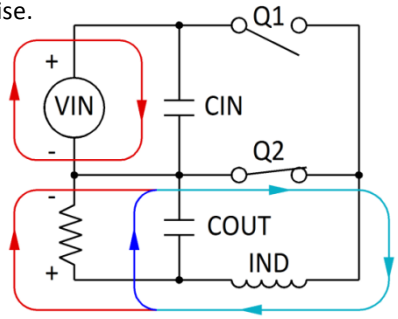


Figure 22 - *Current flow: Q2 closed*

The recommended component placement, shown in Figure 23, illustrates the tight path between CIN and COUT (and VIN and VOUT) for the high AC return current. This optimized layout is used on the PI354X-00 evaluation board.

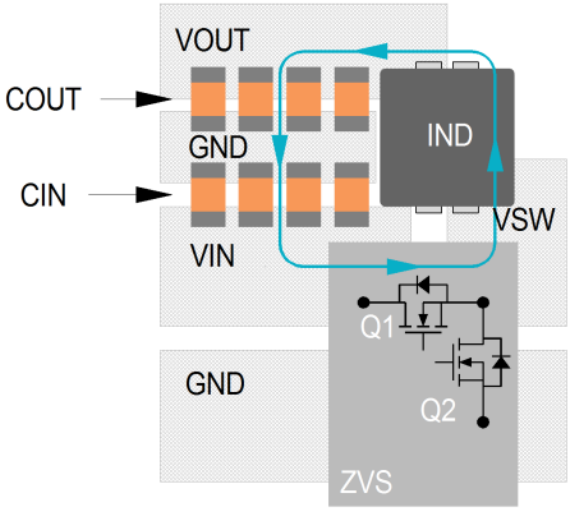


Figure 23 - *Recommended component placement and metal routing*

Recommended PCB Footprint and Stencil

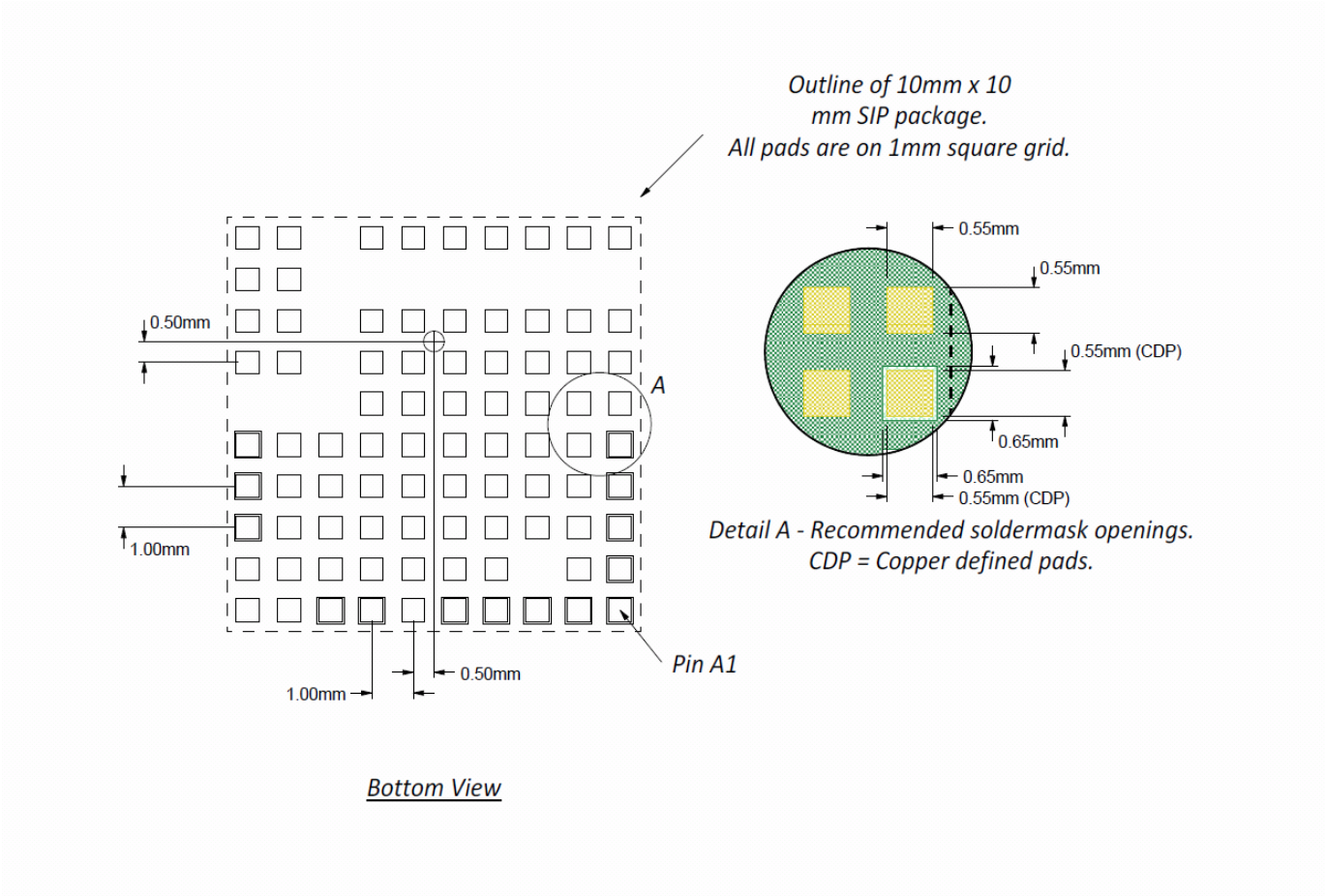
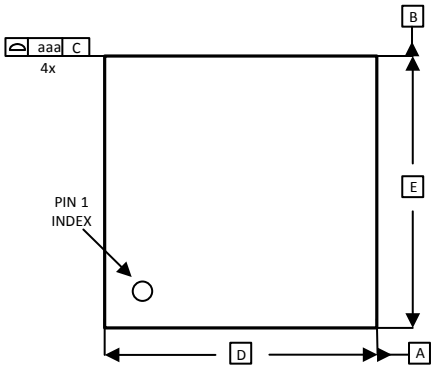


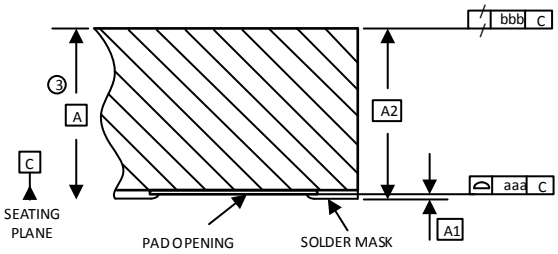
Figure 24 - *Recommended Receiving PCB footprint.*

Figure 24 details the recommended receiving footprint for PI354X-00 10mm x 10mm package. All pads should have a final copper size of 0.55mm x 0.55mm, whether they are solder-mask defined or copper defined, on a 1mm x 1mm grid. All stencil openings are 0.45mm when using either a 5mil or 6mil stencil.

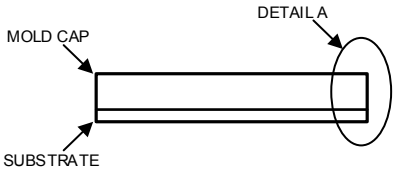
Package Drawings



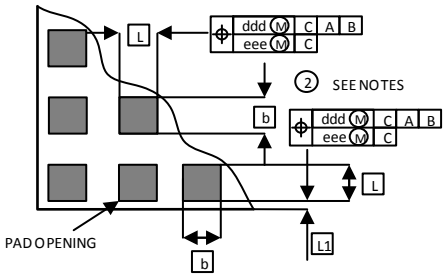
PACKAGE TOP VIEW



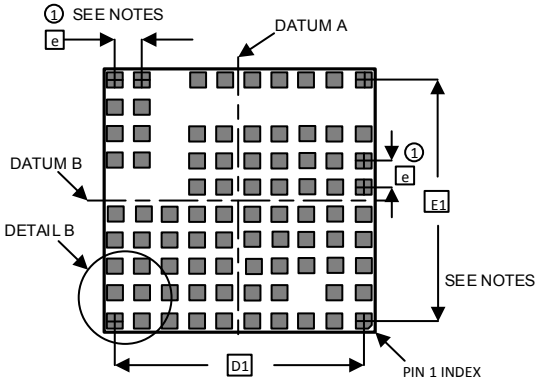
DETAIL A



PACKAGE SIDE VIEW



DETAIL B



PACKAGE BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	2.49	2.56	2.63
A1	–	–	0.04
A2	–	–	2.59
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D	10.00 BSC		
E	10.00 BSC		
D1	9.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		
L1	0.175	0.225	0.275
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.08

DIMENSIONS

NOTES

1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED PAD OPENING.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
4. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
5. ALL DIMENSIONS IN MILLIMETERS.

Warranty

Information furnished by Vicor is believed to be accurate and reliable. However, no responsibility is assumed by Vicor for its use. Vicor makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication. Vicor reserves the right to make changes to any products, specifications, and product descriptions at any time without notice. Information published by Vicor has been checked and is believed to be accurate at the time it was printed; however, Vicor assumes no responsibility for inaccuracies. Testing and other quality controls are used to the extent Vicor deems necessary to support Vicor's product warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.
Specifications are subject to change without notice.

Vicor's Standard Terms and Conditions

All sales are subject to Vicor's Standard Terms and Conditions of Sale, which are available on Vicor's webpage or upon request.

Product Warranty

In Vicor's standard terms and conditions of sale, Vicor warrants that its products are free from non-conformity to its Standard Specifications (the "Express Limited Warranty"). This warranty is extended only to the original Buyer for the period expiring two (2) years after the date of shipment and is not transferable.

UNLESS OTHERWISE EXPRESSLY STATED IN A WRITTEN SALES AGREEMENT SIGNED BY A DULY AUTHORIZED VICOR SIGNATORY, VICOR DISCLAIMS ALL REPRESENTATIONS, LIABILITIES, AND WARRANTIES OF ANY KIND (WHETHER ARISING BY IMPLICATION OR BY OPERATION OF LAW) WITH RESPECT TO THE PRODUCTS, INCLUDING, WITHOUT LIMITATION, ANY WARRANTIES OR REPRESENTATIONS AS TO MERCHANTABILITY, FITNESS FOR PARTICULAR PURPOSE, INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT, OR ANY OTHER MATTER.

This warranty does not extend to products subjected to misuse, accident, or improper application, maintenance, or storage. Vicor shall not be liable for collateral or consequential damage. Vicor disclaims any and all liability arising out of the application or use of any product or circuit and assumes no liability for applications assistance or buyer product design. Buyers are responsible for their products and applications using Vicor products and components. Prior to using or distributing any products that include Vicor components, buyers should provide adequate design, testing and operating safeguards.

Vicor will repair or replace defective products in accordance with its own best judgment. For service under this warranty, the buyer must contact Vicor to obtain a Return Material Authorization (RMA) number and shipping instructions. Products returned without prior authorization will be returned to the buyer. The buyer will pay all charges incurred in returning the product to the factory. Vicor will pay all reshipment charges if the product was defective within the terms of this warranty.

Life Support Policy

VICOR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF VICOR CORPORATION. As used herein, life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness. Per Vicor Terms and Conditions of Sale, the user of Vicor products and components in life support applications assumes all risks of such use and indemnifies Vicor against all liability and damages.

Intellectual Property Notice

Vicor and its subsidiaries own Intellectual Property (including issued U.S. and Foreign Patents and pending patent applications) relating to the products described in this data sheet. No license, whether express, implied, or arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Interested parties should contact Vicor's Intellectual Property Department.

The products described on this data sheet are protected by the following U.S. Patents Numbers: RE40,072; 6,788,033; 7,154,250; 6,421,262; 8,669,744; and for use under: 6,984,965; 6,975,098.

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810 USA

Picor Corporation
51 Industrial Drive
North Smithfield, RI 02896 USA

Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А