

1°C Multiple Temperature Sensor with Beta Compensation and Hottest of Thermal Zones

PRODUCT FEATURES

Datasheet

General Description

The EMC1046/EMC1047 are high accuracy, low cost, System Management Bus (SMBus) temperature sensors. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to CPU diodes requiring the BJT or transistor model) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

Each device provides $\pm 1^\circ$ accuracy for external diode temperatures and $\pm 2^\circ$ accuracy for the internal diode temperature. The EMC1046/EMC1047 monitor up to seven temperature channels (up to six external and one internal).

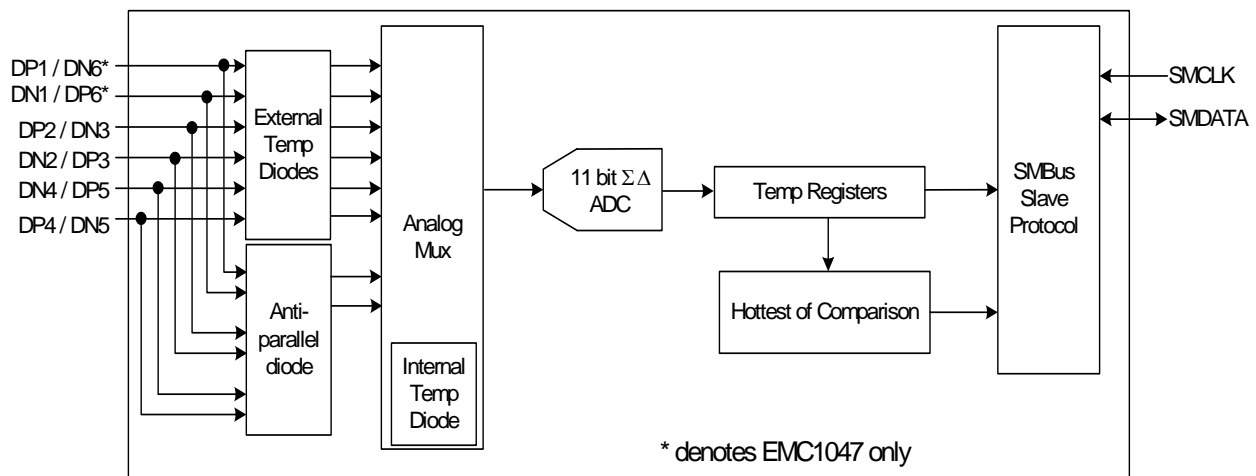
Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

Features

- Designed to support 45nm, 65nm, and 90nm CPU diodes
- Supports diodes requiring the BJT or transistor model
- Resistance Error Correction (up to 100 Ohms)
- Up to six External Temperature Monitors
 - $\pm 1^\circ\text{C}$ Accuracy ($60^\circ\text{C} < T_{\text{DIODE}} < 100^\circ\text{C}$)
 - 0.125°C Resolution
 - Supports up to 2.2nF filter capacitor
 - Anti-parallel diodes for extra diode support and compact design
- Internal Temperature Monitor
 - $\pm 2^\circ\text{C}$ accuracy
- 3.3V Supply Voltage
- Available in a 10-pin TSSOP lead-free RoHS Compliant package

Block Diagram



ORDER NUMBERS:

| ORDERING NUMBER | PACKAGE | FEATURES | DIODE MODES SUPPORTED | SMBUS ADDRESS |
|-------------------|---|--|---------------------------------|---------------|
| EMC1046-1-AIZL-TR | 10-pin TSSOP (Lead-Free RoHS Compliant) | Up to 5 external diodes. "Hottest Of" temperature comparison | Intel CPU, 3904, AMD with setup | 1001_100(r/w) |
| EMC1046-6-AIZL-TR | 10-pin TSSOP (Lead-Free RoHS Compliant) | Up to 5 external diodes. "Hottest Of" temperature comparison | Intel CPU, 3904, AMD with setup | 1001_101(r/w) |
| EMC1047-1-AIZL-TR | 10-pin TSSOP (Lead-Free RoHS Compliant) | Up to 6 external diodes. "Hottest Of" temperature comparison | Intel CPU, 3904, AMD with setup | 1001_100(r/w) |
| EMC1047-2-AIZL-TR | 10-pin TSSOP (Lead-Free RoHS Compliant) | Up to 6 external diodes. "Hottest Of" temperature comparison | Intel CPU, 3904, AMD with setup | 1001_000(r/w) |

Reel Size is 4,000 pieces



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Chapter 1 Pin Description

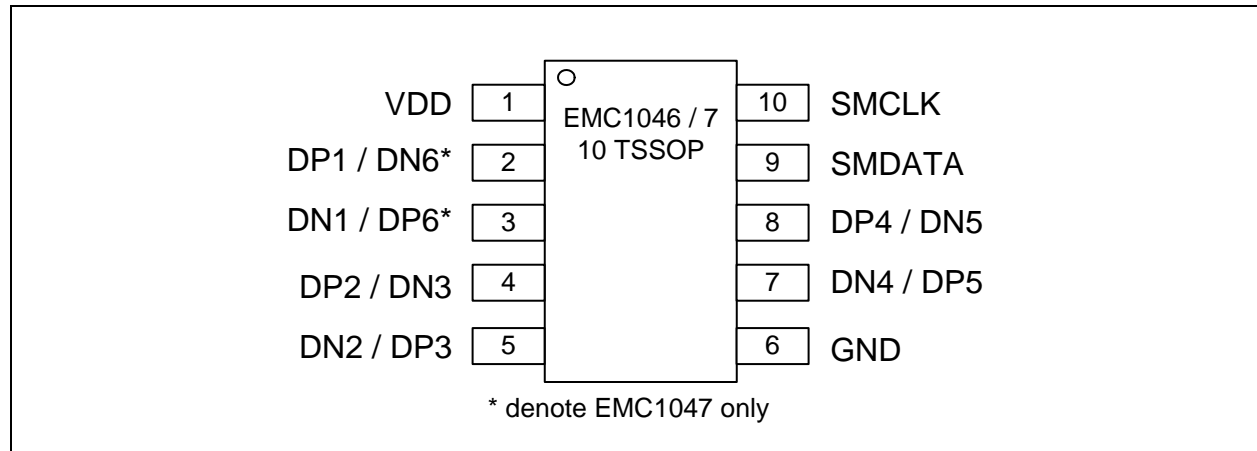


Figure 1.1 EMC1046/EMC1047 Pin Diagram

Table 1.1 EMC1046/EMC1047 Pin Description

| PIN NUMBER | NAME | FUNCTION | TYPE |
|------------|------------|--|-------|
| 1 | VDD | Power supply | Power |
| 2 | DP1 / DN6* | DP1 - External Diode 1 positive (anode) connection (EMC1046) | AIO |
| | | DP1 / DN6 - External Diode 1 positive (anode) connection and External Diode 6 negative (cathode) connection (EMC1047) | |
| 3 | DN1 / DP6* | DN1 - External diode 1 negative (cathode) connection (EMC1046) | AIO |
| | | DN1 / DP6* - External diode 1 negative (cathode) connection and External Diode 6 positive (anode) connection (EMC1047) | |
| 4 | DP2 / DN3 | External Diode 2 positive (anode) connection and External Diode 3 negative (cathode) connection | AIO |
| 5 | DN2 / DP3 | External diode 2 negative (cathode) connection and External Diode 3 positive (anode) connection | AIO |
| 6 | GND | Ground Connection | Power |
| 7 | DN4 / DP5 | External diode 4 negative (cathode) connection and External Diode 5 positive (anode) connection | AIO |

Table 1.1 EMC1046/EMC1047 Pin Description (continued)

| PIN NUMBER | NAME | FUNCTION | TYPE |
|------------|-----------|---|-----------|
| 8 | DP4 / DN5 | External Diode 4 positive (anode) connection and External Diode 5 negative (cathode) connection | AIO |
| 9 | SMDATA | SMBus Data input/output - requires external pullup resistor | DIOD (5V) |
| 10 | SMCLK | SMBus Clock input - requires external pullup resistor | DI (5V) |

The pin types are described below. All pins labelled (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

Table 1.2 Pin Type

| PIN TYPE | FUNCTION |
|----------|--|
| Power | Used to supply either VDD or GND to the device |
| DI | 5V tolerant digital input |
| OD | 5V tolerant Open drain digital output. Requires a pull-up resistor |
| DIOD | 5V tolerant bi-directional digital input / open-drain output. Requires a pull-up resistor. |
| AIO | Analog input / output used for external diodes or analog inputs |

Chapter 2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

| DESCRIPTION | RATING | UNIT |
|---|--------------------------------|------|
| Supply Voltage (V_{DD}) | -0.3 to 4.0 | V |
| Voltage on 5V tolerant pins (V_{5VT_pin}) | -0.3 to 5.5 | V |
| Voltage on 5V tolerant pins ($ V_{5VT_pin} - V_{DD} $) (see Note 2.1) | -0.3 to 3.6 | V |
| Voltage on any other pin to Ground | -0.3 to $V_{DD} + 0.3$ | V |
| Operating Temperature Range | -40 to +125 | °C |
| Storage Temperature Range | -55 to +150 | °C |
| Lead Temperature Range | Refer to JEDEC Spec. J-STD-020 | |
| Package Thermal Characteristics for MSOP-10 | | |
| Thermal Resistance (θ_{j-a}) | 132.2 | °C/W |
| ESD Rating, All pins HBM | 2000 | V |

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 2.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the device is unpowered.

2.2 Electrical Specifications

Table 2.2 Electrical Specifications

| $V_{DD} = 3.0V$ to $3.6V$, $T_A = -40^\circ C$ to $125^\circ C$, all typical values at $T_A = 27^\circ C$ unless otherwise noted. | | | | | | |
|---|----------|-----|-----|-----|-------|--|
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNITS | CONDITIONS |
| DC Power | | | | | | |
| Supply Voltage | V_{DD} | 3.0 | 3.3 | 3.6 | V | |
| Supply Current | I_{DD} | | 395 | 450 | uA | 1 conversion / sec, dynamic averaging disabled |
| Supply Current | I_{DD} | | 700 | 960 | uA | 4 conversions / sec, dynamic averaging enabled |

Table 2.2 Electrical Specifications (continued)

| V _{DD} = 3.0V to 3.6V, T _A = -40°C to 125°C, all typical values at T _A = 27°C unless otherwise noted. | | | | | | |
|--|---------------------|-----|-------|------|-------|---|
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNITS | CONDITIONS |
| Standby Supply Current | I _{STBY} | | 200 | | uA | RUN / STOP bit set. Monitoring disabled. |
| Internal Temperature Monitor | | | | | | |
| Temperature Accuracy | | | ±0.25 | ±1 | °C | 0°C < T _A < 100°C |
| | | | | ±2 | °C | -40°C < T _A < 125°C |
| Temperature Resolution | | | 0.125 | | °C | |
| External Temperature Monitor | | | | | | |
| Temperature Accuracy | | | ±0.25 | ±1 | °C | +40°C < T _{DIODE} < +110°C 0°C < T _A < 110°C |
| | | | | ±0.5 | ±2 | °C |
| Temperature Resolution | | | 0.125 | | °C | |
| Conversion Time all Channels | t _{CONV} | | 190 | | ms | default settings |
| Capacitive Filter | C _{FILTER} | | 2.2 | 2.7 | nF | Connected across external diode |
| Resistance Error Correction | R _{SERIES} | | | 100 | Ω | In series with DP and DN lines |
| Leakage Current | I _{LEAK} | | | ±5 | uA | powered or unpowered T _A < 85°C |
| Power Up Timing | | | | | | |
| First conversion ready | t _{CONV_f} | | | 300 | ms | Time after power up before all channels updated with valid data |
| SMBus delay | t _{SMB_d} | | | 15 | ms | Delay before SMBus communications should be sent by host |

2.3 SMBus Electrical Characteristics

Table 2.3 SMBus Electrical Specifications

| V _{DD} = 3.0V to 3.6V, T _A = -40°C to 125°C, all typical values are at T _A = 27°C unless otherwise noted. | | | | | | |
|--|-----------------------------------|------|-----|-----------------|-------|---|
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNITS | CONDITIONS |
| SMBus Interface | | | | | | |
| Input High Voltage | V _{IH} | 2.0 | | V _{DD} | V | 5V Tolerant |
| Input Low Voltage | V _{IL} | -0.3 | | 0.8 | V | 5V Tolerant |
| Input High/Low Current | I _{IH} / I _{IL} | | | ±5 | uA | Powered or unpowered T _A < 85°C |
| Hysteresis | | | 420 | | mV | |

Table 2.3 SMBus Electrical Specifications (continued)

| V _{DD} = 3.0V to 3.6V, T _A = -40°C to 125°C, all typical values are at T _A = 27°C unless otherwise noted. | | | | | | |
|--|---------------------|-----|-----|------|-------|---|
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNITS | CONDITIONS |
| Input Capacitance | C _{IN} | | 5 | | pF | |
| Output Low Sink Current | I _{OL} | 8.2 | | 15 | mA | SMDATA = 0.4V |
| SMBus Timing | | | | | | |
| Clock Frequency | f _{SMB} | 10 | | 400 | kHz | |
| Spike Suppression | t _{SP} | | | 50 | ns | |
| Bus free time Start to Stop | t _{BUF} | 1.3 | | | us | |
| Hold Time: Start | t _{HD:STA} | 0.6 | | | us | |
| Setup Time: Start | t _{SU:STA} | 0.6 | | | us | |
| Setup Time: Stop | t _{SU:STP} | 0.6 | | | us | |
| Data Hold Time | t _{HD:DAT} | 0.3 | | | us | |
| Data Setup Time | t _{SU:DAT} | 100 | | | ns | |
| Clock Low Period | t _{LOW} | 1.3 | | | us | |
| Clock High Period | t _{HIGH} | 0.6 | | | us | |
| Clock/Data Fall time | t _{FALL} | | | 300 | ns | Min = 20+0.1C _{LOAD} ns |
| Clock/Data Rise time | t _{RISE} | | | 300 | ns | Min = 20+0.1C _{LOAD} ns f _{SMB} > 100kHz |
| Clock/Data Rise time | t _{RISE} | | | 1000 | ns | Min = 20+0.1C _{LOAD} ns f _{SMB} ≤ 100kHz |
| Capacitive Load | C _{LOAD} | | | 400 | pF | per bus line |

Chapter 3 System Management Bus Interface Protocol

3.1 System Management Bus Interface Protocol

The EMC1046/EMC1047 communicate with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in [Figure 3.1](#).

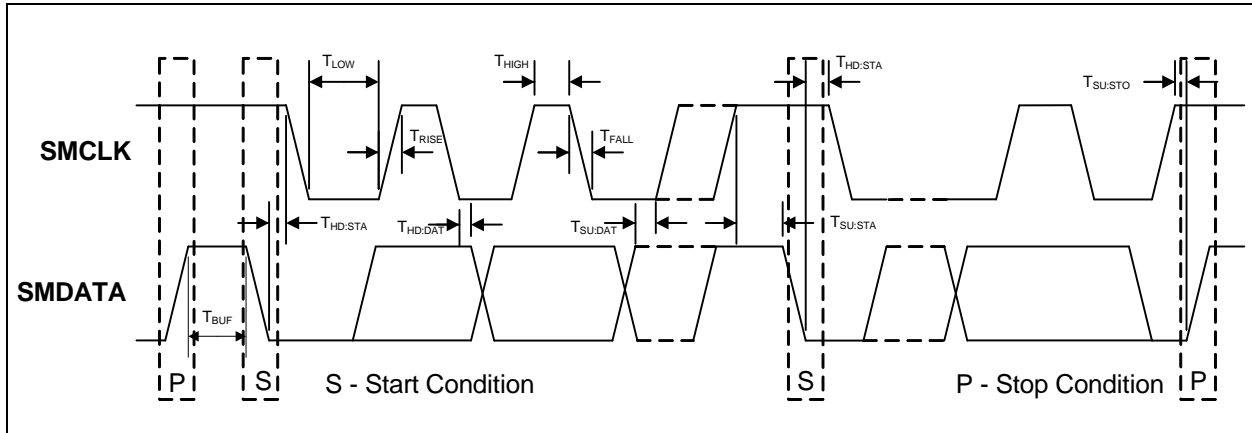


Figure 3.1 SMBus Timing Diagram

The EMC1046/EMC1047 are SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, and Receive Byte, as valid protocols as shown below.

All of the below protocols use the convention in [Table 3.1](#).

Table 3.1 Protocol Format

| DATA SENT TO DEVICE | DATA SENT TO THE HOST |
|---------------------|-----------------------|
|---------------------|-----------------------|

Attempting to communicate with the EMC1046/EMC1047 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

3.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below [Table 3.2](#):

Table 3.2 Write Byte Protocol

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | REGISTER DATA | ACK | STOP |
|--------|---------------|----|-----|------------------|-----|---------------|-----|--------|
| 1 -> 0 | 1001_100 | 0 | 0 | XXh | 0 | XXh | 0 | 0 -> 1 |

3.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in [Table 3.3](#).

Table 3.3 Read Byte Protocol

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | START | SLAVE ADDRESS | RD | ACK | REGISTER DATA | NACK | STOP |
|-------|---------------|----|-----|------------------|-----|-------|---------------|----|-----|---------------|------|------|
| 1->0 | 1001_100 | 0 | 0 | XXh | 0 | 0->1 | 1001_100 | 1 | 0 | XXh | 1 | 0->1 |

3.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in [Table 3.4](#).

Table 3.4 Send Byte Protocol

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | STOP |
|-------|---------------|----|-----|------------------|-----|------|
| 1->0 | 1001_100 | 0 | 0 | XXh | 0 | 1->0 |

3.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in [Table 3.5](#).

Table 3.5 Receive Byte Protocol

| START | SLAVE ADDRESS | RD | ACK | REGISTER DATA | NACK | STOP |
|-------|---------------|----|-----|---------------|------|------|
| 1->0 | 1001_100 | 1 | 0 | XXh | 1 | 1->0 |

3.6 SMBus Address

The EMC1046/EMC1047-1 devices respond to the 7-bit slave address 1001_100xb.

The EMC1046-6 will respond to the 7-bit slave address 1001_101xb.

The EMC1047-2 will respond to the 7-bit slave address 1001_000xb.

Note: Other addresses are available. Contact SMSC for more information.

3.7 SMBus Timeout

The EMC1046/EMC1047 support SMBus Timeout. If the clock line is held low for longer than 30ms, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit in the Consecutive Alert Register (see [Section 5.9](#)).

Chapter 4 Product Description

The EMC1046/EMC1047 are SMBus temperature sensors. The EMC1046/EMC1047 monitor up to six (6) external diodes and one internal diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1046/EMC1047 and using that data to control the speed of one or more fans.

Because the EMC1046/EMC1047 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available devices without resistance error correction. As well, the automatic beta detection feature means that there is no need to program the device according to which type of diode is present. Therefore, the device can power up ready to operate for any system configuration including those diodes that require the BJT or transistor model.

Figure 4.1 shows a system level block diagram of the EMC1046/EMC1047.

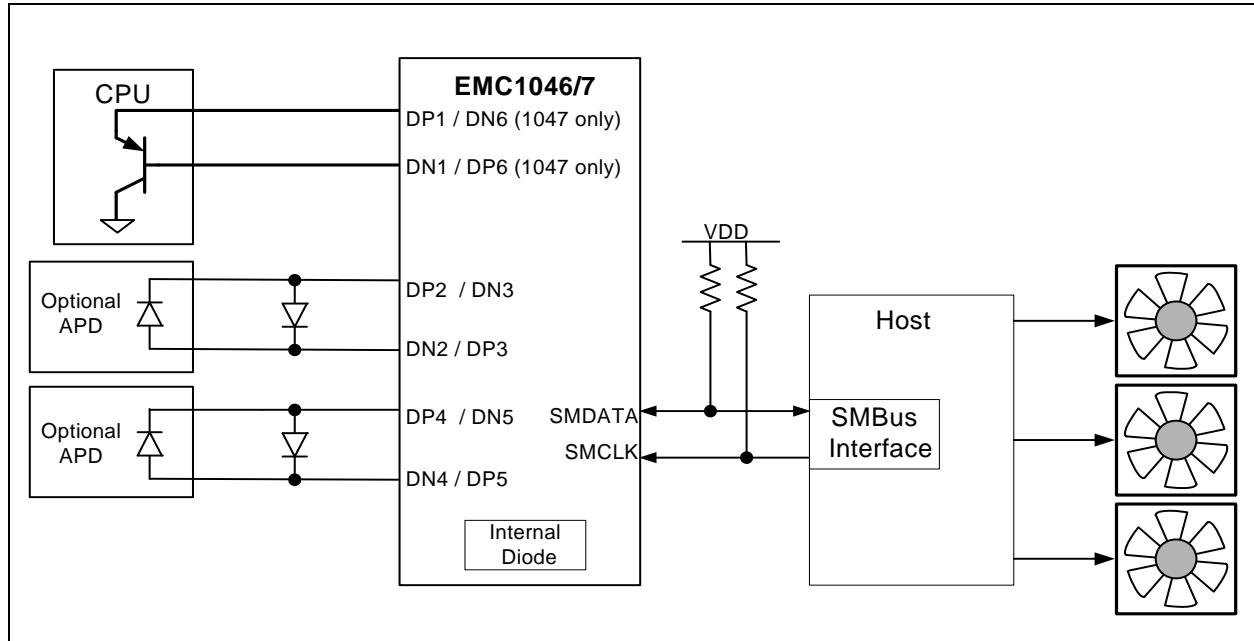


Figure 4.1 System Diagram for EMC1046/EMC1047

4.1 Modes of Operation

The EMC1046/EMC1047 have two modes of operation.

- Active (Run) - In this mode of operation, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion and the limits are checked. In Active mode, writing to the one-shot register will do nothing.
- Standby (Stop) - In this mode of operation, the majority of circuitry is powered down to reduce supply current. The temperature data is not updated and the limits are not checked. In this mode of operation, the SMBus is fully active and the part will return requested data. Writing to the one-shot register will enable the device to update all temperature channels. Once all the channels are updated, the device will return to the Standby mode.

4.2 Temperature Monitoring

The EMC1046/EMC1047 can monitor the temperature of up to six (6) externally connected diodes as well as the internal or ambient temperature. Each channel is configured with the following features enabled or disabled based on user settings and system requirements.

APPLICATION NOTE: When measuring a 45nm CPU diode, the reported temperature has an error of approximately +1.5C at 100°C. This error is related to non-perfect ideality in the CPU diode.

4.2.1 Resistance Error Correction

The EMC1046/EMC1047 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of series resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC1046/EMC1047 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

4.2.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. Compensating for this error is also known as implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC1046/EMC1047 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use.

4.2.3 Digital Averaging

To reduce the effect of noise and temperature spikes on the reported temperature, all of the external diode channels use digital averaging. This averaging acts as a running average using the previous four measured values.

The default setting is to have digital averaging disabled for all channels. It can be enabled for each channel individually by the Filter Control Register (see [Section 5.18](#)).

4.2.4 “Hottest Of” Comparison

At the end of every measurement cycle, the EMC1046/EMC1047 compares all of the user selectable External Diode channels to determine which of these channels is reporting the hottest temperature. The hottest temperature is stored in the Hottest Temperature Registers and the appropriate status bit in the Hottest Status Register is set. As an optional feature, the EMC1046/EMC1047 can also flag an event if the hottest temperature channel changes. For example, suppose that External Diode channels 1, 3, and 4 are programmed to be compared in the “Hottest Of” Comparison. If the External Diode 1 channel reports the hottest temperature of the three, its temperature is copied into the Hottest Temperature Registers (in addition to the External Diode 1 Temperature registers) and it is flagged in the Hottest Status bit. If, on the next measurement, the External Diode 3 channel temperature has increased such that it is now the hottest temperature, the EMC1046/EMC1047 can flag this event.

4.2.5 Conversion Rates

The EMC1046/EMC1047 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in [Section 5.5](#). The default conversion rate is 4 conversions per second. Other available conversion rates are shown in [Table 5.7](#).

4.2.6 Dynamic Averaging

Dynamic averaging causes the EMC1046/EMC1047 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see [Section 5.5](#)). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 4x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging also applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in [Table 4.1](#) for the EMC1046/EMC1047.

Table 4.1 Supply Current vs. Conversion Rate for EMC1046/EMC1047

| CONVERSION RATE | AVERAGE SUPPLY CURRENT | | AVERAGING FACTOR (BASED ON 11-BIT OPERATION) | |
|---|------------------------|----------|--|----------|
| | ENABLED (DEFAULT) | DISABLED | ENABLED (DEFAULT) | DISABLED |
| 1 / sec | 605uA | 395uA | 4x | 1x |
| 2 / sec | 635uA | 465uA | 2x | 1x |
| 4 / sec (default) | 700uA | 700uA | 1x | 1x |
| Continuous (see Table 5.8) | 825uA | 825uA | 0.5x | 0.5x |

4.3 Diode Connections

The diode connection for the External Diode 1 channel is determined based on the selected device. For the EMC1046, this channel can support a diode-connected transistor (such as a 2N3904) or a substrate transistor (such as those found in an CPU or GPU) as shown in [Figure 4.2](#). Anti-parallel diodes are not supported on the External Diode 1 channel.

For the EMC1047, all channels support anti-parallel diodes. If this function is enabled for a specific channel (see [Section 5.17](#)), then both the normal and anti-parallel diodes must use diode connected transistors. Otherwise, they may use a diode connected transistor or a substrate transistor.

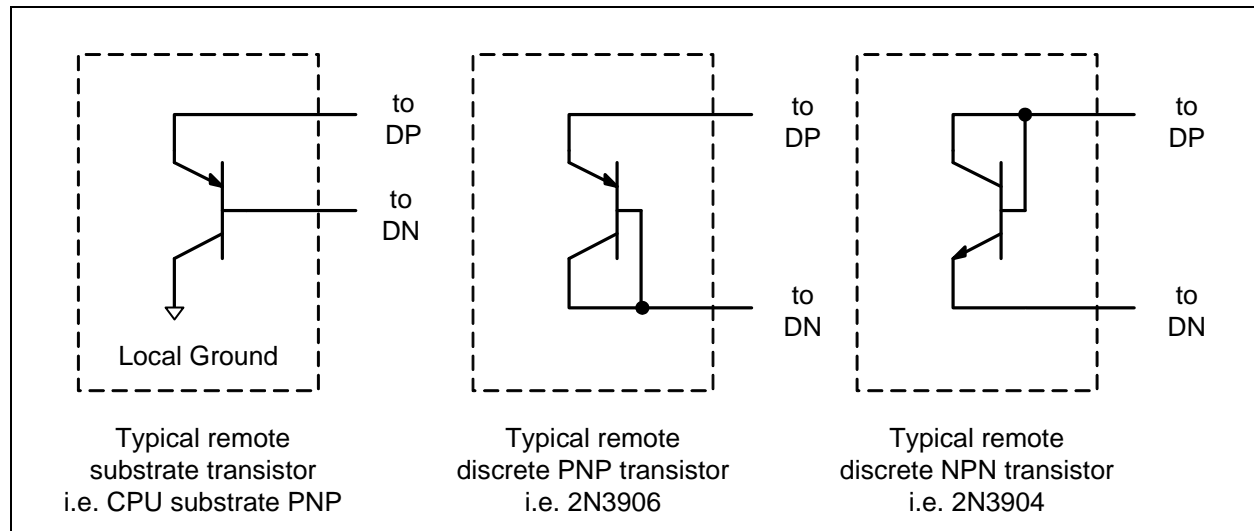


Figure 4.2 Diode Connections

4.3.1 Diode Faults

The EMC1046/EMC1047 actively detects an open and short condition on each measurement channel. When a diode fault is detected, the temperature data MSByte is forced to a value of 80h and the FAULT bit is set in the Status Register. When an external diode channel is configured to operate in APD mode, the circuitry will detect independent open fault conditions, however a short condition will be shared between the APD channels.

Chapter 5 Register Description

The registers shown in [Table 5.1](#) are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|---------------------------------------|--|---------------|-------------------------|
| 00h | R | Internal Diode Data High Byte | Stores the integer data for the Internal Diode | 00h | Page 22 |
| 01h | R | External Diode 1 Data High Byte | Stores the integer data for the External Diode 1 | 00h | Page 22 |
| 02h | R-C | Status | Stores the status bits for the Internal Diode and External Diodes | 00h | Page 23 |
| 03h | R/W | Configuration | Controls the general operation of the device (mirrored at address 09h) | 00h | Page 24 |
| 04h | R/W | Conversion Rate | Controls the conversion rate for updating temperature data (mirrored at address 0Ah) | 06h (4/sec) | Page 24 |
| 05h | R/W | Internal Diode High Limit | Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh) | 55h (85°C) | Page 25 |
| 06h | R/W | Internal Diode Low Limit | Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch) | 00h (0°C) | Page 25 |
| 07h | R/W | External Diode 1 High Limit High Byte | Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 0Dh) | 55h (85°C) | Page 25 |
| 08h | R/W | External Diode 1 Low Limit High Byte | Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 0Eh) | 00h (0°C) | Page 25 |
| 09h | R/W | Configuration | Controls the general operation of the device (mirrored at address 03h) | 00h | Page 24 |
| 0Ah | R/W | Conversion Rate | Controls the conversion rate for updating temperature data (mirrored at address 04h) | 06h (4/sec) | Page 24 |
| 0Bh | R/W | Internal Diode High Limit | Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h) | 55h (85°C) | Page 25 |
| 0Ch | R/W | Internal Diode Low Limit | Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h) | 00h (0°C) | Page 25 |
| 0Dh | R/W | External Diode1 High Limit High Byte | Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 07h) | 55h (85°C) | Page 25 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|---------------------------------------|--|---------------|-------------------------|
| 0Eh | R/W | External Diode1 Low Limit High Byte | Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 08h) | 00h (0°C) | Page 25 |
| 0Fh | W | One shot | A write to this register initiates a one shot update. | 00h | Page 27 |
| 10h | R | External Diode 1 Data Low Byte | Stores the fractional data for the External Diode 1 | 00h | Page 22 |
| 13h | R/W | External Diode 1 High Limit Low Byte | Stores the fractional portion of the high limit for the External Diode 1 | 00h | Page 25 |
| 14h | R/W | External Diode 1 Low Limit Low Byte | Stores the fractional portion of the low limit for the External Diode 1 | 00h | Page 25 |
| 15h | R/W | External Diode 2 High Limit High Byte | Stores the integer portion of the high limit for External Diode 2 | 55h (85°C) | Page 25 |
| 16h | R/W | External Diode 2 Low Limit High Byte | Stores the integer portion of the low limit for External Diode 2 | 00h (0°C) | Page 25 |
| 17h | R/W | External Diode 2 High Limit Low Byte | Stores the fractional portion of the high limit External Diode 2 | 00h | Page 25 |
| 18h | R/W | External Diode 2 Low Limit Low Byte | Stores the fractional portion of the low limit for External Diode 2 | 00h | Page 25 |
| 1Bh | R-C | External Diode Fault | Stores status bits indicating which external diode detected a diode fault | 00h | Page 28 |
| 22h | R/W | Consecutive ALERT | Controls the number of out-of-limit conditions that must occur before the status bit is asserted | 70h | Page 28 |
| 23h | R | External Diode 2 Data High Byte | Stores the integer data for External Diode 2 | 00h | Page 22 |
| 24h | R | External Diode 2 Data Low Byte | Stores the fractional data for External Diode 2 | 00h | Page 22 |
| 25h | R/W | External Diode 1 Beta Configuration | Stores the Beta Compensation circuitry settings for External Diode 1 | 08h | Page 29 |
| 26h | R/W | External Diode 2 Beta Configuration | Stores the Beta Compensation circuitry settings for External Diode 2 | 08h | Page 29 |
| 29h | R | Internal Diode Data Low Byte | Stores the fractional data for the Internal Diode | 00h | Page 22 |
| 2Ah | R | External Diode 3 High Byte | Stores the integer data for External Diode 3 | 00h | Page 22 |
| 2Bh | R | External Diode 3 Low Byte | Stores the fractional data for External Diode 3 | 00h | Page 22 |
| 2Ch | R/W | External Diode 3 High Limit High Byte | Stores the integer portion of the high limit for External Diode 3 | 55h (85°C) | Page 25 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|---------------------------------------|--|---------------|-------------------------|
| 2Dh | R/W | External Diode 3 Low Limit High Byte | Stores the integer portion of the low limit for External Diode 3 | 00h (0°C) | Page 25 |
| 2Eh | R/W | External Diode 3 High Limit Low Byte | Stores the fractional portion of the high limit for External Diode 3 | 00h | Page 25 |
| 2Fh | R/W | External Diode 3 Low Limit Low Byte | Stores the fractional portion of the low limit for External Diode 3 | 00h | Page 25 |
| 32h | R | Hottest Diode High Byte | Stores the integer data for the hottest temperature | 00h | Page 30 |
| 33h | R | Hottest Diode Low Byte | Stores the fractional data for the hottest temperature | 00h | Page 30 |
| 34h | R-C | Hottest Status | Status bits indicating which external diode is hottest | 00h | Page 31 |
| 35h | R-C | High Limit Status | Status bits for the High Limits | 00h | Page 31 |
| 36h | R-C | Low Limit Status | Status bits for the Low Limits | 00h | Page 32 |
| 39h | R/W | REC Configuration | Controls REC for all channels | 00h | Page 32 |
| 3Ah | R/W | Hottest Config | Controls which external diode channels are used in the "hottest of "comparison | 00h | Page 33 |
| 3Bh | R/W | Channel Config | Controls which channels are enabled | 00h | Page 33 |
| 40h | R/W | Filter Control | Controls the digital filter setting for the External Diode 1 channel | 00h | Page 34 |
| 41h | R | External Diode 4 Data High Byte | Stores the integer data for the External Diode 4 channel | 00h | Page 22 |
| 42h | R | External Diode 4 Data Low Byte | Stores the fractional data for the External Diode 4 channel | 00h | Page 22 |
| 43h | R | External Diode 5 Data High Byte | Stores the integer data for the External Diode 5 channel | 00h | Page 22 |
| 44h | R | External Diode 5 Data Low Byte | Stores the fractional data for the External Diode 5 channel | 00h | Page 22 |
| 45h | R | External Diode 6 Data High Byte | Stores the integer data for the External Diode 6 channel | 00h | Page 22 |
| 46h | R | External Diode 6 Data Low Byte | Stores the fractional data for the External Diode 6 channel | 00h | Page 22 |
| 50h | R/W | External Diode 4 High Limit High Byte | Stores the integer data for the high limit for the External Diode 4 channel | 55h (85°C) | Page 25 |
| 51h | R/W | External Diode 4 Low Limit High Byte | Stores the integer data for the low limit for the External Diode 4 channel | 00h (0°C) | Page 25 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|---------------------------------------|---|---------------|-------------------------|
| 52h | R/W | External Diode 4 High Limit Low Byte | Stores the fractional data for the low limit for the External Diode 4 channel | 00h | Page 25 |
| 53h | R/W | External Diode 4 Low Limit Low Byte | Stores the fractional data for the low limit for the External Diode 4 channel | 00h | Page 25 |
| 54h | R/W | External Diode 5 High Limit High Byte | Stores the integer data for the high limit for the External Diode 5 channel | 55h (85°C) | Page 25 |
| 55h | R/W | External Diode 5 Low Limit High Byte | Stores the integer data for the low limit for the External Diode 5 channel | 00h (0°C) | Page 25 |
| 56h | R/W | External Diode 5 High Limit Low Byte | Stores the fractional data for the low limit for the External Diode 5 channel | 00h | Page 25 |
| 57h | R/W | External Diode 5 Low Limit Low Byte | Stores the fractional data for the low limit for the External Diode 5 channel | 00h | Page 25 |
| 58h | R/W | External Diode 6 High Limit High Byte | Stores the integer data for the high limit for the External Diode 6 channel | 55h (85°C) | Page 25 |
| 59h | R/W | External Diode 6 Low Limit High Byte | Stores the integer data for the low limit for the External Diode 6 channel | 00h (0°C) | Page 25 |
| 5Ah | R/W | External Diode 6 High Limit Low Byte | Stores the fractional data for the low limit for the External Diode 6 channel | 00h (0°C) | Page 25 |
| 5Bh | R/W | External Diode 6 Low Limit Low Byte | Stores the fractional data for the low limit for the External Diode 6 channel | 00h (0°C) | Page 25 |
| 71h | R/W | External Diode 4 Beta Configuration | Stores the Beta Compensation circuitry settings for External Diode 4 | 08h | Page 29 |
| FDh | R | Product ID - EMC1046 | Stores a fixed value that identifies each product | 1Ah | Page 34 |
| FDh | R | Product ID - EMC1047 | Stores a fixed value that identifies each product | 1Ch | Page 34 |
| FEh | R | Manufacturer ID | Stores a fixed value that represents SMSC | 5Dh | Page 35 |
| FFh | R | Revision | Stores a fixed value that represents the revision number | 01h | Page 35 |

5.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

5.2 Temperature Data Registers

Table 5.2 Temperature Data Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------------|------|------|-------|----|----|----|----|----|---------|
| 00h | R | Internal Diode High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 29h | R | Internal Diode Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 01h | R | External Diode1 High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 10h | R | External Diode 1 Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 23h | R | External Diode 2 High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 24h | R | External Diode 2 Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 2Ah | R | External Diode 3 High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 2Bh | R | External Diode 3 Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 41h | R | External Diode 4 High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 42h | R | External Diode 4 Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 43h | R | External Diode 5 High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 44h | R | External Diode 5 Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 45h | R | External Diode 6 High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 46h | R | External Diode 6 Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |

All temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits. The data format is standard 2's complement from -64°C to 127.875°C as shown in [Table 5.3](#).

Table 5.3 Temperature Data Format

| TEMPERATURE (°C) | BINARY | HEX (AS READ BY REGISTERS) |
|------------------|----------------|----------------------------|
| Diode Fault | 1000_0000_000b | 80_00h |
| -64 | 1100_0000_000b | C0_00h |
| -63.875 | 1100_0000_001b | C0_20h |
| -1 | 1111_1111_000b | FF_00h |
| -0.125 | 1111_1111_111b | FF_E0h |
| 0 | 0000_0000_000b | 00_00h |
| 0.125 | 0000_0000_001b | 00_20h |
| 1 | 0000_0001_000b | 01_00h |
| 63 | 0011_1111_000b | 3F_00h |
| 64 | 0100_0000_000b | 40_00h |
| 127 | 0111_1111_000b | 7F_00h |
| 127.875 | 0111_1111_111b | 7F_E0h |

5.3 Status Register

Table 5.4 Status Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------|------|----------|----|------|-----|-------|----|----|---------|
| 02h | R | Status | BUSY | HOT TEST | - | HIGH | LOW | FAULT | - | - | 00h |

The Status Register reports general error conditions. To identify specific channels, refer to [Section 5.8](#), [Section 5.13](#), and [Section 5.14](#). The individual Status Register bits (except HOTTEST) are cleared when the appropriate High Limit or Low Limit register has been read or cleared.

Bit 7 - BUSY - This bit indicates that the ADC is currently converting.

Bit 6 - HOTTEST - This bit is set if the REM_HOT bit (see [Section 5.17](#)) is set and the hottest channel changes. This bit is cleared when the register is read.

Bit 4 - HIGH - This bit is set when any of the temperature channels meets or exceeds its programmed high limit. See the High Limit Status Register for specific channel information ([Section 5.13](#)).

Bit 3 - LOW - This bit is set when any of the temperature channels drops below its programmed low limit. See the Low Limit Status Register for specific channel information ([Section 5.14](#)).

Bit 2 - FAULT - This bit is asserted when a diode fault is detected on any of the external diode channels. See the External Diode Fault Register for specific channel information ([Section 5.8](#)).

5.4 Configuration Register

Table 5.5 Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------|----|--------------|----|----|----|----|--------------|----|---------|
| 03h | R/W | Config | - | RUN/ STOP | | - | - | - | DAVG_ DIS | - | 00h |
| 09h | | | | | | | | | | | |

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

Bit 6 - RUN / STOP - Controls Active/Standby modes.

- '0' (default) - The device is in Active mode and converting on all channels.
- '1' -The device is in Standby mode and not converting.

Bit 1 - DAVG_DIS - Disables the dynamic averaging feature on all temperature channels (see [Section 4.2.6](#)).

- '0' (default) - The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in [Table 4.1](#).
- '1' - The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates (i.e. more conversions per second), this averaging factor will be reduced as shown in [Table 4.1](#).

5.5 Conversion Rate Register

Table 5.6 Conversion Rate Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|----|----|----|----|----|-----------|----|----|----------------|
| 04h | R/W | Conversion Rate | - | - | - | - | | CONV[2:0] | | | 06h (4/sec) |
| 0Ah | | | | | | | | | | | |

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

Bits 3-0 - CONV[3:0] - Determines the conversion rate as shown in [Table 5.7](#).

Table 5.7 Conversion Rate

| CONV[2:0] | | | CONVERSIONS / SECOND |
|-----------|---|---|----------------------|
| 2 | 1 | 0 | |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 4 (default) |

Table 5.7 Conversion Rate (continued)

| CONV[2:0] | | | CONVERSIONS / SECOND |
|------------|---|---|----------------------|
| 2 | 1 | 0 | |
| 1 | 1 | 1 | Continuous |
| All Others | | | 4 |

The actual conversion rate for Continuous conversions will depend on the number of diode channels enabled and is shown in [Table 5.8](#).

Table 5.8 Maximum Conversion Rate Per Temperature Channels

| NUMBER OF EXTERNAL DIODE CHANNELS | MAX CONVERSION RATE |
|-----------------------------------|---------------------|
| 3 | 13 / sec |
| 4 | 12 / sec |
| 5 | 11 / sec |
| 6 (EMC1047only) | 10 / sec |

5.6 Limit Registers

Table 5.9 Temperature Limit Registers

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|--------------------------------------|------|------|-------|----|----|----|----|----|------------|
| 05h | R/W | Internal Diode High Limit | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 0Bh | | | | | | | | | | | |
| 06h | R/W | Internal Diode Low Limit | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 0Ch | | | | | | | | | | | |
| 07h | R/W | External Diode1 High Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 0Dh | | | | | | | | | | | |
| 13h | R/W | External Diode 1 High Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 08h | R/W | External Diode 1 Low Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 0Eh | | | | | | | | | | | |
| 14h | R/W | External Diode1 Low Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |

Table 5.9 Temperature Limit Registers (continued)

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|---------------------------------------|------|------|-------|----|----|----|----|----|------------|
| 15h | R/W | External Diode 2 High Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 16h | R/W | External Diode 2 Low Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 17h | R/W | External Diode 2 High Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 18h | R/W | External Diode 2 Low Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 2Ch | R/W | External Diode 3 High Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 2Dh | R/W | External Diode 3 Low Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 2Eh | R/W | External Diode 3 High Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 2Fh | R/W | External Diode 3 Low Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 50h | R/W | External Diode 4 High Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 51h | R/W | External Diode 4 Low Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 52h | R/W | External Diode 4 High Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 53h | R/W | External Diode 4 Low Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |

Table 5.9 Temperature Limit Registers (continued)

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|---------------------------------------|------|------|-------|----|----|----|----|----|------------|
| 54h | R/W | External Diode 5 High Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 55h | R/W | External Diode 5 Low Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 56h | R/W | External Diode 5 High Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 57h | R/W | External Diode 5 Low Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 58h | R/W | External Diode 6 High Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 59h | R/W | External Diode 6 Low Limit High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 5Ah | R/W | External Diode 6 High Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 5Bh | R/W | External Diode 6 Low Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |

The device contains both high and low limits for all temperature channels. If the measured temperature meets or exceeds the high limit, then the corresponding status bit is set. Likewise, if the measured temperature is less than the low limit, the corresponding status bit is set.

The limit registers with multiple addresses are fully accessible at either address.

When the device is in standby mode, updating the limit registers will have no affect until the next conversion cycle occurs. This can be initiated via a write to the One Shot Register or by clearing the RUN / STOP bit in the Configuration Register (see [Section 5.4](#)).

5.7 One Shot Register

Table 5.10 One Shot Register

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|----------|---|----|----|----|----|----|----|----|---------|
| 0Fh | W | One Shot | Writing to this register initiates a single conversion cycle. Data is not stored and always reads 00h | | | | | | | | 00h |

The One Shot Register is used to initiate a one shot command. Writing to the one shot register, when the device is in standby mode and BUSY bit (in Status Register) is '0', will immediately cause the ADC to update all temperature measurements. Writing to the One Shot Register while the device is in active mode will have no affect.

5.8 External Diode Fault Register

Table 5.11 External Diode Fault Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|----|-------|-------|-------|-------|-------|-------|----|---------|
| 1Bh | R-C | External Diode Fault | - | E6FLT | E5FLT | E4FLT | E3FLT | E2FLT | E1FLT | - | 00h |

The External Diode Fault Register indicates which of the external diodes caused the FAULT bit in the Status Register to be set. These bits are cleared when read if the error condition has been removed.

Bit 6 - E6FLT - This bit is set if the External Diode 6 channel reported a diode fault.

Bit 5 - E5FLT - This bit is set if the External Diode 5 channel reported a diode fault.

Bit 4 - E4FLT - This bit is set if the External Diode 4 channel reported a diode fault.

Bit 3 - E3FLT - This bit is set if the External Diode 3 channel reported a diode fault.

Bit 2 - E2FLT - This bit is set if the External Diode 2 channel reported a diode fault.

Bit 1 - E1FLT - This bit is set if the External Diode 1 channel reported a diode fault.

5.9 Consecutive ALERT Register

Table 5.12 Consecutive ALERT Register

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|-------------------|----------|----|----|----|---------|---------|---------|----|---------|
| 22h | R/W | Consecutive ALERT | TIME OUT | - | - | - | CAL RT2 | CAL RT1 | CAL RT0 | - | 70h |

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the interrupt status registers are asserted.

Each out of limit error and diode fault condition has its own counter associated with it. Each counter is incremented whenever the corresponding channel exceeds the appropriate limit. Additionally, each counter is reset if the condition has been removed. (i.e. if External Diode 1 exceeds its high limit, it will increment the high counter. If, on the next measurement, it experiences a diode fault, the high limit counter will be reset and the diode fault counter will be incremented).

When the consecutive alert counter reaches its programmed value then the STATUS bit(s) for that channel and the error condition will be set to '1'. Measurements will continue normally.

For example, if the CALRT[2:0] bits are set for 4 consecutive alerts on an EMC1046/EMC1047 device, the high limits are set at 70°C, and none of the channels are masked, then the status bits will be asserted after the following four measurements:

1. Internal Diode reads 71°C and both external diodes read 69°C. Consecutive alert counter for INT is incremented to 1.

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2. Both the Internal Diode and the External Diode 1 read 71°C and External Diode 2 reads 68°C. Consecutive alert counter for INT is incremented to 2 and for EXT1 is set to 1.
3. The External Diode 1 reads 71°C and both the Internal Diode and External Diode 2 read 69°C. Consecutive alert counter for INT and EXT2 are cleared and EXT1 is incremented to 2.
4. The Internal Diode reads 71°C and both external diodes read 71°C. Consecutive alert counter for INT is set to 1, EXT2 is set to 1, and EXT1 is incremented to 3.
5. The Internal Diode reads 71°C and both the external diodes read 71°C. Consecutive alert counter for INT is incremented to 2, EXT2 is set to 2, and EXT1 is incremented to 4. The HIGH status bit are set for EXT1. The EXT1 counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

Bit 7 - TIMEOUT - Determines whether the SMBus Timeout function is enabled.

- '0' (default) - The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.
- '1' - The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30ms, then the device will reset the SMBus protocol.

Bits 3-1 - CALRT[2:0] - Determine the number of consecutive measurements that must have an out of limit condition or diode fault before the STATUS bits is asserted. All temperature channels use this value to set the respective counters. The bits are decoded as shown in [Table 5.13](#). The default setting is 1 consecutive out of limit conversion.

APPLICATION NOTE: If one of the fault queues is not cleared and the CALRT[2:0] bits are updated, the update won't take affect until fault queue is cleared. All the fault queues are independent so those that are empty will be updated immediately.

Table 5.13 Consecutive Alert Settings

| 2 | 1 | 0 | NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS |
|------------|---|---|---|
| 0 | 0 | 0 | 1 (default for CALRT[2:0]) |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 1 | 1 | 4 |
| All Others | | | 1 (CALRT[2:0]), |

5.10 Beta Configuration Register

Table 5.14 Beta Configuration Register

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|-------------------------------------|----|----|----|----|-------|------------|----|----|---------|
| 25h | R/W | External Diode 1 Beta Configuration | - | - | - | - | AUTO1 | BETA1[2:0] | | | 08h |
| 26h | R/W | External Diode 2 Beta Configuration | - | - | - | - | AUTO2 | BETA2[2:0] | | | 08h |
| 71h | R/W | External Diode 4 Beta Configuration | - | - | - | - | AUTO4 | BETA4[2:0] | | | 08h |

These registers are used to set the Beta Compensation factor that is used for the External Diode channels.

Bit 3 - AUTOx - Enables the Beta Compensation factor autodetection function.

- '0' - The Beta Compensation Factor autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETAx[2:0] bits.
- '1' (default) - The Beta Compensation factor autodetection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETAx[2:0] bits will be automatically updated to indicate the current setting.

Bit 2-0 - BETAx[2:0] - These bits always reflect the current beta configuration settings. If autodetection circuitry is enabled, then these bits will be updated automatically and writing to these bits will have no effect. If the autodetection circuitry is disabled, then these bits will determine the beta configuration setting that is used for their respective channels.

Care should be taken when setting the BETAx[2:0] bits when the autodetection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, then the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an AMD processor diode), then the BETAx[2:0] bits should be set to '111b'.

Table 5.15 Beta Compensation Look Up Table

| BETAX[2:0] | | | MINIMUM BETA |
|------------|---|---|--------------|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | ≤ 0.08 |
| 0 | 0 | 1 | ≤ 0.111 |
| 0 | 1 | 0 | ≤ 0.176 |
| 0 | 1 | 1 | ≤ 0.29 |
| 1 | 0 | 0 | ≤ 0.48 |
| 1 | 0 | 1 | ≤ 0.9 |
| 1 | 1 | 0 | ≤ 2.33 |
| 1 | 1 | 1 | Disabled |

5.11 Hottest Temperature Registers

Table 5.16 Hottest Temperature Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-------------------------------|------|------|-------|----|----|----|----|----|---------|
| 32h | R | Hottest Temperature High Byte | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 80h |
| 33h | R | Hottest Temperature Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |

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The Hottest Temperature Registers store the measured hottest temperature of all the selected external diode channels (see [Section 5.16](#)). If no External diodes are selected then the High Byte Register will read 80h. The data format is the same as the temperature channels.

5.12 Hottest Temperature Status Register

Table 5.17 Hottest Temperature Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------------|----|------|------|------|------|------|------|-----|---------|
| 34h | R | Hottest Temperature Status | - | EXT6 | EXT5 | EXT4 | EXT3 | EXT2 | EXT1 | INT | 00h |

The Hottest Temperature Status Register flags which external diode temperature is hottest. If multiple temperature channels measure the same temperature and are equal to the hottest temperature, then hottest status will be based on the measurement order.

Bit 6 - EXT6 - The External Diode 6 channel is the hottest.

Bit 4 - EXT5 - The External Diode 5 channel is the hottest.

Bit 3 - EXT4 - The External Diode 4 channel is the hottest.

Bit 3 - EXT3 - The External Diode 3 channel is the hottest.

Bit 2 - EXT2 - The External Diode 2 channel is the hottest.

Bit 1 - EXT1 - The External Diode 1 channel is the hottest.

Bit 0 - INT - The Internal Diode channel is the hottest.

5.13 High Limit Status Register

Table 5.18 High Limit Status Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-------------------|----|---------|---------|---------|---------|---------|---------|--------|---------|
| 35h | R-C | High Limit Status | - | E6 HIGH | E5 HIGH | E4 HIGH | E3 HIGH | E2 HIGH | E1 HIGH | I HIGH | 00h |

The High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded for a number of consecutive readings as set by the consecutive alert counts (see [Section 5.9](#)). If any of these bits are set, then the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits if the error condition has been removed. Reading from the register will also clear the HIGH status bit in the Status Register.

Bit 6 - E6HIGH - This bit is set when the External Diode 6 channel meets or exceeds its programmed high limit.

Bit 5 - E5HIGH - This bit is set when the External Diode 5 channel meets or exceeds its programmed high limit.

Bit 4 - E4HIGH - This bit is set when the External Diode 4 channel meets or exceeds its programmed high limit.

Bit 3 - E3HIGH - This bit is set when the External Diode 3 channel meets or exceeds its programmed high limit.

Bit 2 - E2HIGH - This bit is set when the External Diode 2 channel meets or exceeds its programmed high limit.

Bit 1 - E1HIGH - This bit is set when the External Diode 1 channel meets or exceeds its programmed high limit.

Bit 0 - IHIGH - This bit is set when the Internal Diode channel meets or exceeds its programmed high limit.

5.14 Low Limit Status Register

Table 5.19 Low Limit Status Register

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|------------------|----|--------|--------|--------|--------|--------|--------|------|---------|
| 36h | R-C | Low Limit Status | - | E6 LOW | E5 LOW | E4 LOW | E3 LOW | E2 LOW | E1 LOW | ILOW | 00h |

The Low Limit Status Register contains the status bits that are set when a temperature channel drops below the low limit for a number of consecutive readings as set by the consecutive alert counts (see [Section 5.9](#)). If any of these bits are set, then the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits if the error condition has been removed. Reading from the register will also clear the LOW status bit in the Status Register.

Bit 6 - E6LOW - This bit is set when the External Diode 6 channel drops below its programmed low limit.

Bit 5- E5LOW - This bit is set when the External Diode 5 channel drops below its programmed low limit.

Bit 4 - E4LOW - This bit is set when the External Diode 4 channel drops below its programmed low limit.

Bit 3 - E3LOW - This bit is set when the External Diode 3 channel drops below its programmed low limit.

Bit 2 - E2LOW - This bit is set when the External Diode 2 channel drops below its programmed low limit.

Bit 1 - E1LOW - This bit is set when the External Diode 1 channel drops below its programmed low limit.

Bit 0 - ILOW - This bit is set when the Internal Diode channel drops below its programmed low limit.

5.15 REC Configuration Register

Table 5.20 REC Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------|----|--------------|--------------|--------------|--------------|--------------|--------------|----|---------|
| 39h | R/W | REC Config | - | E6_ REC_n | E5_ REC_n | E4_ REC_n | E3_ REC_n | E2_ REC_n | E1_ REC_n | - | 00h |

The REC Control Register controls the Resistance Error Correction circuitry for each of the external diode channels.

Bits 6 - 0 - Ex_REC_n (EMC1047 only) - Disables the Resistance Error Correction (REC) for the External Diode X channel. Note that E6_REC_n can only be written for the EMC1047 only

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- '0' (default) - REC is enabled.
- '1' - REC is disabled.

5.16 Hottest Configuration Register

Table 5.21 Hottest Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------|----|-------|-------|-------|-------|-------|-------|------|---------|
| 3Ah | R/W | Hottest Config | - | E6HOT | E5HOT | E4HOT | E3HOT | E2HOT | E1HOT | IHOT | 00h |

The Hottest Configuration Register determines which External Diode Channels (if any) are compared during the “Hottest Of” comparison that is automatically performed at the end of every conversion cycle.

Bits 6 - 0 - ExHOT - Controls whether the External Diode X temperature data is compared during the “Hottest Of” comparison.

- '0' (default) - The External Diode X channel is not compared during the “Hottest Of” Comparison.
- '1' - The External Diode X channel temperature data is compared to all other indicated channels during the “Hottest Of” Comparison.

Bit 0 - IHOT - Controls whether the Internal Diode temperature data is compared during the “Hottest Of” comparison.

- '0' (default) - The Internal Diode channel is not compared during the “Hottest Of” Comparison.
- '1' - The Internal Diode channel temperature data is compared to all other indicated channels during the “Hottest Of” Comparison.

5.17 Channel Configuration Register

Table 5.22 Channel Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------|---------|----|----|----|----|----------|----------|----------|---------|
| 3Bh | R/W | Channel Config | REM_HOT | - | - | - | - | EXT4_APD | EXT2_APD | EXT1_APD | 00h |

The Channel Configuration Register determines which external diode channels are active in the device.

Bit 7 - REM_HOT - Enables circuitry that will remember the last temperature channel that was determined to be the Hottest and flag an error if the hottest temperature channel changes.

- '0' (default) - The HOTTEST status bit will not be asserted if the hottest temperature channel changes.
- '1' - If the hottest temperature channel changes, then the HOTTEST status bit will be asserted.

Bit 2 - EXT4_APD - Enables the DP4 / DN5 and DN4 / DP5 pins to support two anti-parallel diode connections versus a single diode connection.

- '0' (default) - The DP4 / DN5 and DN4 / DP5 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 4).
- '1' - The DP4 / DN5 and DN4 / DP5 pins support two anti-parallel diode connections (External Diode 4 and External Diode 5).

Bit 1 - EXT2_APD- Enables the DP2 / DN3 and DN2 / DP3 pins to support two anti-parallel diode connections versus a single diode connection.

- '0' (default) - The DP2 / DN3 and DN2 / DP3 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 2).
- '1' - The DP2 / DN3 and DN2 / DP3 pins support two anti-parallel diode connections (External Diode 2 and External Diode 3).

Bit 0 - EXT1_APD (EMC1047 only)- Enables the DP1 / DN6 and DN1 / DP6 pins to support two anti-parallel diode connections versus a single diode connection.

- '0' (default) - The DP1 / DN6 and DN1 / DP6 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 1).
- '1' - The DP1 / DN6 and DN1 / DP6 pins support two anti-parallel diode connections (External Diode 1 and External Diode 6).

5.18 Filter Control Register

Table 5.23 Filter Control Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------|----|-------------|-------------|-------------|-------------|-------------|-------------|----|---------|
| 40h | R/W | Filter Control | - | AVG6_ EN | AVG5_ EN | AVG4_ EN | AVG3_ EN | AVG2_ EN | AVG1_ EN | - | 00h |

The Filter Configuration Register controls the digital filter on the external diode channels.

Bits 6 - 0 - AVGx_EN- Control the digital averaging that is applied to the External Diode X temperature measurements.

- '0' (default) - Digital Averaging is disabled.
- '1' - Digital averaging is enabled as a 4x running average for the External Diode X channel.

5.19 Product ID Register

Table 5.24 Product ID Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------|----|----|----|----|----|----|----|----|----------------|
| FDh | R | Product ID | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1Ah EMC1046 |
| | | | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1Ch EMC1047 |

The Product ID Register holds a unique value that identifies the device.

5.20 Manufacturer ID Register (FEh)

Table 5.25 Manufacturer ID Register

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|-----------------|----|----|----|----|----|----|----|----|---------|
| FEh | R | Manufacturer ID | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5Dh |

The Manufacturer ID Register holds an 8-bit word that identifies SMSC.

5.21 Revision Register (FFh)

Table 5.26 Revision Register

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|-------|-----|----------|----|----|----|----|----|----|----|----|---------|
| FFh | R | Revision | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h |

The Revision register contains an 8 bit word that identifies the die revision.

Chapter 6 Package Information

6.1 EMC1046/EMC1047 Package Drawing

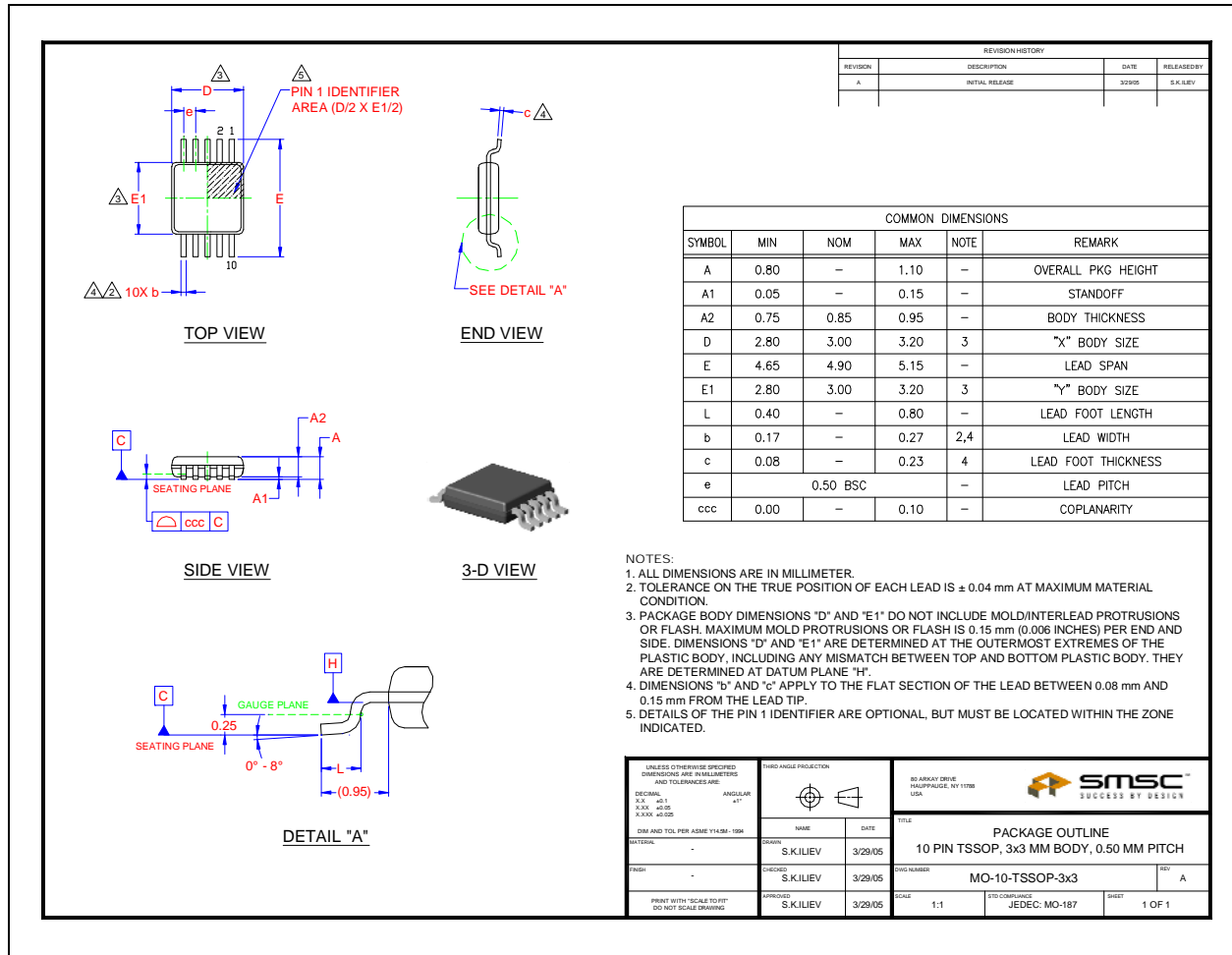


Figure 6.1 10-Pin TSSOP Package Drawing

6.2 Package Markings

6.2.1 EMC1046-X-AIZL (10-Pin TSSOP)

All devices will be marked on the first line of the top side with "1046" or "1047". On the second line, they will be marked with the appropriate -X number (-1, -2, etc), the Functional Revision "B" and Country Code (CC) .

Chapter 7 Revision History

Table 7.1 Customer Revision History

| REVISION LEVEL AND DATE | SECTION/FIGURE/ENTRY | CORRECTION |
|-------------------------|--|--|
| Rev. 0.69 (06-29-09) | Table 1.1, "EMC1046/EMC1047 Pin Description" | Added "requires external pullup resistor" to SMDATA and SMCLK in function column |
| | Table 1.1, "EMC1046/EMC1047 Pin Description" | Added the following application note below table: "For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V." |
| | Table 2.1, "Absolute Maximum Ratings" | Updated voltage limits for 5V tolerant pins with pull-up resistors. Added the following note below table: "For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the device is unpowered." |

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