

SIGNAL LEVEL SENSOR SYSTEM

■ GENERAL DESCRIPTION

The **NJU7181** is a signal level sensor system IC. It sends a High flag to the microprocessor or other equipments whenever it detects the existence of the audio signal.

The **NJU7181** includes a delay circuit which allows the IC continue to hold the flag after the absence of the audio signal. This holding time can be adjusted with external capacitor.

Together with its adjustable Input Sensitivity (*by external resistor*) & its characteristic of low current consumption and low operating voltage, **NJU7181** is suitable for Eco-Design of Energy-using Products and for battery operated applications.

■ PACKAGE OUTLINE



NJU7181RB1
MSOP8 (TVSP8)



NJU7181KU1

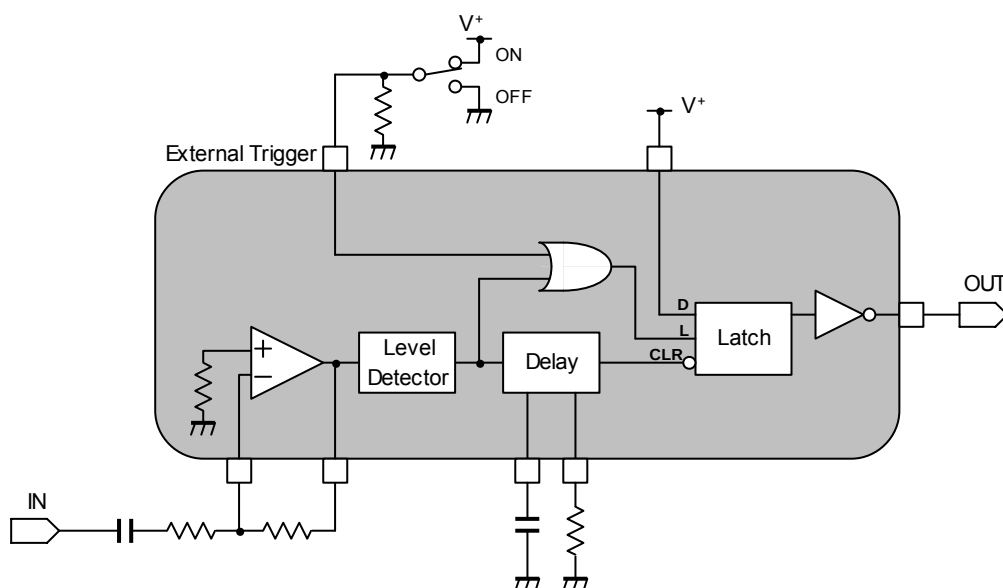
■ FEATURES

- Operating Voltage 0.9 to 5.5V
- Low Operating Current 55µA typ.
- Delay circuit for long Recovery time
- Adjustable Recovery time by external capacitor
- Adjustable Input Sensitivity by external resistance
- C-MOS Technology
- Package Outline MSOP8 (TVSP8)*
ESON8
*MEET JEDEC MO-187-DA / THIN TYPE

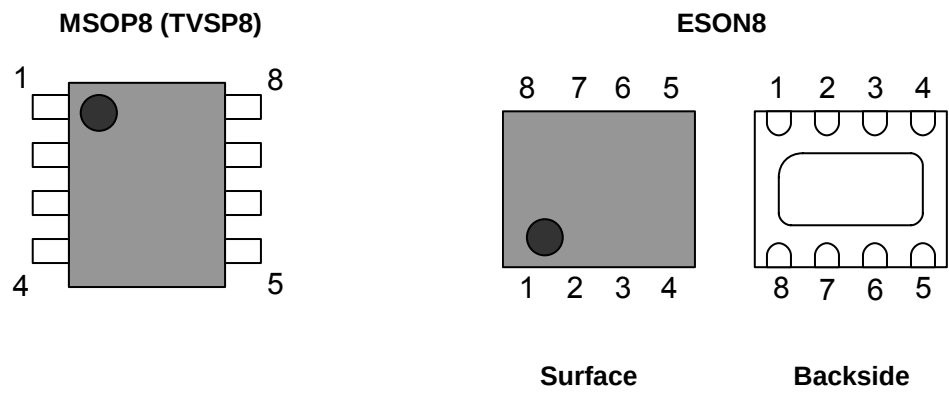
■ APPLICATIONS

- Power Saving for battery operated devices
- Muting Application
- Memory saving for recording devices
- Half- duplex transmission application

■ BLOCK DIAGRAM



PIN CONFIGURATION



No.	Symbol	Function
1	IN	AC Input
2	AMP_OUT	Amplifier Output
3	TRIN	External Trigger Input
4	GND	Ground
5	CAP_D	Delay Time Capacitor
6	RES_D	Delay Time Resister
7	OUT	DC Output
8	V ⁺	Supply Voltage

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V ⁺	+7	V
Power Dissipation	P _D	MSOP8 (TVSP8): 470 (Note1) ESON8: 450	mW
Maximum Input Voltage	V _{IMAX}	0 ~ V ⁺ (Note2)	V
Operating Temperature Range	T _{opr}	-40 ~ +85	°C
Storage Temperature Range	T _{stg}	-40 ~ +125	°C

(Note1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting

(Note2) Don't put Input Voltage more than Power Supply Voltage.

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V⁺=3V, R₁=10kΩ, R₂=100kΩ, R_d=220kΩ, C_d=10nF)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		0.9	-	5.5	V
Operating Current	I _{DD}	No signal, R _L =∞	-	55	100	μA
Input Sensitivity	V _{INS}	f=1kHz	-45	-41.5	-38	dBV
Delay Time 1	T _{delay1}		1.0	1.5	2.0	Sec
Delay Time 2	T _{delay2}	V ⁺ =0.9V	1.0	1.5	2.0	Sec
Delay Time 3	T _{delay3}	C _d =10μF	-	1,500	-	Sec

■ DC CHARACTERISTICS

DC Output Terminal (7pin)

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Output Voltage	V _{OH}	I _{SOURCE} =1mA	V ⁺ -0.2	-	V ⁺	V
Low Level Output Voltage	V _{OL}	I _{SINK} =1mA	0	-	0.2	V

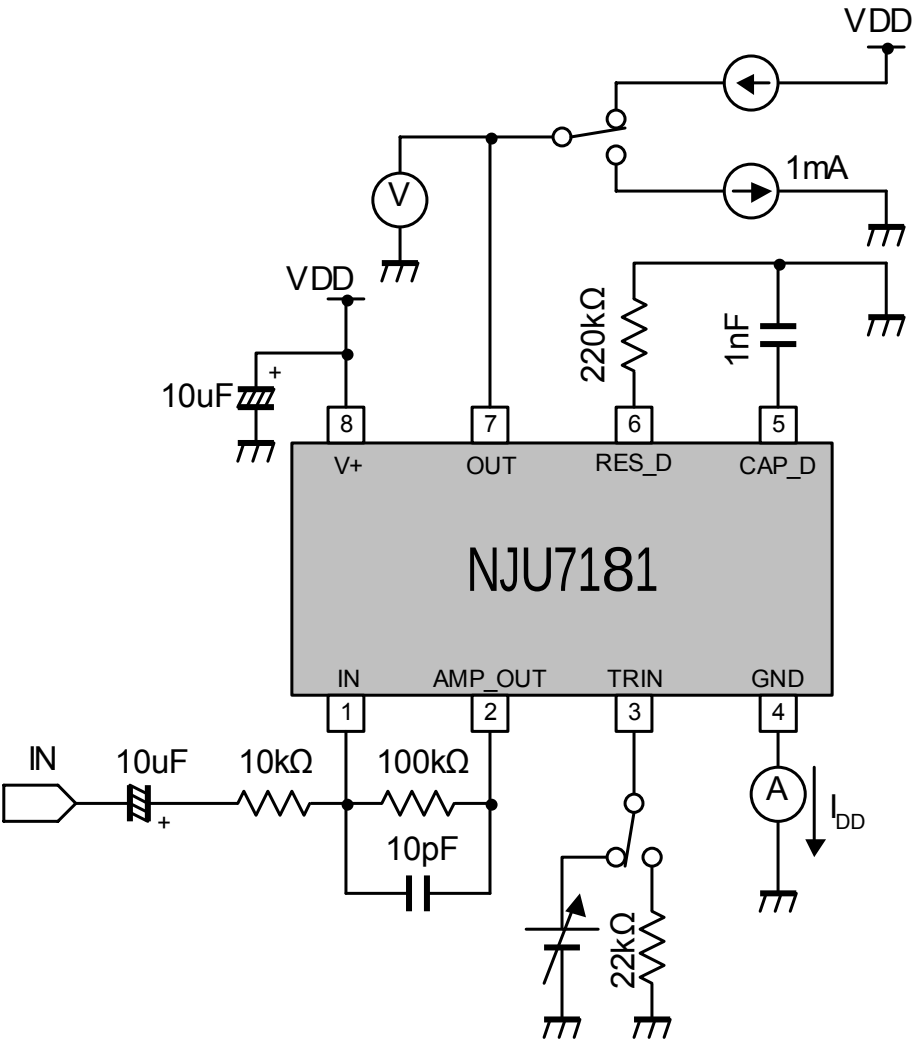
External Trigger Switch Terminal (3pin)

(Ta=25°C)

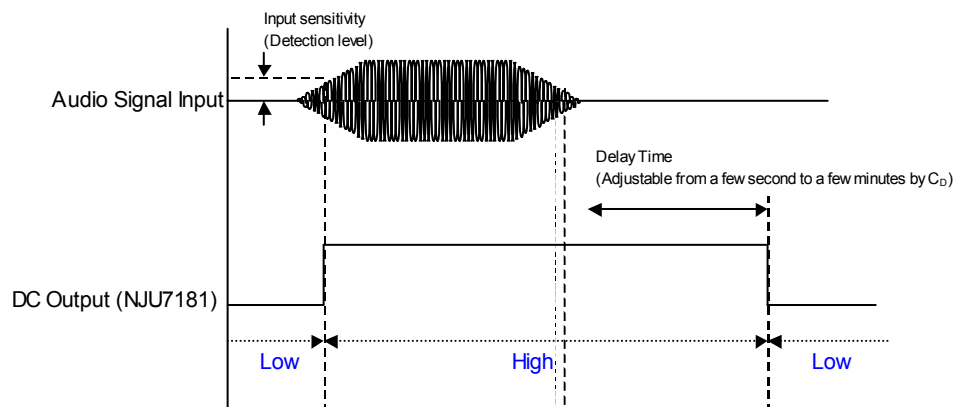
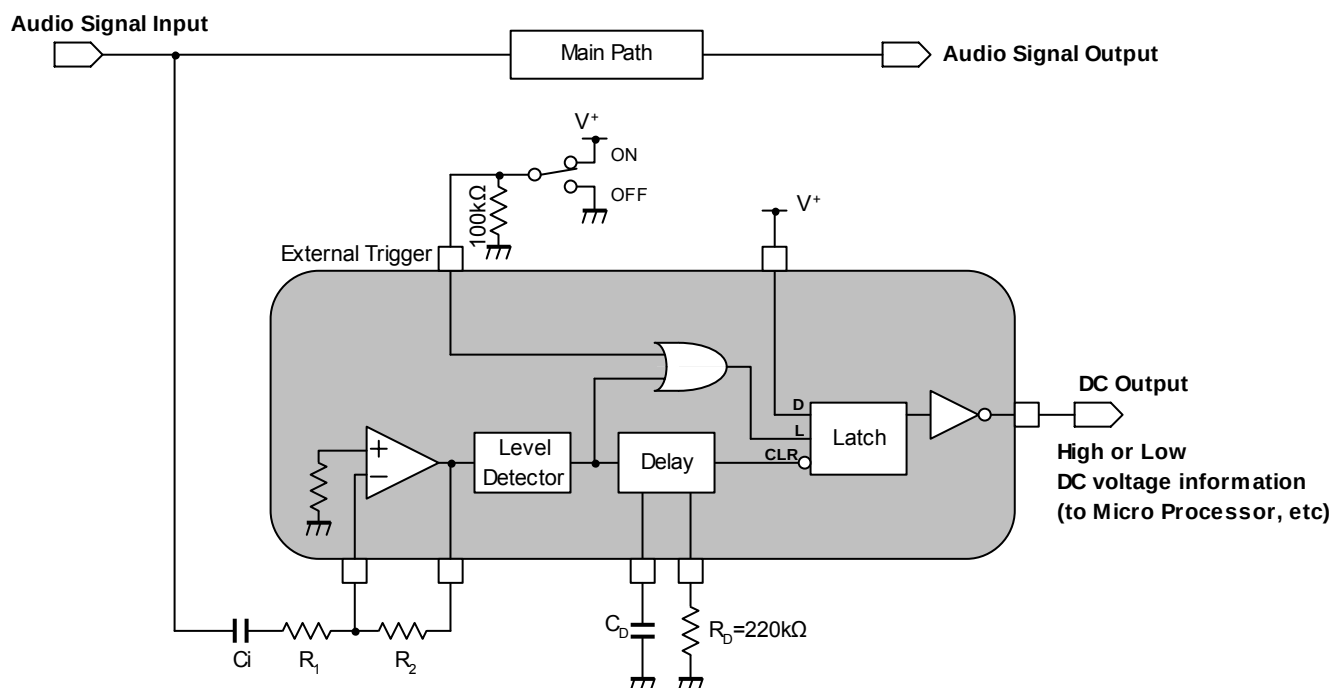
High Level Input Voltage	V _{IH}		V ⁺ -0.2	-	V ⁺	V
Low Level Input Voltage	V _{IL}		0	-	0.2	V



■ TEST CIRCUIT



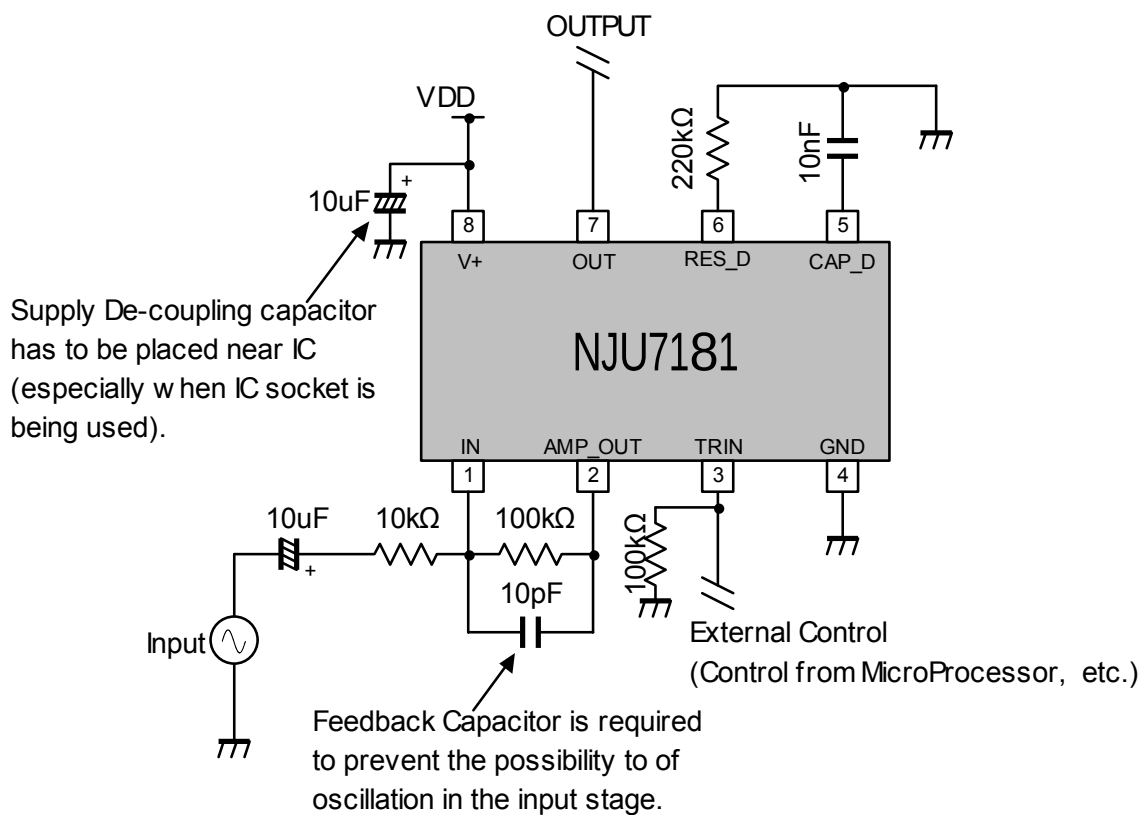
■ APPLICATION CIRCUIT



Attack Time:



Note:

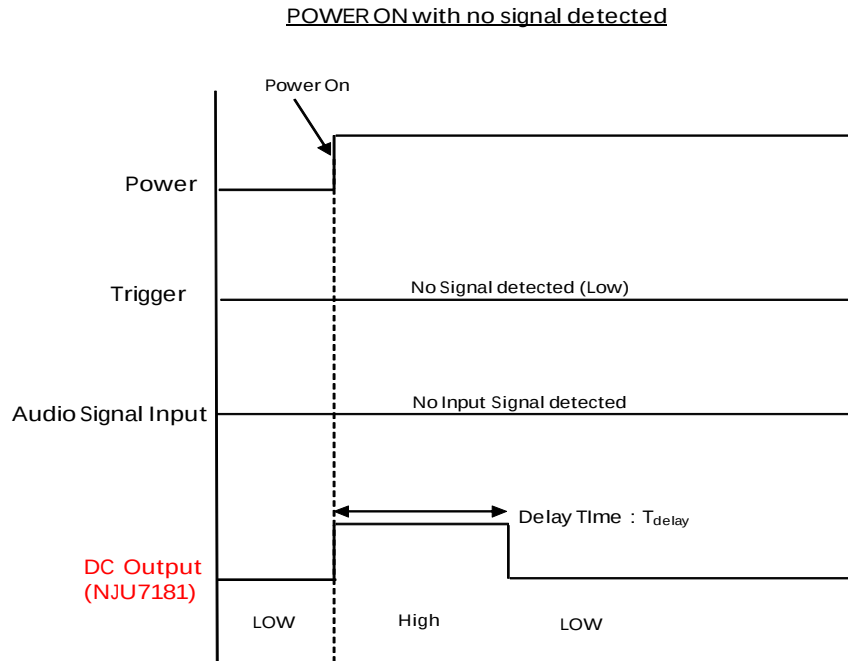


■ APPLICATION NOTE

• DC Output Waveform Scenario

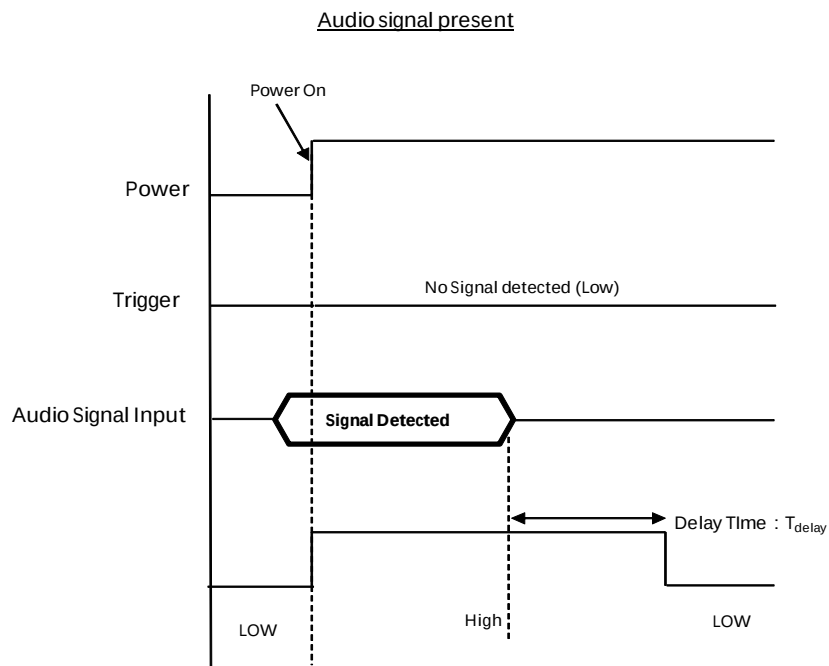
Scenario 1: Power-ON

– Output will be high initially when NJU7181 is first powered up even if there is no input signal detected.



Scenario 2: Only Audio Signal detected

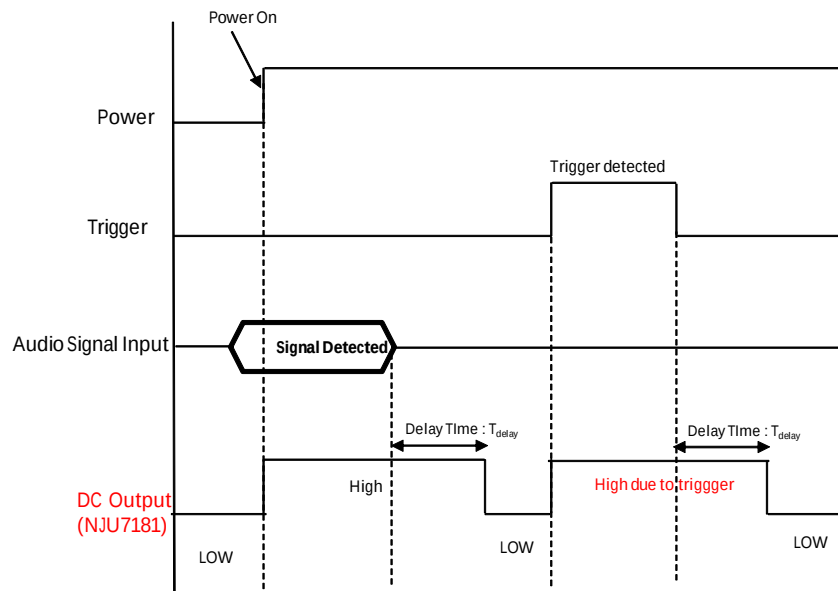
– Output will be or maintain high when **either an input signal or trigger signal is detected**. The delay circuit will only be activated **when both signals is not present**. NJU7181 will then hold the output level for a delay time which can be adjusted by the Capacitor value @ pin 5.



Scenario 3: Trigger Signal detected (Case 1)

– Output will be or maintain high when **either an input signal or trigger signal is detected**. The delay circuit will only be activated **when both signals is not present**. Output is set to Low state when a delay time passes. Output is set to High state when either an input signal or trigger signal is detected again.

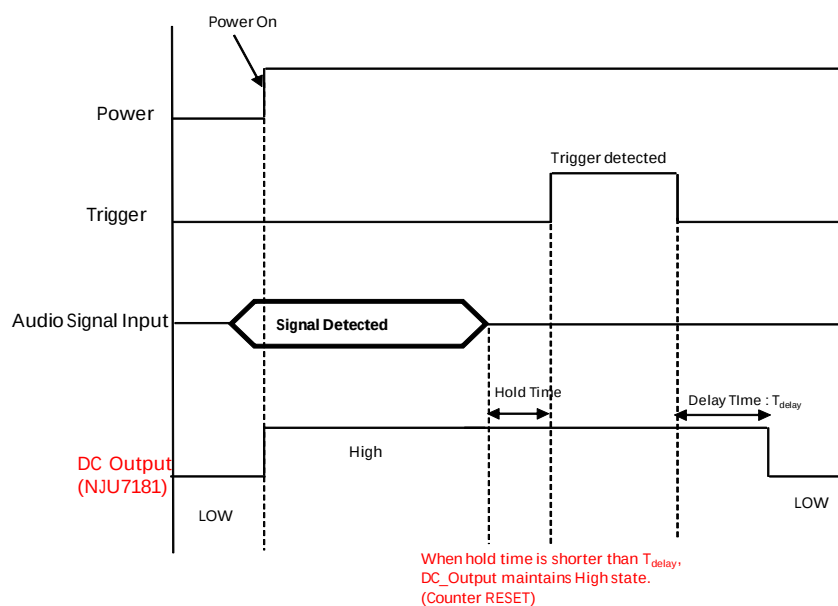
Case 1: Trigger signal present (After output LOW)



Scenario 4: Trigger Signal detected (Case 2)

– Output will be or maintain high when **either an input signal or trigger signal is detected**. When hold time is shorter than a delay time, output maintains High state (Counter RESET). NJU7181 will then hold the output level for a delay time which can be adjusted by the Capacitor value @ pin 5.

Case 2: Trigger signal present (During output HIGH)



◆ Input Sensitivity [Ta =25°C]

The input sensitivity is defined as follows.

$$V_{INS}=20*\log(R1/R2) - 21.5 \text{ [dBV]} \text{ ----- (1)}$$

Note) The input sensitivity recommends the setting of -60dBV (1mVrms) or more.

Note) The R2 value should be 100kΩ or more.

◆ Frequency Response

The input capacitor “Ci” forms HPF with “R1”. The cut-off frequency is defined as follows. Please decide C1 value in consideration of the frequency response necessary for the signal-detecting.

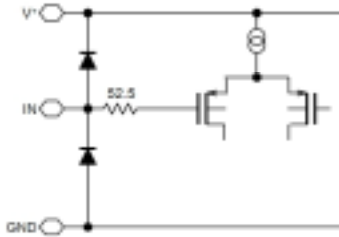
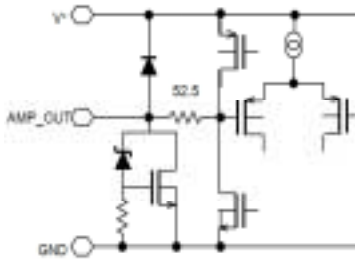
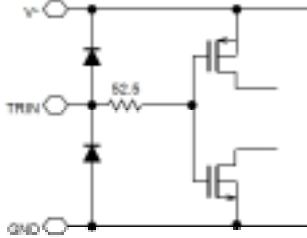
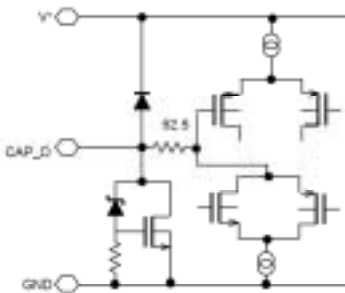
$$f_c=1/(2\pi\times C_i\times R_1) \text{ [Hz]} \text{ ----- (2)}$$

◆ Delay time [With R_p = 220Kohm]

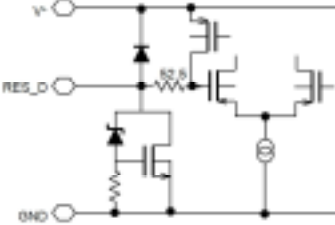
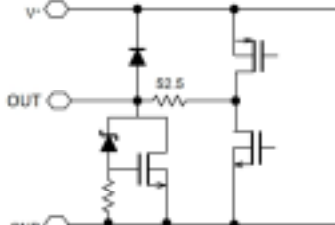
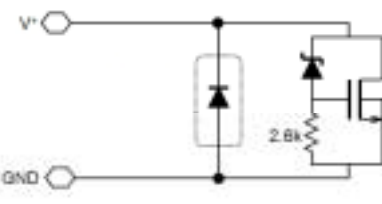
The Recovery time is defined as follows.

$$T_{\text{delay}}=1.5*10^8*C_R \text{ [sec]} \text{ ----- (3)}$$

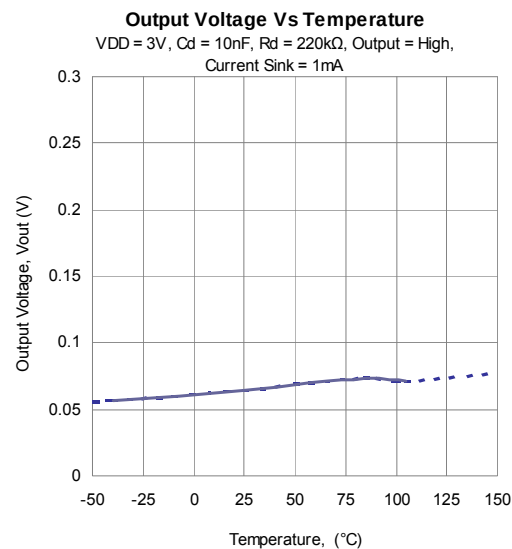
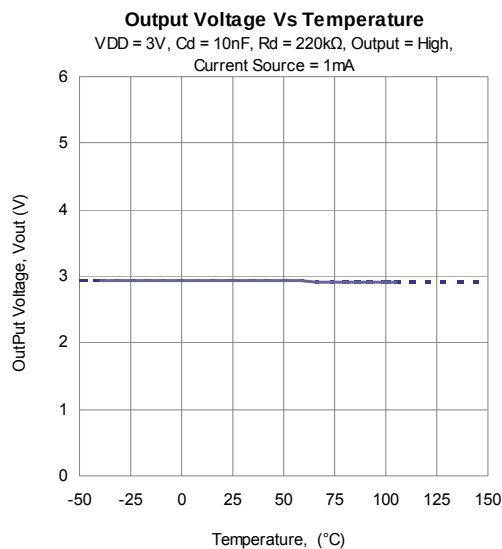
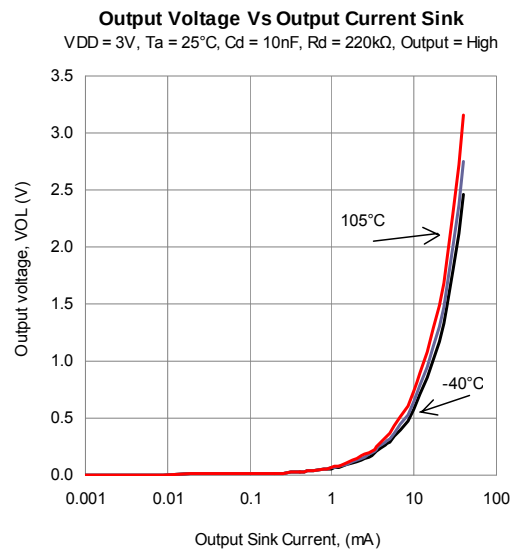
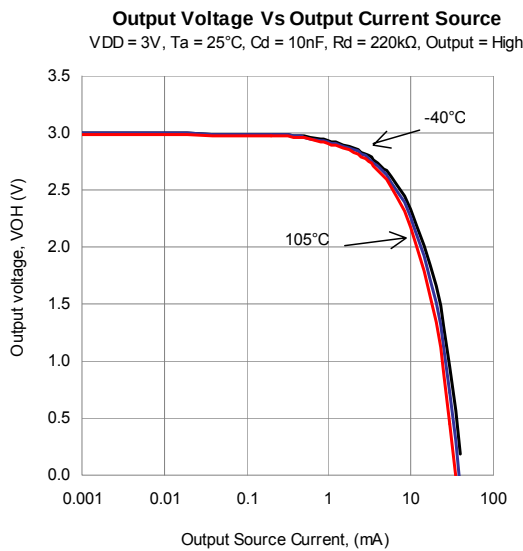
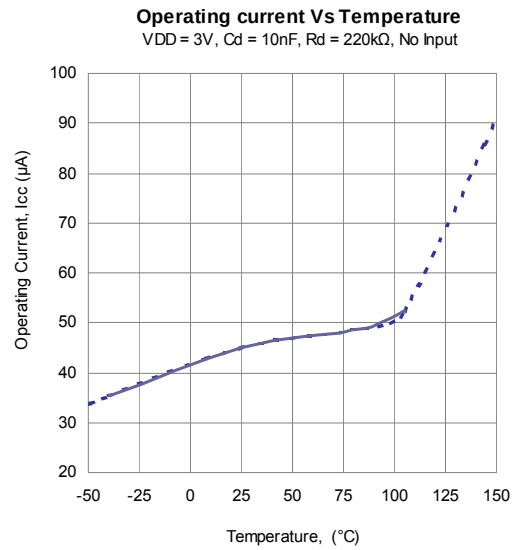
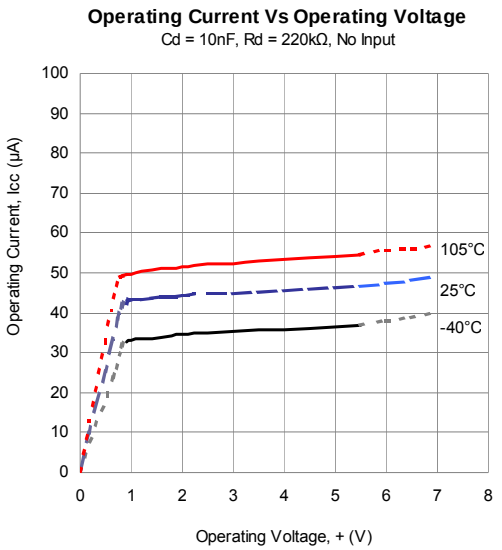
■ TERMINAL DESCRIPTION

Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
1	IN	AC Input		0.3V
2	AMP_OUT	Amplifier Output		0.3V
3	TRIN	External Trigger Input		-
5	CAP_D	Delay Time Capacitor		0V

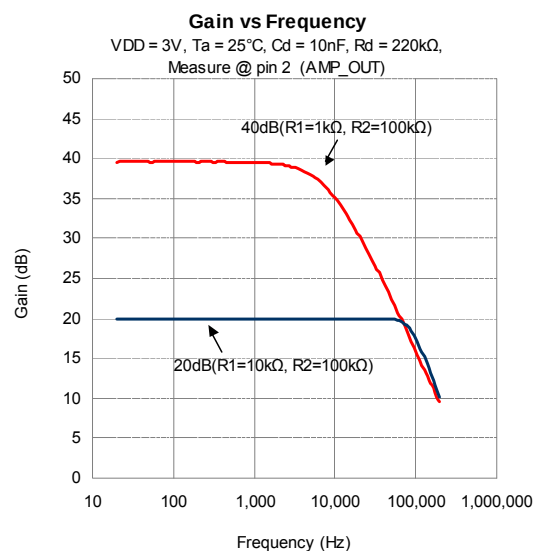
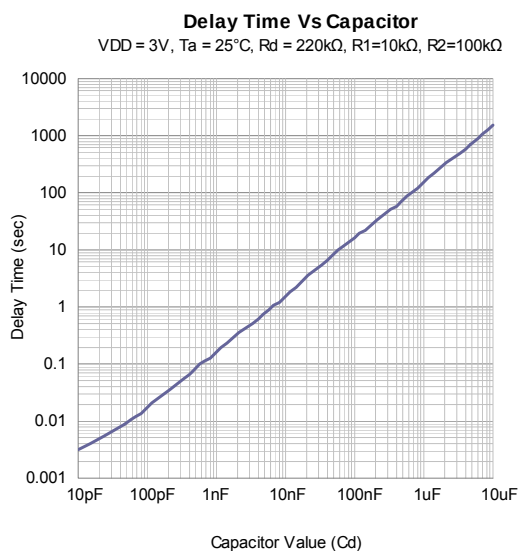
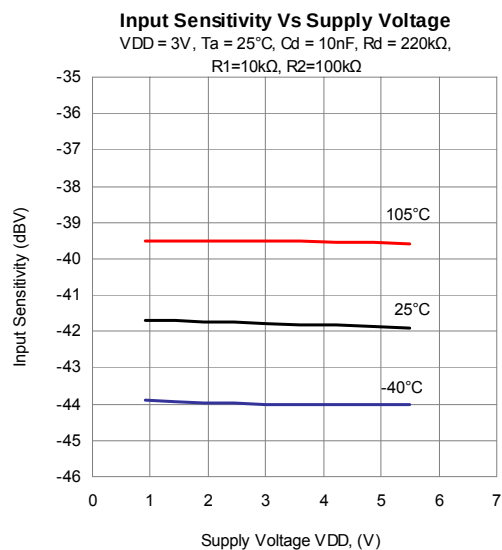
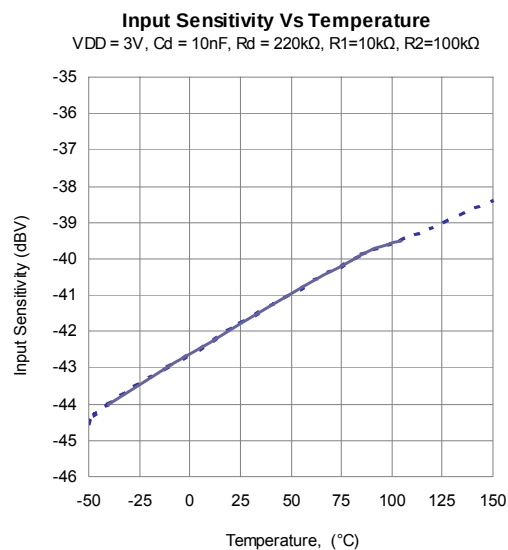
■ TERMINAL DESCRIPTION

Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
6	RES_D	Delay Time Resistor		$3\mu\text{A} \times R_D$
7	OUT	DC Output		0 or V^+
8	V^+	Supply Voltage		V^+

TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



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JONHON

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А