EL5421T

12MHz Rail-to-Rail Input-Output Buffer

FN6922
Rev 0.00
September 25, 2009

The EL5421T is a high voltage rail-to-rail input-output buffer with low power consumption. The EL5421T contains four buffers. Each buffer exhibits beyond the rail input capability, rail-to-rail output capability and is unity gain stable.

The maximum operating voltage range is from 4.5V to 19V. It can be configured for single or dual supply operation, and typically consumes only 500µA per buffer. The EL5421T has an output short circuit capability of ±200mA and a continuous output current capability of ±70mA.

The EL5421T features a slew rate of 12V/µs. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 12MHz (-3dB). This enables the buffers to offer maximum dynamic range at any supply voltage. These features make the EL5421T an ideal buffer solution for use in TFT-LCD panels as a V_{COM} or static gamma buffer, and in high speed filtering and signal conditioning applications. Other applications include battery power and portable devices, especially where low power consumption is important.

The EL5421T is available in a space saving 10 Ld MSOP package and operates over an ambient temperature range of -40°C to +85°C.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
EL5421TIYZ*	BBBLA	10 Ld MSOP	M10.118A

*Add “-T7” or “-T13” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

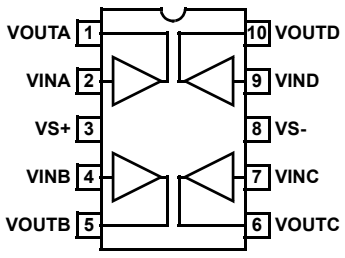
- 12MHz -3dB bandwidth
- 4 Unity Gain Buffers
- 4.5V to 19V Maximum Supply Voltage Range
- 12V/µs Slew Rate
- 500µA Supply Current (per buffer)
- ±70mA Continuous Output Current
- ±200mA Output Short Circuit Current
- Unity-gain Stable
- Beyond the Rails Input Capability
- Rail-to-rail Output Swing
- Built-in Thermal Protection
- -40°C to +85°C Ambient Temperature Range
- Pb-free (RoHS compliant)

Applications

- TFT-LCD Panels
- V_{COM} Buffers
- Electronics Notebooks
- Electronics Games
- Personal Communication Devices
- Personal Digital Assistants (PDA)
- Portable Instrumentation
- Wireless LANs
- Office Automation
- Active Filters
- ADC/DAC Buffers

Pinout

EL5421T
(10 LD MSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . . +19.8V
Input Voltage Range (V_{INx}) . . . . . (V_S-)-0.5V to (V_S+)+0.5V
Maximum Continuous Output Current . . . . . ±70mA
ESD Rating
Human Body Model 3000V

Thermal Information

Thermal Resistance Junction-to-Ambient (Typical) θ_{JA} (°C/W)
10 Ld MSOP (Note 1). 160
Storage Temperature . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Maximum Junction Temperature . . . . . .+150°C
Power Dissipation . . . . . .See Figure 27 and 28
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 10kΩ to 0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3	13	mV
TCV_{OS}	Average Offset Voltage Drift (Note 2)			4		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
A_V	Voltage Gain	-4.5V ≤ V_{OUTx} ≤ 4.5V	0.992		1.008	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.94	-4.85	V
V_{OH}	Output Swing High	I_L = +5mA	4.85	4.94		V
I_{SC}	Short Circuit Current	V_{CM} = 0V, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±200		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
(V_S+) - (V_S-)	Supply Voltage Range		4.5		19	V
I_S	Supply Current (Per Buffer)	V_{CM} = 0V, No load		500	750	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from ±2.25V to ±9.5V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	-4.0V ≤ V_{OUTx} ≤ 4.0V, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 4)	A_V = +1, V_{OUTx} = 2V step, R_L= 10kΩ, C_L= 8pF		500		ns
BW	-3dB Bandwidth	R_L= 10kΩ, C_L= 8pF		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

Electrical Specifications

V_S+ = +5V, V_S- = 0V, R_L = 10kΩ to 2.5V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 2.5V		3	13	mV
TCV_{OS}	Average Offset Voltage Drift (Note 2)			4		µV/°C
I_B	Input Bias Current	V_{CM} = 2.5V		2	50	nA

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 10k\Omega$ to 2.5V, $T_A = +25°C$ unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
R_{IN}	Input Impedance			1		GW
C_{IN}	Input Capacitance			2		pF
A_V	Voltage Gain	$0.5 \le V_{OUTx} \le 4.5V$	0.992		1.008	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -2.5mA		30	150	mV
V_{OH}	Output Swing High	I_L = +2.5mA	4.85	4.97		V
I_{SC}	Short Circuit Current	V_{CM} = 0V, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±125		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current (Per Buffer)	V_{CM} = 2.5V, No load		500	750	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$1V \le V_{OUTx} \le 4V$, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 4)	A_V = +1, V_{OUTx} = 2V step, R_L= 10kΩ, C_L= 8pF		500		ns
BW	-3dB Bandwidth	R_L= 10kΩ, C_L= 8pF		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

Electrical Specifications $V_S+ = +18V$, $V_S- = 0V$, $R_L = 10k\Omega$ to 9V, $T_A = +25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 9V		4	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 2)			5		µV/°C
I_B	Input Bias Current	V_{CM} = 9V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
A_V	Voltage Gain	$0.5 \le V_{OUTx} \le 17.5V$	0.992		1.008	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -9mA		100	150	mV
V_{OH}	Output Swing High	I_L = +9mA	17.85	17.90		V
I_{SC}	Short Circuit Current	V_{CM} = 9V, Source: V_{OUTx} short to V_S-, Sink: V_{OUTx} short to V_S+		±200		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current (Per Buffer)	V_{CM} = 9V, No load		550	750	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$1V \le V_{OUTx} \le 14V$, 20% to 80%		12		V/µs

Electrical Specifications $V_S+ = +18V$, $V_S- = 0V$, $R_L = 10k\Omega$ to 9V, $T_A = +25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
t_S	Settling to +0.1% (Note 4)	$A_V = +1$, $V_{OUTx} = 2V$ step, $R_L = 10k\Omega$, $C_L = 8pF$		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 8pF$		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

2. Measured over -40°C to +85°C ambient operating temperature range. See the typical TCV_{OS} production distribution shown in the "Typical Performance Curves" on page 5
3. Typical slew rate is an average of the slew rates measured on the rising (20% to 80%) and the falling (80% to 20%) edges of the output signal.
4. Settling time measured as the time from when the output level crosses the final value on rising/falling edge to when the output level settles within a ±0.1% error band. The range of the error band is determined by: Final Value(V)±[Full Scale(V)*0.1%]

Typical Performance Curves

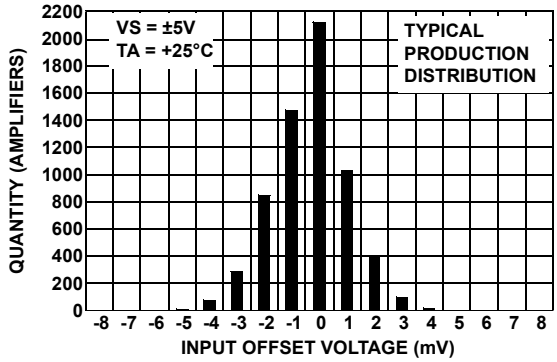


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

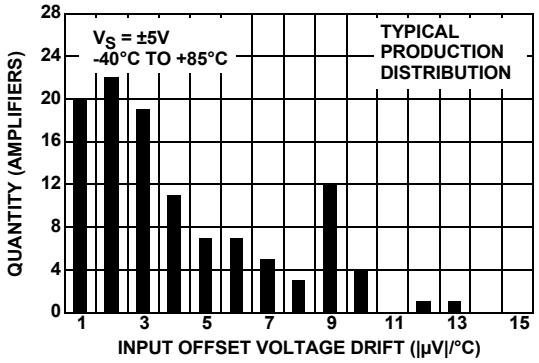


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT

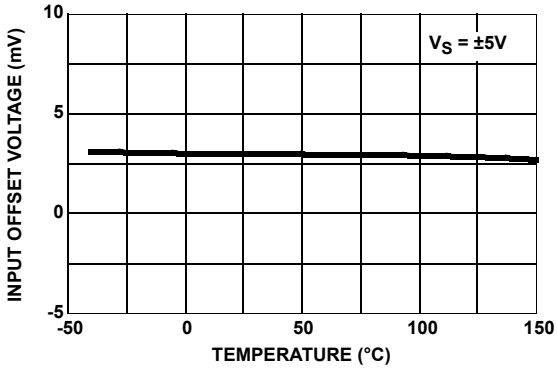


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

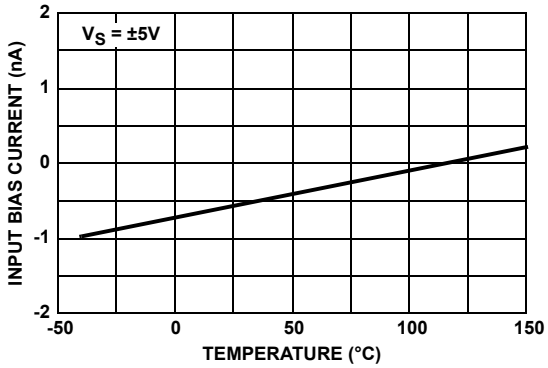


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

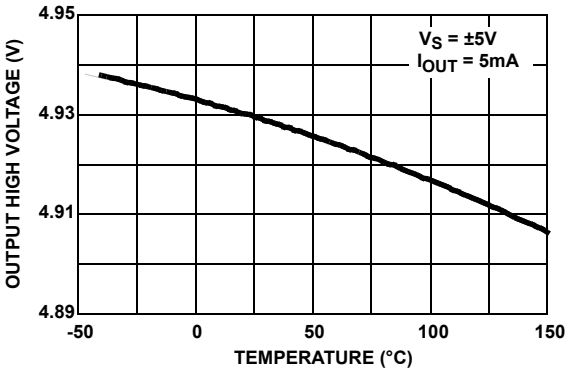


FIGURE 5. OUTPUT HIGH VOLTGE vs TEMPERATURE

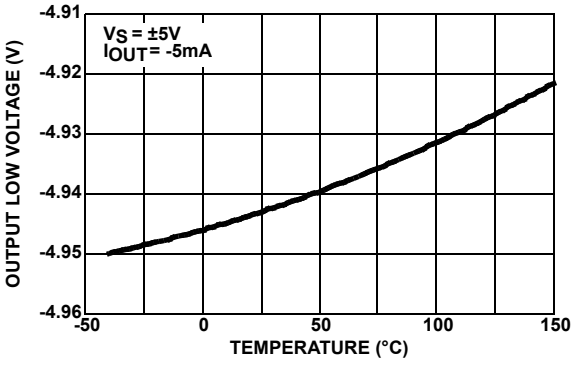


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

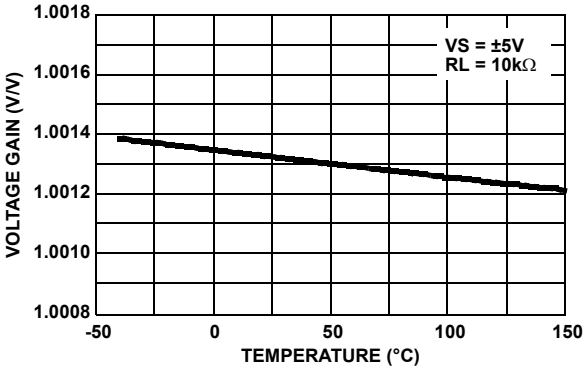


FIGURE 7. VOLTAGE GAIN vs TEMPERATURE

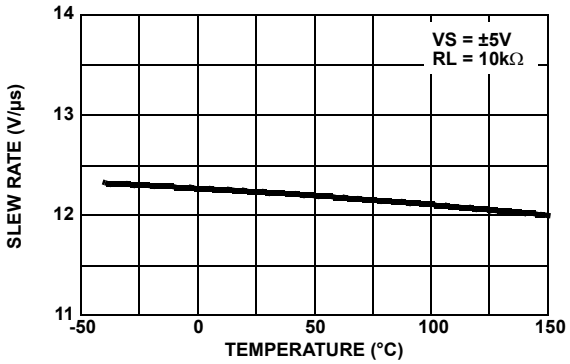


FIGURE 8. SLEW RATE vs TEMPERATURE

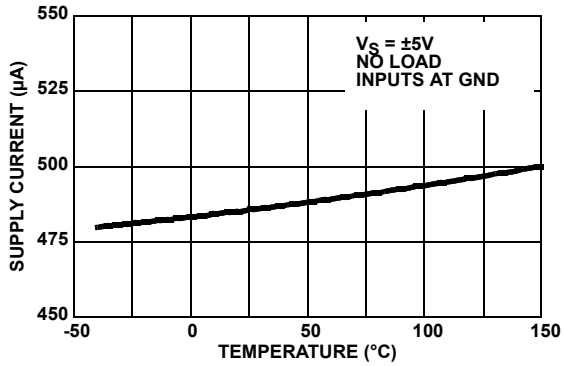


FIGURE 9. SUPPLY CURRENT PER CHANNEL vs TEMPERATURE

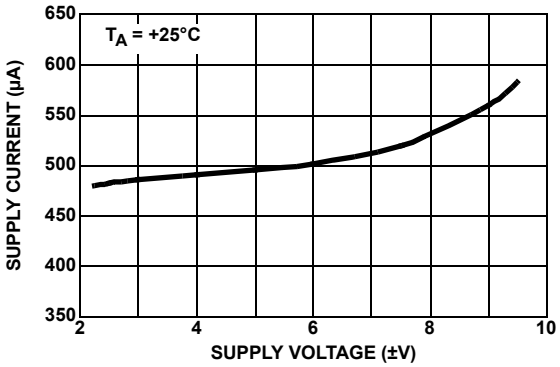


FIGURE 10. SUPPLY CURRENT PER CHANNEL vs SUPPLY VOLTAGE

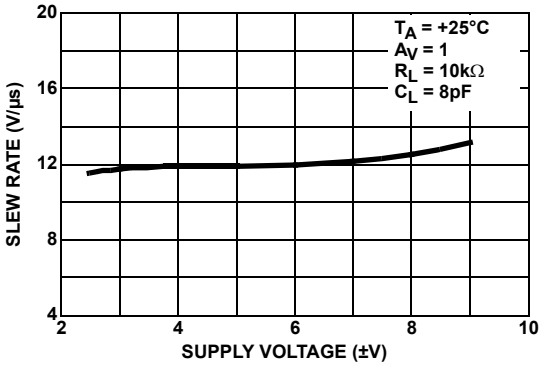


FIGURE 11. SLEW RATE vs SUPPLY VOLTAGE

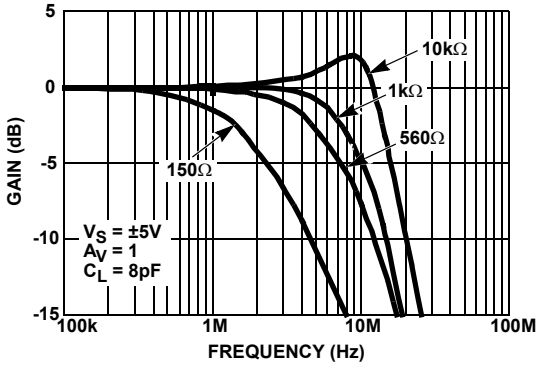


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS R_L

Typical Performance Curves (Continued)

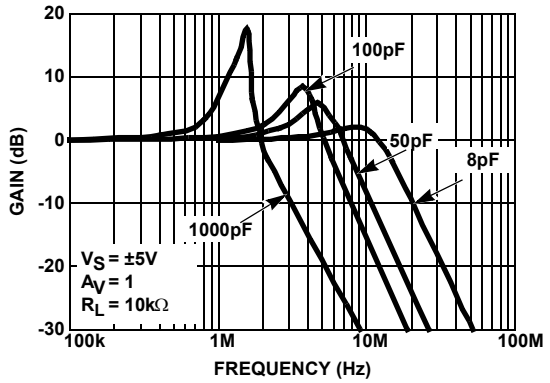


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS C_L

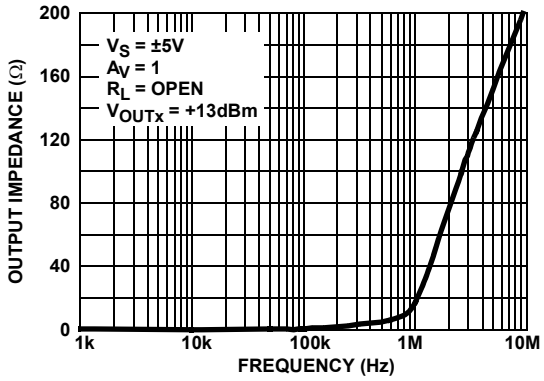


FIGURE 14. OUTPUT IMPEDANCE vs FREQUENCY

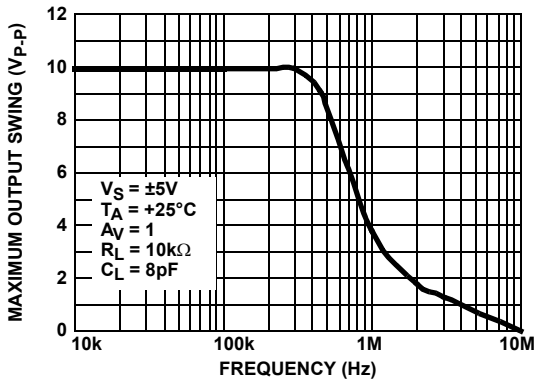


FIGURE 15. MAXIMUM OUTPUT SWING vs FREQUENCY

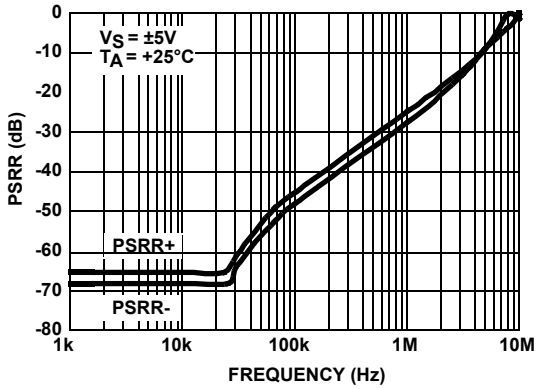


FIGURE 16. PSRR vs FREQUENCY

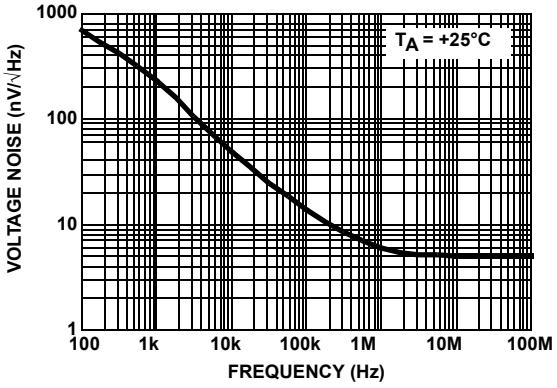


FIGURE 17. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

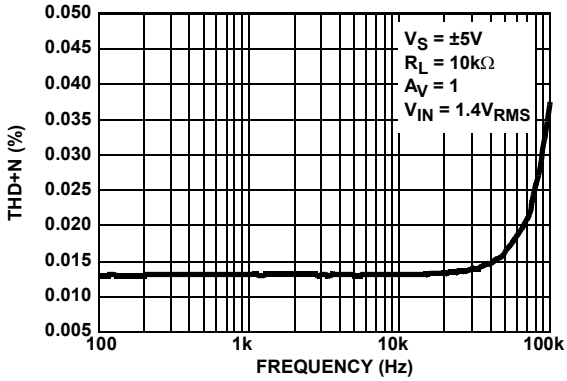


FIGURE 18. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

Typical Performance Curves (Continued)

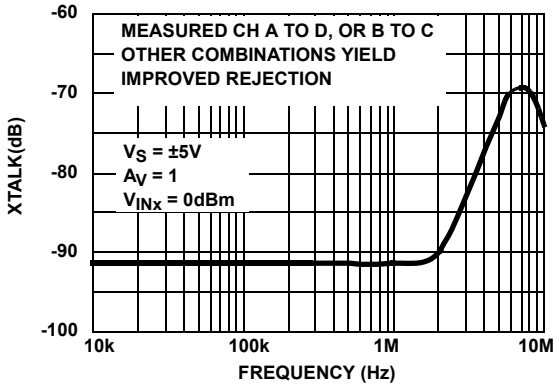


FIGURE 19. CHANNEL SEPARATION vs FREQUENCY RESPONSE

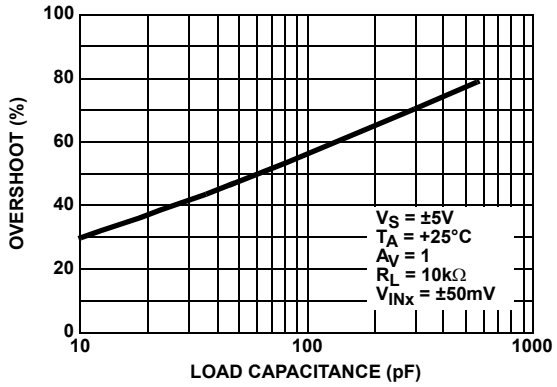


FIGURE 20. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE

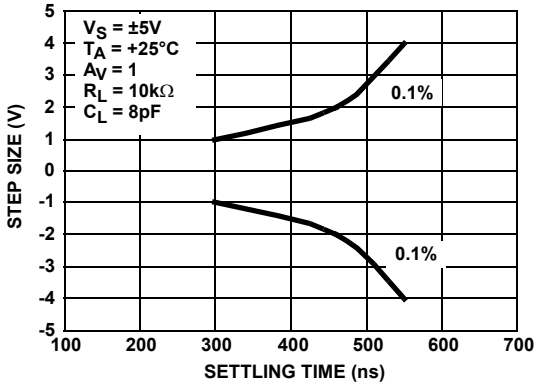


FIGURE 21. STEP SIZE vs SETTLING TIME

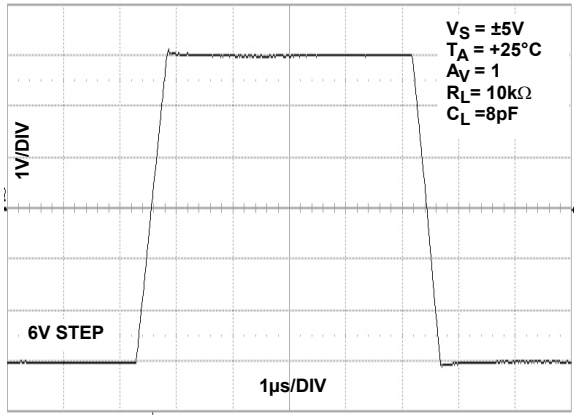


FIGURE 22. LARGE SIGNAL TRANSIENT RESPONSE

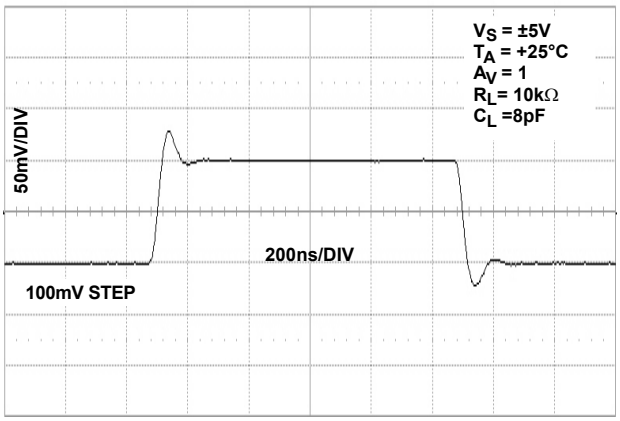


FIGURE 23. SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

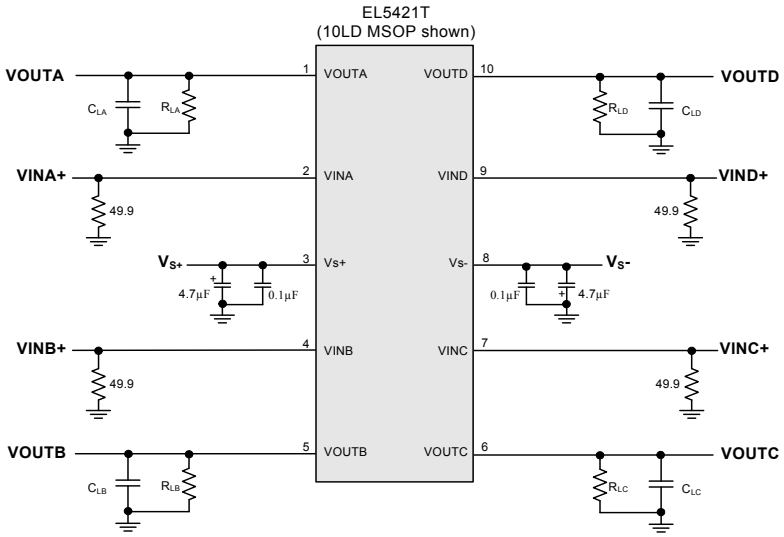
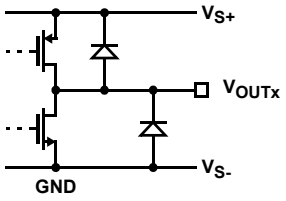


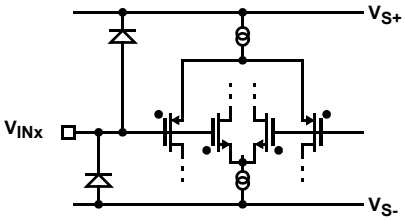
FIGURE 24. BASIC TEST CIRCUIT

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUTA	Buffer A Output	(Reference Circuit 1)
2	VINA	Buffer A Input	(Reference Circuit 2)
3	VS+	Positive Power Supply	
4	VINB	Buffer B Input	(Reference Circuit 2)
5	VOUTB	Buffer B Output	(Reference Circuit 1)
6	VOUTC	Buffer C Output	(Reference Circuit 1)
7	VINC	Buffer C Input	(Reference Circuit 2)
8	VS-	Negative Power Supply	
9	VIND	Buffer D Input	(Reference Circuit 1)
10	VOUTD	Buffer D Output	(Reference Circuit 2)



CIRCUIT 1



CIRCUIT 2

Applications Information

Product Description

The EL5421T is a high voltage rail-to-rail input-output buffer with low power consumption. The EL5421T contains four buffers. Each buffer exhibits beyond the rail input capability, rail-to-rail output capability and is unity gain stable.

The EL5421T features a slew rate of 12V/µs. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 12MHz (-3dB). This enables the buffers to offer maximum dynamic range at any supply voltage.

Operating Voltage, Input and Output Capability

The EL5421T can operate on a single supply or dual supply configuration. The EL5421T operating voltage ranges from a minimum of 4.5V to a maximum of 19V. This range allows for a standard 5V (or ±2.5V) supply voltage to dip to -10%, or a standard 18V (or ±9V) to rise by +5.5% without affecting performance or reliability.

The input common-mode voltage range of the EL5421T extends 500mV beyond the supply rails. Also, the EL5421T is immune to phase reversal. However, if the common mode input voltage exceeds the supply voltage by more than 0.5V, electrostatic protection diodes in the input stage of the device begin to conduct. Even though phase reversal will not occur, to maintain optimal reliability it is suggested to avoid input overvoltage conditions. Figure 25 shows the input voltage driven 500mV beyond the supply rails and the device output swinging between the supply rails.

The EL5421T output typically swings to within 50mV of positive and negative supply rails with load currents of ±5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 26 shows the input and output waveforms for the device in a unity-gain configuration. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid and the output voltage is approximately $9.9V_{P-P}$.

Refer to the “Electrical Specifications” Table beginning on page 2 for specific device parameters. Parameter variations with operating voltage, loading and/or temperature are shown in the “Typical Performance Curves” on page 5.

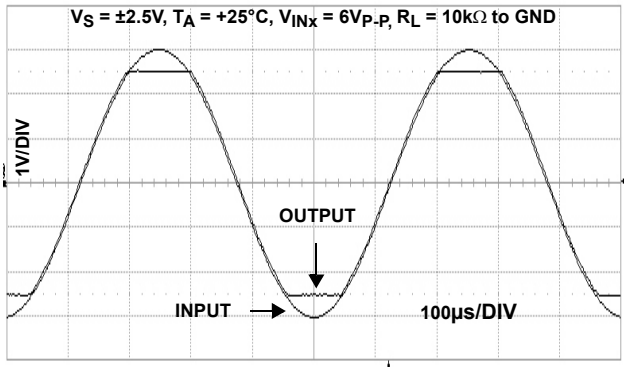


FIGURE 25. OPERATION WITH BEYOND-THE-RAILS INPUT

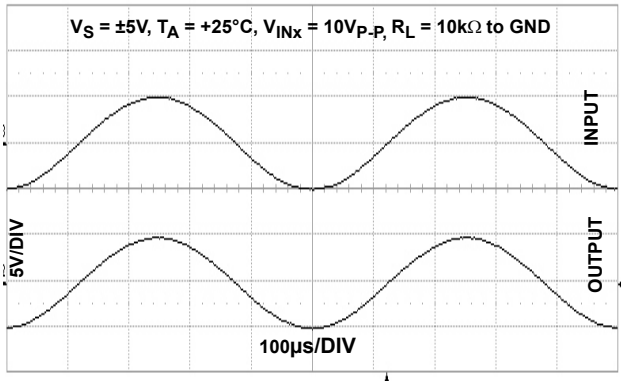


FIGURE 26. OPERATION WITH RAIL-TO-RAIL INPUT AND

Output Current

The EL5421T is capable of output short circuit currents of 200mA (source and sink), and the device has built-in protection circuitry which limits the short circuit current to ±200mA (typical).

To maintain maximum reliability the continuous output current should never exceed ±70mA. This ±70mA limit is determined by the characteristics of the internal metal interconnects. Also, see “Power Dissipation” on page 11 for detailed information on ensuring proper device operation and reliability for temperature and load conditions.

Unused Buffers

It is recommended that any unused buffers have their inputs tied to the ground plane.

Driving Capacitive Loads

As load capacitance increases, the -3dB bandwidth will decrease and peaking can occur. Depending on the application, it may be necessary to reduce peaking and to improve device stability. To improve device stability a snubber circuit or a series resistor may be added to the output of the EL5421T.

A snubber is a shunt load consisting of a resistor in series with a capacitor. An optimized snubber can improve the

phase margin and the stability of the EL5421T. The advantage of a snubber circuit is that it does not draw any DC load current or reduce the gain.

Another method to reduce peaking is to add a series output resistor (typically between 1Ω to 10Ω). Depending on the capacitive loading, a small value resistor may be the most appropriate choice to minimize any reduction in gain.

Power Dissipation

With the high-output drive capability of the EL5421T buffers, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. It is important to calculate the maximum power dissipation of the EL5421T in the application. Proper load conditions will ensure that the EL5421T junction temperature stays within a safe operating region.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation allowed

The total power dissipation produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power dissipation in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S+ - V_{OUT}i) \times I_{LOAD}i] \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S-) \times I_{LOAD}i] \quad \text{(EQ. 3)}$$

when sinking.

Where:

- i = 1 to 4

  (1, 2, 3, 4 corresponds to Channel A, B, C, D respectively)
- V_S = Total supply voltage ($V_S+ - V_S-$)
- V_S+ = Positive supply voltage
- V_S- = Negative supply voltage
- I_{SMAX} = Maximum supply current per buffer

  (I_{SMAX} = EL5421T quiescent current ÷ 4)
- V_{OUT} = Output voltage
- I_{LOAD} = Load current

Device overheating can be avoided by calculating the minimum resistive load condition, R_{LOAD}, resulting in the highest power dissipation. To find R_{LOAD} set the two P_{DMAX} equations equal to each other and solve for V_{OUT}/I_{LOAD}. Reference the package power dissipation curves, Figures 27 and 28, for further information.

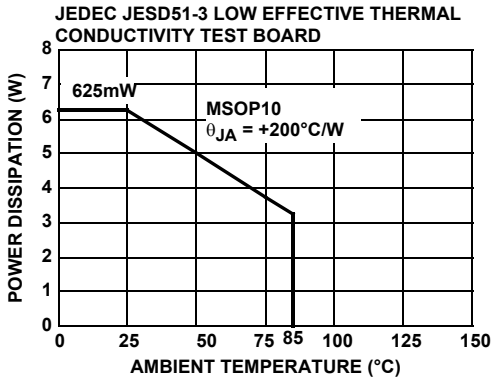


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

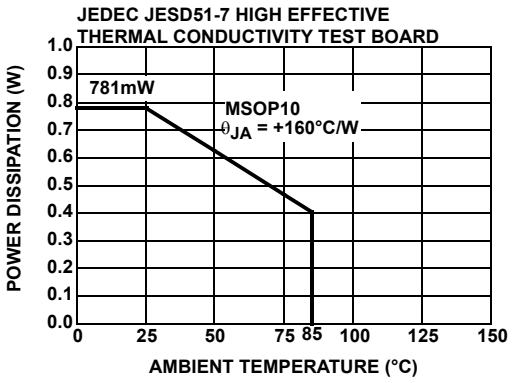


FIGURE 28. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Thermal Shutdown

The EL5421T has a built-in thermal protection which ensures safe operation and prevents internal damage to the device due to overheating. When the die temperature reaches +165°C (typical) the device automatically shuts OFF the outputs by putting them in a high impedance state. When the die cools by +15°C (typical) the device automatically turns ON the outputs by putting them in a low impedance or (normal) operating state.

Power Supply Bypassing and Printed Circuit Board Layout

The EL5421T can provide gain at high frequency, so good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, trace lengths should be as short as possible and the power supply pins must be well bypassed to reduce any risk of oscillation.

For normal single supply operation (the V_S- pin is connected to ground) a 4.7µF capacitor should be placed from V_S+ to ground, then a parallel 0.1µF capacitor should be connected as close to the device as possible. One 4.7µF capacitor may be used for multiple devices. For dual supply operation the same capacitor combination should be placed at each supply pin to ground.

Revision History

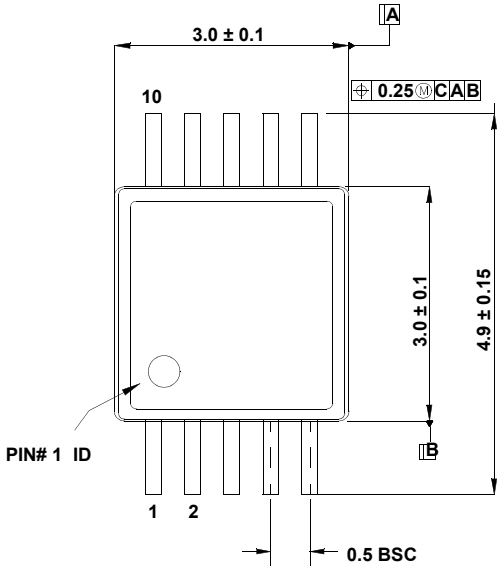
DATE	REVISION	CHANGE
9/10/09	FN6922.0	Issued File Number FN6922. Initial release of Datasheet with file number FN6922 making this a Rev 0.

Package Outline Drawing

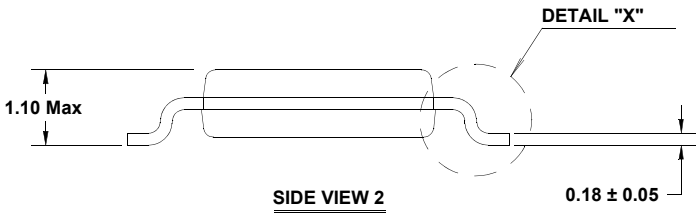
M10.118A (JEDEC MO-187-BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

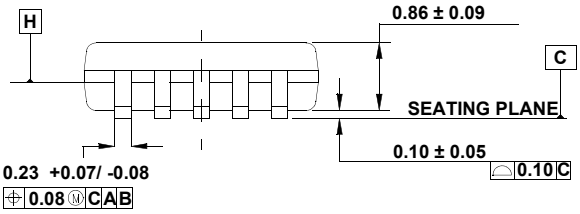
Rev 0, 9/09



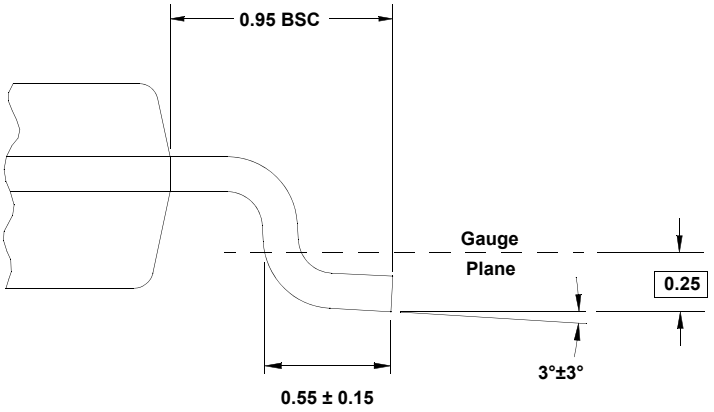
TOP VIEW



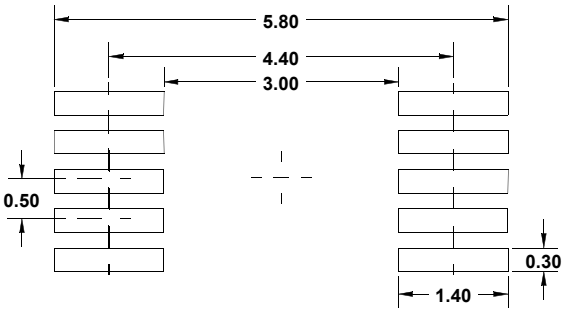
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.

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