APDS-9151

Digital Proximity and RGB Sensor in Small Aperture

Data Sheet

Description

The Broadcom® APDS-9151 is an integrated RGB, proximity detector and IR LED in an optical module.

The APDS-9151 provides digital RGB, ambient light sensing (ALS), IR LED, and a complete proximity detection system in a single 8-pin package that is suitable to be used under a small aperture of the devices' cover windows. The APDS-9151 device uses four individual channels of red, green, blue, and IR (RGB+IR) in a specially designed matrix arrangement. This allows the device to have optimal angular response and accurate RGB spectral response with high lux accuracy over various light sources. The proximity detection feature operates well from bright sunlight to dark rooms. The APDS-9151 is particularly useful for display management with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions.

The APDS-9151 has a wide dynamic range. Current is programmable in eight different steps and the LED pulse number can be varied from by pulse step, and the LED modulation frequency can be set from 60 kHz to 100 kHz in five steps. PS resolution can be varied from 8 bits to 11 bits, and the measurement rate is from 6.25 ms to 400 ms. To offset unwanted reflected light from the cover glass, a PS intelligent cancellation level register allows for an on-chip subtraction of the ADC count caused by the unwanted reflected light from PS ADC output.

Both the PS and ALS function independently allowing for maximum flexibility in application.

Features

- RGB and ambient light sensing (RGB and ALS)
  - Accuracy of correlated colour temperature (CCT)
  - Individual channels for red, green, blue, and infrared
  - Approximates human eye response with green channel
  - Light output proportional to light intensity
  - Utilizes optical coating technology to emulate human eye spectral response
  - Works well under different light source conditions
  - Low light sensitivity; operates behind darkened glass
  - 50 Hz/60 Hz light flicker immunity
  - Fluorescent light flicker immunity
  - Programmable interrupt function with upper, lower thresholds and persists function
  - Programmable LS integration time
  - Programmable LS gain setting
- Proximity detection (PS)
  - Integrated IR LED and Synchronous LED driver
  - 100K lux sunlight suppression
  - Cancellation of crosstalk
  - Programmable interrupt function with upper, lower thresholds and persists function
  - Programmable LED drive current
- Supply voltage 1.7V to 3.6V
- Power management
  - Low active current
  - Low standby current
- I^2C interface compatible
  - Up to 400 kHz (I^2C Fast-Mode)
  - Dedicated interrupt pin
- Miniature package
  - 2.55 mm (length) × 2.05 mm (width) × 0.95 mm (height)

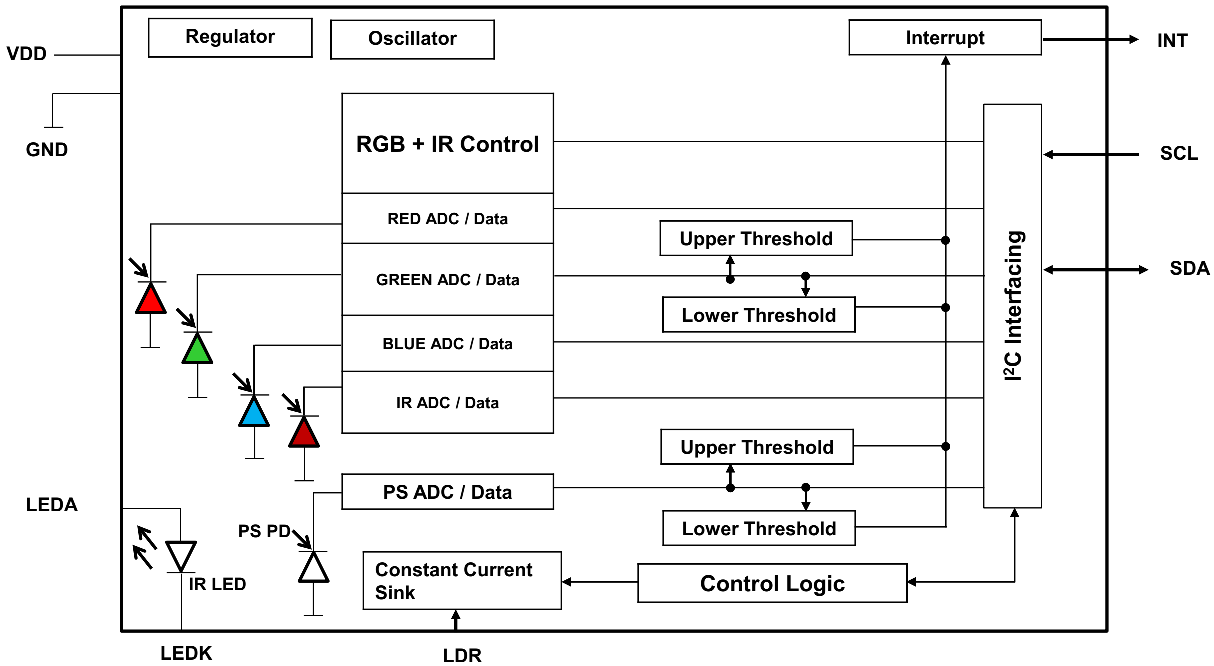
Applications

- OLED display control
- RGB backlight control
- Cell phone touch-screen disable
- Automatic speakerphone enable
- Digital camera eye sensor

Ordering Information

Part Number	Packaging	Quantity
APDS-9151	Tape and Reel	10,000

Functional Block Diagram



I/O Pins Configuration

Pin	Name	Type	Description
1	GND	Ground	Power supply ground. All voltages are referenced to GND
2	INT	O	Interrupt. Open drain
3	LDR	I	LED driver for proximity emitter – up to 125 mA, open drain.
4	LEDK	O	LED Cathode, connect to LDR pin in most systems to use internal LED driver circuit
5	LEDA	I	LED supply voltage
6	V_{DD}	Supply	Power supply voltage
7	SDA	I/O	Serial data I/O for I^2C
8	SCL	I	I^2C serial clock input terminal. Clock signal for I^2C serial data

Absolute Maximum Ratings

Over operating free-air temperature range (see note).

Parameter	Symbol	Min.	Max.	Units	Conditions
Power Supply Voltage[a]	V_{DD}	—	3.63	V	
Digital Voltage Range		–0.5	3.63	V	
Storage Temperature Range	Tstg	–40	100	°C	

a. All voltages are with respect to GND.

NOTE Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Ambient Temperature	T_A	–40	—	85	°C
Supply Voltage	V_{DD}	1.7	—	3.6	V
Supply Voltage Accuracy, V_{DD} total error Including transients		–1	—	1	%
LED Supply Voltage	V_{LED}	2.5	—	4.6	V

Operating Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
SCL, SDA Input High Voltage	V_{IH}	1.5	—	V_{DD}	V	
SCL, SDA Input Low Voltage	V_{IL}	0	—	0.4	V	
INT, SDA Output Low Voltage	V_{OL}	0	—	0.4	V	
Leakage Current, SDA, SCL, INT Pins	I_{LEAK}	–5	—	5	µA	

RGB Optical Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Test Condition	Red Channel		Green Channel		Blue Channel		IR Channel		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Irradiance Response	λ = 465	0	8	6	22	80	120	0	4	%
	λ = 525	2	14	80	120	10	30	0	3	
	λ = 625	80	120	18	37	0	3	0	3	
	λ = 850	0	3	0	3	0	3	80	120	

NOTE

1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the IR channel value.
2. The 465-nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 22 nm.
3. The 525-nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 35 nm.
4. The 625-nm input irradiance is supplied by an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 625 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 15 nm.
5. The 850-nm input irradiance is supplied by an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 850 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 40 nm.

RGB/ALS Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current	I_{DD}	—	118	154	µA	Active mode
		—	1	2	µA	Standby mode
Peak Wavelength	$\lambda_{P\_ALS/Green}$	—	550	—	nm	
	λ_{P_Red}	—	610	—	nm	
	λ_{P_Blue}	—	470	—	nm	
Min. Integration Time	$T_{intmin1}$	—	3.125	—	ms	
	$T_{intmin2}$	—	50	—	ms	With 50 Hz/60 Hz rejection
Max Integration Time	T_{intmax}	—	400	—	ms	With 50Hz/60 Hz rejection
Output Resolution	RES_{ALS}	13	18	20	bit	Programmable
ADC Count Value (ALS/Green)		800	1000	1200	counts	λ = 525 nm, 50 ms, Gain = 3x, Ee = 72 µW/cm^2
ADC Count Value (Red)		800	1000	1200	counts	λ = 625 nm, 50 ms, Gain = 3x, Ee = 78 µW/cm^2
ADC Count Value (Blue)		800	1000	1200	counts	λ = 465 nm, 50 ms, Gain = 3x, Ee = 73 µW/cm^2
Dark Count Value (ALS/Green)		0	—	3	counts	Gain = 18×, 50 ms, Ee = 0[a]
Dark Count Value (Red)		0	—	3	counts	Gain = 18×, 50 ms, Ee = 0[a]
Dark Count Value (Blue)		0	—	3	counts	Gain = 18×, 50 ms, Ee = 0[a]

a. At any one time, under dark environment, not more than one channel (Red, Green, Blue) dark count value is more than 1.

IR LED Characteristics

T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Wavelength	λ_P	—	950	—	nm	I_F = 20 mA
Spectrum Width, Half Power	Δλ	—	50	—	nm	I_F = 20 mA
Optical Rise Time	T_R	—	20	—	ns	I_F = 100 mA
Optical Fall Time	T_F	—	20	—	ns	I_F = 100 mA

PS Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current [w/o LED Current]		—	99	—	µA	Active mode, 32 pulse, 60 kHz, 125 mA, 100 ms wait time
Supply Curent (PS + LED only)		—	432	—	µA	Active mode, 32 pulse, 125 mA, 100 ms wait time
Full Scale ADC Count Value		—	—	2047	counts	11 bit
PS Resolution		8	—	11	bit	
IR LED Pulse Count		1	—	255	pulses	
Proximity LED Drive		2.5	—	125	mA	I_{SINK} Sink current at 600 mV, LDR Pin
Frequency of PS LED Pulses (Programmable)		60	—	100	kHz	
Duty Ratio of PS LED Pulses		50%	—	—		
PS ADC Count Value (No Object)		—	—	300	counts	Dedicated duo power supply, Vdd = 2.8 V and VLED = 3V, LED driving 32 pulses, 125 mA, 60 kHz, 11-bit, (0.7-mm thickness clear glass, 0.2-mm air gap) and no reflective object above the module
PS Signal Delta ADC Count Value (30-mm Distance Object)		120	150	180	counts	Dedicated duo power supply, Vdd = 2.8 V and VLED =3V, reflecting object – 73 mm × 83 mm Kodak 18% grey card, 30-mm distance, LED driving 32 pulses, 125 mA, 60 kHz, 11-bit. (0.7-mm thickness clear glass, 0.2-mm air gap)

Figure 1 Spectral Response

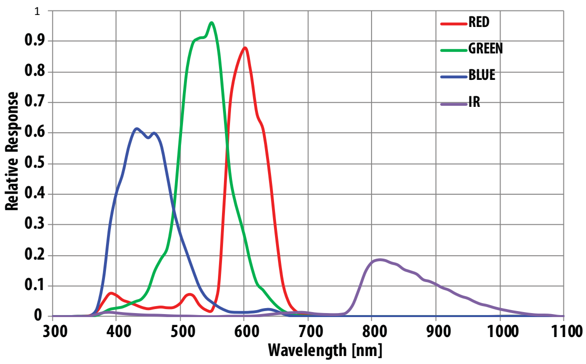


Figure 2 ALS Sensor LUX vs. Meter LUX Using White Light

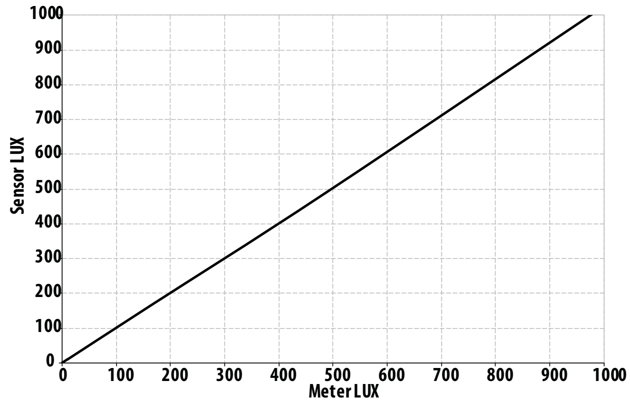


Figure 3 Normalized IDD vs. Temperature

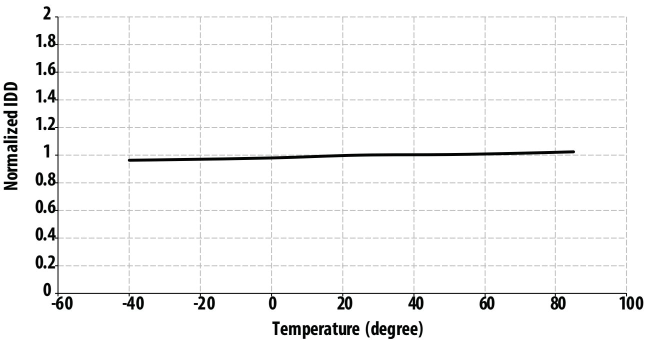


Figure 4 Normalized IDD vs. VDD

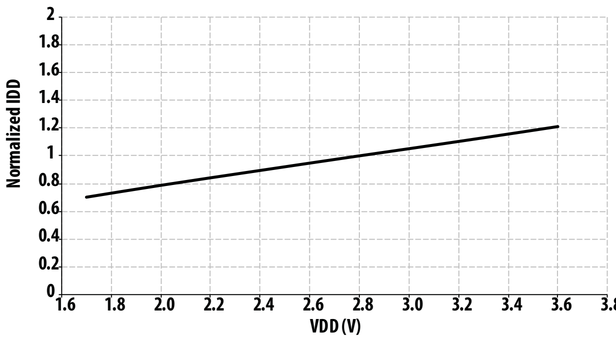


Figure 5 Normalized PD Responsitivity vs. Angular Displacement (Perpendicular Axis)

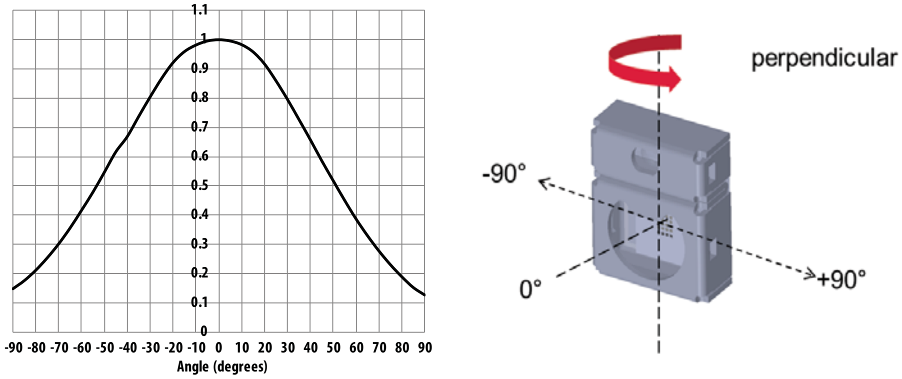
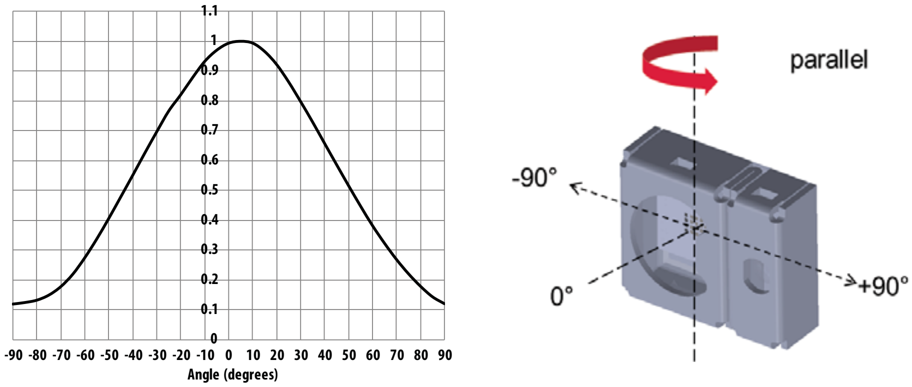


Figure 6 Normalized PD Responsitivity vs. Angular Displacement (Parallel Axis)



ALS Gain and Resolution Settings

Gain	itime (ms)	min lux	max lux	res (lux/ct)
1X	3.125	28.8288	236166	28.8288
	25	3.6036	236166	3.6036
	50	1.8018	236166	1.8018
	100 (default)	**0.9009**	**236166**	**0.9009**
	200	0.4505	236166	0.4505
	400	0.2252	236166	0.2252
3X (default)	3.125	9.4675	77557	9.4675
	25	1.1834	77557	1.1834
	50	0.5917	77557	0.5917
	100 (default)	**0.2959**	**77557**	**0.2959**
	200	0.1479	77557	0.1479
	400	0.0740	77557	0.0740
6X	3.125	4.7267	38721	4.7267
	25	0.5908	38721	0.5908
	50	0.2954	38721	0.2954
	100 (default)	**0.1477**	**38721**	**0.1477**
	200	0.0739	38721	0.0739
	400	0.0369	38721	0.0369
9X	3.125	3.1189	25550	3.1189
	25	0.3899	25550	0.3899
	50	0.1949	25550	0.1949
	100 (default)	**0.0975**	**25550**	**0.0975**
	200	0.0487	25550	0.0487
	400	0.0244	25550	0.0244
18X	3.125	1.5459	12664	1.5459
	25	0.1932	12664	0.1932
	50	0.0966	12664	0.0966
	100 (default)	**0.0483**	**12664**	**0.0483**
	200	0.0242	12664	0.0242
	400	0.0121	12664	0.0121

Principles of Operation

System State Machine

Start Up after Power-On or Software Reset

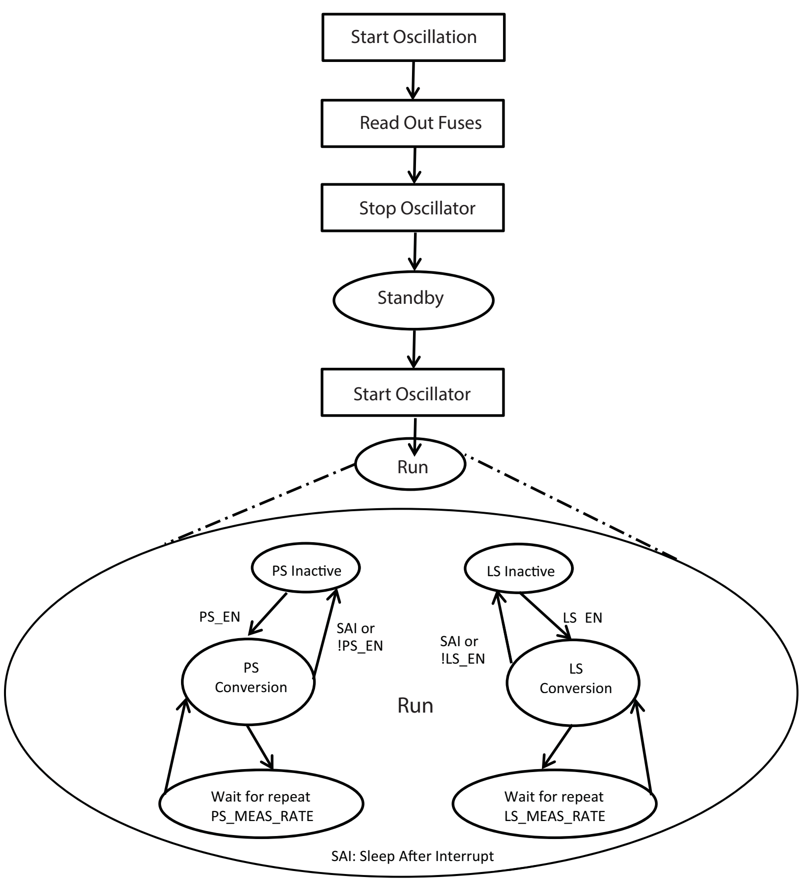
The main state machine is set to Start State during power-on or software reset. As soon as the reset is released, the internal oscillator is started and the programmed I^2C address and the trim values are read from the internal non-volatile memory (NVM) trimming data block. The device enters Standby Mode as soon as the Idle State is reached.

If any of the sensor operation modes becomes activated through an I^2C command (i.e., the LS_EN bit is set to 1 and the sensor mode is selected with the respective bit in the MAIN_CTRL register), the internal support blocks are immediately powered on. Once the voltages and currents are settled (typical after 500 µs), the state machine checks for trigger events from a measurement scheduler to start conversions according to the selected measurement repeat rates.

When the user resets the LS_EN bit (or the PS_EN bit) to 0, a running conversion is completed and the relevant ADCs move to Standby Mode thereafter. The support blocks only move to Standby Mode if all Sensors are Inactive. If any of the sensors is programmed to *sleep after interrupt* with the according bit in the MAIN_CTRL register, the relevant ADCs move to Standby Mode after the interrupt condition occurred. Also the sensor's Enable bit LS_EN or PS_EN are reset after following read out of Main Status register.

The deactivation of either LS or PS in the MAIN_CTRL register does not clear the related status bit in the MAIN_STATUS register. They are always reset upon activation of the respective sensor.

Figure 7 State Diagram



Light Sensor and Proximity Sensor Operation

The Light Sensor (LS) can be operated independently and in parallel to the Proximity Sensor (PS). It can be configured to run in ALS mode or in RGB mode. The difference between both submodes of the Light Sensor is in the activation of the sensor channels. ALS mode is offered for power saving if the full RGB functionality is not needed.

The proximity sensor can be operated independently and in parallel to the light sensor. To reduce the influence of crosstalk, the APDS-9151 has an analog and a digital crosstalk cancellation built in. By using the analog cancellation, a reduction of the sensor's dynamic range can be avoided. Additionally, a digital cancellation value can still be automatically subtracted from the PS conversion result if needed. Both values are accessible via a register and the external application must determine the appropriate cancelation values prior to the start of the measurement.

Light Sensor Interrupt

The interrupt is configured by the bit in the INT_CFG register. It can function as either threshold triggered (LS_VAR_MODE = 0) or variance trigged (LS_VAR_MODE = 1).

The threshold interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 0. The interrupt is set when the respective *_DATA register of the selected interrupt source channel is above the upper or below the lower threshold configured in the LS_THRES_UP and LS_THRES_LOW registers for a specified number of consecutive measurements as configured in the INT_PST register (1+LS_PERSIST).

The variance interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 1. It is set when the absolute value difference between the preceding and the current output data of the selected interrupt source channel is above the decoded variance threshold for a specified number of consecutive measurements (1+LS_PERSIST).

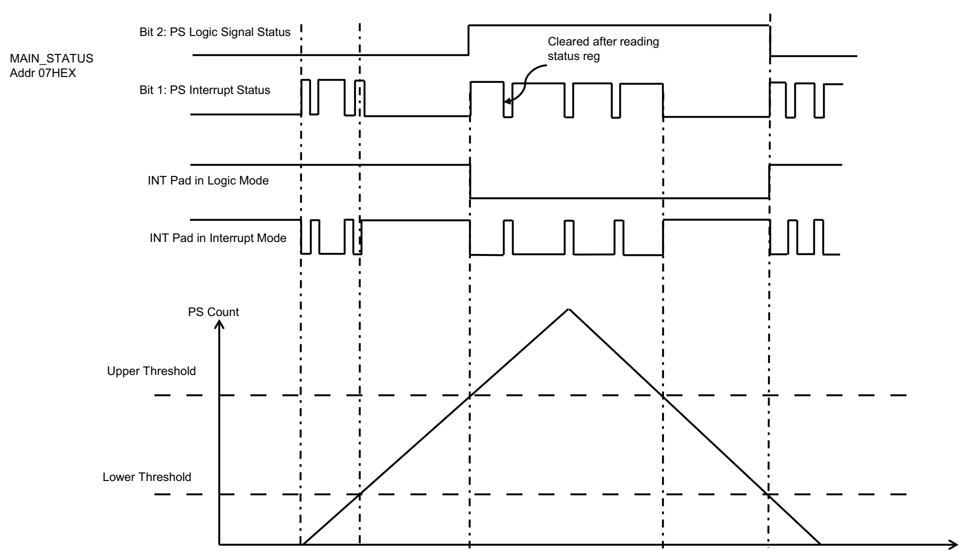
Proximity Sensor Interrupt

The interrupt is configured by the bit in the INT_CFG register. It is threshold triggered.

The interrupt is enabled with PS_INT_EN = 1. The interrupt is set when the PS_DATA register content is above the upper or below the lower threshold configured in the PS_THRES_UP and PS_THRES_LOW registers for a specified number of consecutive measurements as configured in the INT_PST register (1+PS_PERSIST).

The ps_logic signal (PS_LOGIC_STAT bit in the MAIN_STATUS register) is set to 0 if the PS data is below the lower PS threshold, and it is set to 1 if the PS data is above the upper PS threshold.

Figure 8 PS Interrupt Behavior



NOTE The MAIN_STATUS register should be read out closely after an interrupt transition occurred on the INT pad. Because the interrupt is not reset automatically, an interrupt event caused by crossing the opposite threshold could be missed.

Interrupt

The APDS-9151 generates independent ALS and PS interrupt signals.

For LS, an interrupt can also be triggered if the output variation of consecutive conversions has exceeded a defined limit.

The PS logic output mode has priority over any other interrupt signal. If selected PS_LOGIC_MODE = 1), no LS interrupt can be signaled at the INT pad. Both LS and PS, as well as PS_LOGIC_MODE are active low at the INT pin. A cleared LS interrupt status or PS interrupt status flag also clears the interrupt signal on the INT pin.

Another feature is the option to deactivate both sensors after and interrupt event occurred. Therefore, a bit for the respective sensor has to be set in the MAIN_CTRL register (SAI_PS and SAI_LS). This feature is independently available for both sensors.

Optical Design Characteristics

The APDS-9151 simplifies the optical system design by eliminating the need for light pipes and optical barrier with specially designed apertures and package shielding which will reduce crosstalk when placed in the final system. The module package design has been optimized for minimum package foot print and short distance proximity of 30 mm typical. The spacing between the cover glass surface and package top surface is critical to controlling the crosstalk. With some simple mechanical design implementations, the APDS-9151 will perform well in the end equipment system.

APDS-9151 module optimized design parameters:

- Cover glass thickness, t ≤ 1.3 mm
- Air gap, g ≤ 0.3 mm
- Cover glass IR transmittance ≥ 80%.

The APDS-9151 is available in a miniaturize and low profile package that contains optics that provide optical gain on both the LED and the sensor side of the package. The device has a package Z height of 0.95 mm and will support an air gap of ≤ 0.3 mm between the cover glass and the package. The assumption of the optical system level design is that cover glass surface above the module is ≤0.3 mm.

Figure 9 Optical Design Considerations

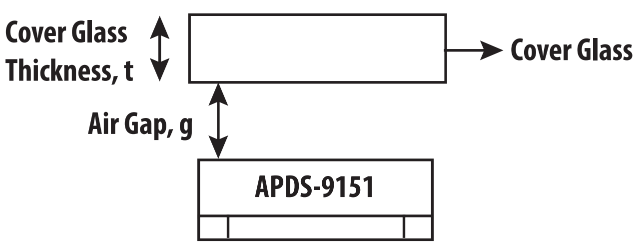
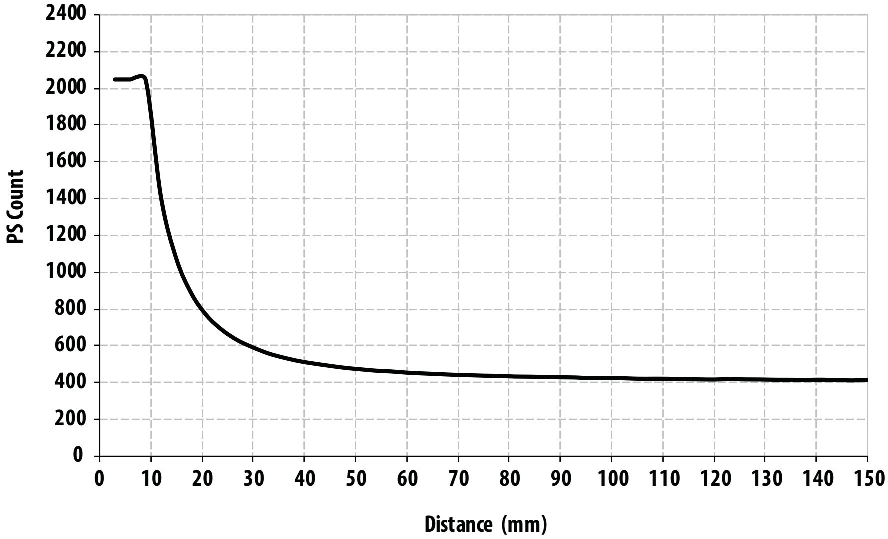


Figure 10 PS Output vs. Distance at 125 mA at 32 Pulse Count. No Glass in Front of Module, 18% Kodak Grey Card.



I^2C Protocol

Interface and control of the APDS-9151 is accomplished through an I^2C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x52 hex using 7 bit addressing protocol. (Contact factory for other addressing options.)

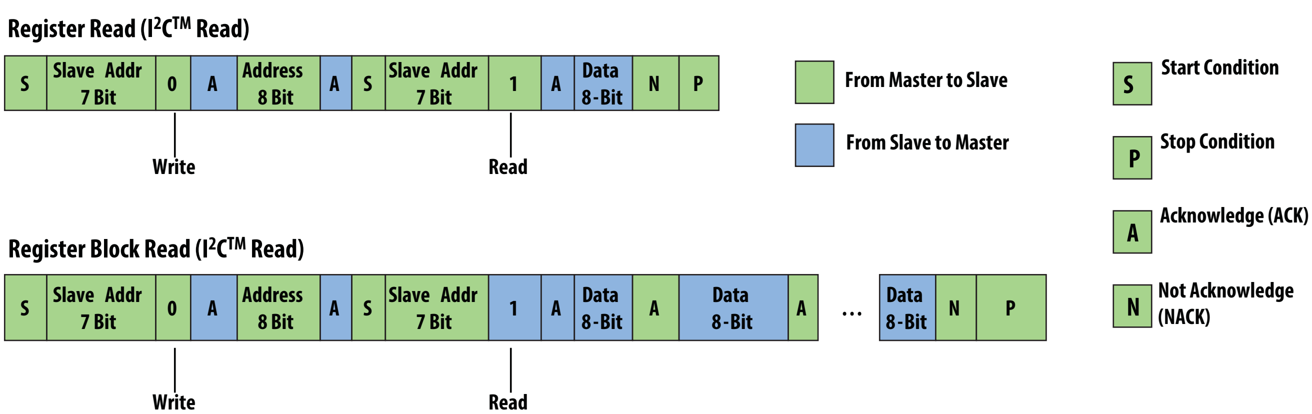
I^2C Register Read

The registers can be read individually or in block read mode. When two or more bytes are read in block read mode, reserved register addresses are skipped and the next valid address is referenced. If the last valid address has been reached, but the master continues with the block read, the address counter in the device does not roll over and the device returns 00HEX for every subsequent byte read.

The block read operation is the only way to ensure correct data read out of multi-byte registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. During block read access on ALS result registers, the result update is blocked.

If a read access is started on an address belonging to a non-readable register, the APDS-9151 returns NACK until the I^2C operation is ended.

Read operations must follow this timing diagram.



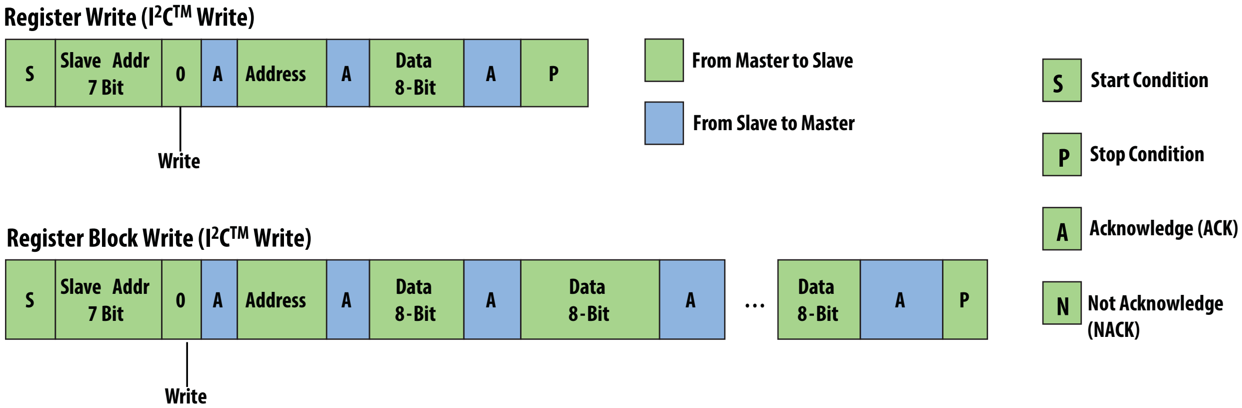
I^2C Register Write

The APDS-9151 registers can be written to individually or in block write mode. When two or more bytes are written in block write mode, reserved registers and read-only registers are skipped. The transmitted data is automatically applied to the next writable register. If a register includes read (R) and read/write (RW) bit, the register is not skipped. Data written to read-only bit is ignored.

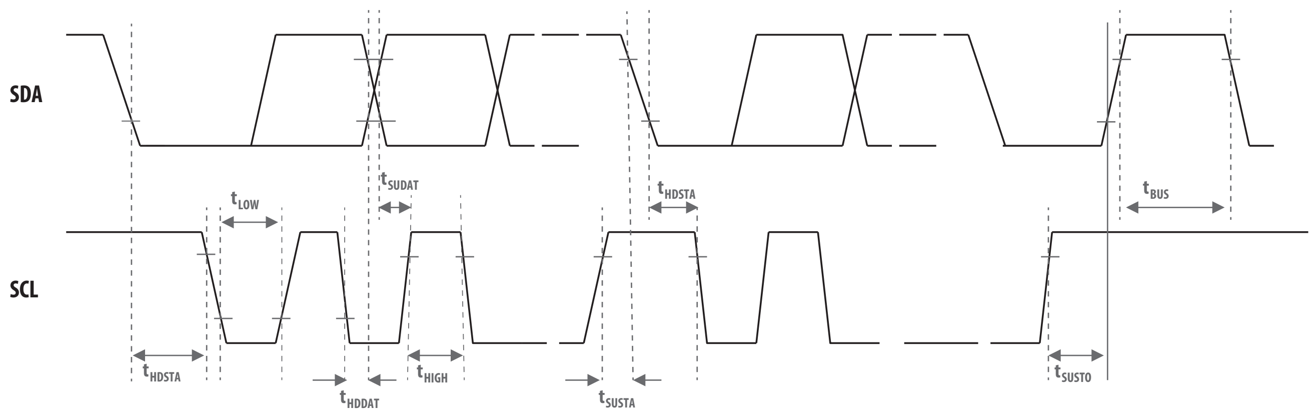
If the last valid address of the APDS-9151 address range is reached but the master attempts to continue the block write operation, the address counter of the APDS-9151 does not roll over. The APDS-9151 returns NACK for every following byte sent by the master until the I^2C operation is ended.

If a write access is started on an address belonging to a non-writeable register, the APDS-9151 returns NACK until the I^2C operation is ended.

Write operations must follow this timing.



I²C Interface – Bus Timing



Bus Timing Characteristics

Parameter	Symbol	Standard Mode	Fast Mode	Unit
Maximum SCL Clock Frequency	f_{SCL}	100	400	kHz
Minimum START Condition Hold Time Relative to SCL Edge	t_{DSTA}	4	—	µs
Minimum SCL Clock Low Width	t_{LOW}	4.7	—	µs
Minimum SCL Clock High Width	t_{HIGH}	4	—	µs
Minimum START Condition Setup Time Relative to SCL Edge	t_{SUSTA}	4.7	—	µs
Minimum Data Hold Time on SDA Relative to SCL Edge	t_{HDDAT}	0	—	µs
Minimum Data Setup Time on SDA Relative to SCL Edge	t_{SUDAT}	0.1	0.1	µs
Minimum STOP Condition Setup Time on SCL	t_{SUSTO}	4	—	µs
Minimum Bus Free Time Between Stop Condition and Start Condition	t_{BUS}	4.7	—	µs

Register Set

The APDS-9151 is controlled and monitored by data registers and command registers accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

Address	Type	Name	Description	Reset Value
00HEX	RW	MAIN_CTRL	Operation mode control, SW reset	00HEX
01HEX	RW	PS_LED	PS LED settings	36HEX
02HEX	RW	PS_PULSES	PS number of LED pulses	08HEX
03HEX	RW	PS_MEAS_RATE	PS measurement rate in active mode	05HEX
04HEX	RW	LS_MEAS_RATE	LS measurement rate and resolution	22HEX
05HEX	RW	LS_Gain	LS analog gain range	01HEX
06HEX	R	PART_ID	Part number ID and revision ID	C2HEX
07HEX	R	MAIN_STATUS	Power-on status, interrupt status, data status	20HEX
08HEX	R	PS_DATA_0	PS measurement data, least significant bit	00HEX
09HEX	R	PS_DATA_1	PS measurement data, most significant bit, and overflow	00HEX
0AHEX	R	LS_DATA_IR_0	IR ADC measurement data, LSB	00HEX
0BHEX	R	LS_DATA_IR_1	IR ADC measurement data	00HEX
0CHEX	R	LS_DATA_IR_2	IR ADC measurement data, MSB	00HEX
0DHEX	R	LS_DATA_GREEN_0	ALS/Green ADC measurement data, LSB	00HEX
0EHEX	R	LS_DATA_GREEN_1	ALS/Green ADC measurement data	00HEX
0FHEX	R	LS_DATA_GREEN_2	ALS/Green ADC measurement data, MSB	00HEX
10HEX	R	LS_DATA_BLUE_0	Blue ADC measurement data, LSB	00HEX
11HEX	R	LS_DATA_BLUE_1	Blue ADC measurement data	00HEX
12HEX	R	LS_DATA_BLUE_2	Blue ADC measurement data, MSB	00HEX
13HEX	R	LS_DATA_RED_0	RED ADC measurement data, LSB	00HEX
14HEX	R	LS_DATA_RED_1	RED ADC measurement data	00HEX
15HEX	R	LS_DATA_RED_2	RED ADC measurement data, MSB	00HEX
19HEX	RW	INT_CFG	Interrupt configuration	10HEX
1AHEX	RW	INT_PST	Interrupt persist setting	00HEX
1BHEX	RW	PS_THRES_UP_0	PS interrupt upper threshold, LSB	FFHEX
1CHEX	RW	PS_THRES_UP_1	PS interrupt upper threshold, MSB	07HEX
1DHEX	RW	PS_THRES_LOW_0	PS interrupt lower threshold, LSB	00HEX
1EHEX	RW	PS_THRES_LOW_1	PS interrupt lower threshold, MSB	00HEX
1FHEX	RW	PS_CAN_0	PS intelligent cancellation level setting, LSB	00HEX
20HEX	RW	PS_CAN_1, PS_CAN_ANA	PS intelligent cancellation level setting, MSB	00HEX
21HEX	RW	LS_THRES_UP_0	LS Interrupt upper threshold, LSB	FFHEX
22HEX	RW	LS_THRES_UP_1	LS Interrupt upper threshold	FFHEX
23HEX	RW	LS_THRES_UP_2	LS Interrupt upper threshold, MSB	0FHEX
24HEX	RW	LS_THRES_LOW_0	LS Interrupt lower threshold, LSB	00HEX
25HEX	RW	LS_THRES_LOW_1	LS Interrupt lower threshold	00HEX
26HEX	RW	LS_THRES_LOW_2	LS Interrupt lower threshold, MSB	00HEX
27HEX	RW	LS_THRES_VAR	LS Interrupt variance threshold	00HEX

MAIN_CTRL

Default Value: 00HEX

Address: 00HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	SAI_PS	SAI_LS	SW_RESET	0	RGB_MODE	LS_EN	PS_EN

Field	Bit	Description
SAI_PS	6	Sleep after Interrupt for PS: When this bit is set, the proximity sensor returns to standby (PS_EN is cleared when the measurement is finished and the MAIN_STATUS register is read), once an interrupt occurs. This bit reacts on PS interrupt status bit in the MAIN_STATUS register.
SAI_LS	5	Sleep after Interrupt for LS: When this bit is set, the light sensor returns to standby (LS_EN is cleared when the measurement is finished and the MAIN_STATUS register is read), once an interrupt occurs. This bit reacts on *LS interrupt status* bit in the MAIN_STATUS register.
SW_RESET	4	1: If bit is set to 1, a software reset will be triggered immediately and therefore the I^2C bus command is NOT answered with "ACK".
RGB_MODE	2	0: ALS and IR channels activated (**default**). 1: All Light Sensor (RGB and IR) channels activated.
LS_EN	1	0: Ambient light sensor standby (**default**). 1: Light Sensor active.
PS_EN	0	0: Proximity sensor standby (**default**). 1: Proximity Sensor active.

PS_LED

Default Value: 36HEX

Address: 01HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	LED PULSE MODULATION FREQUENCY			0	LED CURRENT		

Field	Bit	Description
LED PULSE MODULATION FREQUENCY	6:4	000: Reserved. 001: Reserved. 010: Reserved. 011: LED pulse frequency = 60 kHz **(default)**. 100: LED pulse frequency = 70 kHz. 101: LED pulse frequency = 80 kHz. 110: LED pulse frequency = 90 kHz. 111: LED pulse frequency = 100 kHz.
LED CURRENT	2:0	000: LED pulse current level = 2.5 mA. 001: LED pulse current level = 5.0 mA. 010: LED pulse current level = 10 mA. 011: LED pulse current level = 25 mA. 100: LED pulse current level = 50 mA. 101: LED pulse current level = 75 mA. 110: LED pulse current level = 100 mA **(default)**. 111: LED pulse current level = 125 mA.

Writing to this register resets PS state machine and starts new measurements.

PS_PULSES

Default Value: 08HEX

Address: 02HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS NUMBER OF LED PULSES							

Field	Bit	Description
PS_PULSES	7:0	00000000: 0 pulses (no light emission). … …. 00001000: 8 pulses **(default)**. … …. 00100000: 32 pulses. … …. 11111111: 255 pulses.

Writing to this register resets PS state machine and starts new measurements.

PS_MEAS_RATE

Default Value: 05HEX

Address: 03HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	PS RESOLUTION		PS MEASUREMENT RATE		

Field	Bit	Description
PS RESOLUTION	4:3	00: 8 bit **(default)**. 01: 9 bit. 10: 10 bit. 11: 11 bit.
PS MEASUREMENT RATE	2:0	000: Reserved. 001: 6.25 ms. 010: 12.5 ms. 011: 25 ms. 100: 50 ms. 101: 100 ms **(default)**. 110: 200 ms. 111: 400 ms.

Bit 2:0 register controls the timing of the periodic measurements of the PS in active mode.

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register resets PS state machine and starts new measurements.

LS_MEAS_RATE

Default Value: 22HEX

Address: 04HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	LS RESOLUTION			0	LS MEASUREMENT RATE		

Field	Bit	Description
LS RESOLUTION	6:4	000: 20 bit – 400 ms. 001: 19 bit – 200 ms. 010: 18 bit – 100 ms **(default)**. 011: 17 bit – 50 ms. 100: 16 bit – 25 ms. 101: 13 bit – 3.125 ms. 110: Reserved. 111: Reserved.
LS MEASUREMENT RATE	2:0	000: 25 ms. 001: 50 ms. 010: 100 ms **(default)**. 011: 200 ms. 100: 500 ms. 101: 1000 ms. 110: 2000 ms. 111: 2000 ms.

Bit 2:0 register controls the timing of the periodic measurements of the LS in active mode.

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register resets LS state machine and starts new measurements.

LS_Gain

Default Value: 01HEX

Address: 05HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LS GAIN RANGE		

Field	Bit	Description
LS GAIN RANGE	2:0	000: Gain 1. 001: Gain 3 (**default**). 010: Gain 6. 011: Gain 9. 100: Gain 18.

Writing to this register resets LS state machine and starts new measurements.

PART_ID

Default Value: C2HEX

Address: 06HEX

B7	B6	B5	B4	B3	B2	B1	B0
PART ID				REVISION ID			

Field	Bit	Description
PART ID	7:4	Part number ID.
REVISION ID	3:0	Revision ID of the component.

MAIN_STATUS

Default Value: 20HEX

Address: 07HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	POWER ON STATUS	LS INTERRUPT STATUS	LS DATA STATUS	PS LOGIC SIGNAL STATUS	PS INTERRUPT STATUS	PS DATA STATUS

Field	Bit	Description
POWER ON STATUS	5	1: Part went through a power-up event, either because the part was turned on or because there was power supply voltage disturbance (**default at first register read**). All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if necessary. The flag is cleared after the register is read.
LS INTERRUPT STATUS	4	0: Interrupt condition not fulfilled **(default)**. 1: Interrupt condition fulfilled (cleared after read).
LS DATA STATUS	3	0: Old data, already read **(default)**. 1: New data, not yet read (cleared after read).
PS LOGIC SIGNAL STATUS	2	0: Object is far **(default)**. 1: Object is close.
PS INTERRUPT STATUS	1	0: Interrupt condition not fulfilled **(default)**. 1: Interrupt condition fulfilled (cleared after read).
PS DATA STATUS	0	0: Old data, already read **(default)**. 1: New data, not yet read (cleared after read).

PS_DATA

Default Value: 00HEX, 00HEX

Address: 08HEX, 09HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_DATA_0							
0	0	0	0	OVERFLOW	PS_DATA_1		

If an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, both registers PS_DATA_0 and PS_DATA_1 are locked until the I^2C read operation is completed or the specified address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual PS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

The PS conversion result is always written LSB-aligned into the PS_DATA registers, regardless of the conversion resolution selected in the PS_MEAS_RATE register. PS_DATA_1 is filled with 0 for resolutions lower than 11 bit. If the PS data is outside of the measurable range, the Overflow flag (PS_DATA_1, Bit [3]) is set in any resolution mode.

PS_DATA is automatically corrected by the value of the PS cancellation register (PS_CAN).

PS_DATA = PS_MEAS – PS_CAN

PS_MEAS is the internal raw value obtained from the PS ADC. If PS_MEAS is already full-scale, then the value of PS_DATA is set to its maximum value without subtracting the PS cancellation value.

Reg 08HEX	Bit [7:0]	PS measurement least significant data byte, bit 0 is the LSB of the data word.
Reg 09HEX	Bit [3]	0: Valid PS data (**default**). 1: Overflow of PS data.
	Bit [2:0]	PS measurement most significant data byte, bit 2 is the MSB in 11-bit mode.

LS_DATA_IR

Default Value: 00HEX, 00HEX, 00HEX

Address: 0AHEX, 0BHEX, 0CHEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_DATA_IR_0							
LS_DATA_IR_1							
0	0	0	0	LS_DATA_IR_2			

IR channel output data (unsigned integer, 13 bit to 20 bit, LSB aligned).

When an I²C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual IR_DATA registers are updated as soon as there is no ongoing I²C read operation to the address range 07HEX to 18HEX.

Reg 0AHEX	Bit [7:0]	IR diode data least significant data byte.
Reg 0BHEX	Bit [7:0]	IR diode data intervening data byte.
Reg 0CHEX	Bit [3:0]	IR diode data most significant data byte.

LS_DATA_GREEN

Default Value: 00HEX, 00HEX, 00HEX

Address: 0DHEX, 0EHEX, 0FHEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_DATA_GREEN_0							
LS_DATA_GREEN_1							
0	0	0	0	LS_DATA_GREEN_2			

ALS Green channel digital output data (unsigned integer, 13 bit to 20 bit, LSB aligned).

When an I²C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I²C read operation to the address range 07HEX to 18HEX.

Reg 0DHEX	Bit [7:0]	ALS/Green diode data least significant data byte.
Reg 0EHEX	Bit [7:0]	ALS/Green diode data intervening data byte.
Reg 0FHEX	Bit [3:0]	ALS/Green diode data most significant data byte.

LS_DATA_BLUE

Default Value: 00HEX, 00HEX, 00HEX

Address: 10HEX, 11HEX, 12HEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_DATA_BLUE_0							
LS_DATA_BLUE_1							
0	0	0	0	LS_DATA_BLUE_2			

Blue channel digital output data (unsigned integer, 13 bit to 20 bit, LSB aligned).

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 10HEX	Bit [7:0]	Blue diode data least significant data byte.
Reg 11HEX	Bit [7:0]	Blue diode data intervening data byte.
Reg 12HEX	Bit [3:0]	Blue diode data most significant data byte.

LS_DATA_RED

Default Value: 00HEX, 00HEX, 00HEX

Address: 13HEX, 14HEX, 15HEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_DATA_RED_0							
LS_DATA_RED_1							
0	0	0	0	LS_DATA_RED_2			

Red channel digital output data (unsigned integer, 13 bit to 20 bit, LSB aligned).

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 13HEX	Bit [7:0]	Red diode data least significant data byte.
Reg 14HEX	Bit [7:0]	Red diode data intervening data byte.
Reg 15HEX	Bit [3:0]	Red diode data most significant data byte.

INT_CFG

Default Value: 10HEX

Address: 19HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	LS_INT_SEL		LS_VAR_MODE	LS_INT_EN	PS_LOGIC_MODE	PS_INT_EN

Field	Bit	Description
LS_INT_SEL	5:4	00: IR channel. 01: ALS channel/Green channel **(default)**. 10: Red channel. 11: Blue channel.
LS_VAR_MODE	3	0: LS threshold interrupt mode **(default)**. 1: LS variation interrupt mode.
LS_INT_EN	2	0: LS Interrupt disabled **(default)**. 1: LS Interrupt enabled.
PS_LOGIC_MODE	1	0: Normal interrupt function: after interrupt event, INT pad maintains active level until MAIN_STATUS register is read **(default)**. 1: PS Logic Output Mode: INT pad is updated after every measurement and maintains output state between measurements.
PS_INT_EN	0	0: PS Interrupt disabled **(default)**. 1: PS Interrupt enabled.

INT_PST

Default Value: 00HEX

Address: 1AHEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_PERSIST				PS_PERSIST			

Field	Bit	Description
LS_PERSIST	7:4	0000: Every LS value out of threshold range **(default)** asserts an interrupt. 0001: 2 consecutive LS values out of threshold range assert an interrupt. … 1111: 16 consecutive LS values out of threshold range assert an interrupt
PS_PERSIST	3:0	0000: Every PS value out of threshold range **(default)** asserts an interrupt. 0001: 2 consecutive PS values out of threshold range assert an interrupt. … 1111: 16 consecutive PS values out of threshold range assert an interrupt.

These register sets the number of similar consecutive LS and PS interrupt events that must occur before the interrupt is asserted.

PS_THRES_UP

Default Value: FFHEX, 07HEX

Address: 1BHEX, 1CHEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_THRES_UP_0							
0	0	0	0	0	PS_THRES_UP_1		

PS_THRES_UP sets the upper threshold value for the PS interrupt. The interrupt controller compares the value in PS_THRES_UP against measured data in the PS_DATA registers. It generates an interrupt event if PS_DATA exceeds the upper threshold level.

The data format for PS_THRES_UP must match that of the PS_DATA registers.

For resolutions below 11 bit, the threshold is evaluated LSB-aligned.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 1BHEX	Bit [7:0]	PS upper interrupt threshold value, LSB.
Reg 1CHEX	Bit [2:0]	PS upper interrupt threshold value, MSB.

PS_THRES_LOW

Default Value: 00HEX, 00HEX

Address: 1DHEX, 1EHEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_THRES_LOW_0							
0	0	0	0	0	PS_THRES_LOW_1		

PS_THRES_LOW sets the lower threshold value for the PS interrupt. The interrupt controller compares the value in PS_THRES_LOW against measured data in the PS_DATA registers. It generates an interrupt event if PS_DATA is lower than the lower threshold level.

For resolutions below 11 bit, the threshold is evaluated LSB-aligned.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 1DHEX	Bit [7:0]	PS lower interrupt threshold value, LSB.
Reg 1CHEX	Bit [2:0]	PS lower interrupt threshold value, MSB.

PS_CAN

Default Value: 00HEX, 00HEX

Address: 1FHEX, 20HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_CAN_0							
PS_CAN_ANA					PS_CAN_1		

The PS cancellation level is expected to be written by the MCU during system start up. The digital value is subtracted from the measured PS data before the data is transferred to the PS_DATA registers and evaluated by the interrupt controller.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 1FHEX	Bit [7:0]	PS digital cancellation level, LSB.
Reg 20HEX	Bit [7:3]	PS analog cancellation level, MSB.
	Bit [2:0]	PS digital cancellation level, MSB.

LS_THRES_UP

Default Value: FFHEX, FFHEX, 0FHEX

Address: 21HEX, 22HEX, 23HEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_THRES_UP_0							
LS_THRES_UP_1							
0	0	0	0	LS_THRES_UP_2			

LS_THRES_UP sets the upper threshold value for the LS interrupt. The interrupt controller compares the value in LS_THRES_UP against measured data in the LS_DATA registers of the selected ALS interrupt channel. It generates an interrupt event if LS_DATA exceeds the threshold level.

The data format for LS_THRES_UP must match that of the LS_DATA registers.

Writing to these registers resets the LS state machine and starts new measurements.

Reg 21HEX	Bit [7:0]	LS upper interrupt threshold value, LSB.
Reg 22HEX	Bit [7:0]	LS upper interrupt threshold value, intervening byte.
Reg 23HEX	Bit [3:0]	LS upper interrupt threshold value, MSB.

LS_THRES_LOW

Default Value: 00HEX, 00HEX, 00HEX

Address: 24HEX, 25HEX, 26HEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_THRES_LOW_0							
LS_THRES_LOW_1							
0	0	0	0	LS_THRES_LOW_2			

LS_THRES_LOW sets the lower threshold value for the LS interrupt. The interrupt controller compares the value in LS_THRES_LOW against measured data in the LS_DATA registers of the selected LS interrupt channel. It generates an interrupt event if the LS_DATA is below the threshold level.

The data format for LS_THRES_LOW must match that of the LS_DATA registers.

Writing to these registers resets the LS state machine and starts new measurements.

Reg 24HEX	Bit [7:0]	LS lower interrupt threshold value, LSB.
Reg 25HEX	Bit [7:0]	LS lower interrupt threshold value, intervening byte.
Reg 26HEX	Bit [3:0]	LS lower interrupt threshold value, MSB.

LS_THRES_VAR

Default Value: 00HEX

Address: 27HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LS_THRES_VAR		

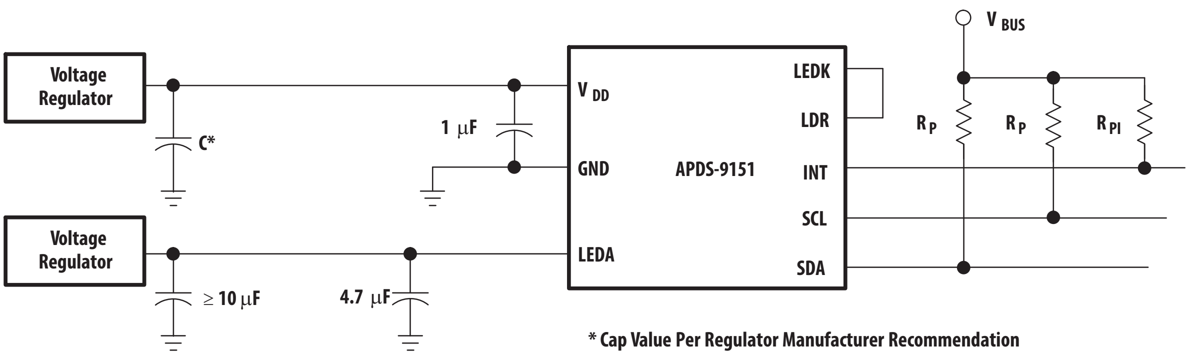
Field	Bit	Description
LS_THRES_VAR	2:0	000: LS result varies by 8 counts compared to previous result (**default**). 001: LS result varies by 16 counts compared to previous result. 010: LS result varies by 32 counts compared to previous result. 011: LS result varies by 64 counts compared to previous result. … 111: LS result varies by 1024 counts compared to previous result.

Application Information: Hardware

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current. Therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

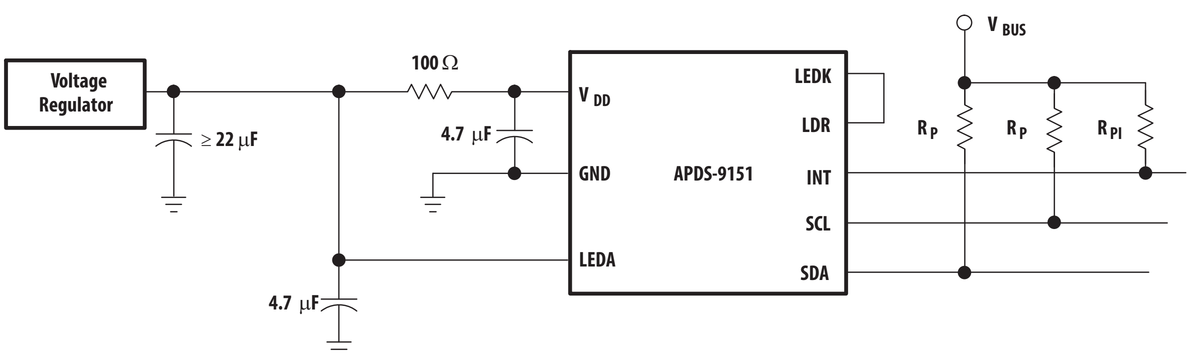
The first recommendation is to use two power supplies: one for the device VDD and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the VDD pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1-µF low-ESR decoupling capacitor as close as possible to the VDD pin and 4.7 µF at the LEDA pin, and at least 10 µF of bulk capacitance to supply the 125-mA current surge.

Proximity Sensing Using Separate Power Supplies



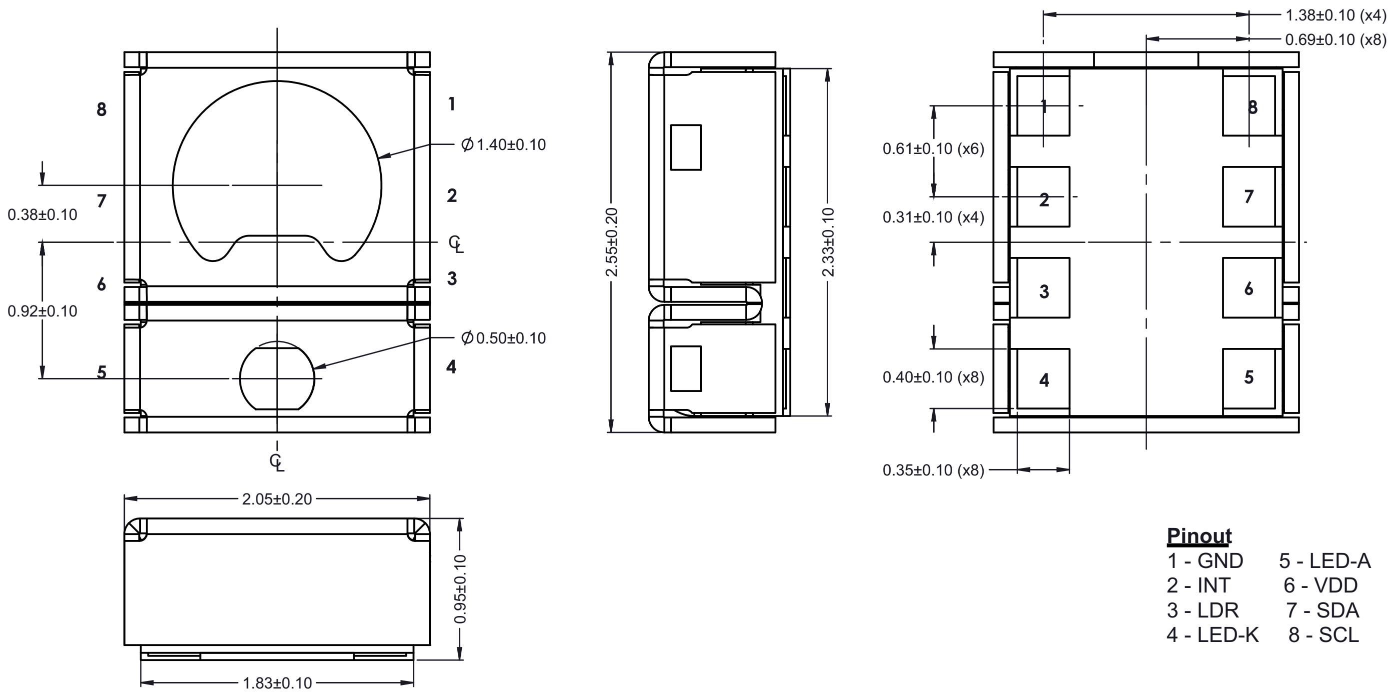
If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 100Ω resistor in series with the VDD supply line and a 4.7-µF ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

Proximity Sensing Using a Single Power Supply



VBUS in the preceding figures refers to the I²C bus voltage. The I²C signals and the interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (RP) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. A 10-kΩ pull-up resistor (RPI) can be used for the interrupt line.

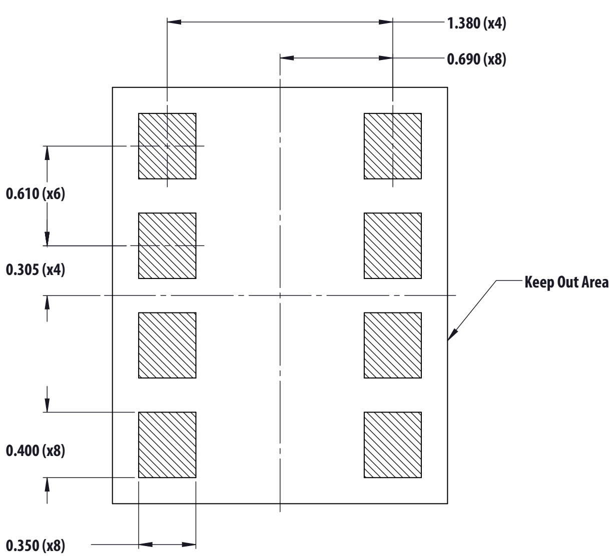
Package Outline Dimensions



NOTE All linear dimensions are in mm.

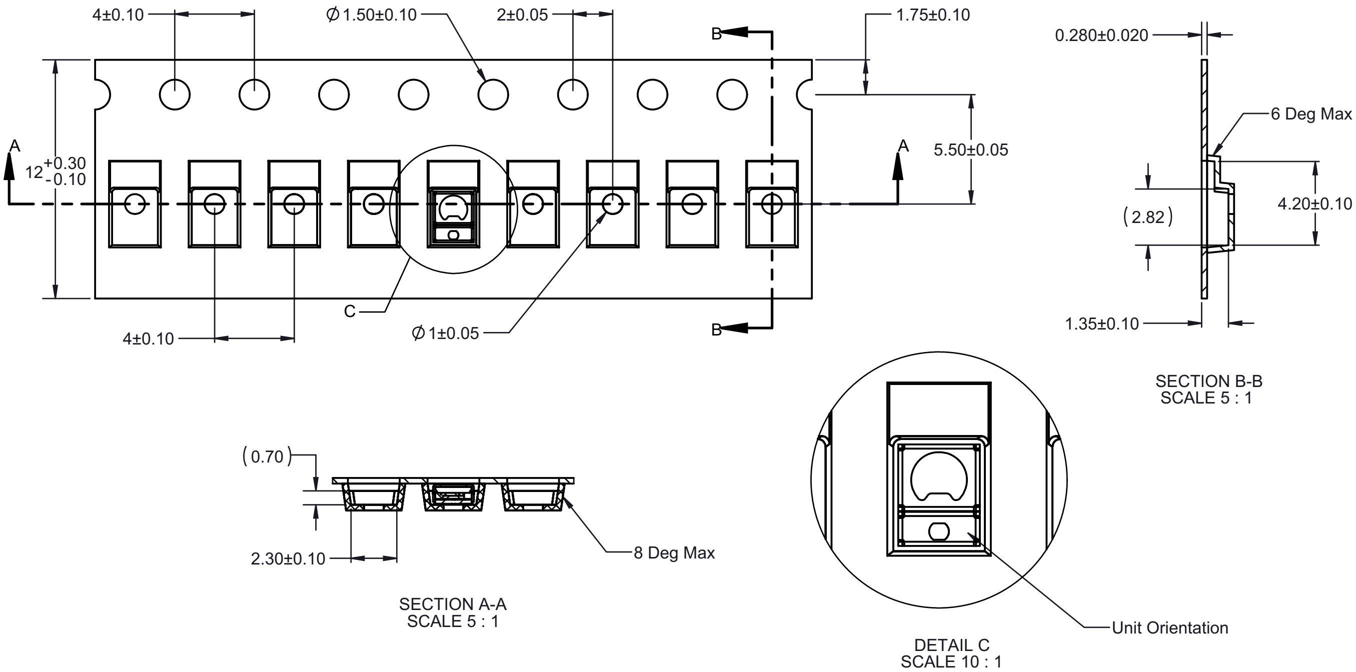
PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are as follows.



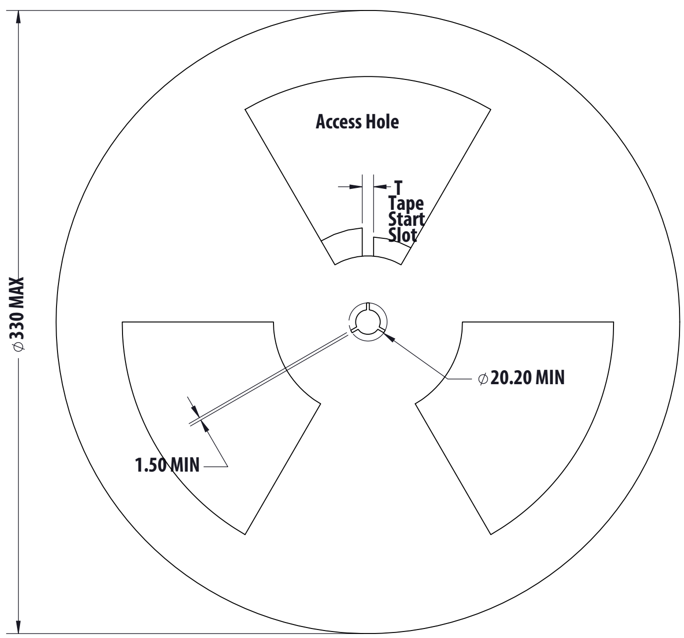
NOTE All linear dimensions are in mm.

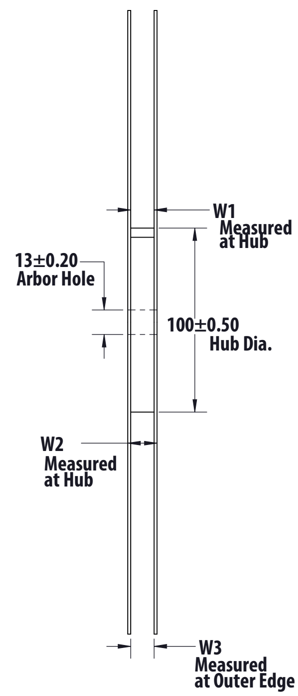
Tape Dimensions



NOTE All linear dimensions are in mm.

Reel Dimensions



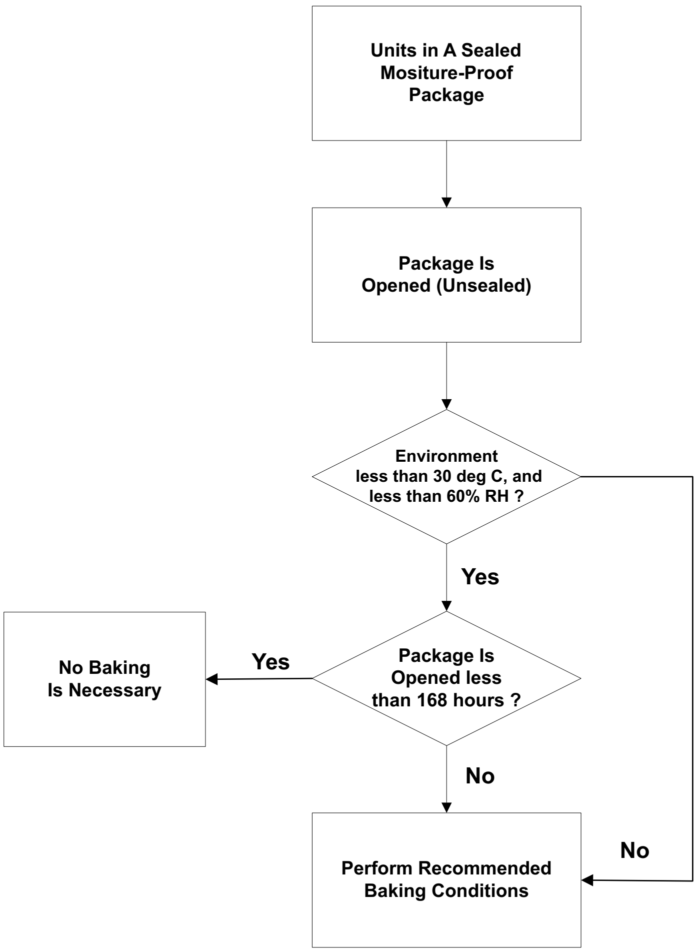


Tape Width	T	W1	W2	W3
12 mm	4 ± 0.50	12.4 + 2.0 −0.0	18.4 Max.	11.9 Min. 15.4 Max.

NOTE All linear dimensions are in mm.

Moisture Proof Packaging

All APDS-9151 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions

Package	Temperature	Time
In Reel	60°C	48 hours
In Bulk	100°C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

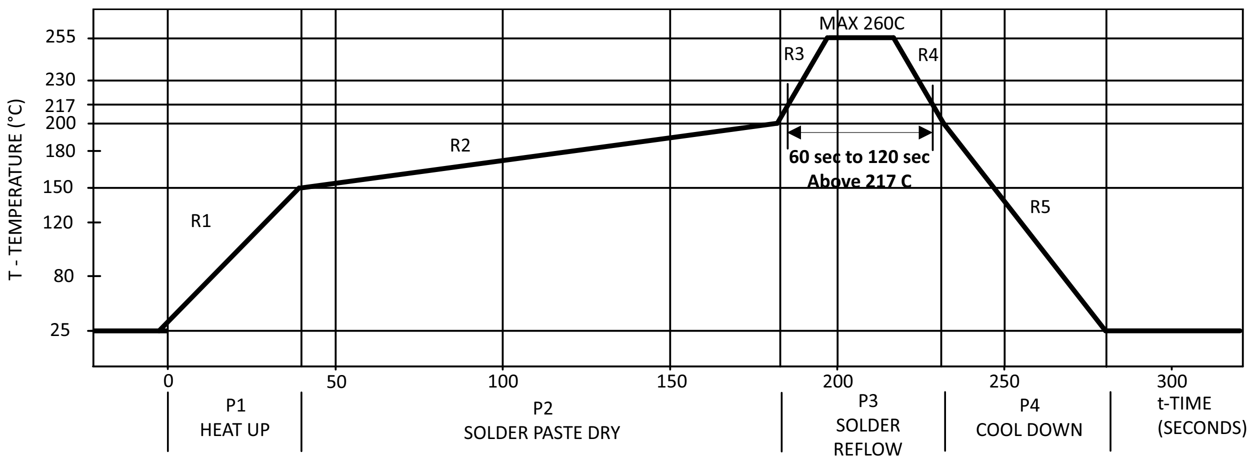
Recommended Storage Conditions

Parameter	Conditions
Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3	200°C to 260°C	3°C/s
	P3, R4	260°C to 200°C	–6°C/s
Cool Down	P4, R5	200°C to 25°C	–6°C/s
Time Maintained above Liquidus Point, 217°C		>217°C	60s to 120s
Peak Temperature		260°C	—
Time within 5°C of Actual Peak Temperature		>255°C	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8 mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the previous table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100s to 180s) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60s and 120s. This is to ensure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

APDS-9151-DS104 – August 29, 2018