



# BUK9K32-100E

Dual N-channel 100 V, 33 mΩ logic level MOSFET

10 December 2013

Product data sheet

## 1. General description

Dual logic level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)}$  rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

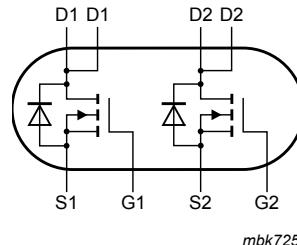
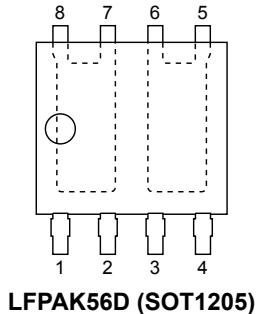
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$		-	-	100	V
$I_D$	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>		-	-	26	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>		-	-	64	W
<b>Static characteristics FET1 and FET2</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>		-	26.6	33	$\text{m}\Omega$
<b>Dynamic characteristics FET1 and FET2</b>							
$Q_{GD}$	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	11	-	nC

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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1		
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		



## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K32-100E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K32-100E	93210E

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}$ ; $T_j \leq 175^\circ\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage	$T_j \leq 175^\circ\text{C}$ ; DC	-10	10	V
		$T_j \leq 175^\circ\text{C}$ ; Pulsed	[1][2]	-15	V
$I_D$	drain current	$T_{mb} = 25^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 1</a>	-	26	A
		$T_{mb} = 100^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 1</a>	-	19	A
$I_{DM}$	peak drain current	$T_{mb} = 25^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Fig. 4</a>	-	106	A

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	-	64	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature		-	260	°C

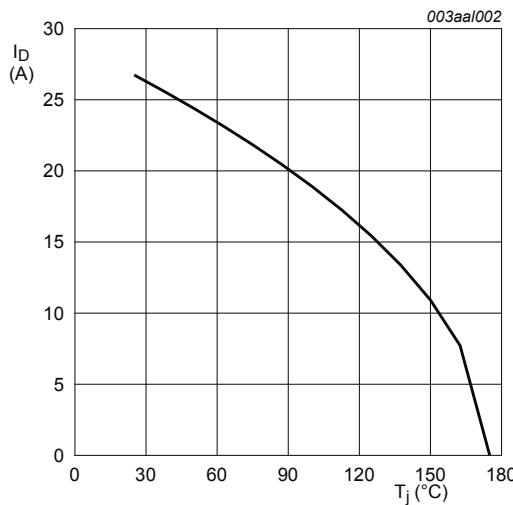
**Source-drain diode FET1 and FET2**

I <sub>S</sub>	source current		-	26	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 µs; T <sub>mb</sub> = 25 °C	-	106	A

**Avalanche Ruggedness FET1 and FET2**

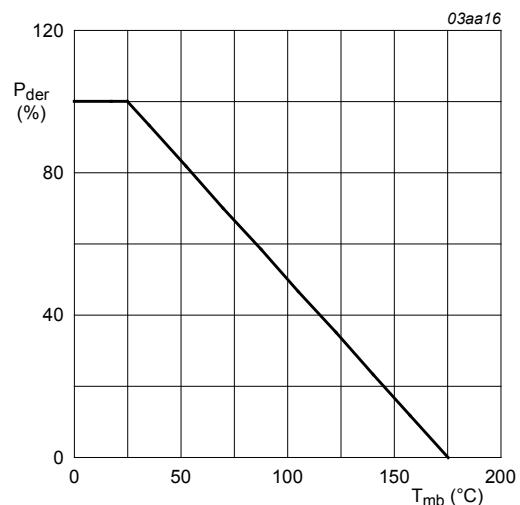
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 26 A; V <sub>sup</sub> ≤ 100 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; <a href="#">Fig. 3</a>	[3][4]	-	74	mJ
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- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>.
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 5V$$



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100 \%$$

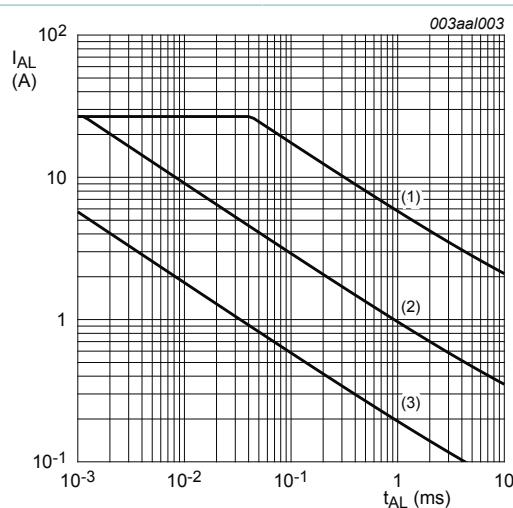


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_j (int) = 25^\circ C$ ; (2)  $T_j (int) = 150^\circ C$ ; (3) Repetitive Avalanche

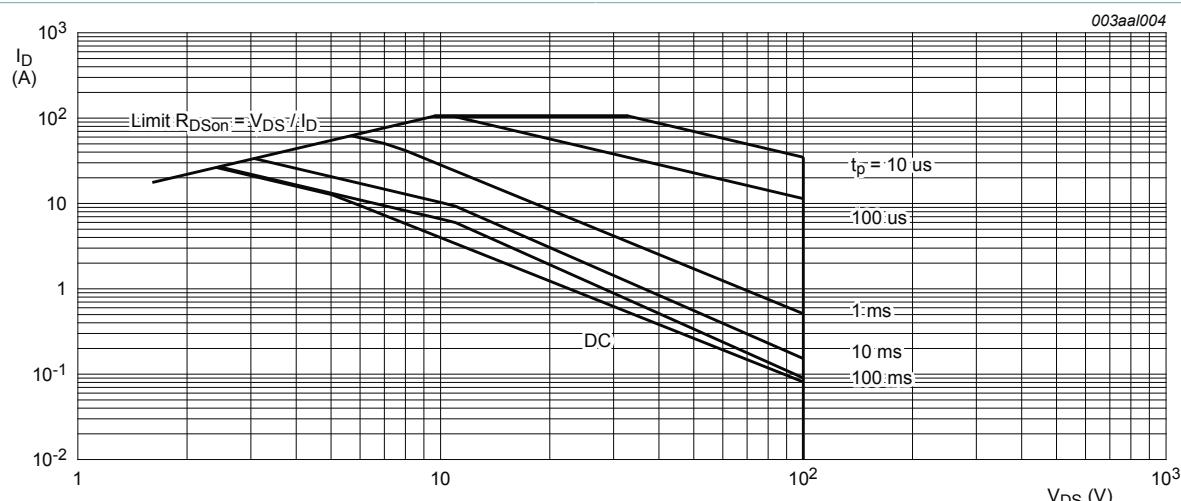


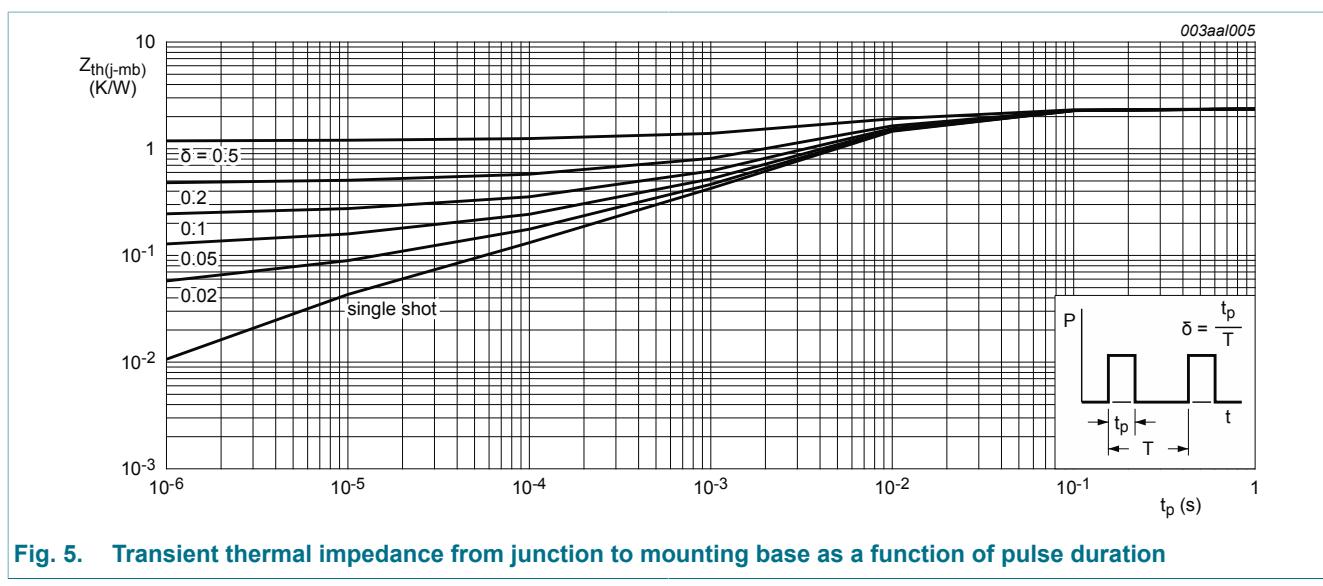
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>		-	-	2.36	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board		-	95	-	K/W

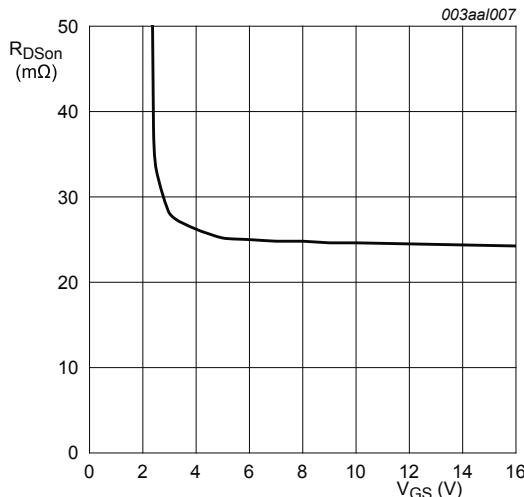


## 10. Characteristics

Table 7. Characteristics

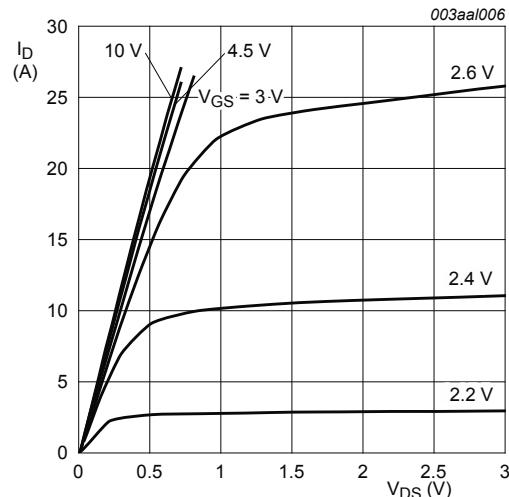
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C		90	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		100	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		1.4	1.7	2.1	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		0.5	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		-	-	2.45	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.02	1	μA
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C		-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	2	100	nA
		V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>		-	73.4	91	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	25.6	31	mΩ
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	26.6	33	mΩ
<b>Dynamic characteristics FET1 and FET2</b>							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	27.3	-	nC
Q <sub>GS</sub>	gate-source charge			-	4.7	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GD}$	gate-drain charge			-	11	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 25 \text{ V}$ ; $f = 1 \text{ MHz}$ ;		-	2377	3168	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 15</a>		-	153	184	pF
$C_{rss}$	reverse transfer capacitance			-	101	139	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80 \text{ V}$ ; $R_L = 15 \Omega$ ; $V_{GS} = 5 \text{ V}$ ;		-	12.6	-	ns
$t_r$	rise time	$R_{G(ext)} = 5 \Omega$ ; $I_D = 5 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$		-	22	-	ns
$t_{d(off)}$	turn-off delay time			-	39.5	-	ns
$t_f$	fall time			-	23.1	-	ns
<b>Source-drain diode FET1 and FET2</b>							
$V_{SD}$	source-drain voltage	$I_S = 5 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 16</a>		-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10 \text{ A}$ ; $dI_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ;		-	35.6	-	ns
$Q_r$	recovered charge	$V_{DS} = 50 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$		-	47.3	-	nC



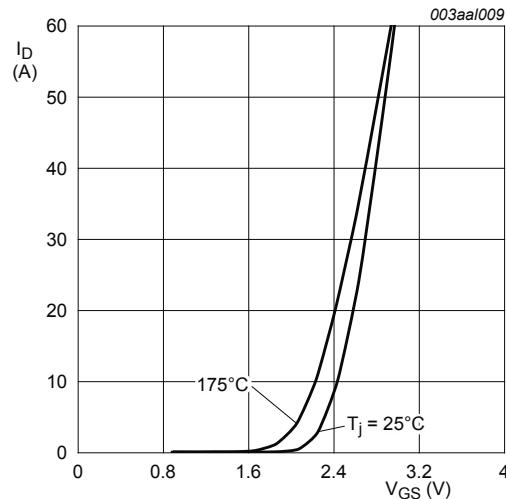
**Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25 \text{ }^\circ\text{C}$ ;  $I_D = 5 \text{ A}$



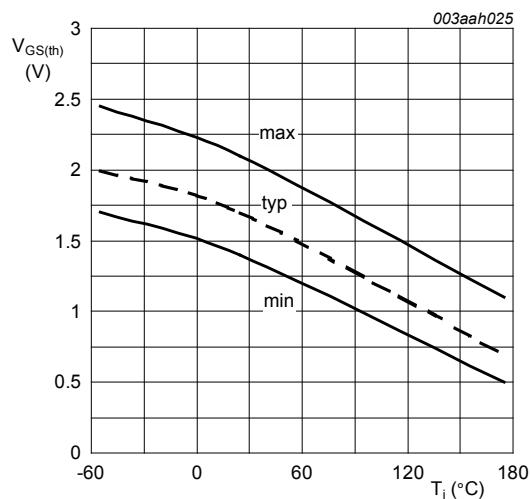
$T_j = 25 \text{ }^\circ\text{C}$ ;  $t_p = 300 \mu\text{s}$

**Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values**



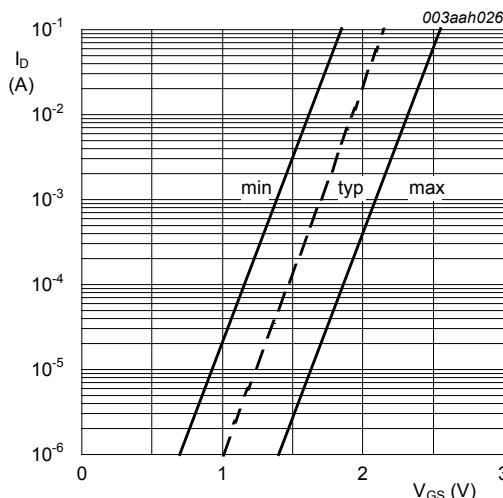
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$$V_{DS} = 10V$$



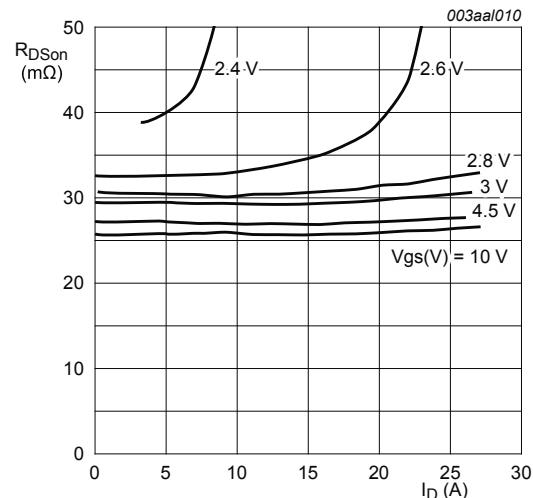
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$$T_j = 25^\circ\text{C}; V_{DS} = 5V$$



$$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$$

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

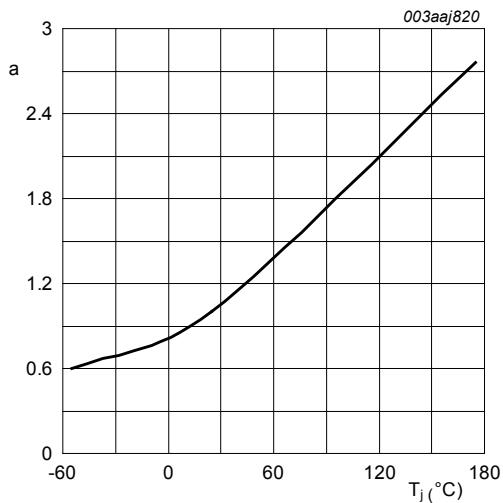


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

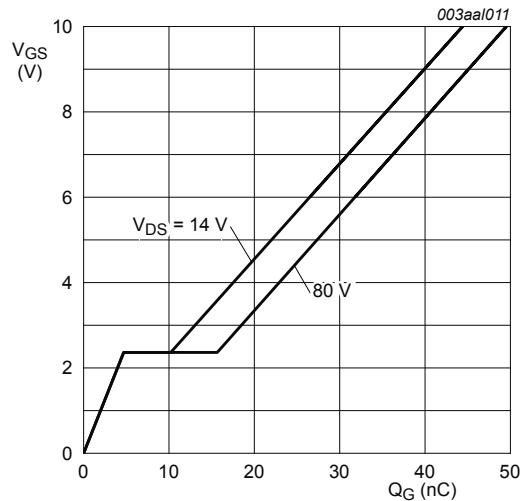


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 5\text{A}$$

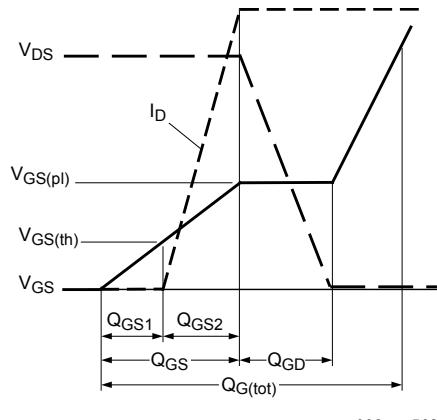


Fig. 13. Gate charge waveform definitions

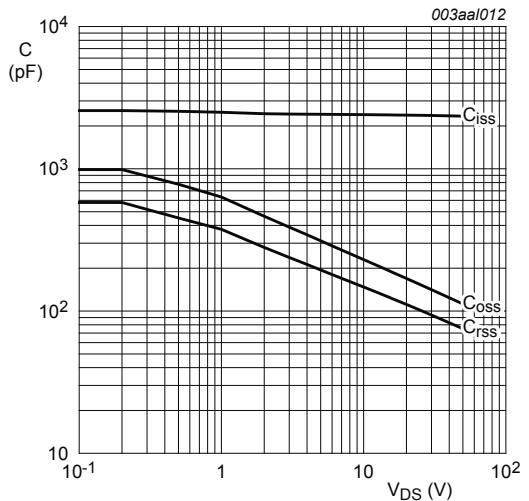


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

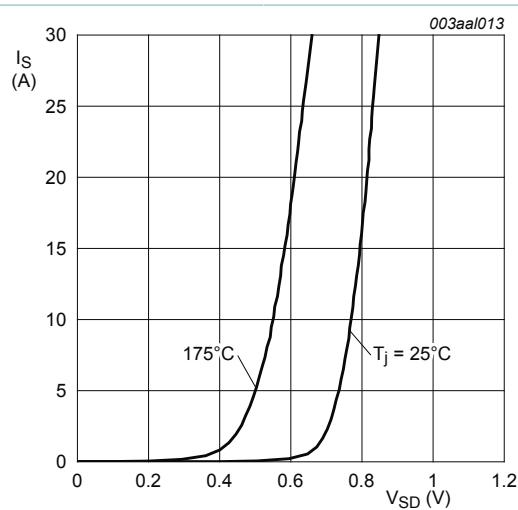
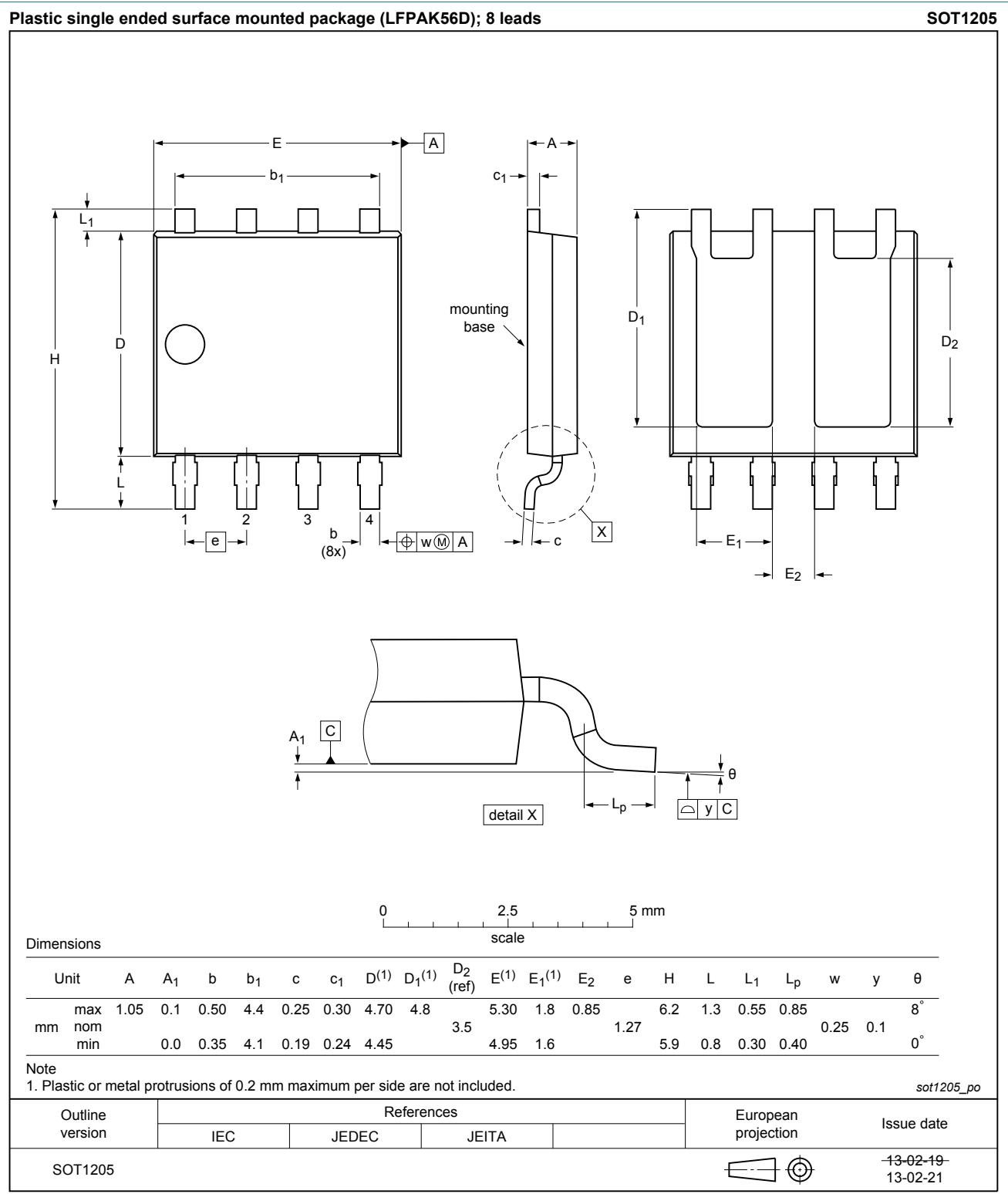


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0\text{ V}$$

## 11. Package outline



## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 10 December 2013

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# OCEAN CHIPS

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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибутором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибутором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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