

Automotive-grade N-channel 40 V, 2.9 mΩ typ., 55 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

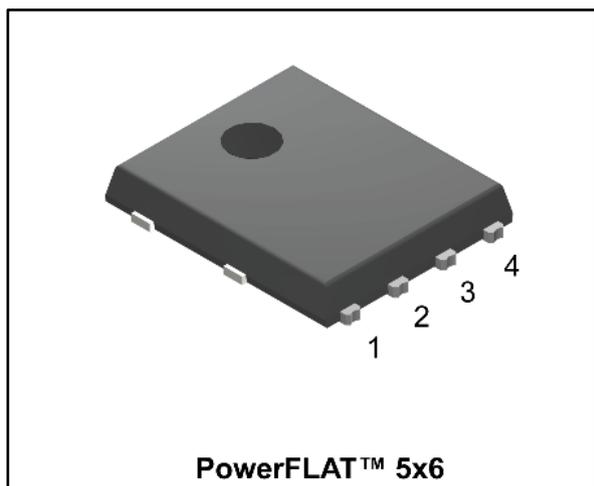
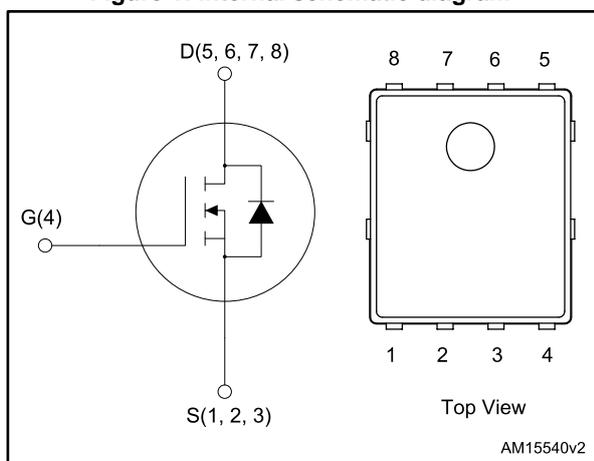


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL120N4F6AG	40 V	3.6 mΩ	55 A



- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL120N4F6AG	120N4F6	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 20	V
V_{DS}	Drain-source voltage	40	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	55	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	55	A
$I_{DM}^{(2)}$	Drain current (pulsed)	220	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	115	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		°C

Notes:

(1) Drain current is limited by package, the current capability of the silicon is 120 A at 25 °C.

(2) Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.3	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

Notes:

(1) When mounted on 1 inch² 2 Oz. Cu board, $t \leq 10\text{ s}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	20	A
E_{AS}	Single pulse avalanche energy ($T_j = 25\text{ °C}$, $I_C = I_{AV}$, $V_{DD} = 25\text{ V}$)	200	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$, $T_J = 125\text{ °C}$ ⁽¹⁾			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$		2.9	3.6	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3700	-	pF
C_{oss}	Output capacitance		-	625	-	pF
C_{rss}	Reverse transfer capacitance		-	295	-	pF
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 26\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	63	-	nC
Q_{gs}	Gate-source charge		-	19	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.5	-	Ω

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 13\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	20	-	ns
t_r	Rise time		-	70	-	ns
$t_{d(off)}$	Turn-off-delay time		-	40	-	ns
t_f	Fall time		-	20	-	ns

Table 8: Source drain diode

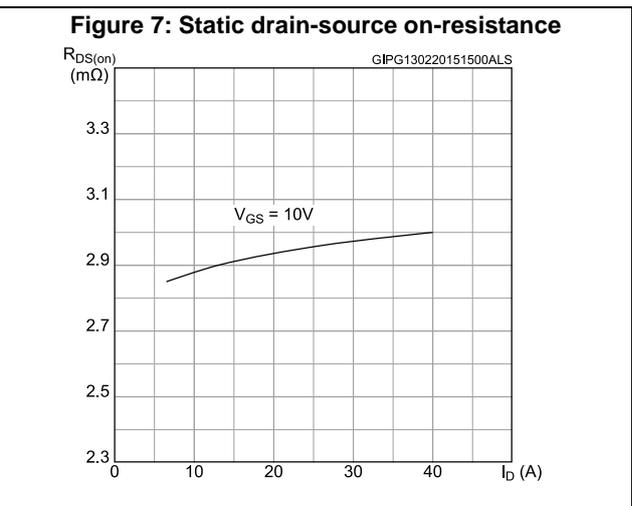
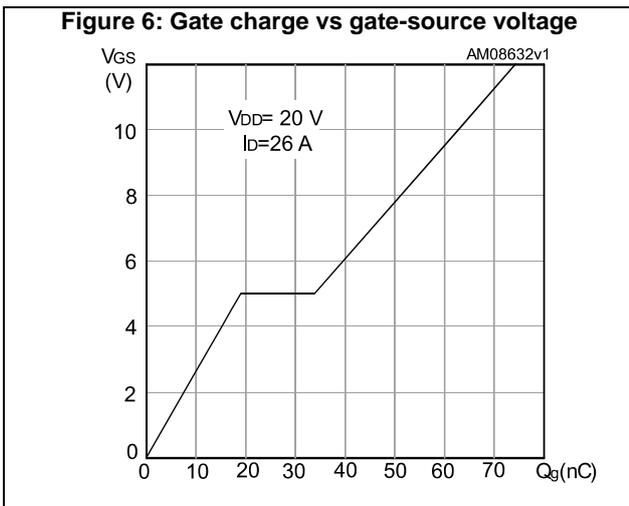
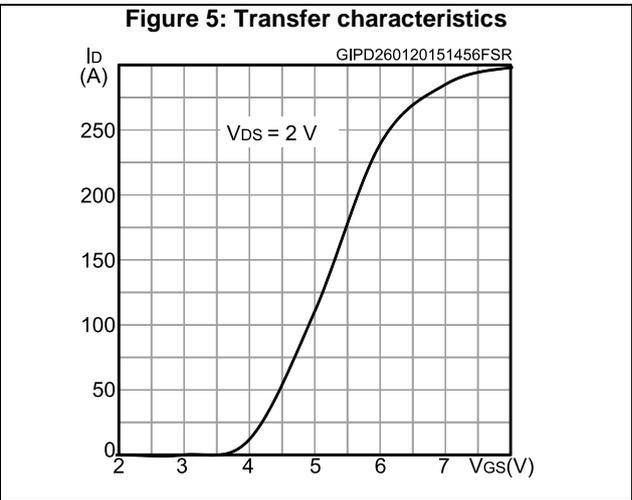
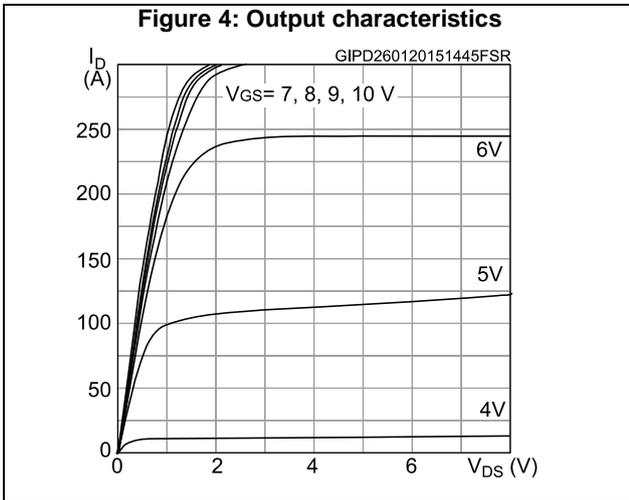
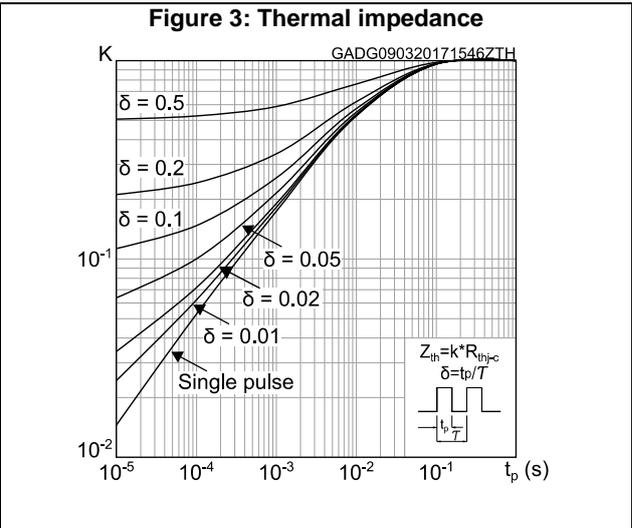
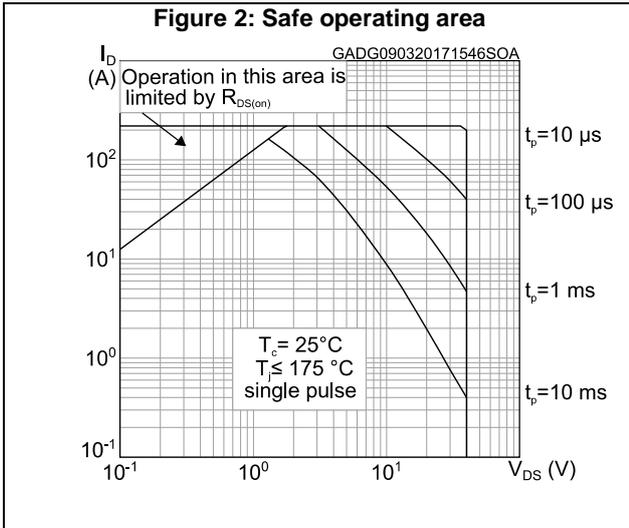
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		55	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		220	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 13\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	40		ns
Q_{rr}	Reverse recovery charge		-	5.6		nC
I_{RRM}	Reverse recovery current		-	2.8		A

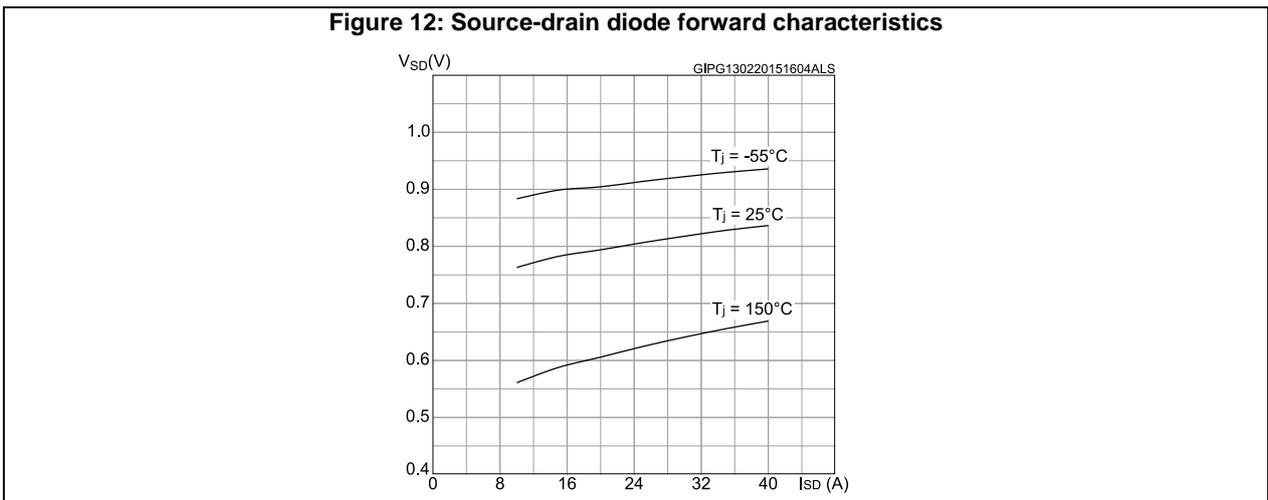
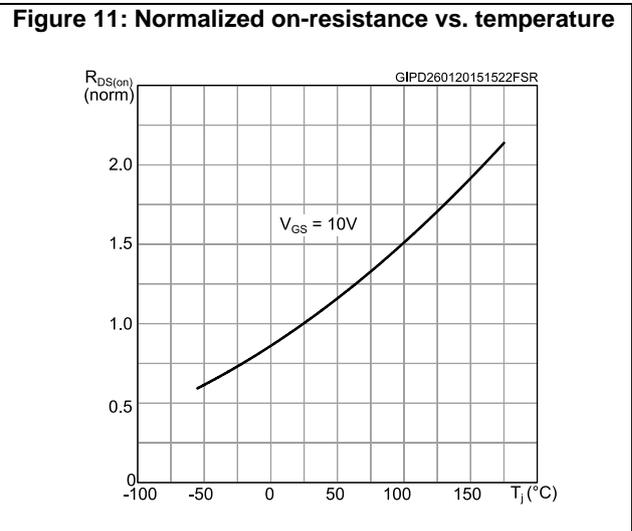
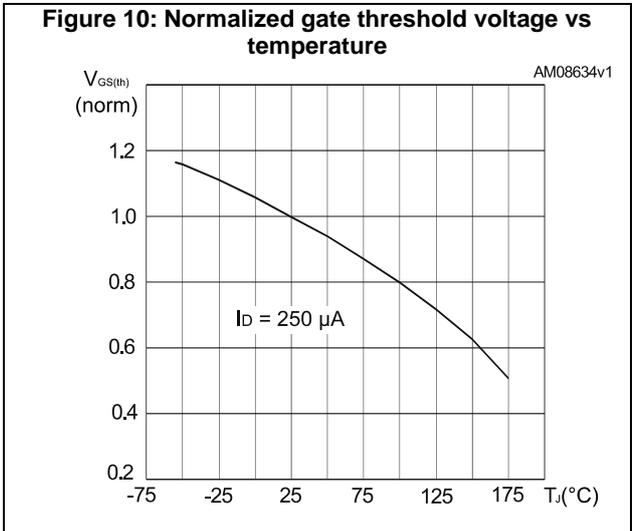
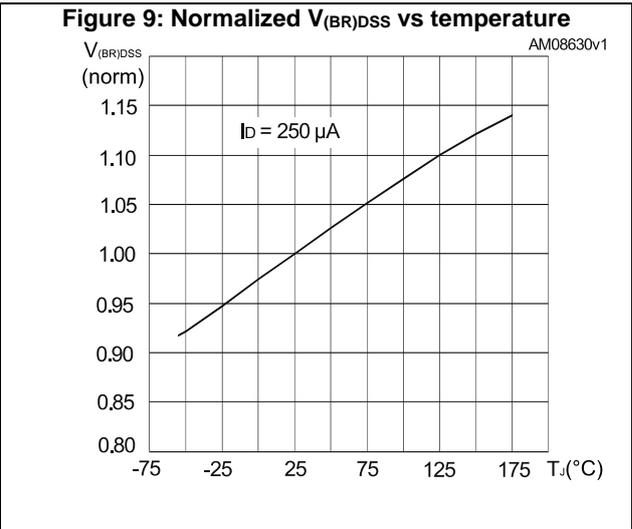
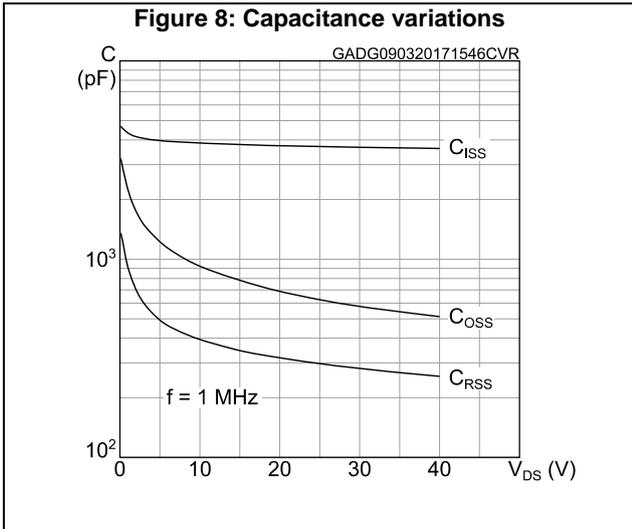
Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%

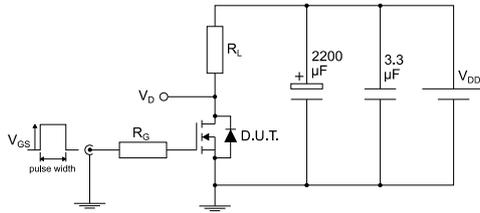
2.1 Electrical characteristics (curves)





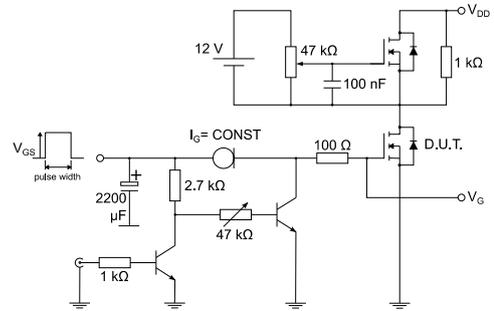
3 Test circuits

Figure 13: Test circuit for resistive load switching times



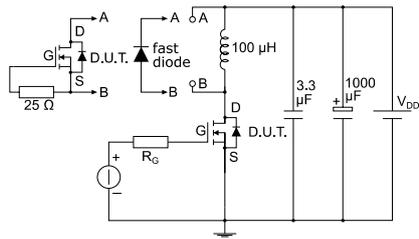
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Figure 14: Test circuit for gate charge behavior



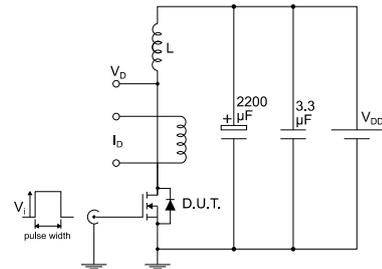
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Figure 15: Test circuit for inductive load switching and diode recovery times



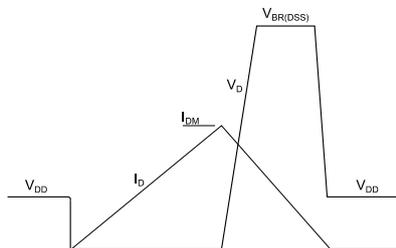
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Figure 16: Unclamped inductive load test circuit



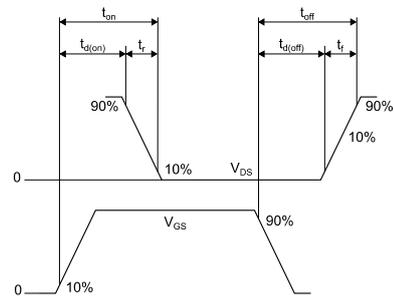
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 19: PowerFLAT™ 5x6 WF type R package outline

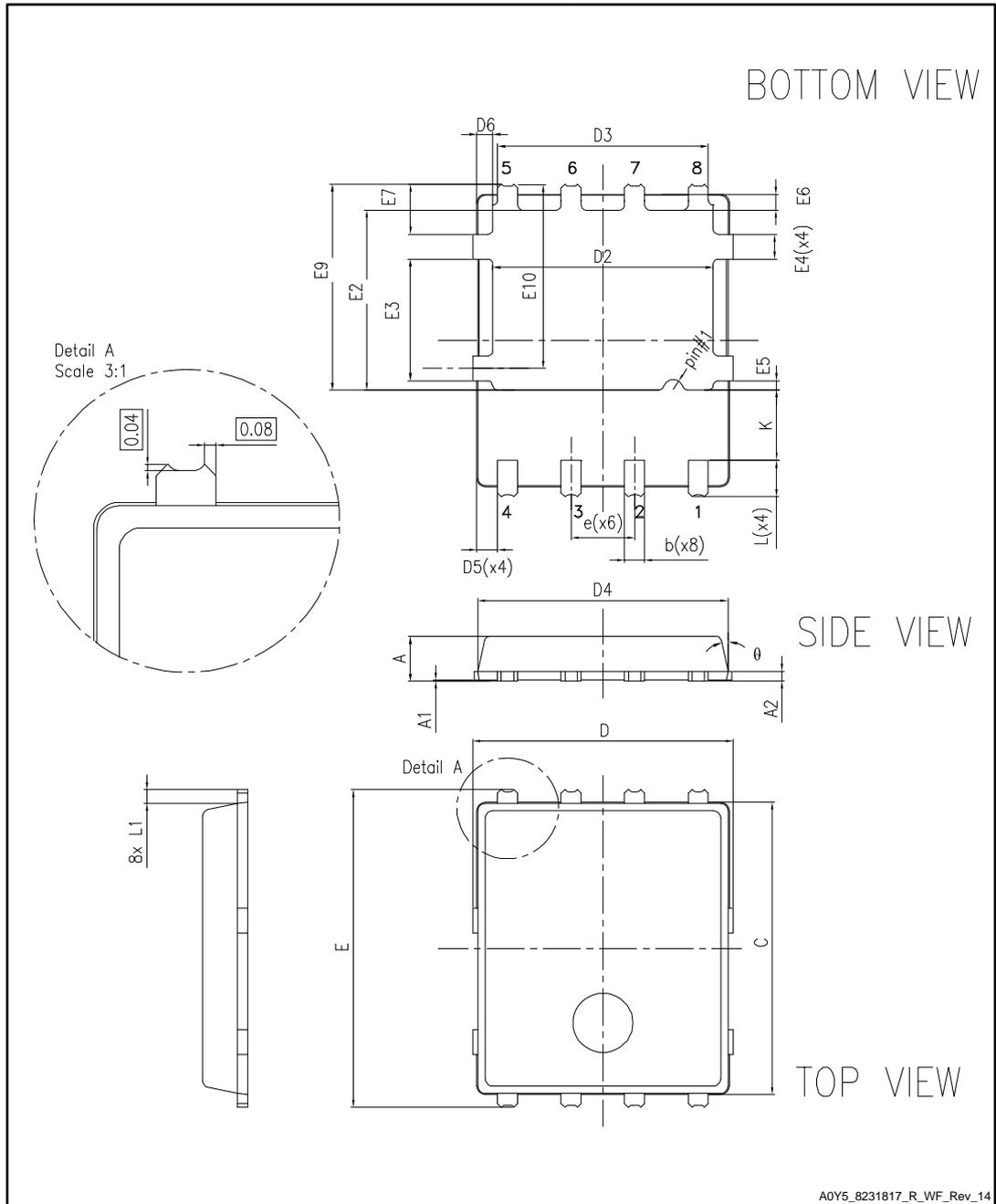
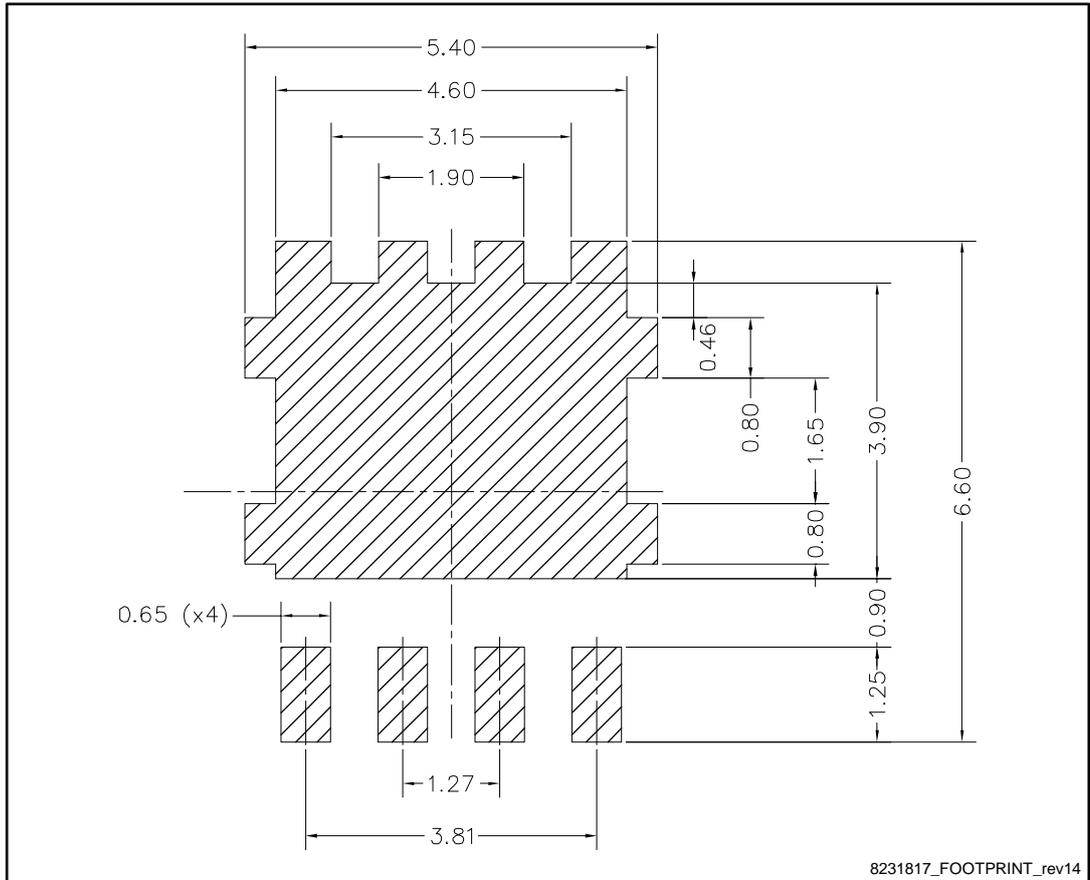


Table 9: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

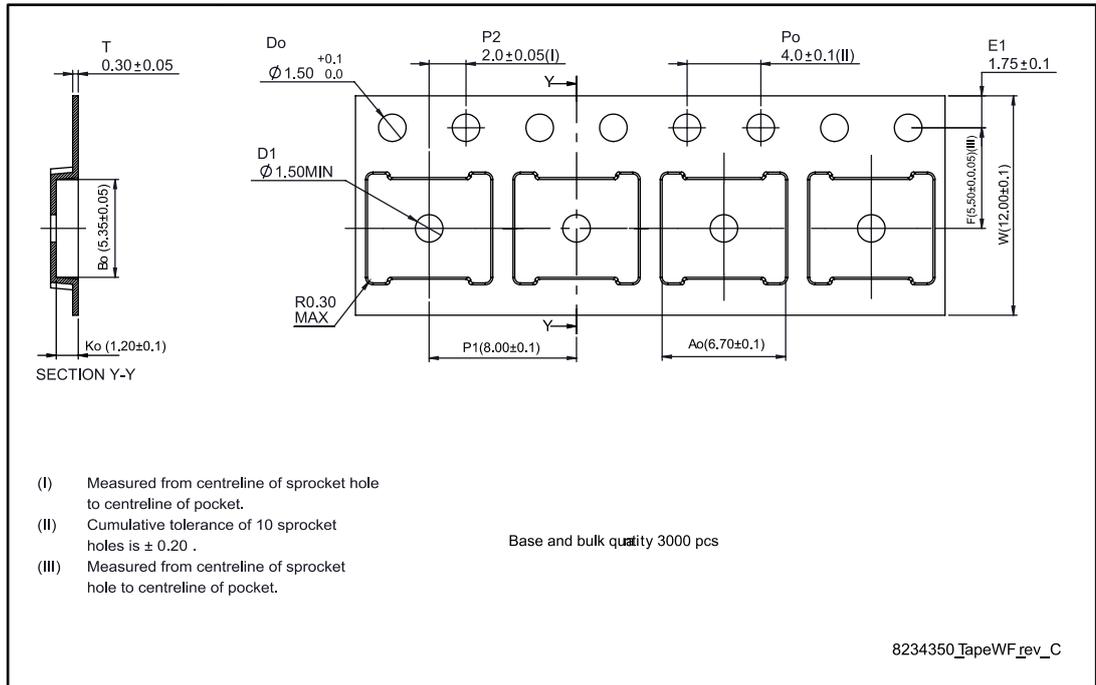


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

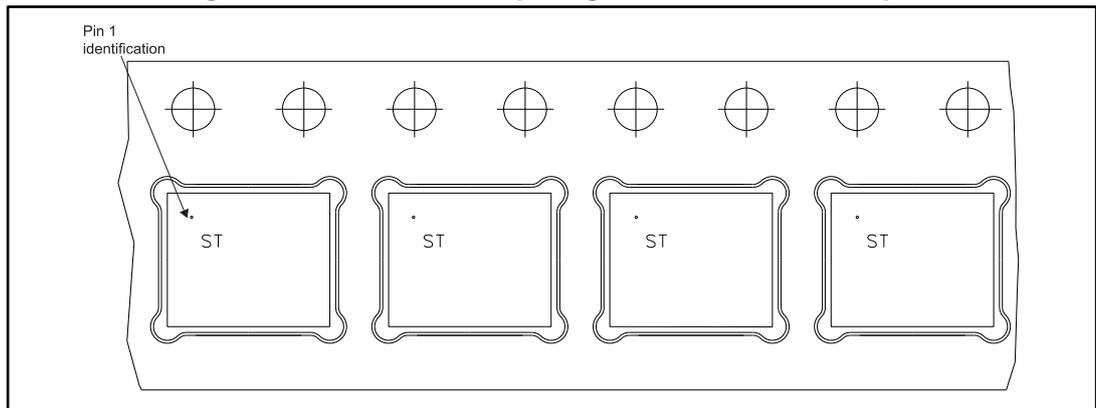
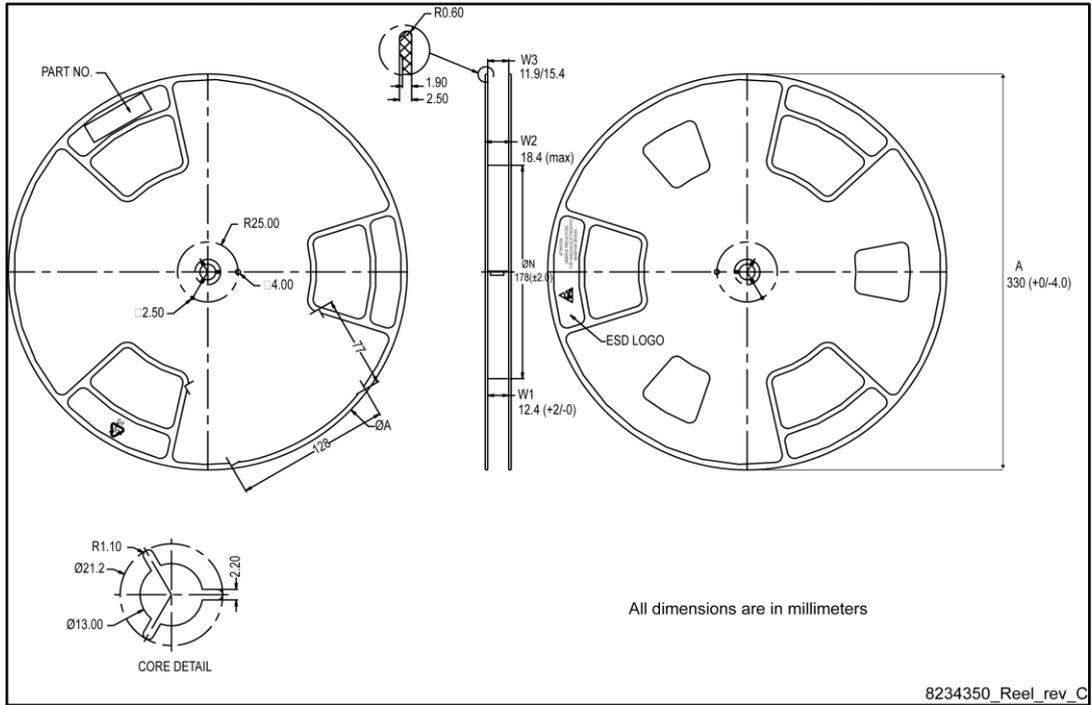


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
19-Feb-2015	1	First release.
11-Apr-2016	2	Updated <i>Table 2: "Absolute maximum ratings"</i> Minor text changes.
10-Jan-2017	3	Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 8: "Source drain diode"</i> . Updated <i>Figure 6: "Gate charge vs gate-source voltage"</i> and <i>Figure 8: "Capacitance variations"</i> . Minor text changes
09-Mar-2017	4	Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 3: "Thermal data"</i> . Updated <i>Figure 2: "Safe operating area"</i> , <i>Figure 3: "Thermal impedance"</i> and <i>Figure 8: "Capacitance variations"</i> . Added <i>Figure 9: "Normalized V(BR)DSS vs temperature"</i> and <i>Figure 10: "Normalized gate threshold voltage vs temperature"</i> . Minor text changes

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