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# FSL176MRT

## Green-Mode Fairchild Power Switch (FPS™)

### Features

- Advanced Soft Burst-Mode Operation for Low Standby Power and Low Audible Noise
- Random Frequency Fluctuation for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output-Short Protection (OSP), and Under-Voltage Lockout (UVLO) with Hysteresis
- Low Operating Current (0.4mA) in Burst Mode
- Internal Startup Circuit
- Internal High-Voltage SenseFET: 650V
- Built-in Soft-Start: 15ms
- Auto-Restart Mode

### Description

The FSL176MRT is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switched-Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSL176MRT can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost-effective design of a flyback converter.

### Applications

- Power Supply for LCD Monitor, STB, and DVD Combination

### Ordering Information

| Part Number   | Package                                | Operating Junction Temperature | Current Limit | R <sub>DS(ON)</sub> (Max.) | Output Power Table <sup>(2)</sup>      |                           |                        |                           | Replaces Device |
|---------------|--|--------------------------------|---------------|----------------------------|--|---------------------------|------------------------|---------------------------|-----------------|
|               |  |                                |               |                            | 230V <sub>AC</sub> ±15% <sup>(3)</sup> |                           | 85~265V <sub>AC</sub>  |                           |                 |
|               |  |                                |               |                            | Adapter <sup>(4)</sup>                 | Open Frame <sup>(5)</sup> | Adapter <sup>(4)</sup> | Open Frame <sup>(5)</sup> |                 |
| FSL176MRTUDTU | TO-220 6-Lead <sup>(1)</sup> U-Forming | -40°C ~ +125°C                 | 3.50A         | 1.6Ω                       | 80W                                    | 90W                       | 48W                    | 70W                       | FSGM0765R       |

#### Notes:

1. Pb-free package per JEDEC J-STD-020B.
2. The junction temperature can limit the maximum output power.
3. 230V<sub>AC</sub> or 100/115V<sub>AC</sub> with voltage doubler.
4. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
5. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.

### Application Circuit

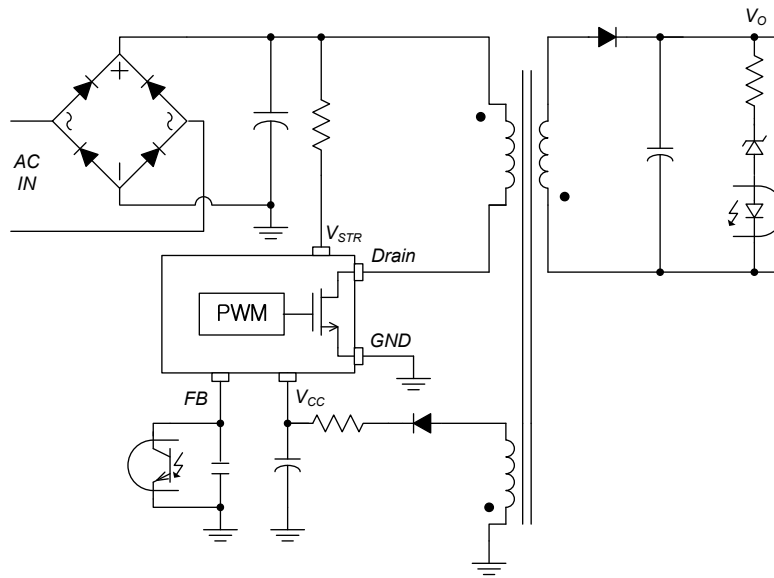


Figure 1. Typical Application Circuit

### Internal Block Diagram

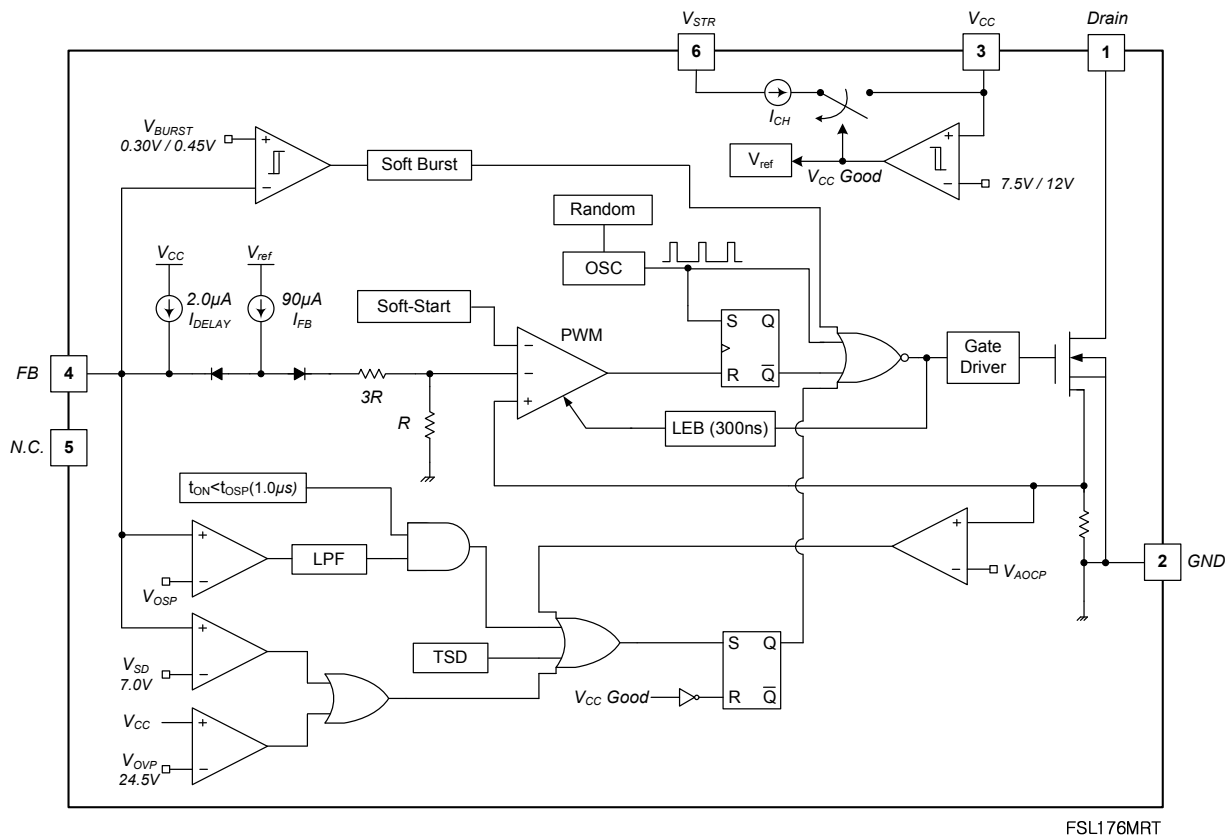


Figure 2. Internal Block Diagram

## Pin Configuration

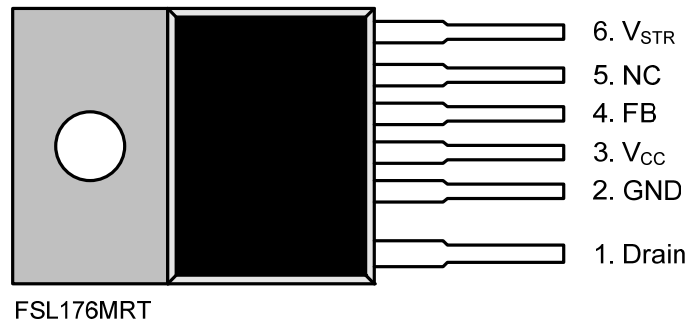


Figure 3. Pin Configuration (Top View)

## Pin Definitions

| Pin # | Name             | Description  |
|-------|------------------|--|
| 1     | Drain            | <b>SenseFET Drain.</b> High-voltage power SenseFET drain connection.   |
| 2     | GND              | <b>Ground.</b> This pin is the control ground and the SenseFET source.   |
| 3     | V <sub>CC</sub>  | <b>Power Supply.</b> This pin is the positive supply input, which provides the internal operating current for both startup and steady-state operation.   |
| 4     | FB               | <b>Feedback.</b> This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7V, the overload protection triggers, which shuts down the FPS.        |
| 5     | NC               | No Connection  |
| 6     | V <sub>STR</sub> | <b>Startup.</b> This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V <sub>CC</sub> pin. Once V <sub>CC</sub> reaches 12V, the internal current source (I <sub>CH</sub> ) is disabled. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol    | Parameter   | Min.                              | Max. | Unit             |
|-----------|---|-----------------------------------|------|------------------|
| $V_{STR}$ | $V_{STR}$ Pin Voltage   |                                   | 650  | V                |
| $V_{DS}$  | Drain Pin Voltage   |                                   | 650  | V                |
| $V_{CC}$  | $V_{CC}$ Pin Voltage  |                                   | 26   | V                |
| $V_{FB}$  | Feedback Pin Voltage  | -0.3                              | 12.0 | V                |
| $I_{DM}$  | Drain Current Pulsed  |                                   | 12.8 | A                |
| $I_{DS}$  | Continuous Switching Drain Current <sup>(6)</sup>                 | $T_C=25^\circ\text{C}$            | 6.4  | A                |
|           |   | $T_C=100^\circ\text{C}$           | 4.0  | A                |
| $E_{AS}$  | Single Pulsed Avalanche Energy <sup>(7)</sup>                     |                                   | 390  | mJ               |
| $P_D$     | Total Power Dissipation ( $T_C=25^\circ\text{C}$ ) <sup>(8)</sup> |                                   | 50   | W                |
| $T_J$     | Maximum Junction Temperature                                      |                                   | 150  | $^\circ\text{C}$ |
|           | Operating Junction Temperature <sup>(9)</sup>                     | -40                               | +125 | $^\circ\text{C}$ |
| $T_{STG}$ | Storage Temperature   | -55                               | +150 | $^\circ\text{C}$ |
| ESD       | Electrostatic Discharge Capability                                | Human Body Model, JESD22-A114     | 4.5  | kV               |
|           |   | Charged Device Model, JESD22-C101 | 2.0  |                  |

### Notes:

6. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty ( $D_{MAX}=0.74$ ) and junction temperature (see Figure 4. ).
7.  $L=45\text{mH}$ , starting  $T_J=25^\circ\text{C}$ .
8. Infinite cooling condition (refer to the SEMI G30-88).
9. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

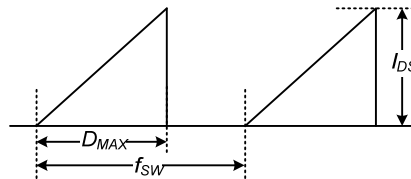


Figure 4. Repetitive Peak Switching Current

## Thermal Impedance

$T_A=25^\circ\text{C}$  unless otherwise specified.

| Symbol        | Parameter   | Value | Unit                      |
|---------------|---|-------|---------------------------|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Impedance <sup>(10)</sup> | 63.5  | $^\circ\text{C}/\text{W}$ |
| $\theta_{JC}$ | Junction-to-Case Thermal Impedance <sup>(11)</sup>    | 2.5   | $^\circ\text{C}/\text{W}$ |

### Notes:

10. Free standing without heat sink under natural convection condition, per JEDEC 51-2 and 1-10.
11. Infinite cooling condition per Mil Std. 883C method 1012.1.

## Electrical Characteristics

T<sub>J</sub> = 25°C unless otherwise specified.

| Symbol                    | Parameter                                      | Conditions   | Min. | Typ. | Max. | Unit |
|---------------------------|--|--|------|------|------|------|
| <b>SenseFET Section</b>   |  |  |      |      |      |      |
| BV <sub>DSS</sub>         | Drain-Source Breakdown Voltage                 | V <sub>CC</sub> = 0V, I <sub>D</sub> = 250μA                     | 650  |      |      | V    |
| I <sub>DSS</sub>          | Zero-Gate-Voltage Drain Current                | V <sub>DS</sub> = 520V, T <sub>A</sub> = 125°C                   |      |      | 250  | μA   |
| R <sub>DS(ON)</sub>       | Drain-Source On-State Resistance               | V <sub>GS</sub> =10V, I <sub>D</sub> =1A                         |      | 1.3  | 1.6  | Ω    |
| C <sub>ISS</sub>          | Input Capacitance <sup>(12)</sup>              | V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f=1MHz              |      | 674  |      | pF   |
| C <sub>OSS</sub>          | Output Capacitance <sup>(12)</sup>             | V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f=1MHz              |      | 93   |      | pF   |
| t <sub>r</sub>            | Rise Time                                      | V <sub>DS</sub> = 325V, I <sub>D</sub> = 4A, R <sub>G</sub> =25Ω |      | 30   |      | ns   |
| t <sub>f</sub>            | Fall Time                                      | V <sub>DS</sub> = 325V, I <sub>D</sub> = 4A, R <sub>G</sub> =25Ω |      | 26   |      | ns   |
| t <sub>d(on)</sub>        | Turn-On Delay                                  | V <sub>DS</sub> = 325V, I <sub>D</sub> = 4A, R <sub>G</sub> =25Ω |      | 16   |      | ns   |
| t <sub>d(off)</sub>       | Turn-Off Delay                                 | V <sub>DS</sub> = 325V, I <sub>D</sub> = 4A, R <sub>G</sub> =25Ω |      | 39   |      | ns   |
| <b>Control Section</b>    |  |  |      |      |      |      |
| f <sub>S</sub>            | Switching Frequency <sup>(12)</sup>            | V <sub>CC</sub> = 14V, V <sub>FB</sub> = 4V                      | 61   | 67   | 73   | kHz  |
| Δf <sub>S</sub>           | Switching Frequency Variation <sup>(12)</sup>  | -25°C < T <sub>J</sub> < 125°C                                   |      | ±5   | ±10  | %    |
| D <sub>MAX</sub>          | Maximum Duty Ratio                             | V <sub>CC</sub> = 14V, V <sub>FB</sub> = 4V                      | 61   | 67   | 73   | %    |
| D <sub>MIN</sub>          | Minimum Duty Ratio                             | V <sub>CC</sub> = 14V, V <sub>FB</sub> = 0V                      |      |      |      | %    |
| I <sub>FB</sub>           | Feedback Source Current                        | V <sub>FB</sub> =0V  | 65   | 90   | 115  | μA   |
| V <sub>START</sub>        | UVLO Threshold Voltage                         | V <sub>FB</sub> = 0V, V <sub>CC</sub> Sweep                      | 11   | 12   | 13   | V    |
| V <sub>STOP</sub>         |  | After Turn-On, V <sub>FB</sub> = 0V                              | 7.0  | 7.5  | 8.0  | V    |
| t <sub>S/S</sub>          | Internal Soft-Start Time                       | V <sub>STR</sub> = 40V, V <sub>CC</sub> Sweep                    |      | 15   |      | ms   |
| <b>Burst-Mode Section</b> |  |  |      |      |      |      |
| V <sub>BURH</sub>         | Burst-Mode Voltage                             | V <sub>CC</sub> = 14V, V <sub>FB</sub> Sweep                     | 0.39 | 0.45 | 0.51 | V    |
| V <sub>BURL</sub>         |  |  | 0.26 | 0.30 | 0.34 | V    |
| V <sub>Hys</sub>          |  |  |      | 150  |      | mV   |
| <b>Protection Section</b> |  |  |      |      |      |      |
| I <sub>LIM</sub>          | Peak Drain Current Limit                       | di/dt = 300mA/μs   | 3.15 | 3.50 | 3.85 | A    |
| V <sub>SD</sub>           | Shutdown Feedback Voltage                      | V <sub>CC</sub> = 14V, V <sub>FB</sub> Sweep                     | 6.45 | 7.00 | 7.55 | V    |
| I <sub>DELAY</sub>        | Shutdown Delay Current                         | V <sub>CC</sub> = 14V, V <sub>FB</sub> = 4V                      | 1.2  | 2.0  | 2.8  | μA   |
| t <sub>LEB</sub>          | Leading-Edge Blanking Time <sup>(12)(14)</sup> |  |      | 300  |      | ns   |
| V <sub>OVP</sub>          | Over-Voltage Protection                        | V <sub>CC</sub> Sweep  | 23.0 | 24.5 | 26.0 | V    |
| t <sub>OSP</sub>          | Output-Short Protection <sup>(12)</sup>        | Threshold Time   | 0.7  | 1.0  | 1.3  | μs   |
| V <sub>OSP</sub>          |  | Threshold V <sub>FB</sub>  | 1.8  | 2.0  | 2.2  | V    |
| t <sub>OSP_FB</sub>       |  | V <sub>FB</sub> Blanking Time                                    | 2.0  | 2.5  | 3.0  | μs   |
| TSD                       | Thermal Shutdown Temperature <sup>(12)</sup>   | Shutdown Temperature   | 130  | 140  | 150  | °C   |
| T <sub>Hys</sub>          |  | Hysteresis   |      | 60   |      | °C   |

Continued on the following page...

## Electrical Characteristics (Continued)

T<sub>J</sub> = 25°C unless otherwise specified.

| Symbol                      | Parameter  | Conditions   | Min. | Typ. | Max. | Unit |
|-----------------------------|--|--|------|------|------|------|
| <b>Total Device Section</b> |  |  |      |      |      |      |
| I <sub>OP</sub>             | Operating Supply Current,<br>(Control Part in Burst Mode)        | V <sub>CC</sub> = 14V, V <sub>FB</sub> = 0V                                  | 0.3  | 0.4  | 0.5  | mA   |
| I <sub>OPS</sub>            | Operating Switching Current,<br>(Control Part and SenseFET Part) | V <sub>CC</sub> = 14V, V <sub>FB</sub> = 2V                                  | 1.1  | 1.5  | 1.9  | mA   |
| I <sub>START</sub>          | Start Current  | V <sub>CC</sub> =11V (Before V <sub>CC</sub><br>Reaches V <sub>START</sub> ) | 85   | 120  | 155  | μA   |
| I <sub>CH</sub>             | Startup Charging Current   | V <sub>CC</sub> = V <sub>FB</sub> = 0V, V <sub>STR</sub> = 40V               | 0.7  | 1.0  | 1.3  | mA   |
| V <sub>STR</sub>            | Minimum V <sub>STR</sub> Supply Voltage                          | V <sub>CC</sub> = V <sub>FB</sub> = 0V, V <sub>STR</sub> Sweep               |      | 26   |      | V    |

### Notes:

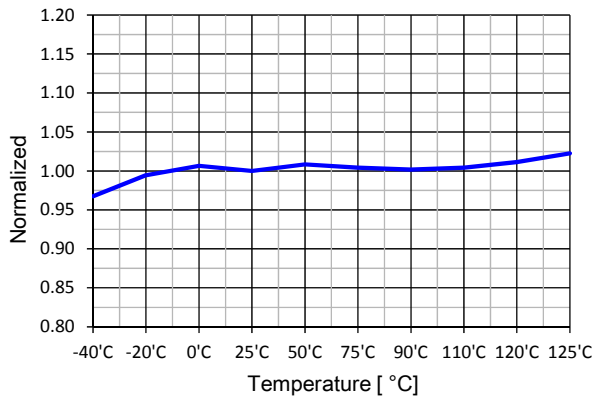
12. Although these parameters are guaranteed, they are not 100% tested in production.
13. Average value.
14. t<sub>LEB</sub> includes gate turn-on time.

## Comparison of FSGM0765R and FSL176MRT

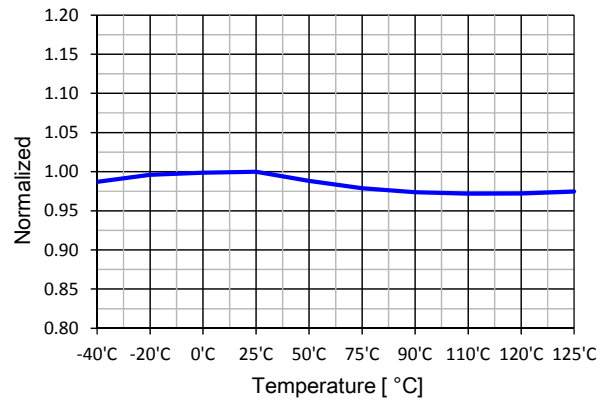
| Function                     | FSGM0765R | FSL176MRT | Advantages of FSL176MRT |
|------------------------------|-----------|-----------|-------------------------|
| Random Frequency Fluctuation |           | Built-in  | Low EMI                 |
| Operating Current            | 1.6mA     | 0.4mA     | Very low standby power  |

## Typical Performance Characteristics

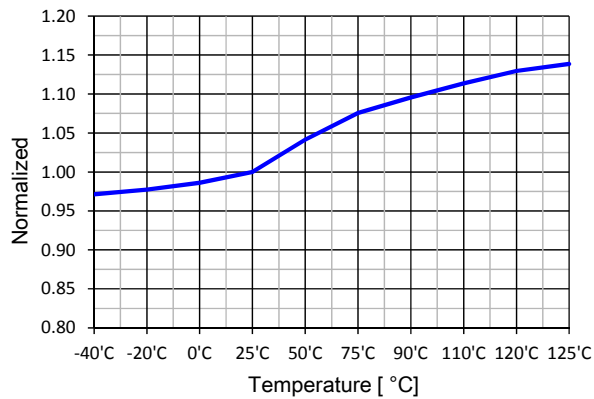
Characteristic graphs are normalized at  $T_A=25^\circ\text{C}$ .



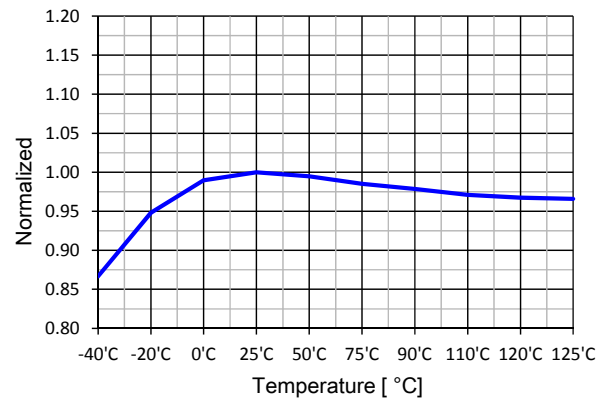
**Figure 5. Operating Supply Current ( $I_{OP}$ ) vs.  $T_A$**



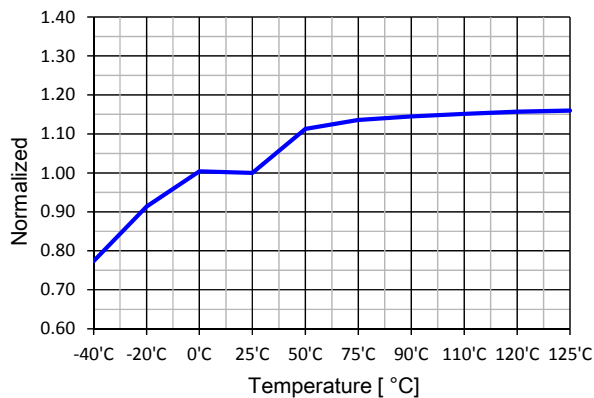
**Figure 6. Operating Switching Current ( $I_{OPS}$ ) vs.  $T_A$**



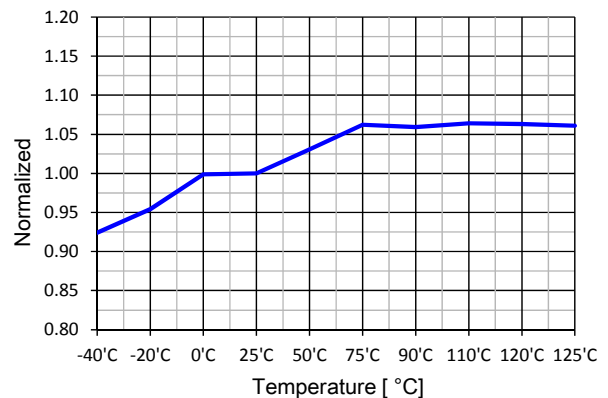
**Figure 7. Startup Charging Current ( $I_{CH}$ ) vs.  $T_A$**



**Figure 8. Peak Drain Current Limit ( $I_{LIM}$ ) vs.  $T_A$**



**Figure 9. Feedback Source Current ( $I_{FB}$ ) vs.  $T_A$**



**Figure 10. Shutdown Delay Current ( $I_{DELAY}$ ) vs.  $T_A$**



## Typical Performance Characteristics

Characteristic graphs are normalized at  $T_A=25^\circ\text{C}$ .

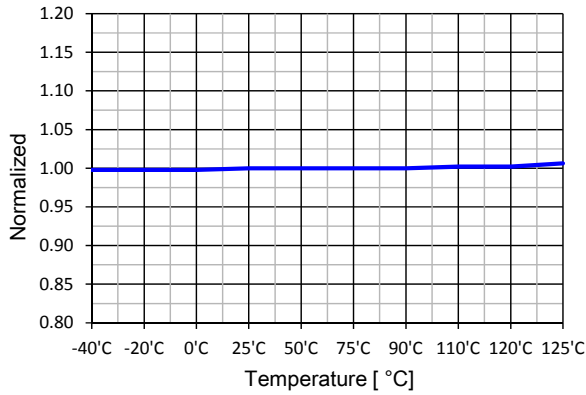


Figure 11. UVLO Threshold Voltage ( $V_{\text{START}}$ ) vs.  $T_A$

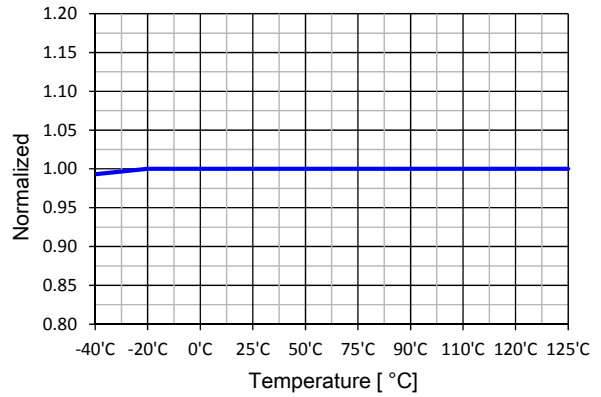


Figure 12. UVLO Threshold Voltage ( $V_{\text{STOP}}$ ) vs.  $T_A$

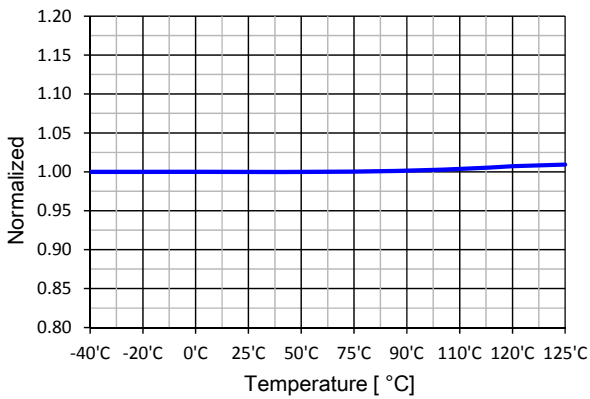


Figure 13. Shutdown Feedback Voltage ( $V_{\text{SD}}$ ) vs.  $T_A$

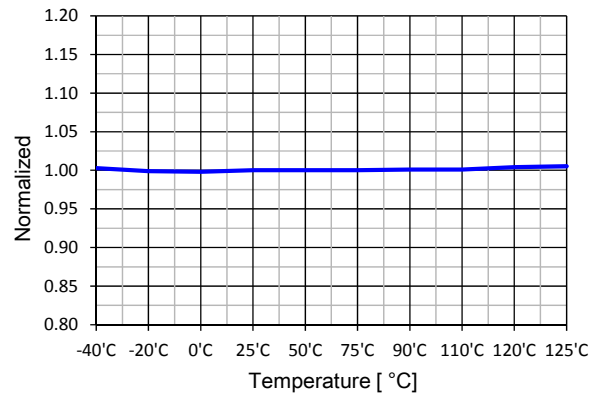


Figure 14. Over-Voltage Protection ( $V_{\text{OVP}}$ ) vs.  $T_A$

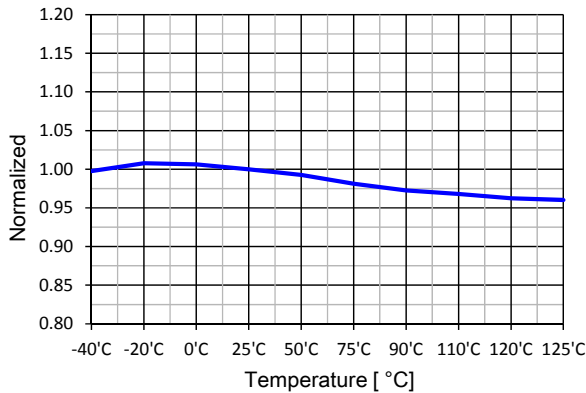


Figure 15. Switching Frequency ( $f_s$ ) vs.  $T_A$

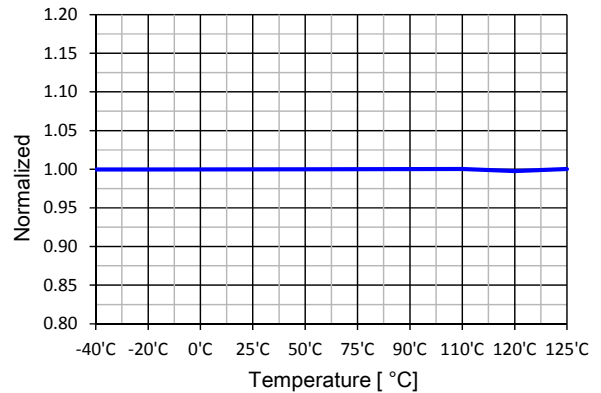
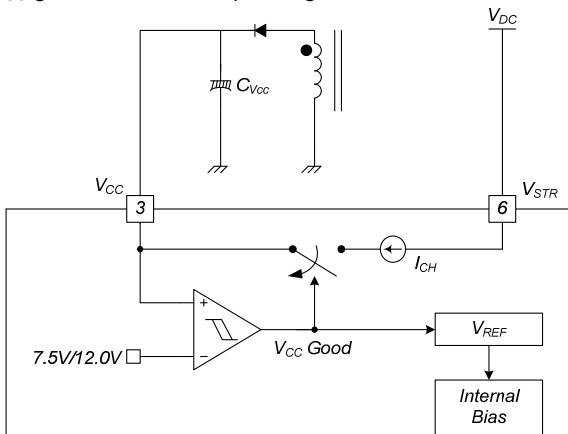


Figure 16. Maximum Duty Ratio ( $D_{\text{MAX}}$ ) vs.  $T_A$

## Functional Description

**1. Startup:** At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor ( $C_{VCC}$ ) connected to the  $V_{CC}$  pin, as illustrated in Figure 17. When  $V_{CC}$  reaches 12V, the FSL176MRT begins switching and the internal high-voltage current source is disabled. The FSL176MRT continues normal switching operation and the power is supplied from the auxiliary transformer winding unless  $V_{CC}$  goes below the stop voltage of 7.5V.



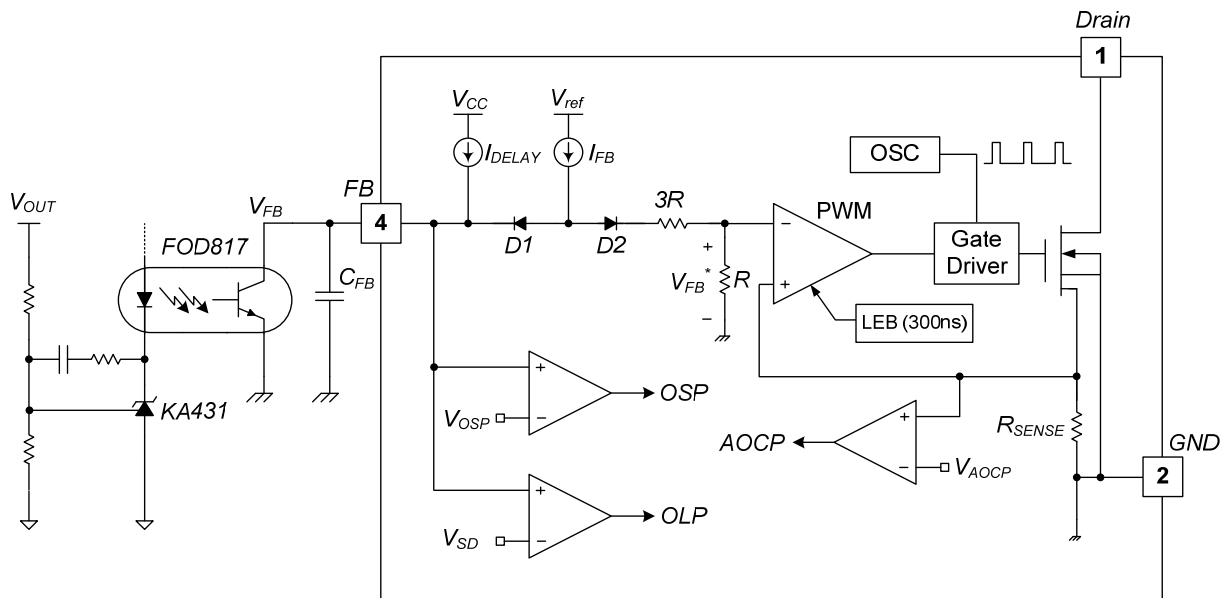
**Figure 17. Startup Block**

**2. Soft-Start:** The internal soft-start circuit increases the PWM comparator inverting input voltage, together with the SenseFET current, slowly after startup. The typical soft-start time is 15ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup.

**3. Feedback Control:** This device employs current-mode control, as shown in Figure 18. An opto-coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the  $R_{SENSE}$  resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing drain current. This typically occurs when the input voltage is increased or the output load is decreased.

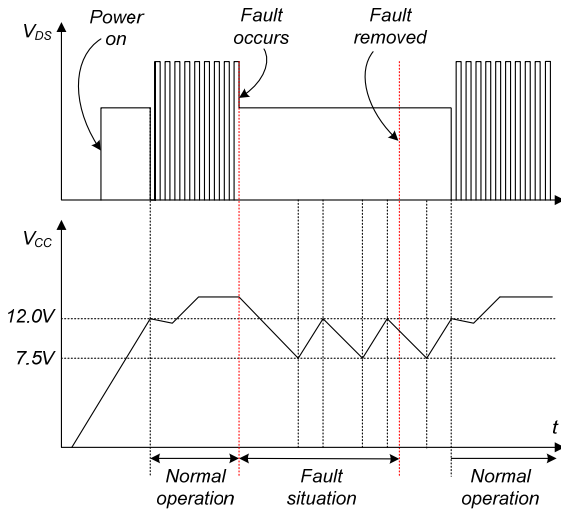
**3.1 Pulse-by-Pulse Current Limit:** Because current-mode control is employed, the peak current through the SenseFET is limited by the inverting input of the PWM comparator ( $V_{FB}^*$ ), as shown in Figure 18. Assuming that the 90 $\mu$ A current source flows only through the internal resistor ( $3R + R = 27k\Omega$ ), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage ( $V_{FB}$ ) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current through the SenseFET is limited.

**3.2 Leading-Edge Blanking (LEB):** At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the  $R_{SENSE}$  resistor leads to incorrect feedback operation in the current-mode PWM control. To counter this effect, the FSL176MRT employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for  $t_{LEB}$  (300ns) after the SenseFET is turned on.



**Figure 18. Pulse Width Modulation Circuit**

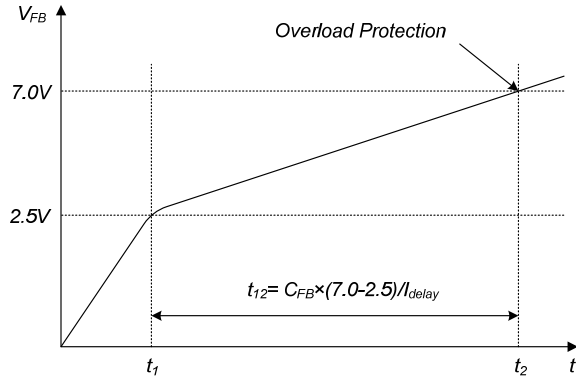
**4. Protection Circuits:** The FSL176MRT has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Output-Short Protection (OSP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once a fault condition is detected, switching is terminated and the SenseFET remains off. This causes  $V_{CC}$  to fall. When  $V_{CC}$  falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5V, the protection is reset and the startup circuit charges the  $V_{CC}$  capacitor. When  $V_{CC}$  reaches the start voltage of 12.0V, the FSL176MRT resumes normal operation. If the fault condition is not removed, the SenseFET remains off and  $V_{CC}$  drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.



**Figure 19. Auto-Restart Protection Waveforms**

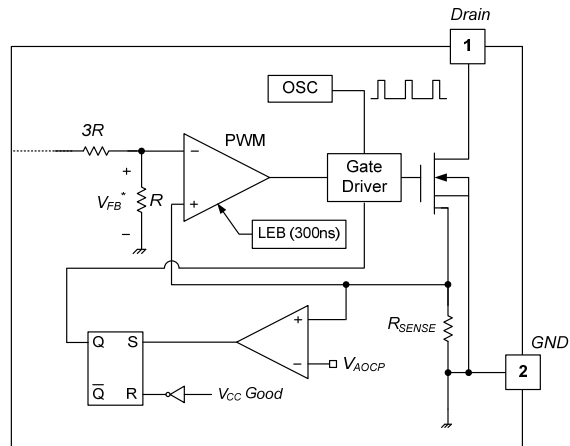
**4.1 Overload Protection (OLP):** Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, when the SMPS is in normal operation, the overload protection circuit can be triggered during load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current-limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage ( $V_{OUT}$ ) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage ( $V_{FB}$ ). If  $V_{FB}$  exceeds 2.5V, D1 is blocked and the 2.0 $\mu$ A current source starts to charge  $C_{FB}$  slowly up. In this condition,  $V_{FB}$  continues increasing until it reaches

7.0V, when the switching operation is terminated, as shown in Figure 20. The delay for shutdown is the time required to charge  $C_{FB}$  from 2.5V to 7.0V with 2.0 $\mu$ A. A 25 ~ 50ms delay is typical. This protection is implemented in auto-restart mode.



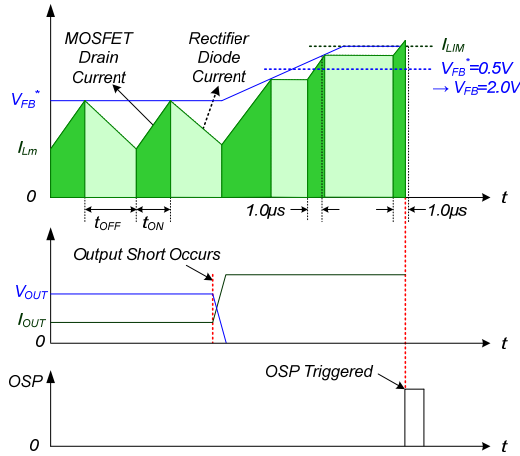
**Figure 20. Overload Protection**

**4.2 Abnormal Over-Current Protection (AOCP):** When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Overload protection is not enough to protect the FSL176MRT in that abnormal case; since severe current stress is imposed on the SenseFET until OLP is triggered. The FSL176MRT internal AOCP circuit is shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the S-R latch, resulting in the shutdown of the SMPS.



**Figure 21. Abnormal Over-Current Protection**

**4.3. Output-Short Protection (OSP):** If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Such a steep current brings high-voltage stress on the drain of the SenseFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting  $V_{FB}$  and SenseFET turn-on time. When the  $V_{FB}$  is higher than 2.0V and the SenseFET turn-on time is lower than 1.0 $\mu$ s, the FSL176MRT recognizes this condition as an abnormal error and shuts down PWM switching until  $V_{CC}$  reaches  $V_{START}$  again. An abnormal condition output short is shown in Figure 22.

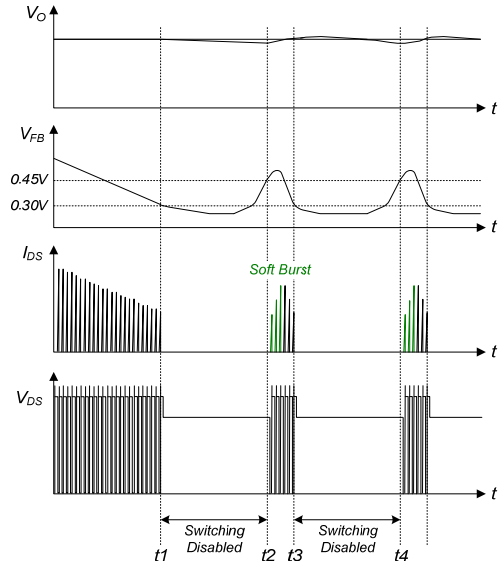


**Figure 22. Output-Short Protection**

**4.4 Over-Voltage Protection (OVP):** If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then  $V_{FB}$  climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the  $V_{CC}$  is proportional to the output voltage and the FSL176MRT uses  $V_{CC}$  instead of directly monitoring the output voltage. If  $V_{CC}$  exceeds 24.5V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation,  $V_{CC}$  should be designed to be below 24.5V.

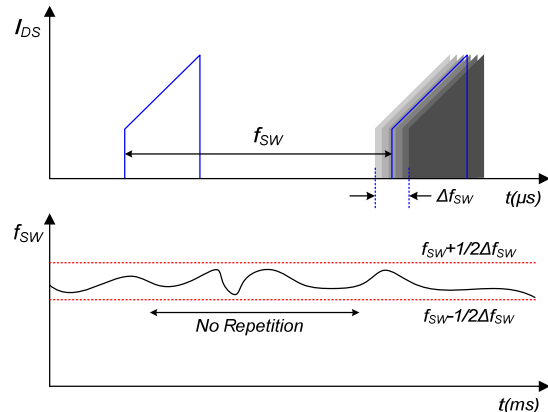
**4.5 Thermal Shutdown (TSD):** The SenseFET and the control IC on a die in one package makes it easier for the control IC to detect high temperature of the SenseFET. If the temperature exceeds ~140°C, the thermal shutdown is triggered and stops operation. The FSL176MRT operates in auto-restart mode until the temperature decreases to around 75°C, when normal operation resumes.

**5. Soft Burst-Mode Operation:** To minimize power dissipation in Standby Mode, the FSL176MRT enters Burst-Mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters Burst Mode when the feedback voltage drops below  $V_{BURL}$  (300mV), as shown in Figure 23. At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes  $V_{BURH}$  (450mV), switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET, reducing switching loss in Standby Mode.



**Figure 23. Burst-Mode Operation**

**6. Random Frequency Fluctuation (RFF):** Fluctuating switching frequency of an SMPS can reduce EMI by spreading the energy over a wide frequency range. The amount of EMI reduction is directly related to the switching frequency variation, which is limited internally. The switching frequency is determined randomly by the external feedback voltage and an internal free-running oscillator at every switching instant. This random frequency fluctuation scatters the EMI noise around typical switching frequency (67kHz) effectively and can reduce the cost of the input filter included to meet the EMI requirements (e.g. EN55022).



**Figure 24. Random Frequency Fluctuation**

## Typical Application Circuit

| Application  | Input Voltage           | Rated Output | Rated Power |
|--------------|-------------------------|--------------|-------------|
| LCD Monitor  | 85 ~ 265V <sub>AC</sub> | 5.0V (3A)    | 64W         |
| Power Supply |                         | 14.0V (3.5A) |             |

### Key Design Notes:

- The delay for overload protection (OLP) is designed to be about 30ms with C105 (8.2nF). OLP time between 39ms (12nF) and 46ms (15nF) is recommended.
- The SMD-type capacitor (C106) must be placed as close as possible to the V<sub>CC</sub> pin to avoid malfunction by abrupt pulsating noises and to improve ESD and surge immunity. Capacitance between 100nF and 220nF is recommended.

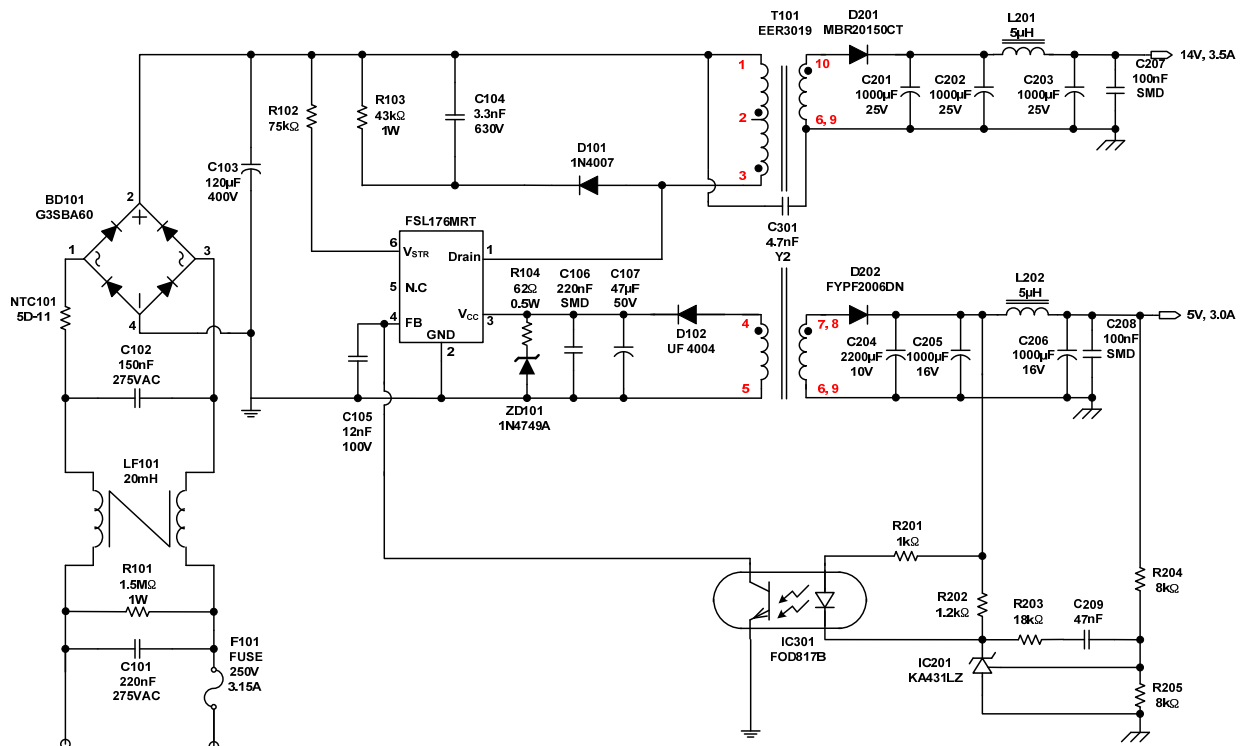


Figure 25. Schematic

### Transformer Specification

- Core: EER3019 ( $A_e=134 \text{ mm}^2$ )
- Bobbin: EER3019

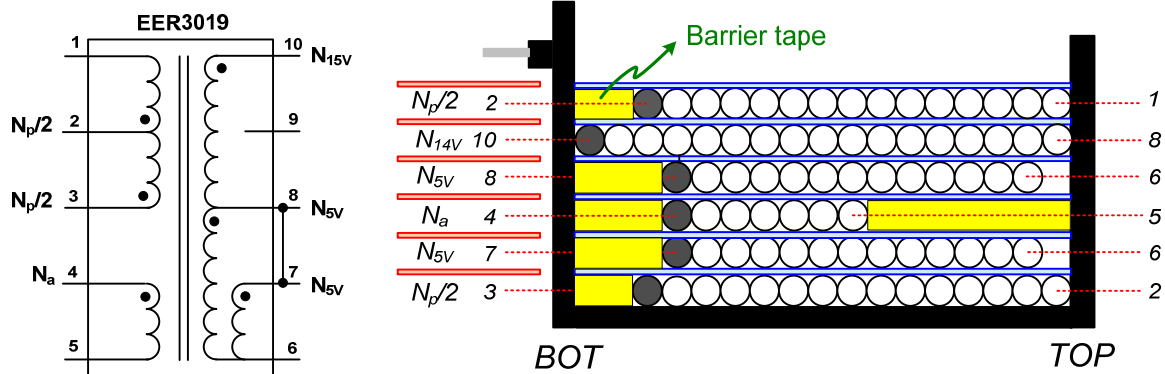


Figure 26. Transformer Specification

Table 1. Winding Specification

|  | Pin (S → F) | Wire         | Turns | Winding Method   | Barrier Tape |       |    |
|--|-------------|--------------|-------|------------------|--------------|-------|----|
|  |             |              |       |                  | TOP          | BOT   | Ts |
| $N_p/2$ (BOT)                                    | 3 → 2       | 0.4φ×1       | 18    | Solenoid Winding |              | 2.0mm | 1  |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers |             |              |       |                  |              |       |    |
| $N_{5V}$   | 7 → 6       | 0.4φ×3 (TIW) | 3     | Solenoid Winding |              | 3.0mm | 1  |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers |             |              |       |                  |              |       |    |
| $N_a$  | 4 → 5       | 0.20φ×1      | 8     | Solenoid Winding | 4.0mm        | 3.0mm | 1  |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers |             |              |       |                  |              |       |    |
| $N_{5V}$   | 8 → 6       | 0.4φ×3 (TIW) | 3     | Solenoid Winding |              | 3.0mm | 1  |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers |             |              |       |                  |              |       |    |
| $N_{14V}$  | 10 → 8      | 0.4φ×3 (TIW) | 5     | Solenoid Winding |              |       | 1  |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers |             |              |       |                  |              |       |    |
| $N_p/2$ (TOP)                                    | 2 → 1       | 0.4φ×1       | 18    | Solenoid Winding |              | 2.0mm | 1  |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers |             |              |       |                  |              |       |    |

Table 2. Electrical Characteristics

|            | Pin   | Specification | Remark               |
|------------|-------|---------------|----------------------|
| Inductance | 1 – 3 | 465μH ±6%     | 67kHz, 1V            |
| Leakage    | 1 – 3 | 10μH Maximum  | Short all other pins |

**Table 3. Bill of Materials**

| Part #          | Value      | Note                    | Part #             | Value        | Note                    |
|-----------------|------------|-------------------------|--------------------|--------------|-------------------------|
| <b>Fuse</b>     |            |                         | <b>Capacitor</b>   |              |                         |
| F101            | 250V 3.15A |                         | C101               | 220nF / 275V | Box (Pilkor)            |
| <b>NTC</b>      |            |                         | C102               | 150nF/275V   | Box (Pilkor)            |
| NTC101          | 5D-11      | DSC                     | C103               | 120µF / 400V | Electrolytic (SamYoung) |
| <b>Resistor</b> |            |                         | C104               | 3.3nF/630V   | Film (Sehwa)            |
| R101            | 1.5MΩ, J   | 1W                      | C105               | 12nF / 100V  | Film (Sehwa)            |
| R103            | 43kΩ, J    | 1W                      | C106               | 220nF        | SMD (2012)              |
| R201            | 1kΩ, F     | 1/4W, 1%                | C107               | 47µF / 50V   | Electrolytic (SamYoung) |
| R202            | 1.2kΩ, F   | 1/4W, 1%                | C201               | 1000µF / 25V | Electrolytic (SamYoung) |
| R203            | 18kΩ, F    | 1/4W, 1%                | C202               | 1000µF / 25V | Electrolytic (SamYoung) |
| R204            | 8kΩ, F     | 1/4W, 1%                | C203               | 1000µF / 25V | Electrolytic (SamYoung) |
| R205            | 8kΩ, F     | 1/4W, 1%                | C204               | 2200µF / 10V | Electrolytic (SamYoung) |
|                 |            |                         | C205               | 1000µF / 16V | Electrolytic (SamYoung) |
|                 |            |                         | C206               | 1000µF / 16V | Electrolytic (SamYoung) |
| <b>IC</b>       |            |                         | C207               | 100nF        | SMD (2012)              |
|                 |            |                         | C208               | 100nF        | SMD (2012)              |
| SMPS            | FSL176MRT  | Fairchild Semiconductor | C301               | 4.7nF / Y2   | Y-cap (Samhwa)          |
| IC201           | KA431LZ    | Fairchild Semiconductor | <b>Inductor</b>    |              |                         |
| IC301           | FOD817B    | Fairchild Semiconductor | LF101              | 20mH         | Line Filter 0.5Ø        |
| <b>Diode</b>    |            |                         | L201               | 5µH          | 5A Rating               |
| D101            | 1N4007     | Vishay                  | L202               | 5µH          | 5A Rating               |
| D102            | UF4004     | Vishay                  | <b>Transformer</b> |              |                         |
| ZD101           | 1N4750     | Vishay                  | T101               | 465µH        |                         |
| D201            | MBR20150CT | Fairchild Semiconductor |                    |              |                         |
| D202            | FYPF2006DN | Fairchild Semiconductor |                    |              |                         |
| BD101           | G3SBA60    | Vishay                  |                    |              |                         |







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