GENERAL DESCRIPTION

The XRT71D03 is a three channel, single chip Jitter Attenuator, that meets the Jitter transfer characteristics requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards.

In addition, the XRT71D03 also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards.

FEATURES

- Meets the E3/DS3/STS-1 jitter requirements
- No external components required
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755, GR-235-CORE, GR-499-CORE,1995 standards
- Meets output jitter requirement as specified by ETSI TBR24
- Meets the Jitter and Wander specifications described in T1.105.03b,GR-253 and GR-499 standards.
- Selectable buffer size of 16 and 32 bits
- Jitter attenuator can be disabled
- Available in a 64 pin LQFP package.
- Single 3.3V or 5.0V supply.
- Operates over - 40° C to 85° C temperature range.

APPLICATIONS

- E3/DS3 Access Equipment.
- DSLAMs

FIGURE 1. BLOCK DIAGRAM OF THE XRT71D03

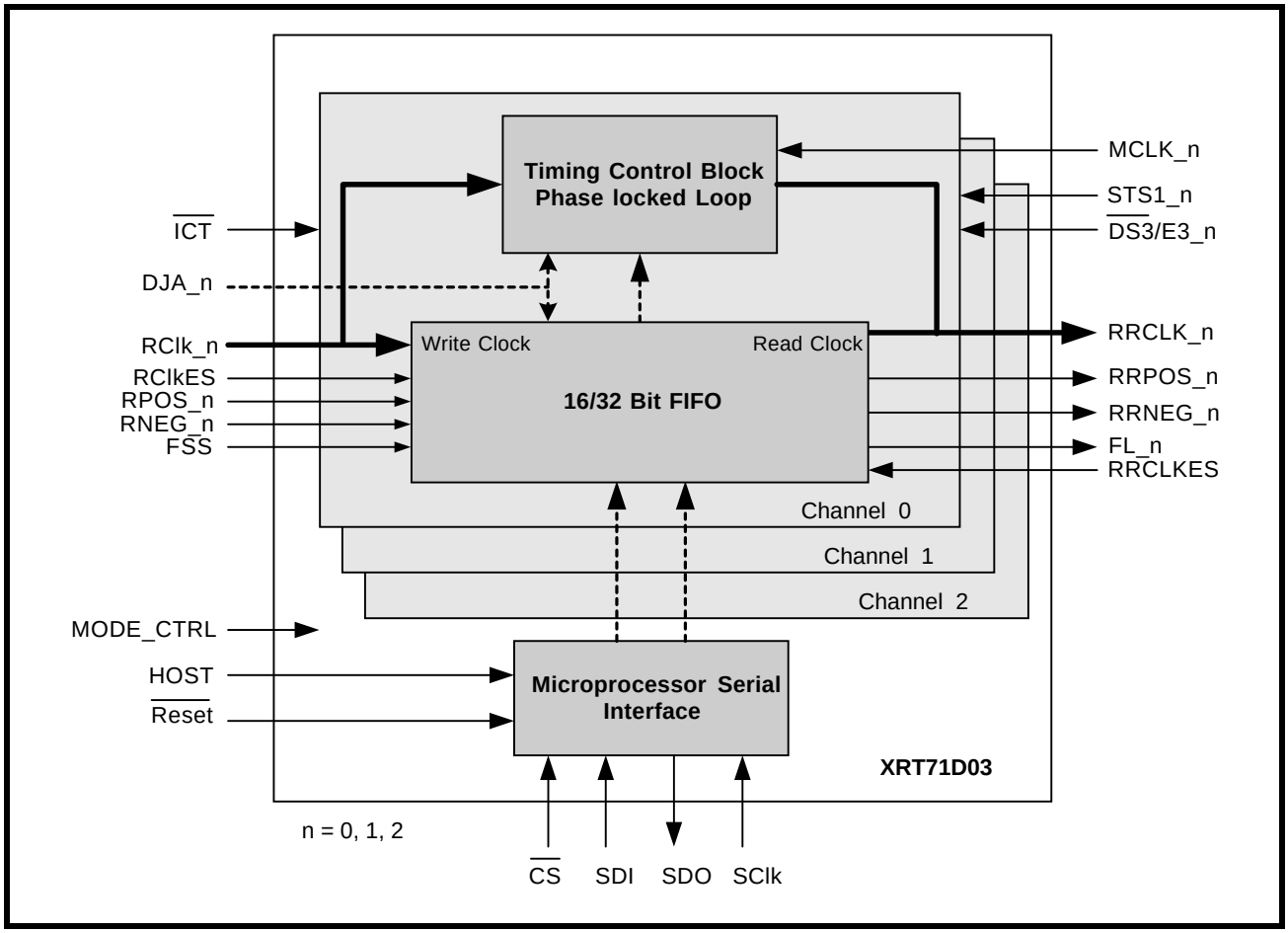
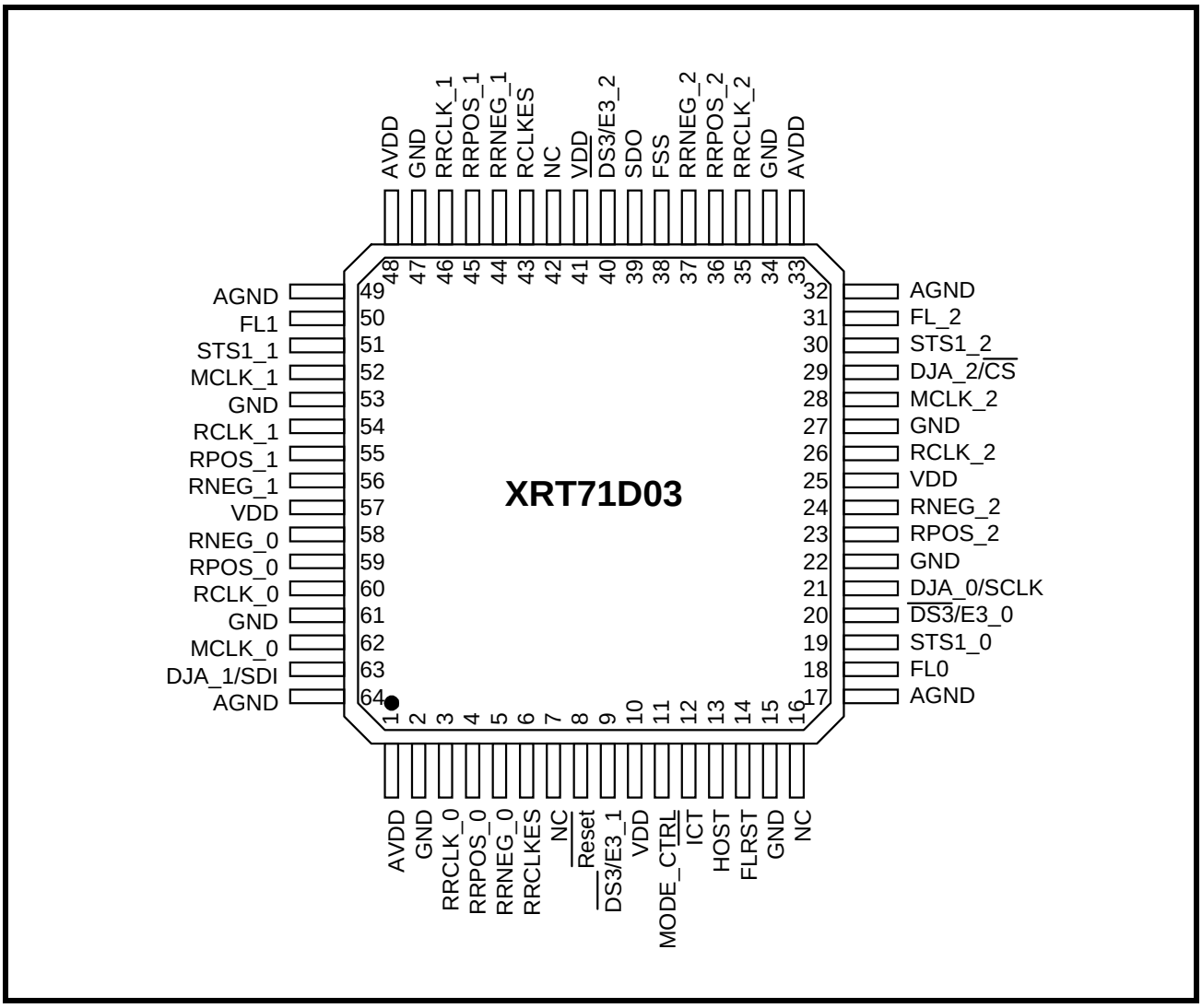


FIGURE 2. PIN OUT OF THE XRT71D03



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D03IV	64 Pin TQFP	-40°C to +85°C

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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
1	AVDD	****	**Analog Power Supply = 5V±5% or 3.3V±5%**
2	GND	****	**Digital Power Supply = 5V±5% or 3.3V±5%**
3	RRCLK_0	O	**Received Recovered Output (De-jittered) Clock - channel 0:** Output the de-jittered or smoothed clock if the jitter attenuator is enabled. The de-jittered data, RRPOS/RRNEG are clocked to this signal. If RRCLKES is "low", RRPOS/RRNEG will be updated at the falling edge of RRCLK. If RRCLKES is "high", RRPOS/RRNEG will be updated at the rising edge of RRCLK.
4	RRPOS_0	O	**Received Recovered Positive Data (De-Jittered) Output - channel 0:** De-jittered positive data output. Updated on the rising or falling edge of RRCLK, depending upon the state of the RRCLKES input pin (or bit-field setting).
5	RRNEG_0	O	**Received Recovered Negative Data (De-Jittered) Output - channel 0:** De-jittered negative data output. Updated on the rising or falling edge of RRCLK, depending upon the state of the RRCLKES input pin (or bit-field setting).
6	RRCLKES	I	**Received Recovered Clock Edge Select Input:** **Hardware Mode:** 1. When RRCLKES = "0", then RRPOS and RRNEG are updated on the falling edge of RRCLK 2. When RRCLKES = "1", then RRPOS and RRNEG are updated on the rising edge of RRCLK ***NOTE:*** *This applies to all channels.* **Host Mode** Connect this pin to GND when the 71D03 is configured in the Host Mode. Internal 50 K Ohm pull-down resistor.
7	NC		No Connection
8	$\overline{\text{Rest}}$	I	**Reset Input.** (Active-Low): A high-low transition will re-center the internal FIFO, and will clear the Command Registers (for Host Mode operation). Resetting this pin may corrupt data within the device. For normal operation, pull this pin to VDD. Internal 50 K Ohm pull-up resistor.
9	$\overline{\text{DS3}}$/E3_1	I	**$\overline{\text{DS3}}$/E3 Select Input - channel 1**: This pin along with the STS-1 mode select pin selects the operating mode. The following table provides the configuration: **STS-1 — $\overline{\text{DS3}}$/E3 — XRT71D04 Operating Mode** 0 — 0 — DS3 (44.736 MHz) 0 — 1 — E3 (34.368 MHz) 1 — 0 — STS-1 (51.84 MHz) 1 — 1 — E3 (34.368 MHz) Internal 50 K Ohm pull-down resistor.
10	VDD	****	**Digital Power Supply = 5V±5% or 3.3V±5%**

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
11	MODE_CTRL	I	**Mode Control:** When "High" in Multimode, all channels are independent. When "Low", the Master Channel (channel0) controls DS3/E3_n, STS1_n, RCLKES, FSS and MCLKn. DJA is NOT affected. Internal 50 K Ohm pull-up resistor.
12	$\overline{\text{ICT}}$	I	**In Circuit Testing Input.** (Active low): With this pin tied to ground, all output pins will be in high impedance mode for in-circuit-testing. For normal operation this input pin should be tied to VDD. Internal 50 K Ohm pull-up resistor.
13	HOST	I	**Host/Hardware Mode Select:** An active-high input enables the Host mode. Data is written to the command registers to configure the XRT71D04. In the Host mode, the states of discrete input pins are inactive. An active-low input enables the Hardware Mode.In this mode, the discrete inputs are active. Internal 50 K Ohm pull-down resistor.
14	FLRST	I	**Fifo Limit Reset** **Hardware Mode** Whenever the FIFO is within 2 bits of either underflow or overflow, the FLn) will be set high. This pin allows the user to reset the state of FL_n, (FIFO Limit) output pin. This pin when pulsed "High", resets the the FL_n output pin, (toggles to GND). ***NOTE:*** *The FL_n could be set "High" again if the FIFO is within 2 bits of either underflow or overflow.* **Host Mode** Reading the FL_n bits in the status registers clears the FL_n pin. Master RESET also clears the FL_n output. This pin is tied to GND. FLRST has no effect in this mode. Internal 50 K Ohm pull-down resistor.
15	GND	****	**Digital Ground**
16	NC		No Connection
17	AGND	****	**Analog Ground**
18	FL_0	O	**FIFO Limit - channel 0:** This output pin is driven high whenever the internal FIFO comes within two-bits of being underflow or overflow.
19	STS1_0	I	**SONET STS1 Mode Select - channel 0:** This pin along with the $\overline{\text{DS3}}$/E3_0 select pin configures the XRT71D03 either in E3, DS3 or STS-1 mode. A table relating to the setting of the pins is given below: **STS-1** **$\overline{\text{DS3}}$/E3** **XRT71D03 Operating Mode** 0 0 DS3 (44.736 MHz) 0 1 E3 (34.368 MHz) 1 0 STS-1 (51.84 MHz) 1 1 E3 (34.368 MHz) This input pin is active only in the Hardware Mode

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
20	$\overline{DS3}$/E3_0	I	**$\overline{DS3}$/E3 Select Input - channel 0**: See description pin 8. Internal 50 K Ohm pull-down resistor.
21	DJA_0/SCLK	I	**Hardware Mode** **Disable Jitter Attenuator Input - Channel 0:** An active-high disables the Jitter Attenuator. The RPOS/RNEG and RCLK will be passed through without jitter attenuation. **Host Mode** **Microprocessor Serial Interface Clock Signal:** This signal will be used to sample the data on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal. Internal 50 K Ohm pull-down resistor.
22	GND	****	**Digital Ground**
23	RPOS_2	I	**Received Positive Data (Jittery) Input: - channel 2:** Data that is input on this pin is sampled on either the rising or falling edge of RCLK depending on the setting of the RCLKES pin (pin 10). If RCLKES is "high", then RPOS will be sampled on the falling edge of RCLK. If RCLKES is "low", then RPOS will be sampled on the rising edge of RCLK. Internal 50 K Ohm pull-up resistor.
24	RNEG_2	I	**Received Negative Data (Jittery) - channel 2:** The input jittery negative data is sampled either on the rising or falling edge of RCLK depending on the setting of RCLKES. If RCLKES is "high", then RNEG will be sampled on the falling edge of RCLK. If RCLKES is "low", then RPOS will be sampled on the rising edge of RCLK. This pin is typically tied to the "RNEG" output pin of the LIU. Internal 50 K Ohm pull-up resistor.
25	VDD	****	**Digital Power Supply = 5V±5% or 3.3V±5%**
26	RCLK_2	I	**Received Clock (Jittery) - channel 2:** Clock input RCLK2 should be connected to the recovered clock. Internal 50 K Ohm pull-up resistor.
27	GND	****	**Digital Ground**
28	MCLK_2	I	**Master Clock Input - channel 2:** Reference clock for internal PLL. 44.736MHz+/-20ppm or 34.368MHz+/-20ppm. This clock must be continuous and jitter free with duty cycle between 30 to 70%. It is permissible to use the EXCLK signal orSTS1 clock. Internal 50 K Ohm pull-up resistor.
29	DJA_2/$\overline{CS}$	I	**Hardware Mode** **Disable Jitter Attenuator Input - Channel 2:** See description of pin 25 **Host Mode** **Chip Select Input:** An active-low input enables the serial interface. Internal 50 K Ohm pull-down resistor.
30	STS1_2	I	**SONET STS1 Mode Select - channel 2:** See description pin 19

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
31	FL_2	O	**FIFO Limit - channel 2:** See description pin 18
32	AGND	****	**Analog Ground**
33	AVDD	****	**Analog Power Supply =5±5% or 3.3V±5%**
34	GND	****	**Digital Ground**
35	RRCLK_2	O	**Received Recovered Output (De-jittered) Clock - channel 2:** See description of pin 3
36	RRPOS_2	O	**Received Recovered Positive Data (De-Jittered) Output - channel 2:** See description of pin 4
37	RRNEG_2	O	**Received Recovered Negative Data (De-Jittered) Output - channel 2:** See description of pin 5
38	FSS	I	**FIFO Size Select Input:** When "High": Selects 32 bits FIFO. When "Low": Selects 16 bits FIFO. Internal 50 K Ohm pull-down resistor.
39	SDO	O	**Serial Data Output:** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SCLK input signal. This pin will be tri-stated upon completion of data transfer.
40	$\overline{DS3}$/E3_2	I	**$\overline{DS3}$/E3 Select Input - channel 2**: See description pin 8 Internal 50 K Ohm pull-down resistor.
41	VDD	****	**Digital Power Supply = 5V±5% or 3.3V±5%**
42	NC		No Connection
43	RCLKES	I	**Received Clock Edge Select Input:** **Hardware Mode** 1. When RCLKES = "0", then RPOS and RNEG are updated on the falling edge of RCLK 2. When RCLKES = "1", then RPOS and RNEG are updated on the rising edge of RCLK ***NOTE:*** *This applies to all channels.* **Host Mode** Connect this pin to GND when the 71D03 is configured in the Host Mode. Internal 50 K Ohm pull-down resistor.
44	RRNEG_1	O	**Received Recovered Negative Data (De-Jittered) Output - channel 1:** See description of pin 5
45	RRPOS_1	O	**Received Recovered Positive Data (De-Jittered) Output - channel 1:** See description of pin 4

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
46	RRCLK_1	O	**Received Recovered Output (De-jittered) Clock - channel 1:** See description of pin 3.
47	GND	****	**Digital Ground**
48	AVDD	****	**Analog Power Supply = 5 V±5% or 3.3V±5%**
49	AGND	****	**Analog Ground**
50	FL_1	O	**FIFO Limit - channel 1:** See description pin 18
51	STS1_1	I	**SONET STS1 Mode Select - channel 1:** See description pin 19
52	MCLK_1	I	**Master Clock Input - channel 1:** See description pin 28. Internal 50 K Ohm pull-up resistor.
53	GND	****	**Digital Ground**
54	RCLK_1	I	**Received Clock (Jittery) - channel 1:** See description of pin 26. Internal 50 K Ohm pull-up resistor.
55	RPOS_1	I	**Received Positive Data (Jittery) Input: - channel 1:** See description of pin 23. Internal 50 K Ohm pull-up resistor.
56	RNEG_1	I	**Received Negative Data (Jittery) - channel 1:** See description of pin 24. Internal 50 K Ohm pull-up resistor.
57	VDD	****	**Digital Power Supply = 5V±5% or 3.3V±5%**
58	RNEG_0	I	**Received Negative Data (Jittery) - channel 0:** See description of pin 24. Internal 50 K Ohm pull-up resistor.
59	RPOS_0	I	**Received Positive Data (Jittery) Input: - channel 0:** See description of pin 23. Internal 50 K Ohm pull-up resistor.
60	RCLK_0	I	**Received Clock (Jittery) - channel 0:** See description of pin 26. Internal 50 K Ohm pull-up resistor.
61	GND	****	**Digital Ground**
62	MCLK_0	I	**Master Clock Input - channel 0:** See description pin 28. Internal 50 K Ohm pull-up resistor.

PIN DESCRIPTION

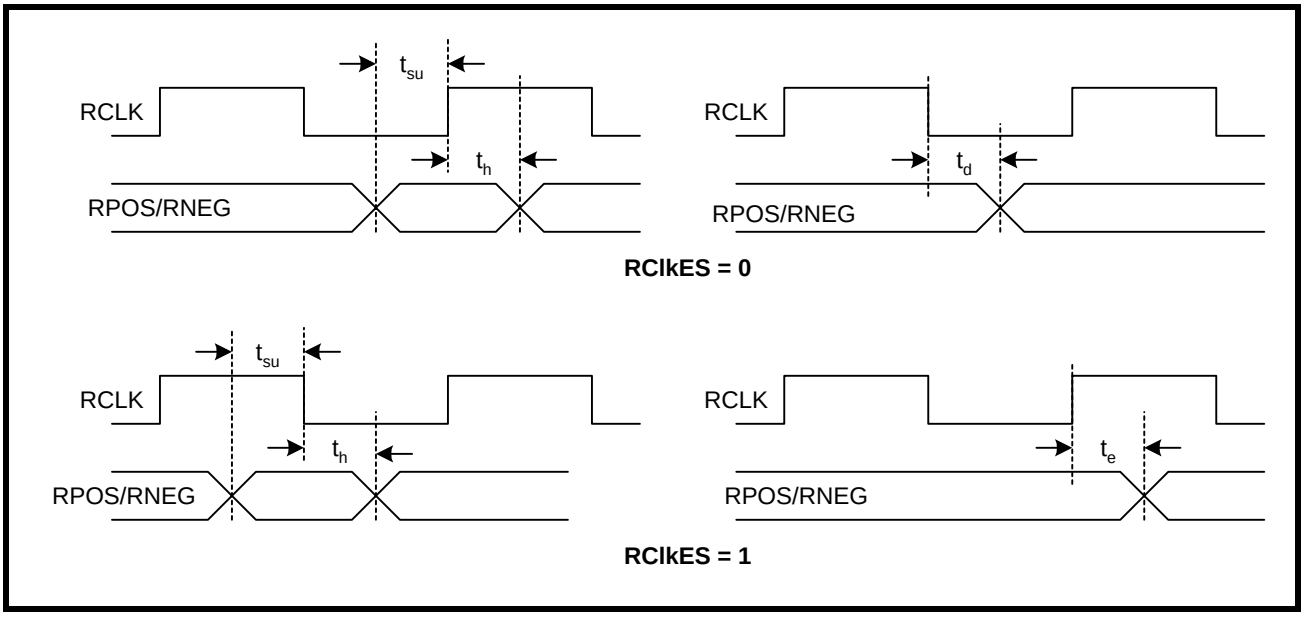
PIN #	NAME	TYPE	DESCRIPTION
63	DJA_1/SDI	I	**Hardware Mode** **Disable Jitter Attenuator Input - Channel 1:** See description of pin 25 **Host Mode** **Serial Data Input** The address value (of the command registers) or the data value is either Read or Written through this pin. The input data will be sampled on the rising edge of the SCLK pin. Internal 50 K Ohm pull-down resistor.
64	AGND	****	**Analog Ground**

ELECTRICAL CHARACTERISTICS

AC Electrical Characteristics

Electrical Characteristics (TA = 25°C, VDD = 3.3 V t0 5.0 V± 5% unless otherwise specified)					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS.**
MClk	Duty Cycle	30	50	70	%
MClk	Frequency E3 ± 20 ppm		34.368		MHz
MClk	Frequency DS3 ± 20 ppm		44.736		MHz
MClk	Frequency STS-1 ± 20 ppm		51.84		MHz
RClk	Duty Cycle	30	50	70	%
RClk	Rise Time			5	ns
RClk	Fall Time			5	ns
t_{su}	RPOS/RNEG to RClk rise time setup	3	2		ns
t_h	RPOS/RNEG to RClk rising hold time	1	2		ns
t_d	RRPOS/RRNEG delay from RRClk rising		3	5	ns
t_e	RRPOS/RRNEG delay from RRClk falling		3	5	ns

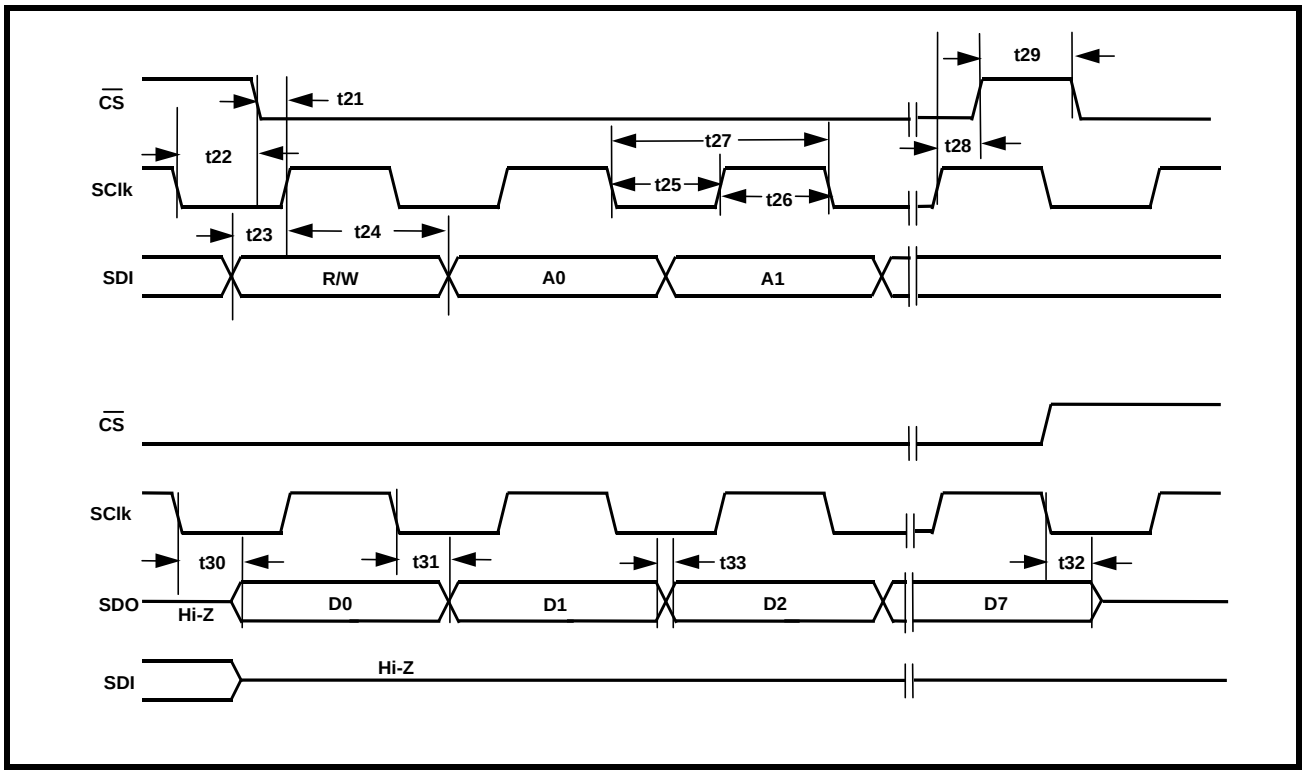
FIGURE 3. INPUT/OUTPUT TIMING



Microprocessor Serial Interface Timing (see Figure 4)

Electrical Characteristics (TA = 25°C, VDD = 3.3 V t0 5.0 V± 5 % unless otherwise specified)					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS.**
t21	$\overline{CS}$ Low to Rising Edge of SClk Setup Time	50			ns
t22	SClk to $\overline{CS}$ Hold Time	20			ns
t23	SDI to Rising Edge of SClk Setup Time	50			ns
t24	SDI to Rising Edge of SClk Hold Time	50			ns
t25	SClk “Low” Time	240			ns
t26	SClk “High” Time	240			ns
t27	SClk Period	500			ns
t28	SClk to CSB Hold Time	50			ns
t29	$\overline{CS}$ “Inactive” Time	250			ns
t30	Falling Edge of SClk to SDO Valid Time			200	ns
t31	Falling Edge of SClk to SDO Invalid Time			100	ns
t32	Falling Edge of SClk, or rising edge of $\overline{CS}$ to High Z		100		ns

FIGURE 4. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



DC Electrical Characteristics (TA = 25 °C, VDD = 3.3 V ± 5% unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	VDD	3.135	3.3	3.465	V
Input High Voltage	VIH	2.0		5.25	V
Input Low Voltage	V_{IL}	-0.5		0.8	V
Output High Voltage @ IOH=-5mA	VOH	2.4			V
Output Low Voltage @ IOL=5mA	VOL			0.4	V
Supply Current (E3) @VDD = 3.465V	Icc		75	85	mA
Supply Current (DS3) @VDD = 3.465V	Icc		95	109	mA
Supply Current (STS-1) @VDD = 3.465V	Icc		105	120	
Input Leakage Current (except Input pins with Pull-up resistor).	IL			± 10	µA
Input Capacitance	CI		5.0		pF
Output Load Capacitance	C_L			25	pF

DC Electrical Characteristics (TA = 25 °C, VDD = 5.0 V ± 5% unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	VDD	4.75	5.0	5.25	V
Input High Voltage	VIH	2.0		5.25	V
Input Low Voltage	V_{IL}	-0.5		0.8	V
Output High Voltage @ IOH=-5mA	VOH	2.4			V
Output Low Voltage @ IOL=5mA	VOL			0.4	V
Supply Current (E3) @VDD = 5.25V	Icc		120	136	mA
Supply Current (DS3) @VDD = 5.25V	Icc		145	160	mA
Supply Current (STS-1) @VDD = 5.25V	Icc		160	180	
Input Leakage Current (except Input pins with Pull-up resistor).	IL			± 10	µA
Input Capacitance	CI		5.0		pF
Output Load Capacitance	C_L			25	pF

ABSOLUTE MAXIMUM RATINGS:

Supply Range	-0.5 V to + 6.0 V
ESD Rating	> 2000 V on all pins
Operating Temperature	-40^0C to $+85^0$C
Storage Temperature	-65°C to + 150°C

SYSTEM DESCRIPTION

The XRT71D03 is an integrated 3-channel E3/DS3/STS-1 jitter attenuator that attenuates the jitter from the input clock and data. The jitter attenuation performance meets the latest specifications such as Bellcore GR-499 CORE,GR-253 CORE, ETSI TBR24,ITU-T G.751,ITU-T G.752 and ITU-T G.755 standards.

In addition, the XRT71D03 also meets both the mapping and pointer adjustment jitter generation criteria for both Category I and Category II interfaces as specified in Bellcore GR-253.

The XRT71D03 also meets the DS3 wander specification that apply to SONET and asynchronous interfaces as specified in the ANSI T1.105.03b 1997 standard.

Additionally, to support loop-timing applications, the XRT71D03 can also be used to reduce and limit the amount of jitter in the recovered line clock signal.

Figure 5 presents a simple block diagram of the XRT71D03, when it is configured to operate in the Hardware Mode and Figure 6 presents a simple block diagram of the XRT71D03, when it is configured to operate in the Host Mode.

FIGURE 5. ILLUSTRATION OF A TYPICAL CHANNEL_N OF THE XRT71D03 CONFIGURED TO OPERATE IN THE HARDWARE MODE

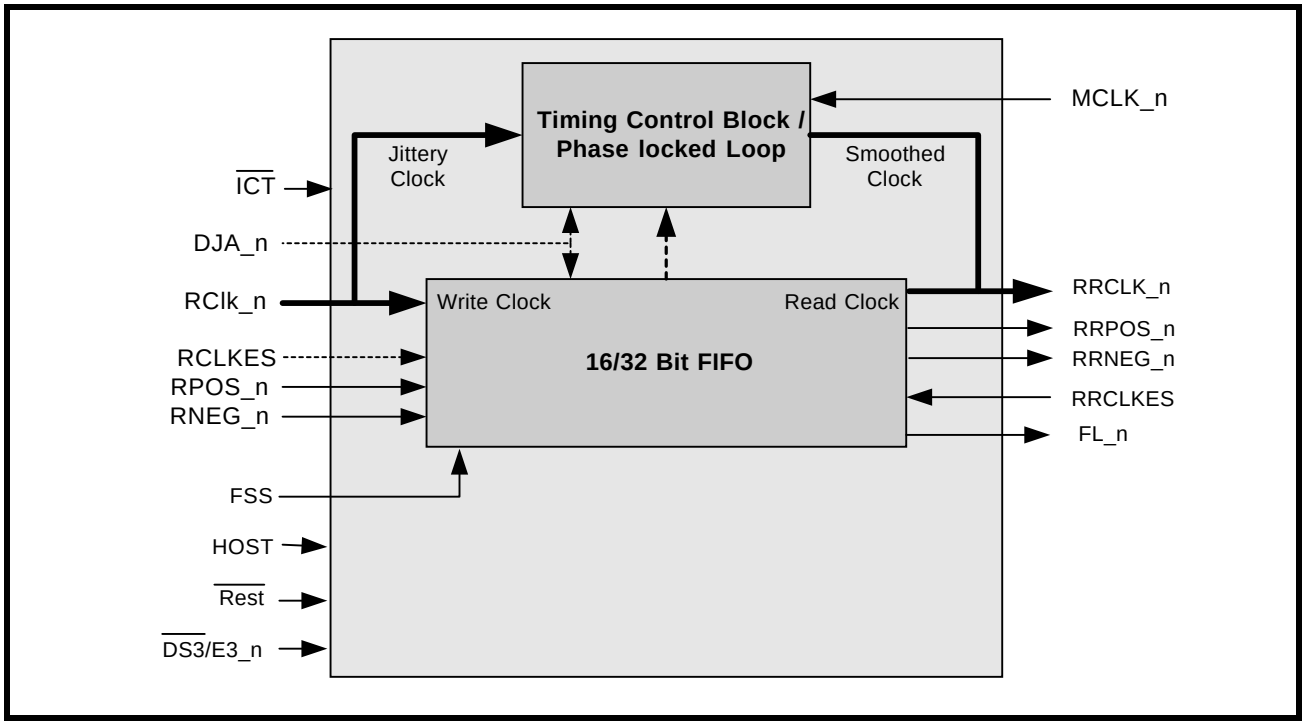
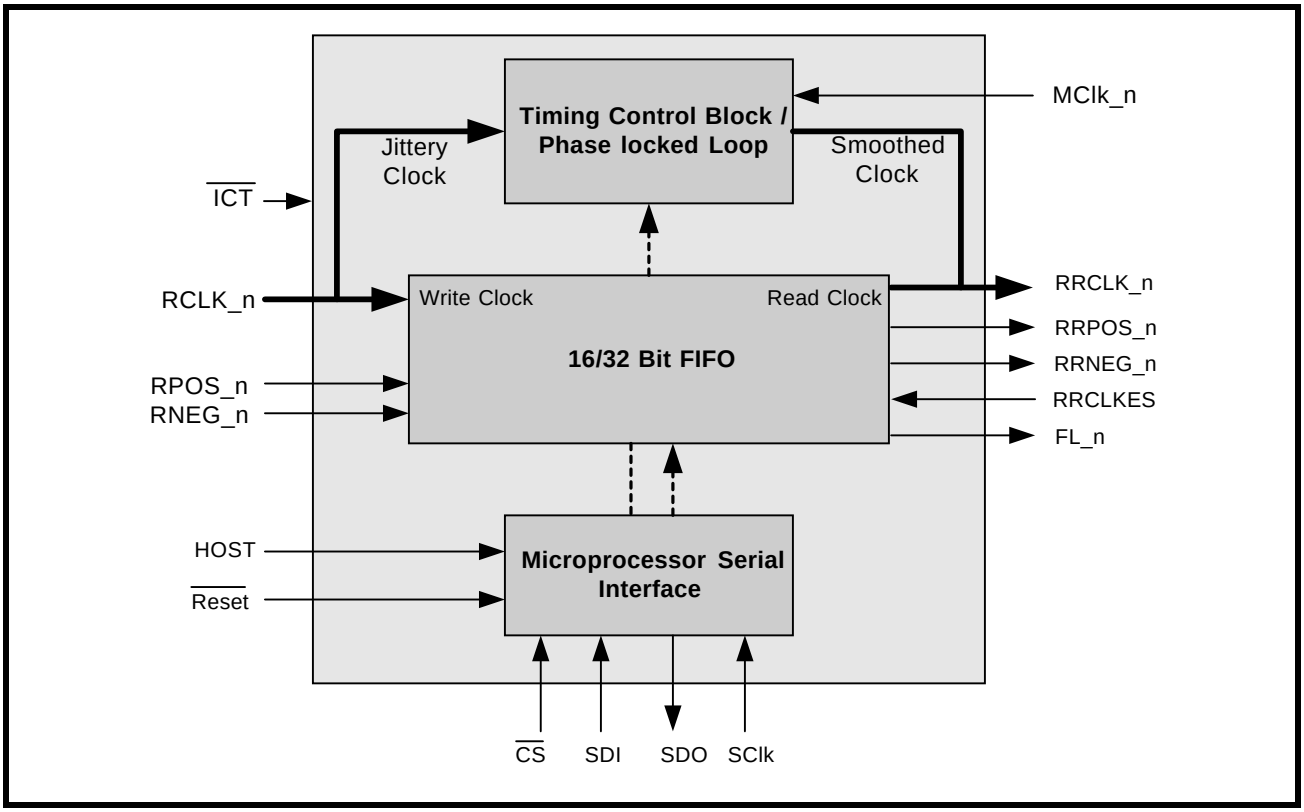


FIGURE 6. ILLUSTRATION OF A TYPICAL CHANNEL_N OF THE XRT71D03 (CONFIGURED TO OPERATE IN THE HOST MODE)



The XRT71D03 DS3/E3 Jitter Attenuator IC consists of the following functional blocks:

- The Jitter-Attenuator PLL
- Timing Control Block
- The 2-Channel 16/32 Bit FIFO
- Serial Microprocessor Interface

1.0 JITTER ATTENUATOR PLL

1.1 BACKGROUND INFORMATION DEFINITION OF JITTER

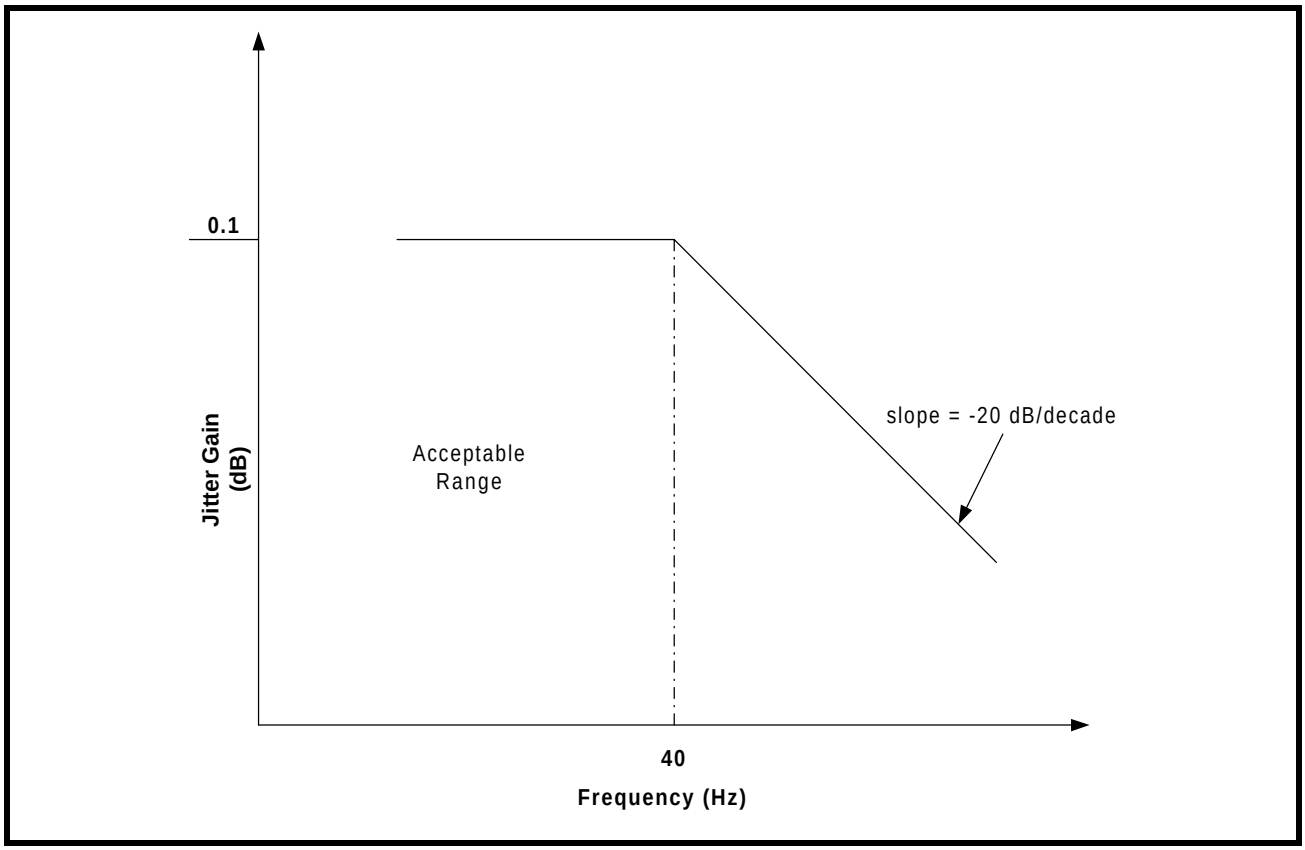
One of the most important and least understood measures of clock performance is jitter. The International Telecommunication Union defines jitter as short term variations of the significant instants of a digital signal from their ideal positions in time. Jitter can occur due to any of the following:

1) Imperfect timing recovery circuit in the system
2) Cross-talk noise
3) Inter-symbol interference/Signal Distortion

1.2 JITTER TRANSFER CHARACTERISTICS

The primary purpose of jitter transfer requirements is to prevent performance degradations by limiting the accumulation of jitter through the system such that it does not exceed the network interface jitter requirements. Thus, it is more important that a system meet the jitter transfer criteria for relatively high input jitter amplitudes. The jitter transferred through the system must be under the jitter mask for any input jitter amplitude within the range as shown in Figure 7

FIGURE 7. CATEGORY 1 DS3 JITTER TRANSFER MASK



1.2.1 Jitter Tolerance

The jitter tolerance in the network element is defined as the maximum amount of jitter in the incoming signal that it can receive in an error-free manner.

1.2.2 Jitter Generation

Jitter generation is defined in Section 7.3.3 of GR-499-CORE. Jitter generation criteria exists for both Category I and II interfaces, which consist of mapping and pointer adjustment jitter generation.

Mapping jitter is the sum of the intrinsic payload mapping jitter and the jitter that is generated as a result of the bit stuffing mechanisms used in all of the asynchronous DSn mapping into STS SPE.

1.2.3 Jitter Attenuation

A digital Jitter Attenuation loop combined with the FIFO provides Jitter attenuation. The Jitter Attenuator requires no external components except for the reference clock.

Data is clocked into the FIFO with the associated clock signal (TClk or RClk) and clocked out of the FIFO with the dejittered clock and data. When the FIFO is within 2 bits of being completely full, the FIFO Limit (FL) will be set.

In Figure 5 and Figure 6, this de-jittered clock is labeled Smoothed Clock. This Smoothed Clock is now used to Read Out the Recovered Data from the 16/32 bit FIFO. This Smoothed Clock will also be output to the Terminal Equipment via the RRClk output pin. Likewise, the Smoothed Recovered Data will output to the Terminal Equipment via the RRPOS and RRNEG output pins.

The XRT71D03 is designed to work as a companion device with XRT73L03 (STS-1/DS3/E3) Line Interface Unit.

ETSI TBR24 specifies the maximum output jitter in loop timing must be no more than 0.4UIpp when measured between 100Hz to 800KHzwith up to 1.5UI input jitter at 100Hz. This means a jitter attenuator with bandwidth less than 100Hz is required to be compliant with the standard. ITU G.751 is another application where low bandwidth jitter attenuator is needed to smooth the gapped clock output in the de-multiplexer system.

1.3 XRT71D03 JITTER TRANSFER AND TOLERANCE

Table 1 summarizes the results of jitter transfer characteristics testing, performed on the XRT71D03.

Table 2 summarizes the results of jitter tolerance testing, performed on the XRT71D03.

Graphs of the measured Jitter Transfer are shown in Figure 8, Figure 9 and Figure 10.

TABLE 1: XRT71D03 JITTER TRANSFER FUNCTION

APPLICATION	DS3		E3		STS-1	
INPUT JITTER	1UIPP	10UIPP	1UIPP	10UIPP	1UIPP	10UIPP
FREQ. (HZ)	Jitter Gain (dB)		Jitter Gain (dB)		Jitter Gain (dB)	
10	-0.10	-0.30	-0.15	-0.22	0.22	0.53
20	-2.04	-2.24	-3.16	-3.24	-0.69	-1.09
30	-3.63	-4.33	-5.51	-5.93	-5.92	-3.01
40	-5.98	-6.16	-7.68	-7.99	-8.10	-4.74
50	-7.55	-7.82	-10.36	-9.61	-10.17	-6.33
60	-9.57	-9.17	-12.50	-11.27	-11.24	-7.64
80	-12.54	-11.28	-15.20	-13.59	-13.65	-9.98
100	-14.67	-13.36	-16.22	-15.51	-14.78	-11.92
125	-16.67	-14.91	-17.38	-17.07	-16.94	-13.75
150	-17.32	-16.78	-19.45	-18.75	-17.38	-15.23
200	-18.77	-18.96	-20.36	-21.11	-19.57	-17.41
300	-21.43	-21.81	-22.96	-24.46	-21.96	-21.69
500	-22.22	-26.09	-23.78	-28.84	-23.59	-25.47
>1000	-25.42	-33.44	-23.51	-35.77	-25.76	-32.99
2000					-26.27	-39.83
3000					-27.41	-41.95
5000					-26.15	-44.16

FIGURE 8. DS3 JITTER TRANSFER CHARACTERISTICS

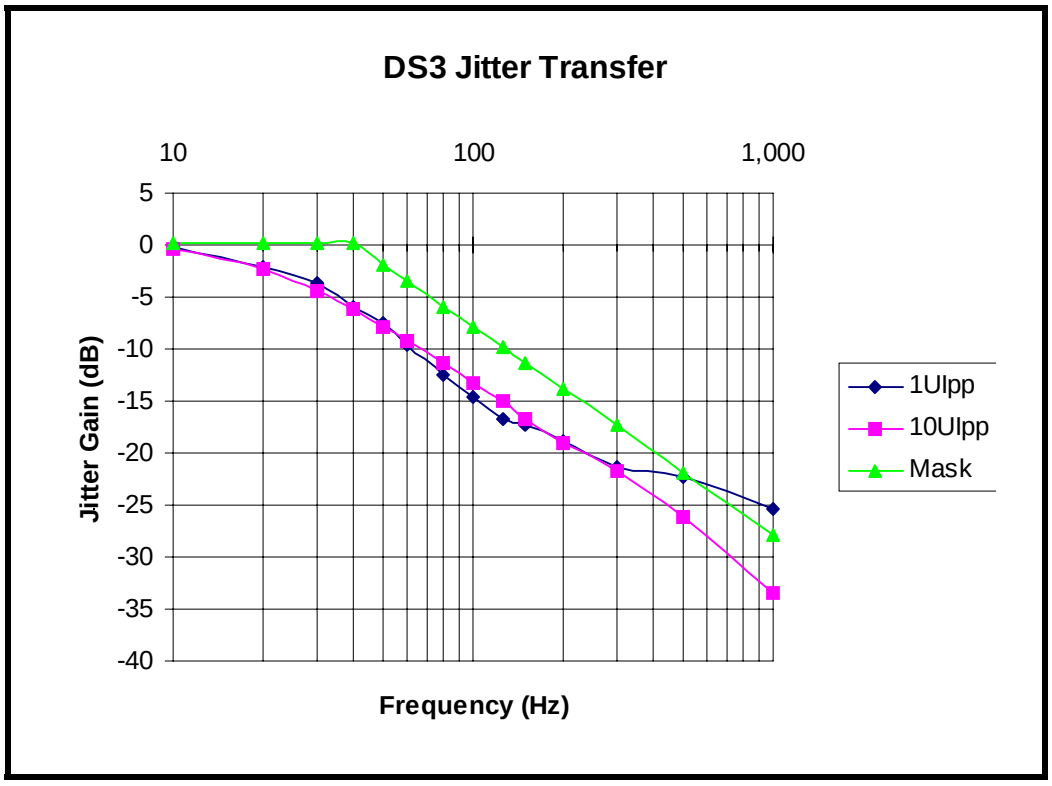


FIGURE 9. E3 JITTER TRANSFER CHARACTERISTICS

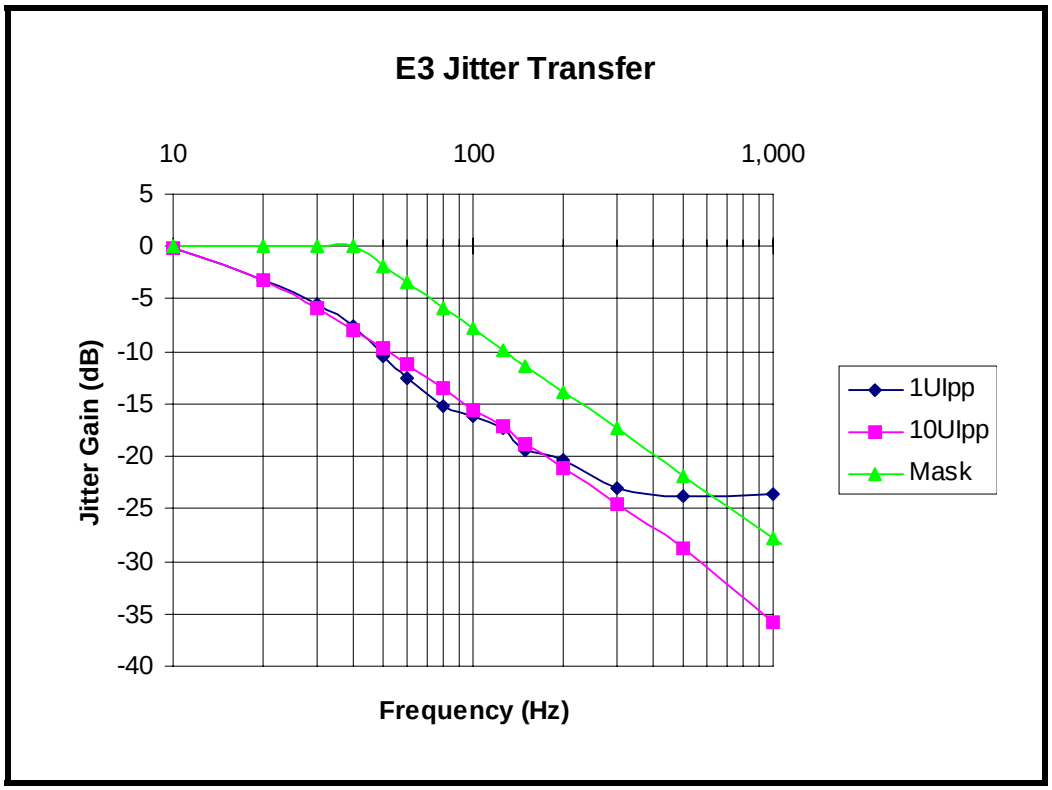


FIGURE 10. STS-1 JITTER TRANSFER CHARACTERISTICS

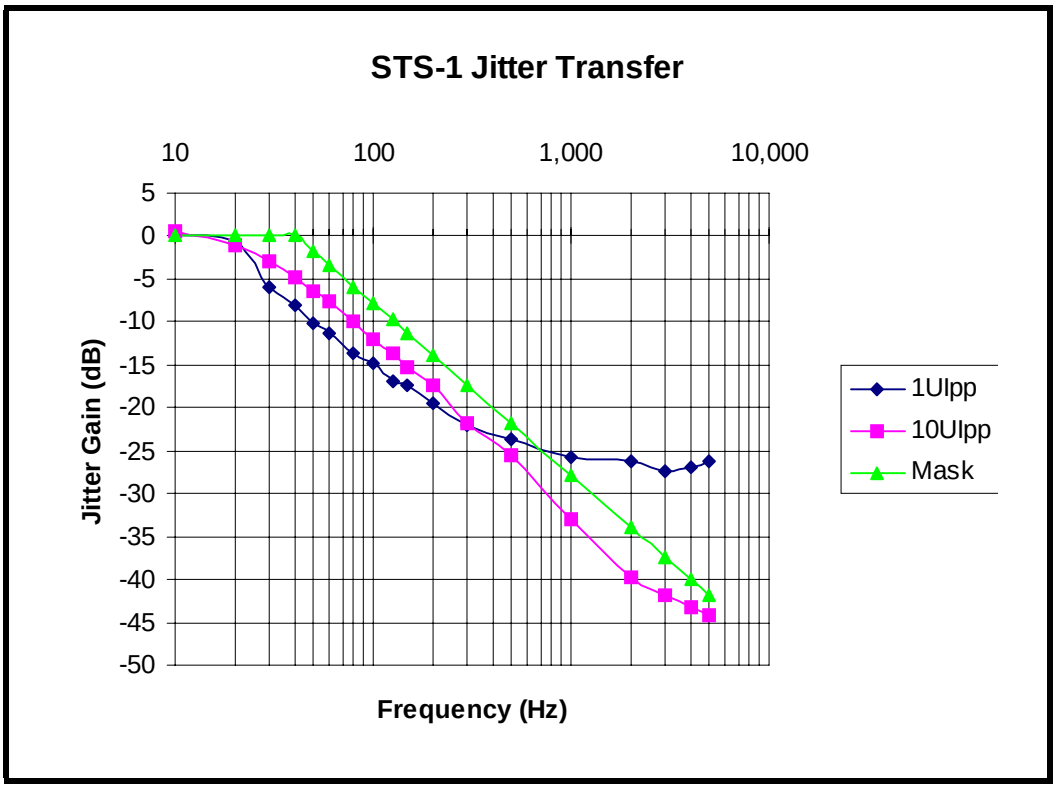


TABLE 2: XRT71D03 MAXIMUM JITTER TOLERANCE

APPLICATION	DS3		E3		STS-1	
FIFO SIZE	16	32	16	32	16	32
FREQ. (HZ)	UI (PEAK TO PEAK)		UI (PEAK TO PEAK)		UI (PEAK TO PEAK)	
10	34.313	>64	26.689	53.313	38.938	>64
20	21.439	43.188	18.564	37.438	22.689	44.813
30	18.314	36.813	16.689	33.938	18.939	37.688
40	16.939	34.313	16.064	32.688	17.439	34.938
50	16.314	33.188	15.689	32.063	16.814	33.563
60	16.064	32.563	15.564	31.689	16.439	32.813
80	15.689	31.814	15.314	31.314	16.064	32.063
100	15.439	31.439	15.314	31.189	15.814	31.814
125	15.439	31.314	15.189	31.064	15.689	31.564
150	15.314	31.189	15.189	31.064	15.689	31.439
200	15.314	31.064	15.189	30.939	15.564	31.314
300	15.189	30.939	15.064	30.939	15.564	31.189
500	15.189	30.939	15.064	30.939	15.564	31.189
>1000	15.0189	30.939	15.189	30.939	15.439	31.189
					15.439	31.189
					15.439	26.189
					15.439	16.189

2.0 OPERATING MODES

2.1 HARDWARE MODE

The HOST pin is used to select the operating mode of the XRT71D03. In Hardware mode (connect this pin to ground), the serial processor interface is disabled and hard-wired pins are used to control configuration and report status.

TABLE 3: FUNCTIONS OF DUAL MODE PINS IN HARDWARE MODE CONFIGURATION

PIN #	PIN NAME	FUNCTION, WHILE IN THE HARDWARE MODE
63	DJA_1/(SDI)	DJA_1
21	DJA_0/SCLK	DJA_0
29	DJA_2($\overline{CS}$)	DJA_2

2.2 HOST MODE

In Host mode (connect the HOST pin to VDD), the serial port interface pins are used to control configuration and status report. In this mode, serial interface pins, SDI, SDO,SCLK and $\overline{CS}$ are used.

A listing of these Command Registers, their Addresses and their bit-formats are listed below in Table 4.

TABLE 4: ADDRESS AND BIT FORMATS OF THE COMMAND REGISTERS

ADDR	COMMAND REGISTER	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0X06	CR6	R/W	***	***	STS-1_0	$\overline{DS3}$/E3_0	DJA_0	RRClkES_0	RClkES_0	FSS_0
0x07	CR7	RO	***	***	***	***	***		***	FL_0
0x0E	CR14	R/W	***	***	STS-1_1	$\overline{DS3}$/E3_1	DJA_1	RRClkES_1	RClkES_1	FSS_1
0x0F	CR15	RO	***	***	***	***	***		***	FL_1
0x16	CR22	R/W	***	***	STS-1_2	$\overline{DS3}$/E3_2	DJA_2	RRClkES_2	RClkES_2	FSS_2
0x17	CR23	RO	***	***	***	***	***		***	FL_2

3.0 MICROPROCESSOR SERIAL INTERFACE

The serial interface for the XRT71D03 and the XRT73L00 family of E3/DS3/STS-1 LIU's are the same, which makes it easy to configure both the XRT71D03 and the LIU with a single $\overline{CS}$, SDI, SDO and SClk input and output pins.

3.1 SERIAL INTERFACE OPERATION.

Serial interface data structure and timings are provided in Figure 5 and 6 respectively.

The clock signal is provided to the SClk and the $\overline{CS}$ is asserted for 50 ns prior to the first rising edge of the SClk.

3.1.1 Bit 1—R/W (Read/Write) Bit

This bit will be clocked into the SDI input, on the first rising edge of SClk (after $\overline{CS}$ has been asserted). This bit indicates whether the current operation is a Read or Write operation.

A "1" in this bit specifies a Read operation, a "0" in this bit specifies a Write operation.

3.1.2 Bits 2 through 5—A0, A1, A2, A3, and A4

The five (5) bit Address Values (labeled A0, A1, A2, A3, and A4).

The next five rising edges of the SClk signal will clock in the 5-bit address value for this particular Read (or Write) operation. The address selects the Command Register for reading data from, or writing data to. The address bits to the SDI input pin is applied in ascending order with the LSB (least significant bit) first.

3.1.3 Bit 7—A5

A5 must be set to "0", as shown in Figure 11.

3.1.4 Bit 8—A6

The value of A6 is a don't care.

Once these first 8 bits have been written into the Serial Interface, the subsequent action depends upon whether the current operation is a Read or Write operation.

3.1.5 Read Operation

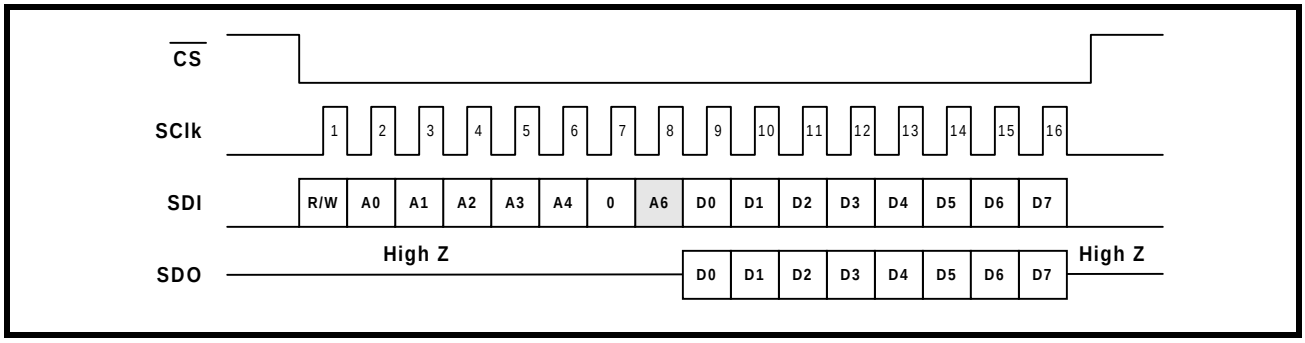
Once the last address bit (A4) has been clocked into the SDI input, the Read operation will proceed through an idle period, lasting three SClk periods. On

the falling edge of SClk Cycle #8 (see Figure 11) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A4, A3, A2, A1, A0]) via the SDO output pin. The Serial Interface will output this eight bit data word (D0 through D7) in ascending order (with the LSB first), on the falling edges of the SClk. The data (on the SDO output pin) is stable for reading on the very next rising edge of the SClk.

3.1.6 Write Operation

Once the last address bit (A4) has been clocked into the SDI input, the Write operation will proceed through an idle period, lasting three SClk periods. Prior to the rising edge of SClk Cycle #9, the eight bit data word is applied to SDI input. Data on SDI is latched on the rising edge of SClk.

FIGURE 11. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

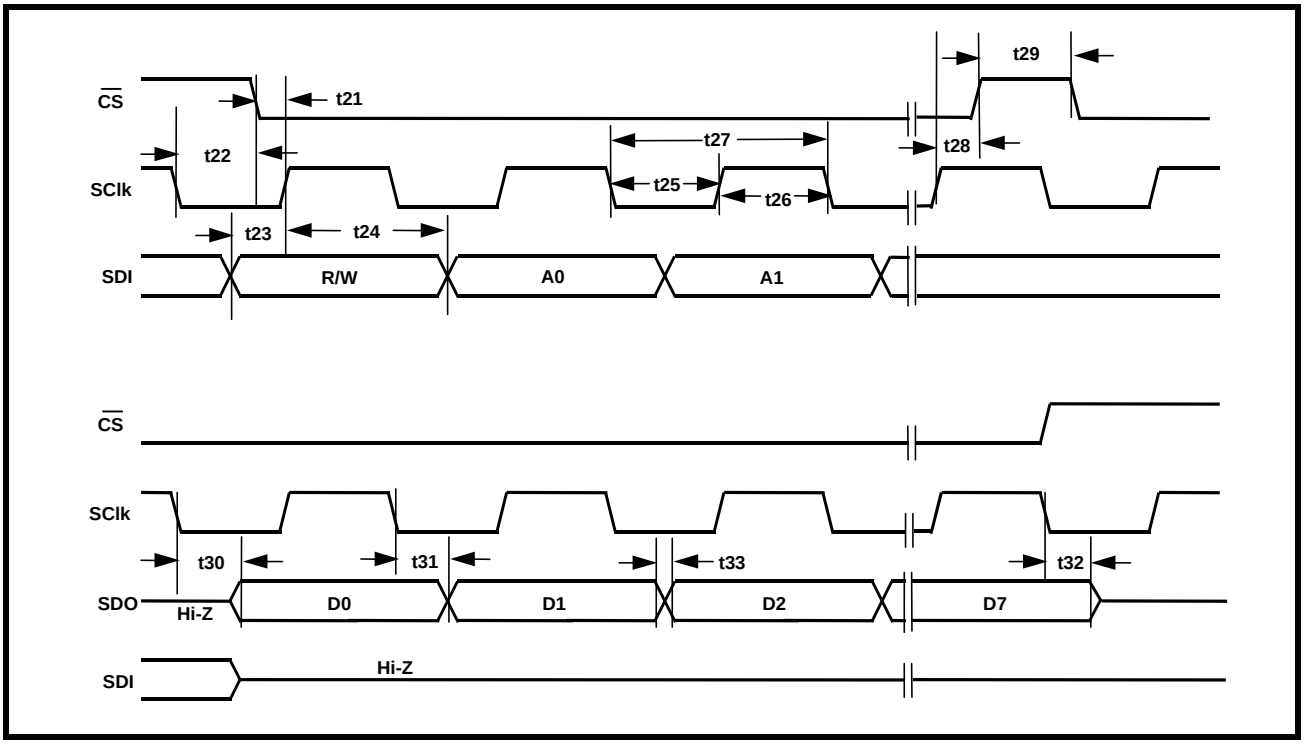
1. *A5 is always "0".*
2. *R/W = "1" for Read Operations*
3. *R/W = "0" for Write Operations*
4. *Denotes a "don't care" value (shaded areas)*

3.1.7 Simplified Interface Option

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this combined signal. This simplification is possible because only one of

these signals are active at any given time. The inactive signal will be tri-stated.

FIGURE 12. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

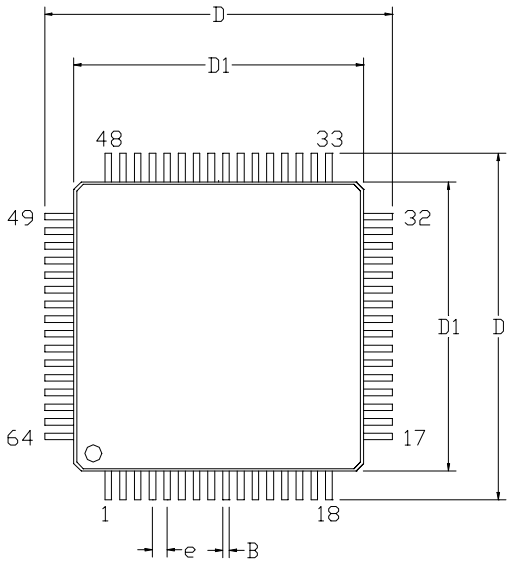


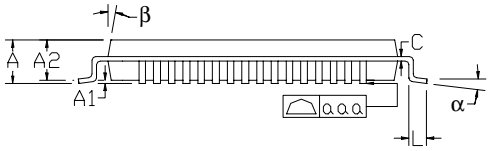
ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D03IV	64 Pin TQFP	-40°C to +85°C
THERMAL INFORMATION	Theta - J_A = 38° C/W	Theta J_C = 7° C/W

PACKAGE DIMENSIONS

64 Lead Thin Quad Flat Pack
(10 x 10 x 1.4 mm LQFP)





	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.0020 BSC		0.05 BSC	
L	0.018	0.050	0.45	0.75
α	0°	7°	0°	7°
β	7° typ		7° typ	
aaa	-	0.003	-	0.08

Note: Control Dimensions are the Millimeter Column

REVISION HISTORY

Rev. P1.0.1; Revised pull-up/pull-down resistors on various pins.

Rev. P1.0.2; Changed date and made minor edits to page 1.

Rev. P1.0.3; Corrected Pin List descriptions. Modified pin names to be consistent, ie MCLK0, RPOS0, RNEG0, etc. changed to MCLK_0, RPOS_0, RNEG_0, etc. Changed VSS to GND. Changed figures to reflect pin name changes.

Rev. 1.1.0 Removed preliminary designation. Added electrical tables.

Rev. 1.1.1 Corrected Table 4 adding RRClkES_n as data D2, STS-1_n as D5, added D7. Corrected the description of the section 3 Serial Microprocessor Interface. Moved figure 9 into Electrical Characteristics Section. Moved Jitter Transfer/Tolerance tables into Jitter Attenuator Section 1. Edited electrical tables.

Rev. 1.1.2 Corrected ordering information from XRT71DO3 to 71D03IV.

Rev. 1.2.0 Removed all reference to STS-1 to DS3 desynchronizer.

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