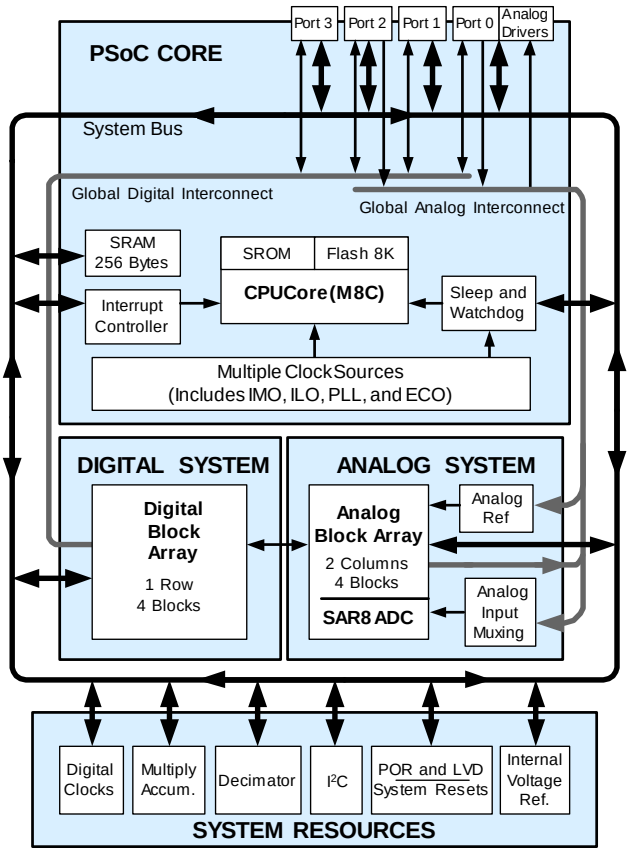
CY8C23433, CY8C23533

PSoC® Programmable System-on-Chip™

Features

- Powerful Harvard-architecture processor
  - M8C processor speeds to 24 MHz
  - 8x8 multiply, 32-bit accumulate
  - Low power at high speed
  - 3.0 V to 5.25 V operating voltage
  - Industrial temperature range: –40 °C to +85 °C
- Advanced peripherals (PSoC blocks)
  - Four Rail-to-Rail analog PSoC blocks provide:
    - Up to 14-bit ADCs
    - Up to 8-bit DACs
    - Programmable gain amplifiers
    - Programmable filters and comparators
  - Four digital PSoC blocks provide:
    - 8- to 32-bit timers and counters, 8- and 16-bit pulse-width modulators (PWMs)
    - CRC and PRS modules
    - Full-duplex UART
    - Multiple SPI™ masters or slaves
    - Connectable to all GPIO Pins
  - Complex peripherals by combining blocks
  - High-Speed 8-Bit SAR ADC optimized for motor control
- Precision, programmable clocking
  - Internal ±2.5% 24/48 MHz oscillator
  - High accuracy 24 MHz with optional 32 KHz crystal and PLL
  - Optional external oscillator, up to 24 MHz
  - Internal oscillator for watchdog and sleep
- Flexible on-chip memory
  - 8K bytes flash program storage 50,000 erase/write cycles
  - 256 bytes SRAM data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Programmable pin configurations
  - 25 mA Sink, 10 mA source on all GPIO
  - Pull-up, pull-down, high Z, strong, or open drain drive modes on all GPIO
  - Up to eight analog inputs on GPIO plus two additional analog inputs with restricted routing
  - Two 30 mA analog outputs on GPIO
  - Configurable interrupt on all GPIO
- Additional system resources
  - I^2C™ slave, master, and multi-master to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low voltage detection
  - Integrated supervisory circuit
  - On-chip precision voltage reference
- Complete development tools
  - Free development software (PSoC Designer™)
  - Full-featured in-circuit emulator and programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory

Logic Block Diagram



Contents

PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low-cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture make it possible for you to create customized peripheral configurations that match the requirements of each individual application. additionally, a fast central processing unit (CPU), flash memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the Logic Block Diagram on page 1, consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows combining all of the device resources into a complete custom system. The PSoC CY8C23x33 family can have up to three I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and four analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO)

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four million instructions per second MIPS 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with 11 vectors, to simplify programming of real time embedded events. program execution is timed and protected using the included sleep and watch dog timers (WDT).

Memory encompasses 8 KB of flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

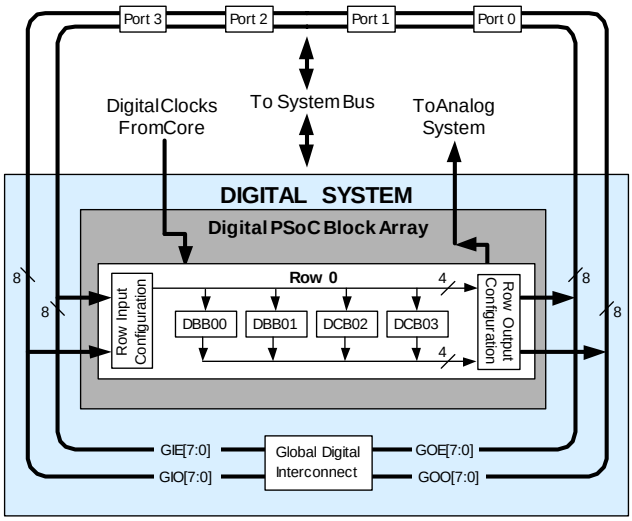
The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to ±2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

Digital System

The Digital system consists of 4 digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations are:

- PWMs (8-and 16-bit)
- PWMs with Dead band (8- and 16-bit)
- Counters (8- to 32- bit)
- Timers (8- to 32- bit)
- UART 8 bit with selectable parity (up to 1)
- Serial peripheral interface (SPI) master and slave (up to 1)
- I^2C slave and multi master (1 available as a system resource)
- Cyclical redundancy checker (CRC)/Generator (8 to 32 bit)
- IrDA (up to 1)
- Pseudo Random Sequence Generators (8- to 32- bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in the table titled PSoC Device Characteristics on page 5.

Analog System

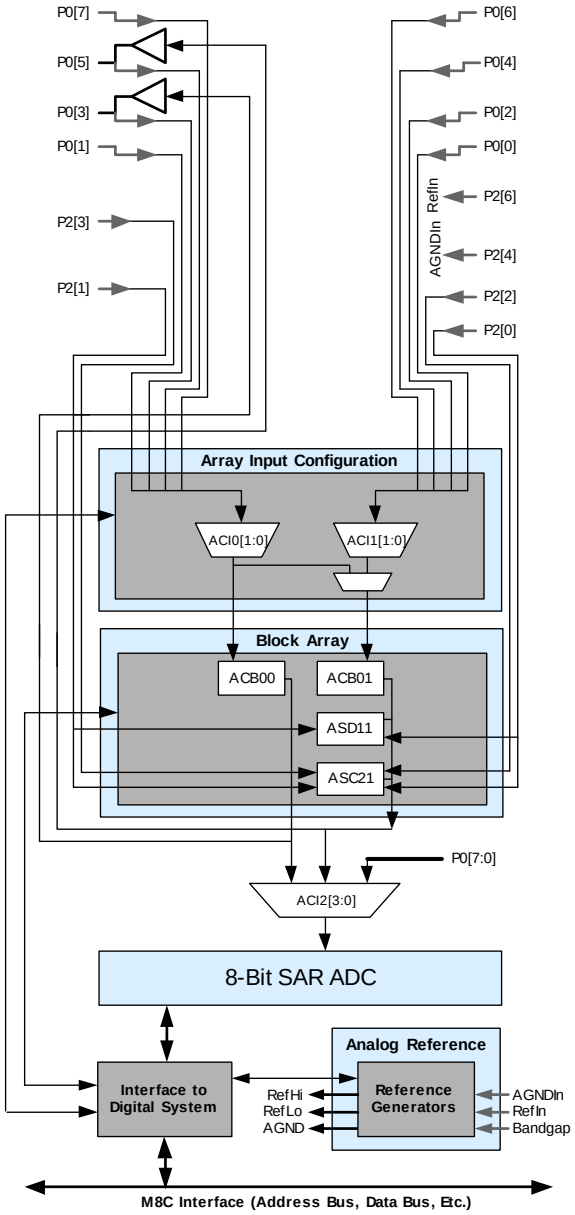
The analog system consists of an 8-bit SAR ADC and four configurable blocks. The programmable 8-bit SAR ADC is an optimized ADC that runs up to 300 Ksps, with monotonic guarantee. It also has the features to support a motor control application.

Each analog block consists of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Filters (2 band pass, low-pass)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (1, with 16 selectable thresholds)
- DAC (6 or 9-bit DAC)
- Multiplying DAC (6 or 9-bit DAC)
- High current output drivers (two with 30 mA drive)
- 1.3-V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. The Analog column 0 contains the SAR8 ADC block rather than the standard SC blocks.

Figure 2. Analog System Block Diagram



Notes
1. One complete column, plus one Continuous Time Block.
2. Limited analog functionality.
3. Two analog blocks and one CapSense.

Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on-reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta sigma ADCs.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-Voltage detection interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on the PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. Table 1 lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	SAR ADC
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K	No
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K	Yes
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K	No
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K	No
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K	No
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K	Yes
CY8C24x33	up to 26	1	4	up to 12	2	2	4	256	8 K	Yes
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K	No
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K	Yes
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K	No
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K	No
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K	No
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K	No

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer integrated development environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in-depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs and can be found at http://www.cypress.com

Development Kits

PSoC Development Kits are available online from cypress at http://www.cypress.com and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online at http://www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to http://www.cypress.com and look for CYPros.

Solutions Library

Visit our growing library of solution-focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, and read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

The CY8C23X33 PSoC is available in 32-pin QFN and 28-pin SSOP packages. Every port pin (labeled with a “P”), except for Vss and Vdd in the following table and figure, is capable of Digital I/O.

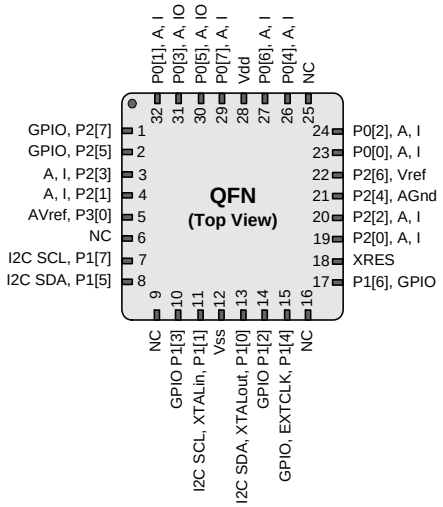
32-Pin Part Pinout

Table 2. Pin Definitions - 32-Pin (QFN)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O		P2[7]	GPIO
2	I/O		P2[5]	GPIO
3	I/O	I	P2[3]	Direct switched capacitor block input
4	I/O	I	P2[1]	Direct switched capacitor block input
5	I/O	AVref	P3[0][4]	GPIO/ADC Vref (optional)
6			NC	No connection
7	I/O		P1[7]	I^2C serial clock (SCL)
8	I/O		P1[5]	I^2C serial data (SDA)
9			NC	No connection
10	I/O		P1[3]	GPIO
11	I/O		P1[1]	GPIO, crystal Input (XTAL in), I^2C serial clock (SCL), ISSP-SCLK*
12	Power		Vss	Ground connection
13	I/O		P1[0]	GPIO, crystal output (XTAL out), I^2C serial data (SDA), ISSP-SDATA*
14	I/O		P1[2]	GPIO
15	I/O		P1[4]	GPIO, external clock IP
16			NC	No connection
17	I/O		P1[6]	GPIO
18	Input		XRES	Active high external reset with internal pull down
19	I/O	I	P2[0]	Direct switched capacitor block input
20	I/O	I	P2[2]	Direct switched capacitor block input
21	I/O		P2[4]	External analog ground (AGnd)
22	I/O		P2[6]	External voltage reference (VRef)
23	I/O	I	P0[0]	Analog column mux input and ADC input
24	I/O	I	P0[2]	Analog column mux input and ADC input
25			NC	No connection
26	I/O	I	P0[4]	Analog column mux input and ADC input
27	I/O	I	P0[6]	Analog column mux input and ADC input
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	Analog column mux input and ADC input
30	I/O	I/O	P0[5]	Analog column mux input, column output and ADC input
31	I/O	I/O	P0[3]	Analog column mux input, column output and ADC input
32	I/O	I	P0[1]	Analog column mux input.and ADC input

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C23533 32-Pin PSoC Device



Note
4. Even though P3[0] is an odd port, it resides on the left side of the pinout.

28-Pin Part Pinout

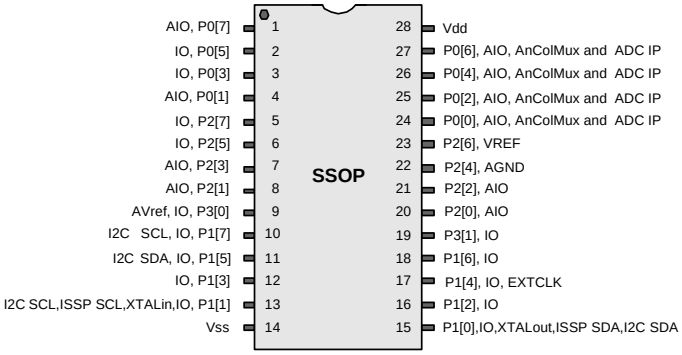
Table 3. Pin Definitions - 28-Pin (SSOP)

Pin No.	Type			
	Digital	Analog	Pin Name	Description
1	I/O	I	P0[7]	Analog column mux IP and ADC IP
2	I/O	I/O	P0[5]	Analog column mux IP and column O/P and ADC IP
3	I/O	I/O	P0[3]	Analog column mux IP and column O/P and ADC IP
4	I/O	I	P0[1]	Analog column mux IP and ADC IP
5	I/O		P2[7]	GPIO
6	I/O		P2[5]	GPIO
7	I/O	I	P2[3]	Direct switched capacitor input
8	I/O	I	P2[1]	Direct switched capacitor input
9	I/O	AVref	P3[0][5]	GPIO/ADC Vref (optional)
10	I/O		P1[7]	I2C SCL
11	I/O		P1[5]	I2C SDA
12	I/O		P1[3]	GPIO
13	I/O		P1[1][6]	GPIO, Xtal input, I2C SCL, ISSP SCL
14	Power		Vss	Ground Pin
15	I/O		P1[0][6]	GPIO, Xtal output, I2C SDA, ISSP SDA
16	I/O		P1[2]	GPIO
17	I/O		P1[4]	GPIO, External clock IP
18	I/O		P1[6]	GPIO
19	I/O		P3[1][7]	GPIO
20	I/O	I	P2[0]	Direct switched capacitor input
21	I/O	I	P2[2]	Direct switched capacitor input
22	I/O		P2[4]	External analog ground (AGnd)
23	I/O		P2[6]	Analog voltage reference (VRef)
24	I/O	I	P0[0]	Analog column mux IP and ADC IP
25	I/O	I	P0[2]	Analog column mux IP and ADC IP
26	I/O	I	P0[4]	Analog column mux IP and ADC IP
27	I/O	I	P0[6]	Analog column mux IP and ADC IP
28	Power		Vdd	Supply Voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4.

Figure 5. CY8C23433 28-Pin PSoC Device



Notes
5. Even though P3[0] is an odd port, it resides on the left side of the pinout.
6. ISSP pin, which is not High Z at POR.
7. Even though P3[1] is an even port, it resides on the right side of the pinout.

Register Reference

This section lists the registers of the CY8C23433 PSoC device by using mapping tables, in offset order.

Register Conventions

The register conventions specific to this section are listed in Table 4.

Table 4. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks Bank 0 and Bank 1. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set to 1 the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#	SARADC_DL	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL0_X	E8	W
DCB02DR1	29	W	SARADC_CR0	69	#		A9		MUL0_Y	E9	W
DCB02DR2	2A	RW	SARADC_CR1	6A	RW		AA		MUL0_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1 *	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Gray fields are reserved. # Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68		SARADC_TRS	A8	RW	IMO_TR	E8	W
DCB02IN	29	RW		69		SARADC_TRCL	A9	RW	ILO_TR	E9	W
DCB02OU	2A	RW		6A		SARADC_TRCH	AA	RW	BDG_TR	EA	RW
	2B			6B		SARADC_CR2	AB	#	ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW	SARADC_LCR	AC	RW		EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Gray fields are reserved. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C23433 PSoC device. For up-to-date latest electrical specifications, visit http://www.cypress.com.

Specifications are valid for –40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

Refer to Table 23 on page 31 for the electrical specifications for the IMO using SLIMO mode.

Figure 6. Voltage versus CPU Frequency

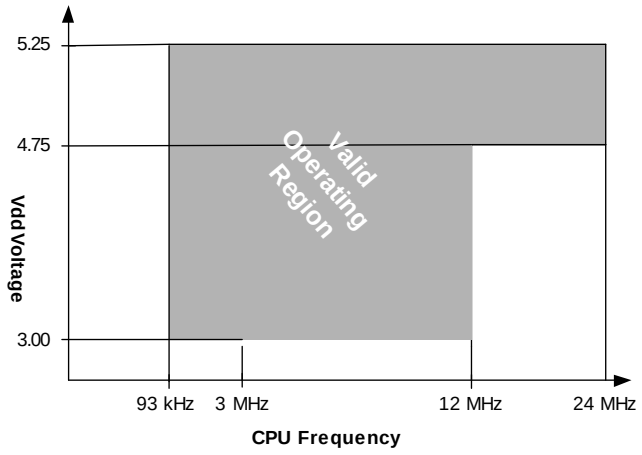
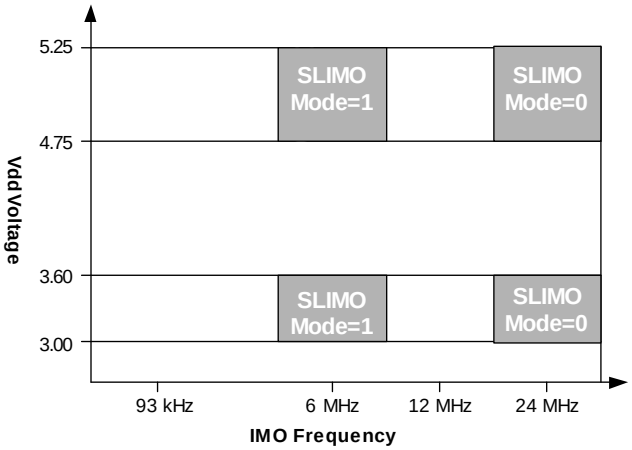


Figure 8. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
Vdd	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 37 on page 42. You must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 9. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.0	–	5.25	V	See Table 19 on page 28.
I_{DD}	Supply current	–	5	8	mA	Conditions are V_{DD} = 5.0V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{DD3}	Supply current	–	3.3	6.0	mA	Conditions are V_{DD} = 3.3V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{SB}	Sleep (mode) current with POR, LVD, Sleep Timer, and WDT.[8]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3V, –40°C ≤ T_A ≤ 55°C, analog power = off.
I_{SBH}	Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature.[8]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55°C < T_A ≤ 85°C, analog power = off.
I_{SBXTL}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and external crystal.[8]	–	4	7.5	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3V, –40°C ≤ T_A ≤ 55°C, analog power = off.
I_{SBXTLH}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature.[8]	–	5	26	µA	Conditions are with properly loaded, 1µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, 55°C < T_A ≤ 85°C, analog power = off.
V_{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} > 3.0V

Note
8. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC General-Purpose I/O Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3V at 25°C and are for design guidance only.

Table 10. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} - 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 100 mA maximum combined I_{OH} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD}-1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25
V_H	Input hysterisis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C

DC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

The Operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched cap PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block. Typical parameters apply to 5 V at 25°C and are for design guidance only.

Table 11. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB – –	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – –	 300 600 1200 2400 4600	 400 800 1600 3200 6400	 µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	V_{SS} ≤ VIN ≤ (V_{DD} - 2.25) or (V_{DD} - 1.25V) ≤ VIN ≤ V_{DD}

Table 12. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low Opamp bias. For high Opamp bias mode (except high power, high Opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 mA mA mA mA mA mA	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	V_{SS} £ V_{IN} £ (V_{DD} – 2.25) or (V_{DD} – 1.25 V) £ V_{IN} £ V_{DD}

DC Low Power Comparator Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1.0	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

DC Analog Output buffer specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 0.5 x V_{DD} + 1.1 0.5 x V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 x V_{DD} - 1.3 0.5 x V_{DD} - 1.3	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} >(V_{DD} - 1.25)

Table 15. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 1k ohms to V_{DD}/2) Power = low Power = high	 0.5 x V_{DD} + 1.0 0.5 x V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1k ohms to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 x V_{DD} - 1.0 0.5 x V_{DD} - 1.0	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} - 1.25)

DC Analog Reference Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the analog continuous time PSoC block. The power levels for RefHi and RefLo refer to the analog reference control register. The limits stated for AGND include the offset error of the AGND buffer local to the analog continuous time PSoC block. reference control power is high.

Table 16. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.136	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.409	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.138	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.132	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.417	$V_{DD}/2$ – 1.289	$V_{DD}/2$ – 1.154	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.358	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.055	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.369	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.218	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.211	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.357	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$	$V_{DD}/2$ + 0.052	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.224	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.215	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.353	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.225	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.076	P2[4] + P2[6] – 0.021	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.025	P2[4] – P2[6] + 0.011	P2[4] – P2[6] + 0.085	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.069	P2[4] + P2[6] – 0.014	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.052	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.048	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.039	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.121	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.019	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.083	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.016	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.075	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.032	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.074	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.032	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
0b011	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.753	3.874	3.979	V
		V_{AGND}	AGND	2 × Bandgap	2.511	2.590	2.657	V
		V_{REFLO}	Ref Low	Bandgap	1.243	1.297	1.333	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.767	3.881	3.974	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.592	2.652	V
		V_{REFLO}	Ref Low	Bandgap	1.241	1.295	1.330	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	2.771	3.885	3.979	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.593	2.649	V
		V_{REFLO}	Ref Low	Bandgap	1.240	1.295	1.331	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.771	3.887	3.977	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.594	2.648	V
		V_{REFLO}	Ref Low	Bandgap	1.239	1.295	1.332	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b100	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.481 + P2[6]	2.569 + P2[6]	2.639 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.511	2.590	2.658	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.515 – P2[6]	2.602 – P2[6]	2.654 – P2[6]	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.498 + P2[6]	2.579 + P2[6]	2.642 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.592	2.652	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.598 – P2[6]	2.650 – P2[6]	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.504 + P2[6]	2.583 + P2[6]	2.646 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.592	2.650	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.596 – P2[6]	2.649 – P2[6]	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.586 + P2[6]	2.648 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.594	2.648	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.595 – P2[6]	2.648 – P2[6]	V
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.228	P2[4] + 1.284	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.358	P2[4] – 1.293	P2[4] – 1.226	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.236	P2[4] + 1.289	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.357	P2[4] – 1.297	P2[4] – 1.229	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.237	P2[4] + 1.291	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.356	P2[4] – 1.299	P2[4] – 1.232	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.237	P2[4] + 1.292	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.357	P2[4] – 1.300	P2[4] – 1.233	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.512	2.594	2.654	V
		V_{AGND}	AGND	Bandgap	1.250	1.303	1.346	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.027	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.592	2.654	V
		V_{AGND}	AGND	Bandgap	1.253	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.02	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.518	2.593	2.651	V
		V_{AGND}	AGND	Bandgap	1.254	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.517	2.594	2.650	V
		V_{AGND}	AGND	Bandgap	1.255	1.300	1.337	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.011	4.143	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.075	2.118	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.026	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.022	4.138	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.026	4.141	4.207	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.030	4.143	4.206	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.076	2.112	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.013	V

Table 17. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.170	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.376	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.098	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.097	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.386	$V_{DD}/2$ – 1.287	$V_{DD}/2$ – 1.169	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.210	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.355	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.054	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.359	$V_{DD}/2$ – 1.292	$V_{DD}/2$ – 1.214	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.198	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.368	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.041	$V_{DD}/2$	$V_{DD}/2$ + 0.04	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.362	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.220	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.364	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.033	$V_{DD}/2$	$V_{DD}/2$ + 0.030	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.364	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.222	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.048	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.066	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.034	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.053	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.028	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.033	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.056	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6]	P2[4] – P2[6] + 0.032	V

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.102	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.039	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.020	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.082	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.031	$V_{DD}/2$	$V_{DD}/2$ + 0.028	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.083	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.032	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.081	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.033	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.013	V
0b011	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–
0b100	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.211	P2[4] + 1.285	P2[4] + 1.348	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.354	P2[4] – 1.290	P2[4] – 1.197	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.209	P2[4] + 1.289	P2[4] + 1.353	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.352	P2[4] – 1.294	P2[4] – 1.222	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.218	P2[4] + 1.291	P2[4] + 1.351	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.351	P2[4] – 1.296	P2[4] – 1.224	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.215	P2[4] + 1.292	P2[4] + 1.354	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.352	P2[4] – 1.297	P2[4] – 1.227	V

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.460	2.594	2.695	V
		V_{AGND}	AGND	Bandgap	1.257	1.302	1.335	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.01	V_{SS} + 0.029	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.462	2.592	2.692	V
		V_{AGND}	AGND	Bandgap	1.256	1.301	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.473	2.593	2.682	V
		V_{AGND}	AGND	Bandgap	1.257	1.301	1.330	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.014	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.470	2.594	2.685	V
		V_{AGND}	AGND	Bandgap	1.256	1.300	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
0b111	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and–40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ
C_{SC}	Capacitor unit value (switch cap)	–	80[9]	–	fF

DC POR and LVD Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Mixed-Signal Array Technical Reference Manual* for more information on the VLT_CR register.

Table 19. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR1} V_{PPOR2}	V_{DD} value for PPOR trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.55	2.95 4.70	V V	V_{DD} must be greater than or equal to 2.5 V during startup or reset from watchdog.
V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd value for LVD trip VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.85 2.95 3.06 4.37 4.50 4.62 4.71	2.92 3.02 3.13 4.48 4.64 4.73 4.81	2.99[10] 3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V V	

Notes
9. C_{SC} is a design guarantee parameter, not tested value
10. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.

DC Programming Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 20. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input current when applying vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} - 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total)[11]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 21. DC I^2C Specifications[12]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Notes

11. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to 0xthe Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
12. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

SAR8 ADC DC Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 22. SAR8 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{ADCVREF}$	Reference voltage at pin P3[0] when configured as ADC reference voltage	3.0	–	5.25	V	The voltage level at P3[0] (when configured as ADC reference voltage) must always be maintained to be less than chip supply voltage level on V_{DD} pin. $V_{ADCVREF} < V_{DD}$.
$I_{ADCVREF}$	Current when P3[0] is configured as ADC V_{REF}	3	–	–	mA	
INL	Integral non-linearity	–1.5	–	+1.5	LSB	
INL (limited range)	Integral non-linearity accommodating a shift in the offset at 0x80	–1.2[12]	–	+1.2	LSB	The maximum LSB is over a sub-range not exceeding 1/16 of the full-scale range. 0x7F and 0x80 points specs are excluded here
DNL	Differential non-linearity	–2.3	–	+2.3	LSB	ADC conversion is monotonic over full range
DNL (limited range)	Differential non-linearity excluding 0x7F-0x80 transition	–1	–	+1	LSB	ADC conversion is monotonic over full range. 0x7F to 0x80 transition specs are excluded here.

Note

12. SAR converters require a stable input voltage during the sampling period. If the voltage into the SAR8 changes by more than 1 LSB during the sampling period then the accuracy specifications may not be met

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 23. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal main oscillator frequency for 24 MHz	23.4	24	24.6[13],[14],[15]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8 on page 14. SLIMO mode = 0.
F_{IMO6}	Internal main oscillator frequency for 6 MHz	5.5	6	6.5[13],[14],[15]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8 on page 14. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5-V nominal)	0.093	24	24.6[13],[14]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3-V nominal)	0.093	12	12.3[13],[14]	MHz	SLIMO mode = 0.
F_{48M}	Digital PSoC block frequency	0	48	49.2[13],[14],[16]	MHz	Refer to the AC digital block Specifications.
F_{24M}	Digital PSoC block frequency	0	24	24.6[14],[16]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	75	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the system resets section of the PSoC technical reference manual for details on timing this
F_{PLL}	PLL frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
$T_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	
T_{OS}	External crystal oscillator startup to 1%	–	1700	2620	ms	
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V £ V_{DD} £ 5.5V, –40 °C £ T_A £ 85°C.
T_{XRST}	External reset pulse width	10	–	–	ms	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[13],[15]	MHz	Trimmed. Using factory trim values.

Notes

13. 4.75V < Vdd < 5.25V.
14. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
15. 3.0V < Vdd < 3.6V.
16. See the individual user module data sheets for information on maximum frequencies for user modules.
17. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Table 23. 5-V and 3.3-V AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0V. See the System Resets section of the PSoC technical reference manual.
t_{jit_IMO} [17]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{jit_PLL} [17]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	700	ps	

Figure 9. PLL Lock Timing Diagram

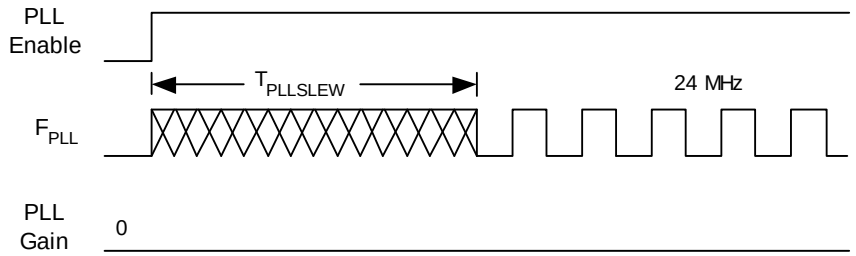


Figure 10. PLL Lock for Low Gain Setting Timing Diagram

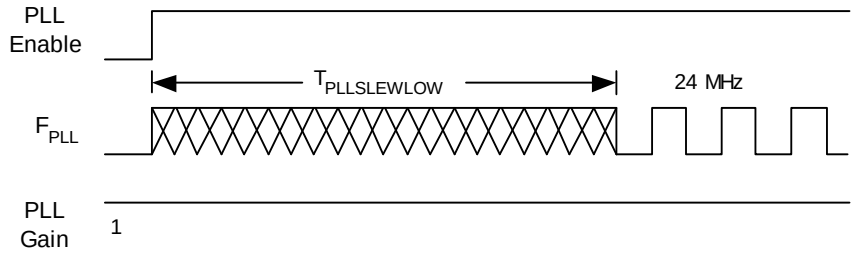
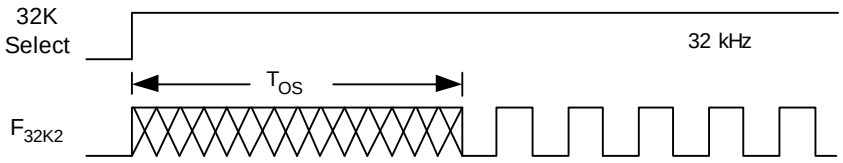


Figure 11. External Crystal Oscillator Startup Timing Diagram



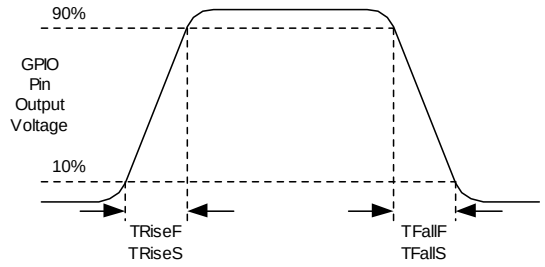
AC GPIO Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 24. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.3	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 V to 5.25 V, 10% - 90%
TFallF	Fall time, normal strong mode, cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 V to 5.25 V, 10% - 90%
TRiseS	Rise time, slow strong mode, cload = 50 pF	10	27	–	ns	V_{DD} = 3 V to 5.25 V, 10% - 90%
TFallS	Fall time, slow strong mode, cload = 50 pF	10	22	–	ns	V_{DD} = 3 V to 5.25 V, 10% - 90%

Figure 12. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V.

Table 25. 5-V AC Operational Amplifier Specifications

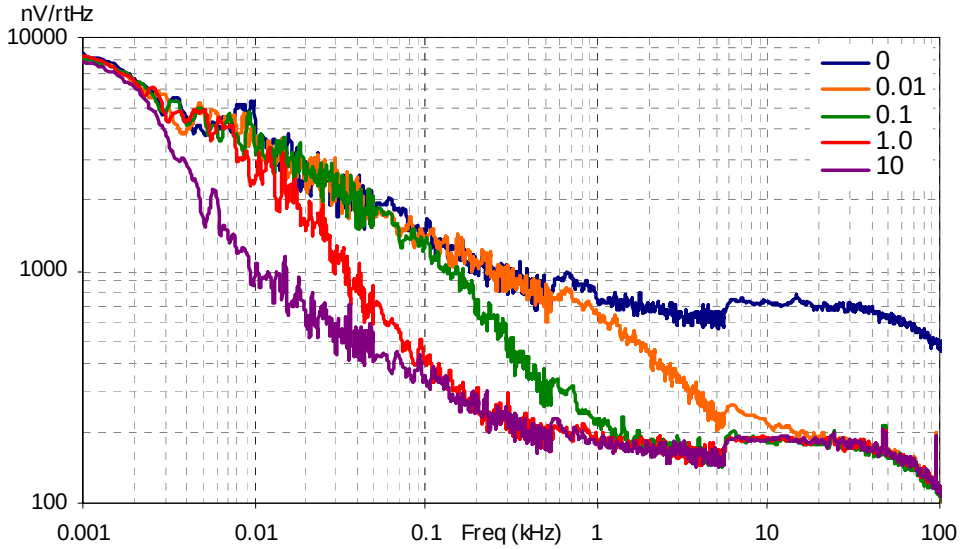
Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
T_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz

Table 26. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 3.92 0.72	 µs µs
T_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.67 2.8	 – –	 – –	 MHz MHz

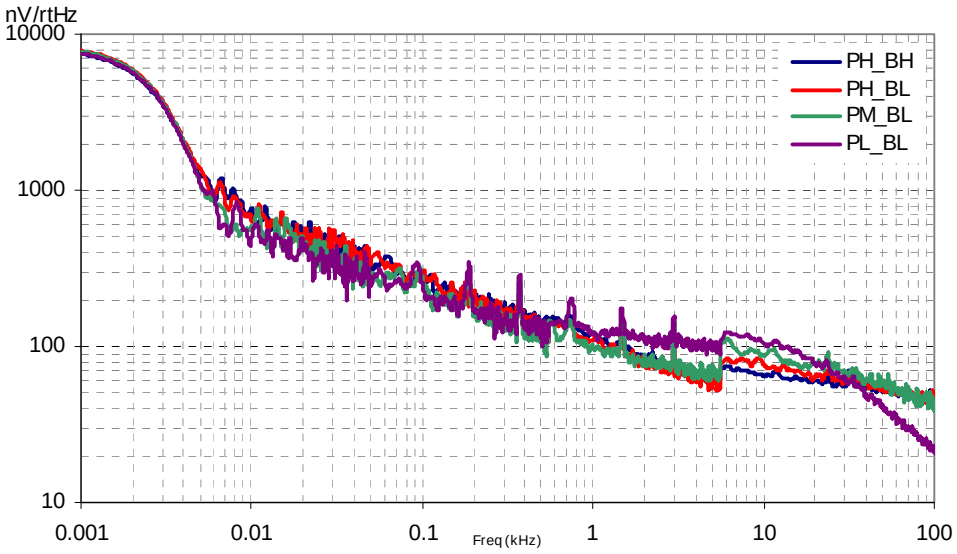
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 13. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 14. Typical Opamp Noise



AC Low Power Comparator Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 27. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	ms	[3] 50 mV overdrive comparator reference set within V_{REFLPC}

AC Digital Block Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 28. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[18]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[18]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[18]	–	–	ns	
	Disable mode	50[18]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[18]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note
18. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 29. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs
T_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz

Table 30. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs
T_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 2.6 2.6	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 31. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power up IMO to switch	150	–	–	µs

Table 32. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU clock divide by 1[19]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[20]	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power up IMO to switch	150	–	–	µs

AC Programming Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 33. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall time of SCLK	1	–	20	ns	
T_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash erase time (block)	–	20	–	ms	
T_{WRITE}	Flash block write time	–	20	–	ms	
T_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
T_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \le V_{DD} \le 3.6$
$T_{ERASEALL}$	Flash erase time (bulk)	–	80	–	ms	Erase all Blocks and protection fields at once
$T_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100[22]	ms	0 °C <= Tj <= 100°C
$T_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200[22]	ms	–40 °C <= Tj <= 0 °C

Notes
19. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
20. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
21. The max sample rate in this R2R ADC is 3.0/8=375KSPS
22. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

SAR8 ADC AC Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 34. SAR8 ADC AC Specifications[21]

Symbol	Description	Min	Typ	Max	Units
$Freq_3$	Input clock frequency 3 V	–	–	3.075	MHz
$Freq_5$	Input clock frequency 5 V	–	–	3.075	MHz

AC I^2C Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 35. AC Characteristics of the I^2C SDA and SCL Pins for V_{DD} > 3.0 V

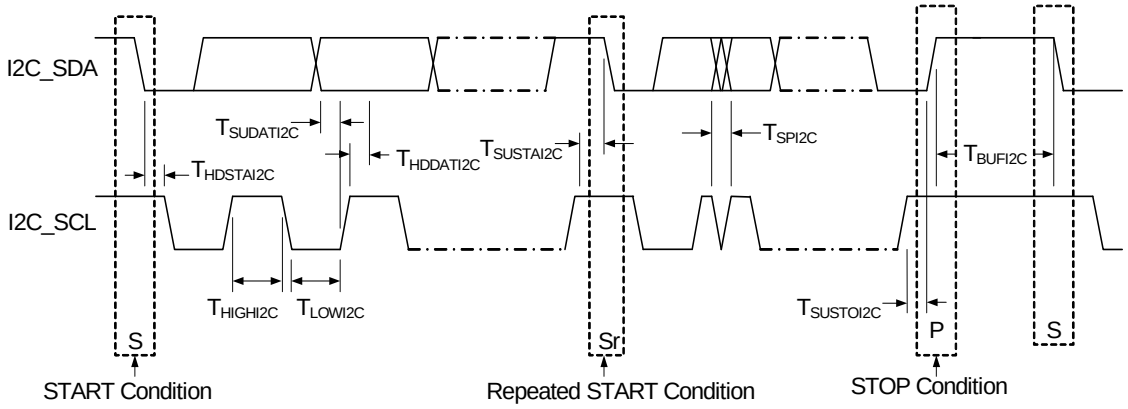
Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[23]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Note
23. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Table 36. AC Characteristics of the I²C SDA and SCL Pins for $V_{DD} < 3.0$ V (Fast Mode Not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	–	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	–	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	–	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	–	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns

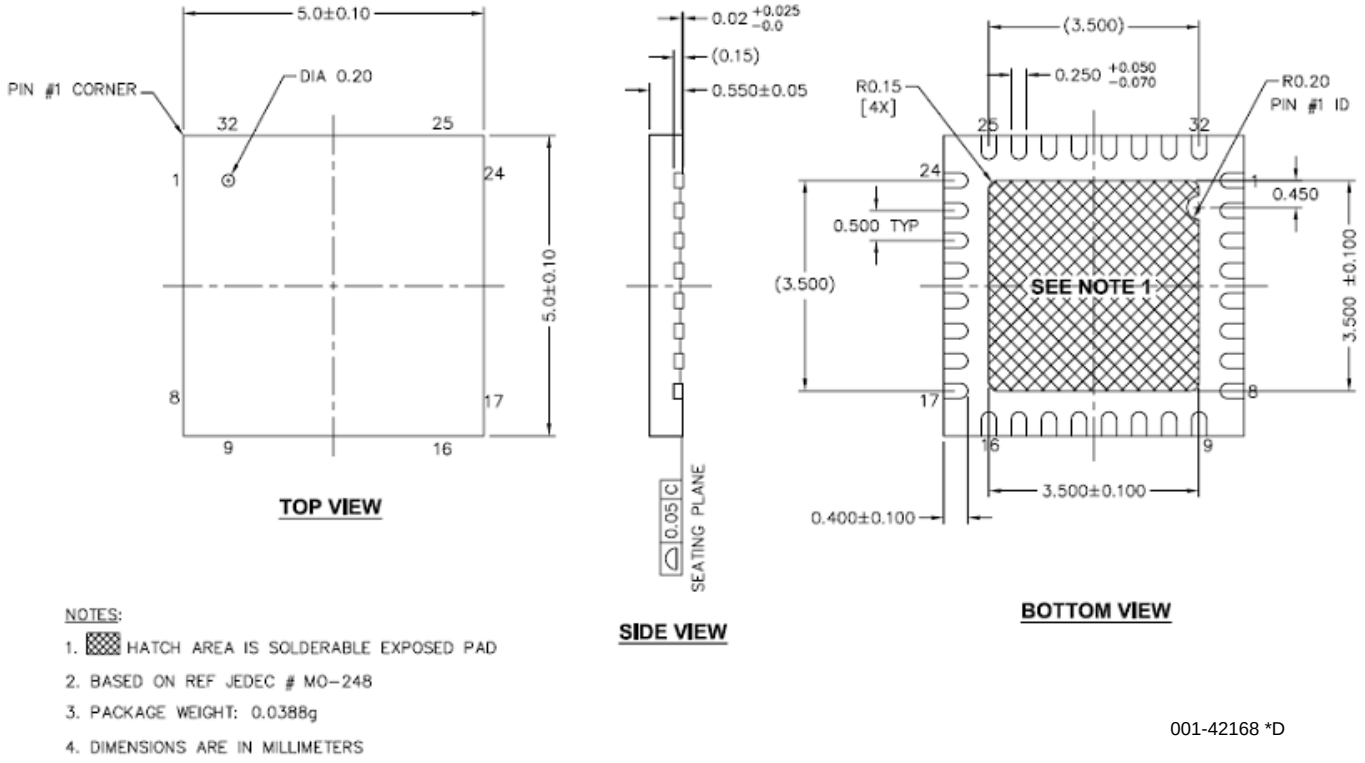
Figure 15. Definition for Timing for Fast/Standard Mode on the I²C Bus



Packaging Information

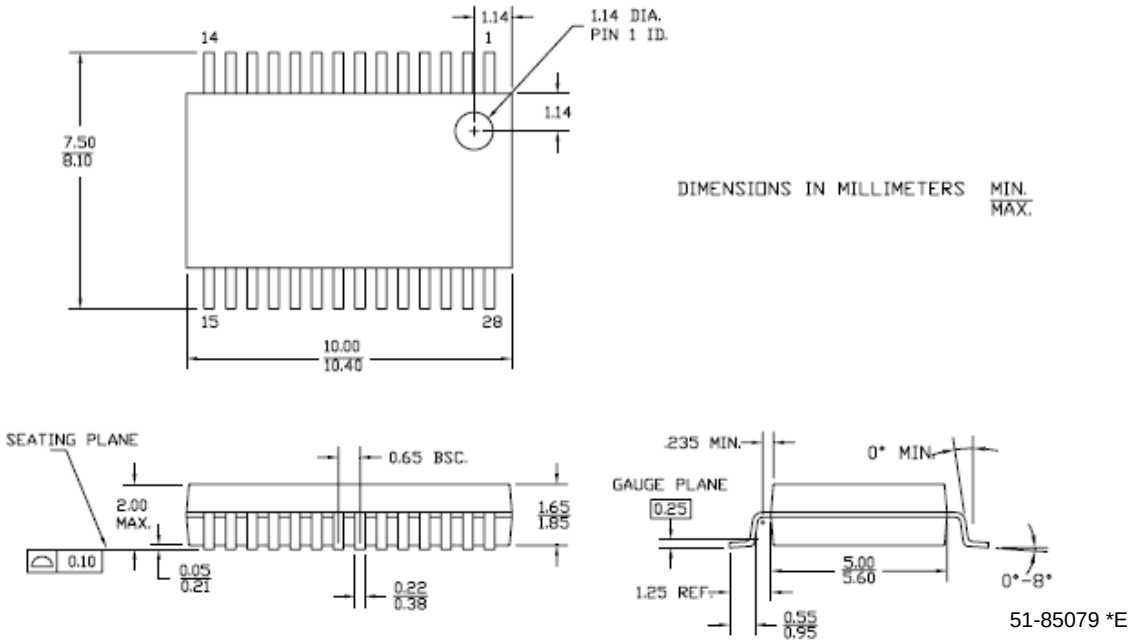
This section illustrates the packaging specifications for the CY8C23x33 PSoC device, along with the thermal impedances for each package, solder reflow peak temperature, and the typical package capacitance on crystal pins.

Figure 16. 32-Pin (5x5 mm) QFN



001-42168 *D

Figure 17. 28-Pin (210-Mil) SSOP



Thermal Impedances

Table 37. Thermal Impedances by Package

Package	Typical θ_{JA} [22]
32 QFN	19.4 °C/W
28 SSOP	95 °C/W

Capacitance on Crystal Pins

Table 38. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 QFN	2.0 pF
28 SSOP	2.8 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 39. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
32 QFN	260 °C	30 s
28 SSOP	260 °C	30 s

Note
22. $T_J = T_A + POWER \times \theta_{JA}$.

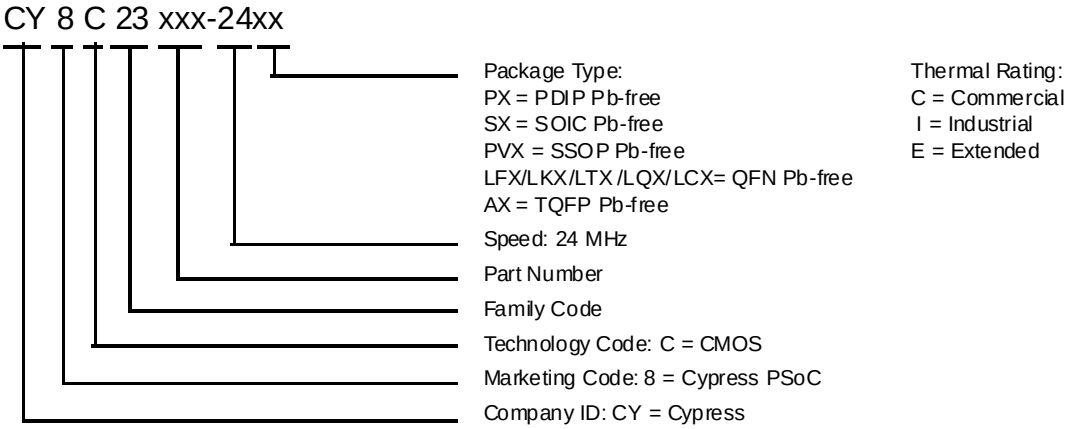
Ordering Information

The following table lists the CY8C23X33 PSoC device family key package features and ordering codes.

Table 40. CY8C23X33 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
32 Pin QFN	CY8C23533-24LQXI	8	256	–40 °C to +85 °C	4	4	26	12	2	Yes
32 Pin QFN (Tape and Reel)	CY8C23533-24LQXIT	8	256	–40 °C to +85 °C	4	4	26	12	2	Yes
28 Pin (210 Mil) SSOP	CY8C23433-24PVXI	8	256	–40 °C to +85 °C	4	4	26	12	2	No
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C23433-24PVXIT	8	256	–40 °C to +85 °C	4	4	26	12	2	No

Ordering Code Definitions



Acronyms

Acronyms Used

Table 41 lists the acronyms that are used in this document.

Table 41. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	PCB	printed circuit board
API	application programming interface	PGA	programmable gain amplifier
CPU	central processing unit	PLL	phase-locked loop
CRC	cyclic redundancy check	POR	power on reset
CT	continuous time	PPOR	precision power on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DNL	differential nonlinearity	PWM	pulse width modulator
DTMF	dual-tone multi-frequency	QFN	quad flat no leads
ECO	external crystal oscillator	RTC	real time clock
EEPROM	electrically erasable programmable read-only memory	SAR	successive approximation
GPIO	general purpose I/O	SC	switched capacitor
ICE	in-circuit emulator	SLIMO	slow IMO
IDE	integrated development environment	SMP	switch mode pump
ILO	internal low speed oscillator	SOIC	small-outline integrated circuit
IMO	internal main oscillator	SPI™	serial peripheral interface
INL	integral nonlinearity	SRAM	static random access memory
I/O	input/output	SROM	supervisory read only memory
IrDA	infrared data association	SSOP	shrink small-outline package
ISSP	in-system serial programming	UART	universal asynchronous reciever / transmitter
LPC	low power comparator	USB	universal serial bus
LVD	low voltage detect	WDT	watchdog timer
MAC	multiply-accumulate	XRES	external reset
MCU	microcontroller unit		

Reference Documents

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Document Conventions

Units of Measure

Table 42 lists the unit sof measures.

Table 42. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	ms	millisecond
dB	decibels	ns	nanosecond
°C	degree Celsius	ps	picosecond
fF	femto farad	µV	microvolts
pF	picofarad	mV	millivolts
kHz	kilohertz	mVpp	millivolts peak-to-peak
MHz	megahertz	nV	nanovolts
LSB	least significant bit	V	volts
kΩ	kilohm	µW	microwatts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
µs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	5. A logic signal having its asserted state as the logic 1 state. 6. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.

Glossary (continued)

compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.

Glossary (continued)

ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device*.**
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.

Glossary (continued)

port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.

Glossary (continued)

tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C23433, CY8C23533 PSoC® Programmable System-on-Chip™ Document Number: 001-44369				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2044848	KIY/AESA	01/30/2008	Data sheet creation
*A	2482967	HMI/AESA	05/14/2008	Moved from Preliminary to Final. Part number changed to CY8C23433, CY8C23533. Adjusted placement of the block diagram; updated description of DAC; updated package pinout description, updated POR and LVD spec, Added Csc , Flash Vdd, SAR ADC spec. Updated package diagram 001-42168 to *A. Updated data sheet template.
*B	2616862	OGNE/AESA	12/05/2008	Changed title to: “CY8C23433, CY8C23533 PSoC® Programmable System-on-Chip™” Updated package diagram 001-42168 to *C. Changed names of registers on page 11. "SARADC_C0" to "SARADC_CR0" "SARADC_C1" to "SARADC_CR1"
*C	2883928	JVY	02/24/2010	Updated the following parameters: DC_{ILO}, $SR_{POWERUP}$, F32K_U, F_{IMO6}, $T_{POWERUP}$, T_{ERASE_ALL}, $T_{PROGRAM\_HOT}$, $T_{PROGRAM\_COLD}$ Updated package diagrams Added Table of Contents
*D	3118801	NJF	12/23/10	Updated PSoC Device Characteristics table . Added DC I^2C Specifications table. Added Tjit_IMO specification, removed existing jitter specifications. Updated 3.3 V operational amplifier specifications and DC analog reference specifications tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Added ordering code definitions.
*E	3283782	SHOB	08/16/11	Updated Getting Started, Development Tools and Designing with PSoC Designer. Updated Solder Reflow Peak Temperature Removed reference to obsolete Application Note AN2012.
*F	3598316	LURE/XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.

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