

**600V ACTIVE OR'ING MOSFET CONTROLLER IN SO7**

**Description**

The ZXGD3114N7 is a 600V active ORing MOSFET controller designed for driving a very-low  $R_{DS(ON)}$  power MOSFET as an ideal diode. This replaces the standard rectifier to reduce the forward voltage drop and overall increase the power transfer efficiency.

The ZXGD3114N7 can be used on both high-side and low-side power supply units (PSU) with rails up to  $\pm 600V$ . It enables very-low  $R_{DS(ON)}$  MOSFETs to operate as ideal diodes as the turn-off threshold is only -3mV with  $\pm 2mV$  tolerance. In the typical 48V configuration, the standby power consumption is <50mW as the low quiescent supply current is <1mA. During PSU fault condition, the ORing controller detects the power reduction and rapidly turns off the MOSFET in <600ns to block reverse current flow and avoid the common bus voltage dropping.

**Applications**

Active ORing Controller in:

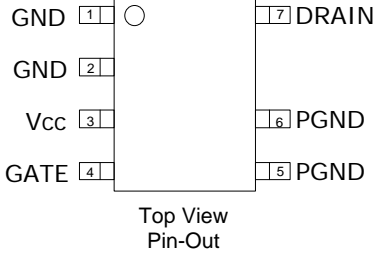
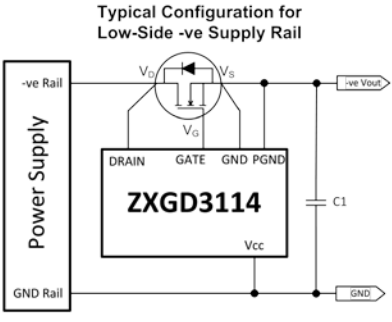
- (N + 1) Redundant Power Supplies
- Telecom and Networking
- Data Centers and Servers

**Features**

- Active ORing MOSFET Controller for High- or Low-Side PSU
- Ideal Diode to Reduce Forward Voltage Drop
- -3mV Typical Turn-Off Threshold with  $\pm 2mV$  Tolerance
- 600V Drain Voltage Rating
- 25V  $V_{CC}$  Rating
- <50mW Standby Power with Quiescent Supply Current <1mA
- <600ns Turn-Off Time to Minimize Reverse Current
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

**Mechanical Data**

- Case: SO-7
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (Approximate)

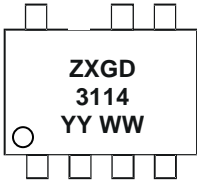


**Ordering Information (Note 4)**

Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
ZXGD3114N7TC	ZXGD3114	13	12	2500

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



ZXGD = Product Type Marking Code, Line 1  
 3114 = Product Type Marking Code, Line 2  
 YY = Year (ex: 17 = 2017)  
 WW = Week (01 to 53)



**Pin Functions**

Pin Number	Pin Name	Pin Function and Description
1, 2	GND	<b>Ground</b> Connect this pin to the MOSFET source terminal and ground reference point.
3	V <sub>CC</sub>	<b>Power Supply</b> This supply pin should be closely decoupled to ground with a X7R type capacitor.
4	GATE	<b>Gate Drive</b> This pin sources (I <sub>SOURCE</sub> ) and sinks (I <sub>SINK</sub> ) current into the MOSFET gate. If V <sub>CC</sub> > 12V, then the GATE-to-GND will clamp at 12V. The turn on time of the MOSFET can be programmed through an external gate resistor (R <sub>G</sub> ).
5, 6	PGND	<b>Power Ground</b> Connect this pin to the MOSFET source terminal and ground reference point.
7	DRAIN	<b>Drain Sense</b> Connect this pin to the MOSFET drain terminal to detect the change in drain-source voltage.

**Absolute Maximum Ratings** (Voltage relative to GND, @ T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	25	V
Drain Pin Voltage	V <sub>D</sub>	-3 to 600	V
Gate Output Voltage**	V <sub>G</sub>	-3 to V <sub>CC</sub> + 3	V
Gate Driver Peak Source Current	I <sub>SOURCE</sub>	2	A
Gate Driver Peak Sink Current	I <sub>SINK</sub>	5	A

\*\*Gate voltage is clamped to 12V.

**Thermal Characteristics**

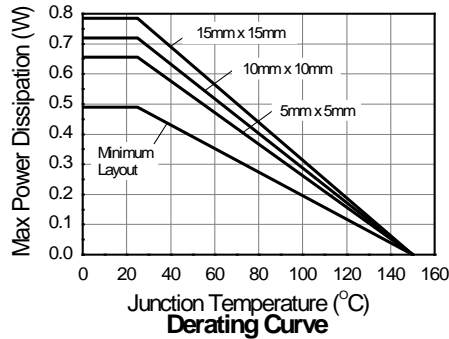
Characteristic	Symbol	Value	Unit	
Power Dissipation Linear Derating Factor	P <sub>D</sub>	490	mW mW/°C	
		(Note 5)		3.92
		(Note 6)		655
		(Note 7)		5.24
		(Note 8)		720
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	785	°C/W	
		(Note 5)		6.28
		(Note 6)		255
		(Note 7)		191
(Note 8)	173			
(Note 9)	159			
Thermal Resistance, Junction to Lead	R <sub>θJL</sub>	135	°C/W	
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-50 to +150	°C	

**ESD Ratings** (Note 10)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge—Human Body Model	ESD HBM	2000	V	3A
Electrostatic Discharge—Machine Model	ESD MM	200	V	B

- Notes:
- For a device surface mounted on minimum recommended pad layout FR-4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  - Same as Note 5, except pin 3 (V<sub>CC</sub>) and pins 5 & 6 (PGND) are both connected to separate 5mm x 5mm 1oz copper heat-sinks.
  - Same as Note 6, except both heat-sinks are 10mm x 10mm.
  - Same as Note 6, except both heat-sinks are 15mm x 15mm.
  - Thermal resistance from junction to solder-point at the end of each lead on pins 2 & 3 (GND) and pins 5 & 6 (V<sub>CC</sub>).
  - Refer to JEDEC specification JESD22-A114 and JESD22-A115.

## Thermal Derating Curve



## Electrical Characteristics (@ $V_{CC} = 12V$ , $T_A = +25^\circ C$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>Input Supply</b>						
Operating Supply Voltage	$V_{CC}$	4	—	20	V	—
Quiescent Current	$I_Q$	—	260	400	$\mu A$	$-0.6V \leq V_{DRAIN} \leq 600V$
Drain Low Input Current	$I_{DL}$	-100	-15	—	nA	$V_D = -0.1V$
Drain High Input Current	$I_{DH}$	—	0.85	10	$\mu A$	$V_D = 600V$
<b>Gate Driver</b>						
Gate Peak Source Current	$I_{SOURCE}$	—	0.66	—	A	$C_L = 47nF$
Gate Peak Sink Current	$I_{SINK}$	—	3.3	—		
Gate Peak Source Current (Note 11)	$I_{SOURCE}$	1	—	—	A	$V_{GATE} = 5V$ & $V_{DRAIN} = -1V$
Gate Peak Sink Current (Note 11)	$I_{SINK}$	1.8	—	—	A	$V_{GATE} = 5V$ & $V_{DRAIN} = 1V$
<b>Detector Under DC Condition</b>						
Turn-Off Threshold Voltage	$V_T$	-5	-3	-1	mV	$V_G \leq 1V$
Gate Output Voltage	$V_{G(OFF)}$	—	0.1	0.3	V	$V_{DRAIN} \geq 0mV$ & $V_{CC} = 12V$
	$V_G$	10.5	10.85	—		$V_{DRAIN} = -8mV$ & $V_{CC} = 12V$
	$V_{G(OFF)}$	—	0.1	0.3		$V_{DRAIN} \geq 0mV$ & $V_{CC} = 4V$
	$V_G$	2.5	2.85	—		$V_{DRAIN} = -8mV$ & $V_{CC} = 4V$
	$V_{G(OFF)}$	—	0.1	0.3		$V_{DRAIN} \geq 0mV$ & $V_{CC} = 20V$
	$V_G$	10.5	11.2	—		$V_{DRAIN} = -8mV$ & $V_{CC} = 20V$
<b>Switching Performance</b>						
Turn-On Propagation Delay	$t_{D(RISE)}$	—	400	—	ns	$C_L = 47nF$ Rise and Fall Measured 10% to 90% Refer to Application Test Circuit Below
Gate Rise Time	$t_R$	—	695	—		
Turn-Off Propagation Delay	$t_{D(FALL)}$	—	400	—		
Gate Fall Time	$t_F$	—	131	—		

Note: 11. Measured under pulsed conditions. Pulse width = 300 $\mu s$ . Duty cycle  $\leq 2\%$ .

## Layout Considerations

The GATE pin should be close to the MOSFET gate to minimize trace resistance and inductance to maximize switching performance. While the  $V_{CC}$  to GND pin requires an X7R type capacitor closely decoupling the supply. Trace widths should be maximized in the high current paths through the MOSFET and ground return in order to minimize the effects of circuit resistance and inductance. Also, the ground return loop should be as short as possible. For thermal consideration, the main heat path is from pin 3 ( $V_{CC}$ ) and pins 5 & 6 (PGND). For best thermal performance, the copper area connected to pin 3 ( $V_{CC}$ ) and pins 5 & 6 (PGND) should be maximized.

## Active ORing or (N+1) Redundancy Application

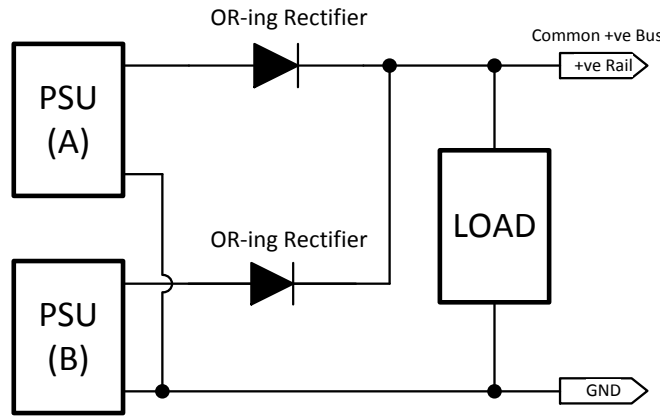


Figure 1

Critical systems require fault-tolerant power supplies that can be achieved by paralleling two or more PSUs into (N+1) redundancy configuration. During normal operation, usually all PSUs equally share the load for maximum reliability. If one of the PSU is unplugged or fails, the other PSUs fully support the load. To avoid the faulty PSU from affecting the common bus, an ORING rectifier blocks the reverse current flow into the faulty PSU. Likewise during hot-swapping, the ORING rectifiers isolate a PSU's discharged output capacitors from the common bus.

As the load current is in the tens of amps then a standard rectifier has a significant forward voltage drop. This both wastes power and significantly drops the potential on low voltage rails. Hence, very low  $R_{DS(ON)}$  power MOSFETs can replace the standard rectifiers and the ZXGD3114 controls the MOSFET as an ideal diode.

## Functional Block Diagram

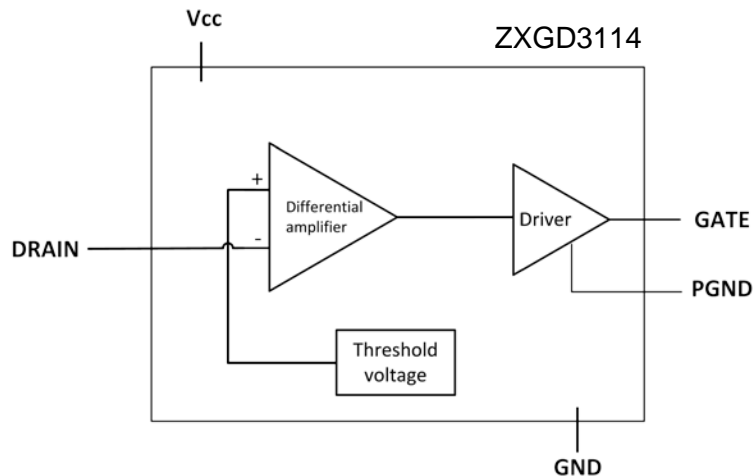
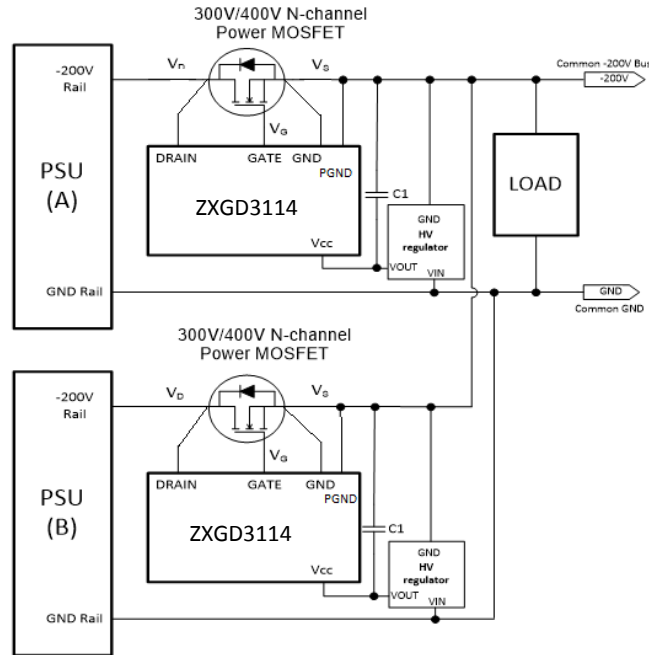


Figure 2

The device is comprised of a differential amplifier and high current driver. The differential amplifier acts as a detector and monitors the DRAIN-to-GND pin voltage difference. When this difference is less than the threshold voltage ( $V_T$ ), a positive output voltage approaching  $V_{CC}$  is given on the GATE pin. If  $V_{CC} > 12V$ , the GATE-to-GND clamps at 12V. Conversely, when the DRAIN-to-GND pin voltage difference is greater than  $V_T$ , the GATE pin voltage rapidly reduces towards the GND voltage.

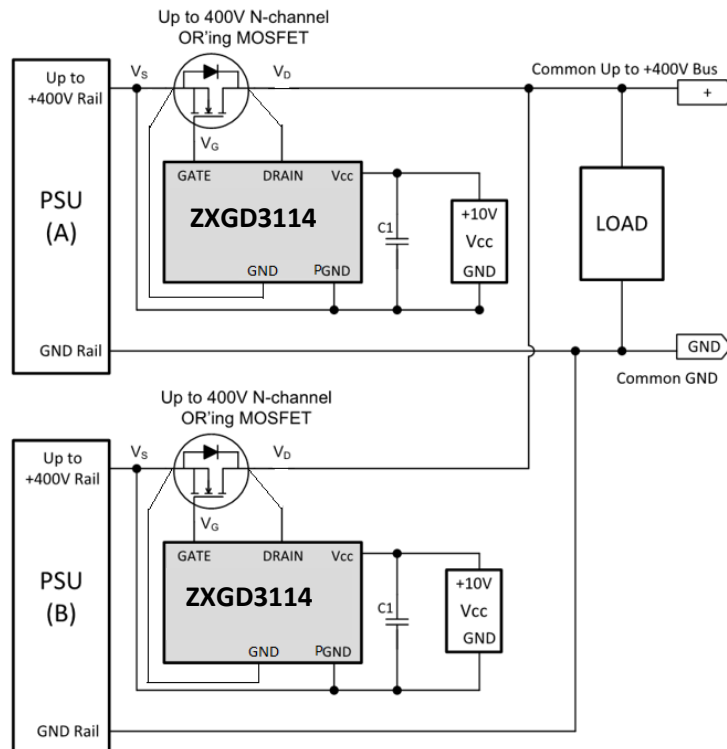
**Typical Application Circuits**

The focus application of the ZXGD3114 ORing controller is for the redundant low-side -400V power supply rail. HV to 12V regulator or a potential divider is recommended to power the V<sub>CC</sub> of ZXGD3114 from high-voltage lines (see Figure 3).



**Figure 3**

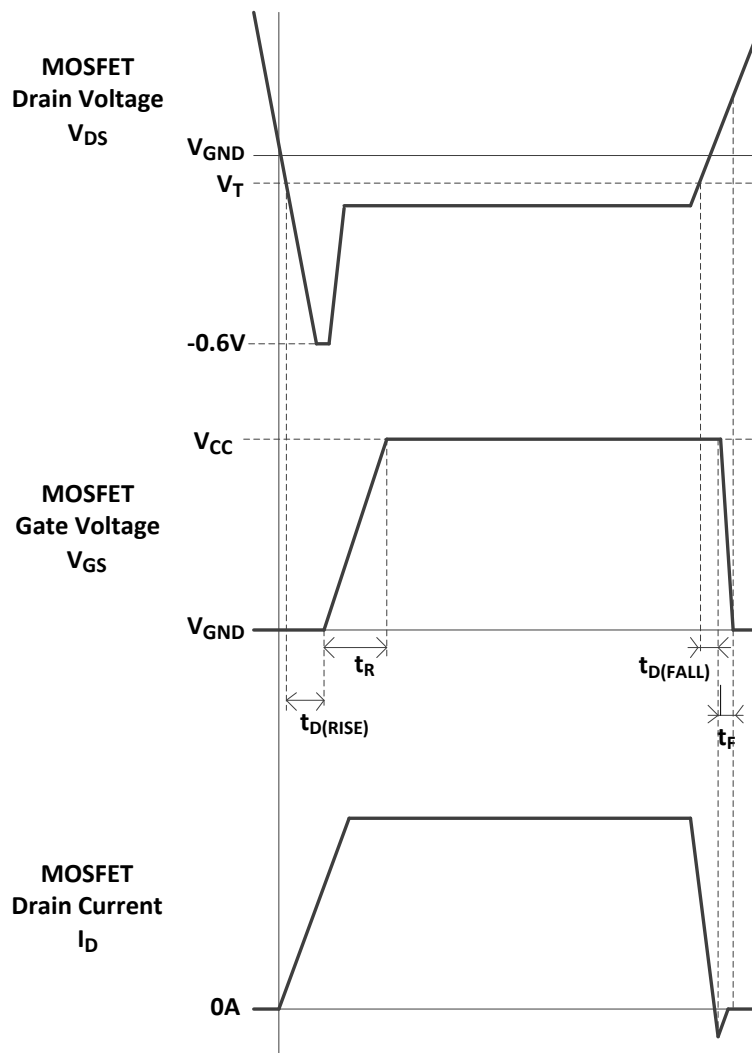
Figure 4 is an example of the ZXGD3114 ORing controller in a redundant high-side +400V power supply rail using an additional V<sub>CC</sub> supply.



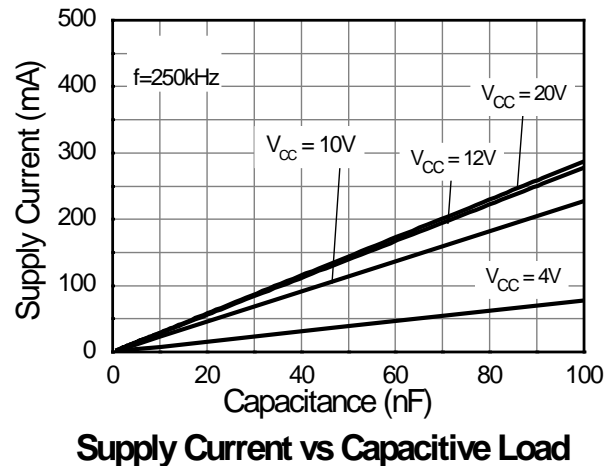
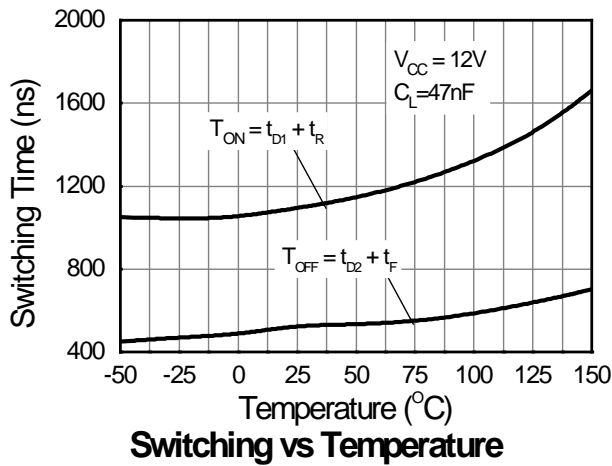
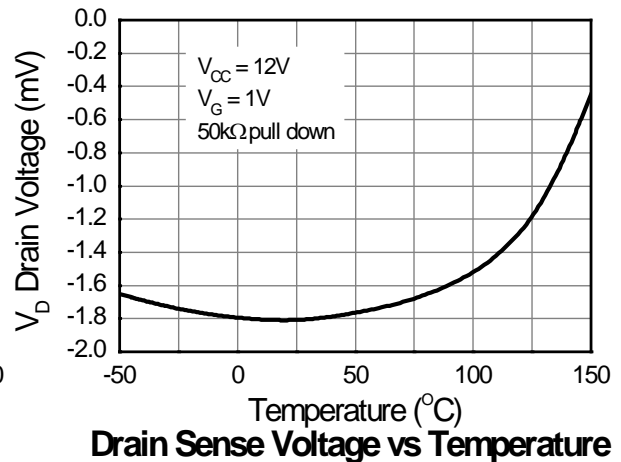
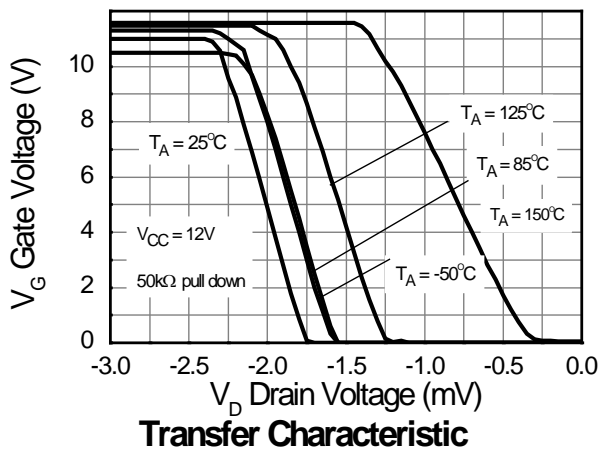
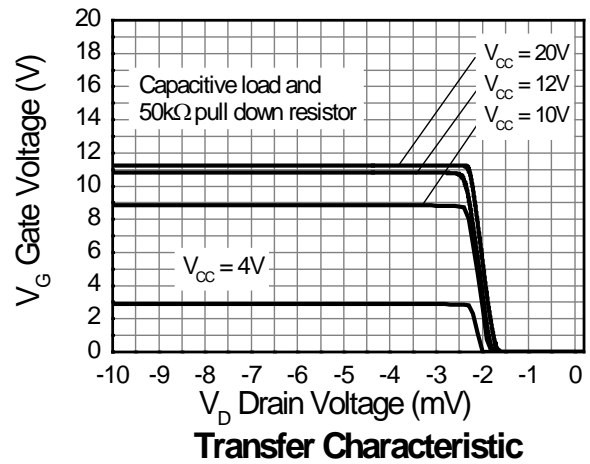
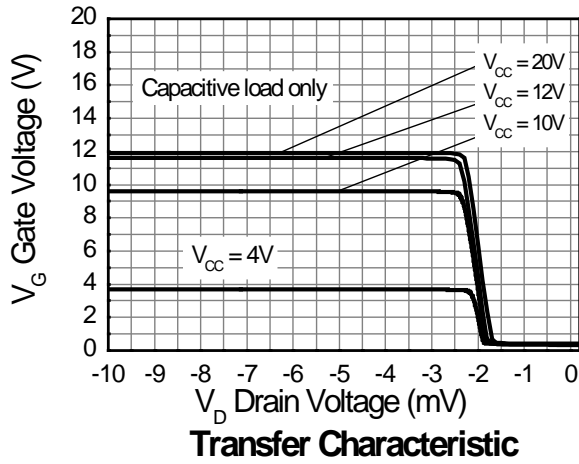
## Operation in Typical Application

The ZXGD3114 operation is described step-by-step with reference to the typical application circuits and the timing diagram below:

1. The ZXGD3114 differential amplifier monitors the MOSFET's drain-source voltage ( $V_{DS}$ ).
2. At system start up, the MOSFET body diode is forced to conduct current from the input PSU to the load, and  $V_{DS}$  is approximately  $-0.6V$  as measured by the differential amplifier between DRAIN-to-GND pins.
3.  $V_{DS} < V_T$  (threshold voltage), the differential amplifier, outputs a positive voltage approaching  $V_{CC}$  with respect to GND. This feeds the driver stage where the GATE pin voltage rises towards  $V_{CC}$ . If  $V_{CC} > 12V$ , then the GATE-to-GND clamps at  $12V$ .
4. The sourcing current out of the GATE pin drives the MOSFET gate to enhance the channel and turns it on.
5. If a short condition occurs on the input PSU, it causes the MOSFET  $V_{DS}$  to increase.
6. When  $V_{DS} > V_T$ , the differential amplifier's output goes to GND, and the driver stage rapidly pulls the GATE pin voltage to GND turning off the MOSFET channel. This prevents high reverse current flow from the load to the PSU, which could pull down the common bus voltage causing catastrophic system failure.

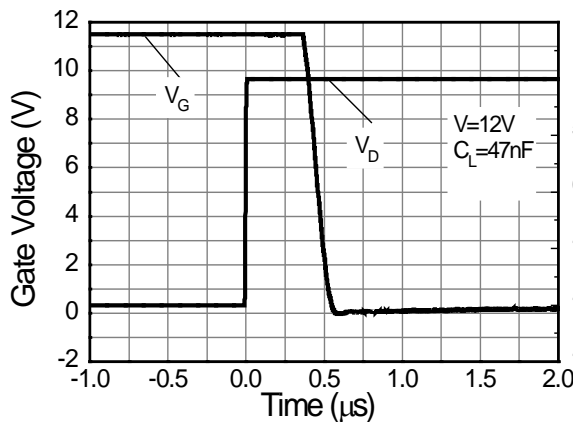


**Typical Electrical Characteristics**

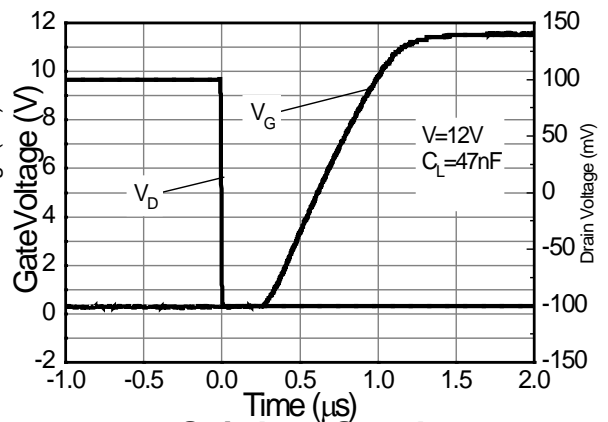




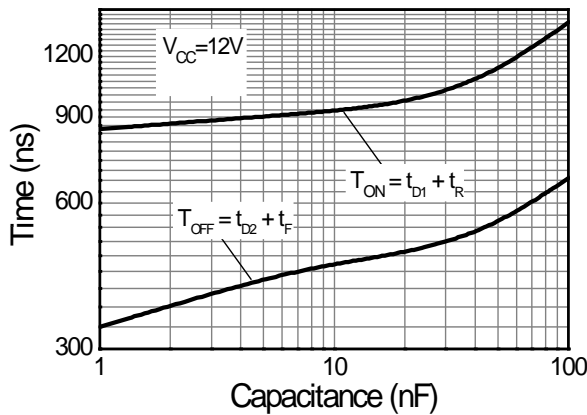
**Typical Electrical Characteristics** (continued)



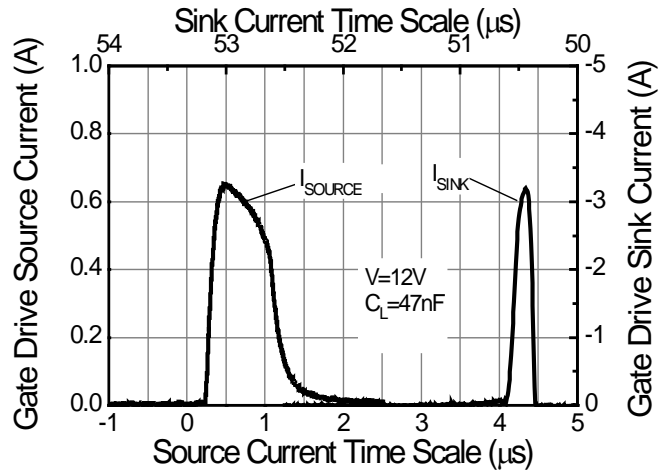
**Switch Off Speed**



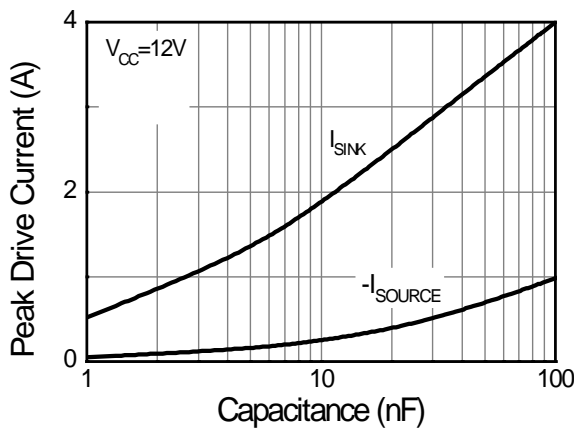
**Switch On Speed**



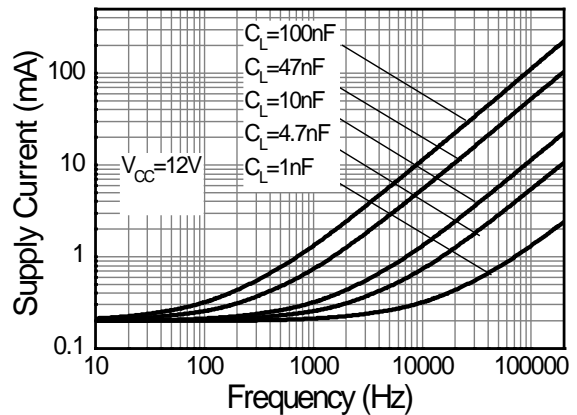
**Switching vs Capacitive Load**



**Gate Drive Current**



**Gate Current vs Capacitive Load**

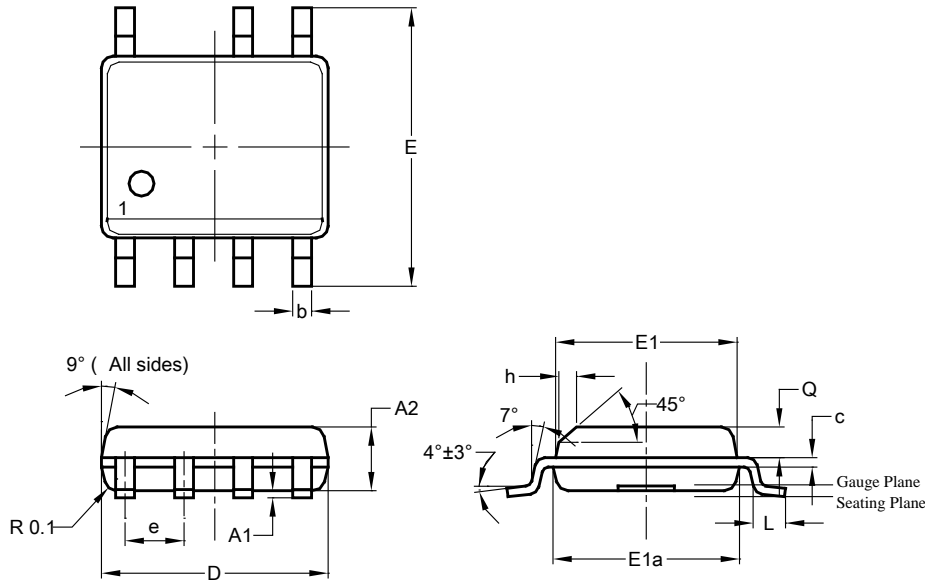


**Supply Current vs Frequency**

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-7**

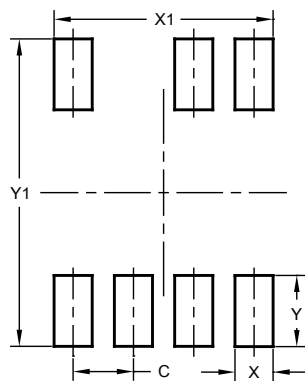


SO-7			
Dim	Min	Max	Typ
A2	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E1a	3.85	3.95	3.90
e	—	—	1.27
h	—	—	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
<b>All Dimensions in mm</b>			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-7**



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	4.612
Y	1.505
Y1	6.500

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