

## DATA SHEET

### General Description

The IDT8T49N222I is a highly flexible FemtoClock® NG general purpose, low phase noise Frequency Translator / Synthesizer with alarm and monitoring functions suitable for networking and communications applications. It is able to generate any output frequency in the 7.29MHz to 833.33MHz range and most output frequencies in the 925MHz to 1200MHz range (see Table 3A for details). A wide range of input reference clocks and a range of low-cost fundamental mode crystal frequencies may be used as the source for the output frequency.

The IDT8T49N222I has three operating modes to support a very broad spectrum of applications:

- 1) Frequency Synthesizer
  - Synthesizes output frequencies from a 16MHz - 40MHz fundamental mode crystal.
  - Fractional feedback division is used, so there are no requirements for any specific crystal frequency to produce the desired output frequency with a high degree of accuracy.
- 2) High-Bandwidth Frequency Translator
  - Applications: PCI Express, Computing, General Purpose
  - Translates any input clock in the 16MHz - 710MHz frequency range into any supported output frequency.
  - This mode has a high PLL loop bandwidth in order to track input reference changes, such as Spread-Spectrum Clock modulation, so it will not attenuate much jitter on the input reference.
- 3) Low-Bandwidth Frequency Translator
  - Applications: Networking & Communications.
  - Translates any input clock in the 8kHz - 710MHz frequency range into any supported output frequency.
  - This mode supports PLL loop bandwidths in the 10Hz - 580Hz range and makes use of an external crystal to provide significant jitter attenuation.

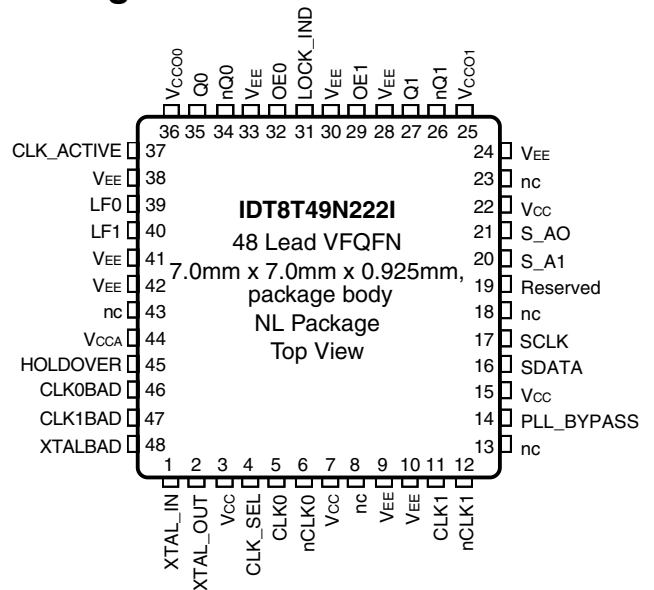
This device provides a factory-programmed default power-up configuration burned into One-Time Programmable (OTP) memory. The configuration is specified by the customer and is programmed by IDT during the final test phase from an on-hand stock of blank devices.

To implement other configurations, these power-up default settings can be overwritten after power-up using the I<sup>2</sup>C interface and the device can be completely reconfigured. However, these settings would have to be written every time the device powers-up.

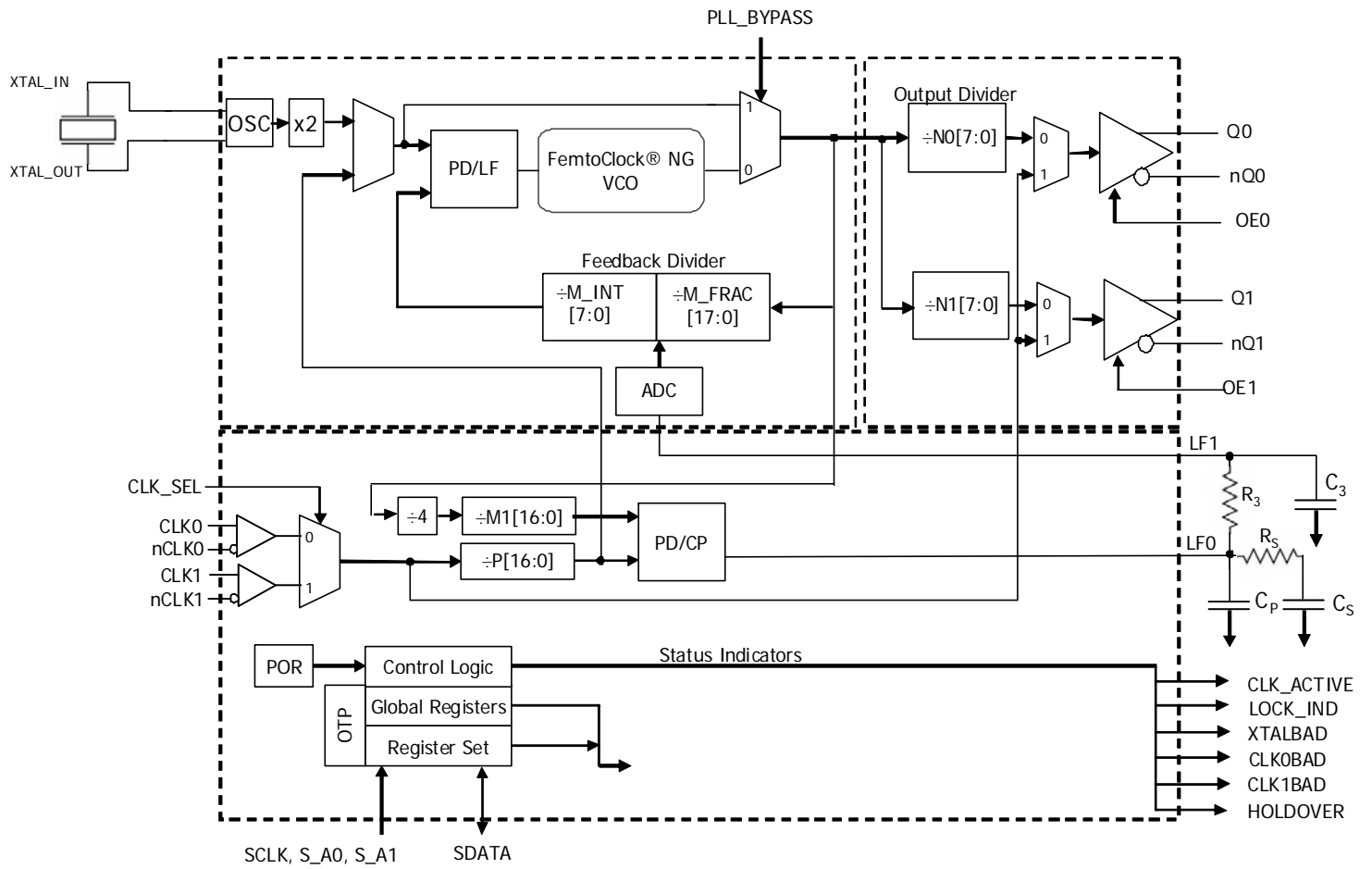
### Features

- Fourth generation FemtoClock® NG technology
- Universal Frequency Translator
  - Zero ppm frequency translation
- Two outputs, individually programmable as LVPECL or LVDS
  - Outputs may be individually set to use 2.5V or 3.3V output levels
  - Individually programmable output frequencies: 7.29MHz up to 1200MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, HCSL
  - Input frequency range: 8kHz to 710MHz
  - Hitless switching between inputs
- Crystal input frequency range: 16MHz to 40MHz
  - Holdover support in the event both inputs fail
- One factory-set register configuration for power-up default state
  - Configurations customized via One-Time Programmable ROM
  - Settings may be overwritten after power-up via I<sup>2</sup>C
  - I<sup>2</sup>C Serial interface for register programming
- RMS phase jitter at 156.25MHz, using a 40MHz crystal (12kHz - 20MHz): 507fs (typical), Low Bandwidth Mode (FracN)
- Supports ITU-T G.8262 Synchronous Ethernet equipment slave clocks (EEC option 1 and 2)
- Output supply voltage modes:
  - $V_{CC}/V_{CCA}/V_{CCOx}$
  - 3.3V/3.3V/3.3V
  - 3.3V/3.3V/2.5V (LVPECL only)
  - 2.5V/2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Pin Assignment



# Block Diagram



## Pin Descriptions and Pin Characteristic Tables

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1 2	XTAL_IN XTAL_OUT	Input		Crystal Oscillator interface designed for 12pF parallel resonant crystals. XTAL_IN (pin 1) is the input and XTAL_OUT (pin 2) is the output.
3, 7, 15, 22	V <sub>CC</sub>	Power		Core supply pins. All must be either 3.3V or 2.5V.
4	CLK_SEL	Input	Pulldown	Input clock select. Selects the active differential clock input. 0 = CLK0, nCLK0 (default) 1 = CLK1, nCLK1
5	CLK0	Input	Pulldown	Non-inverting differential clock input.
6	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating (set by the internal pullup and pulldown resistors).
8, 13, 18, 23, 43	nc	Unused		No connect. These pins are to be left unconnected.
9, 10, 24, 28, 30, 33, 38, 41, 42	V <sub>EE</sub>	Power		Negative supply pins.
11	CLK1	Input	Pulldown	Non-inverting differential clock input.
12	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating (set by the internal pullup and pulldown resistors).
14	PLL_BYPASS	Input	Pulldown	Bypasses the VCXO PLL. 0 = PLL Mode (default) 1 = PLL Bypassed
16	SDATA	I/O	Pullup	I <sup>2</sup> C Data Input/Output. Open drain.
17	SCLK	Input	Pullup	I <sup>2</sup> C Clock Input. LVCMOS/LVTTL Interface Levels.
19	Reserved	Unused		Must be left unconnected.
20	S_A1	Input	Pulldown	I <sup>2</sup> C Address Bit 1. LVCMOS/LVTTL Interface Levels.
21	S_A0	Input	Pulldown	I <sup>2</sup> C Address Bit 0. LVCMOS/LVTTL Interface Levels.
25	V <sub>CCO1</sub>	Power		Output supply pins for Q1, nQ1 outputs. Either 2.5V or 3.3V.
26, 27	nQ1, Q1	Output		Differential output. Output type is programmable to LVDS or LVPECL interface levels.
29	OE1	Input	Pullup	Active High Output Enable for Q1, nQ1. 0 = Output pins high-impedance 1 = Output switching (default)
31	LOCK_IND	Output		Lock Indicator - indicates that the PLL is in a locked condition. LVCMOS/LVTTL interface levels.
32	OE0	Input	Pullup	Active High Output Enable for Q0, nQ0. 0 = Output pins high-impedance 1 = Output switching (default)
34, 35	nQ0, Q0	Output		Differential output. Output type is programmable to LVDS or LVPECL interface levels.
36	V <sub>CCO0</sub>	Power		Output supply pins for Q0, nQ0 outputs. Either 2.5V or 3.3V.
37	CLK_ACTIVE	Output		Indicates which of the two differential clock inputs is currently selected. 0 = CLK0, nCLK0 differential input pair 1 = CLK1, nCLK1 differential input pair
39, 40	LF0, LF1	Input		Loop filter connection node pins. LF0 is the output. LF1 is the input.

**Table 1. Pin Descriptions**

Number	Name	Type	Description
Continued on next page.			
44	V <sub>CCA</sub>	Power	Analog supply voltage.
45	HOLDOVER	Output	Alarm output reflecting if the device is in a holdover state. LVCMOS/LVTTL interface levels. 0 = Device is locked to a valid input reference 1 = Device is not locked to a valid input reference
46	CLK0BAD	Output	Alarm output reflecting the state of CLK0. LVCMOS/LVTTL interface levels. 0 = Input Clock 0 is switching within specifications 1 = Input Clock 0 is out of specification
47	CLK1BAD	Output	Alarm output reflecting the state of CLK1. LVCMOS/LVTTL interface levels. 0 = Input Clock 1 is switching within specifications 1 = Input Clock 1 is out of specification
48	XTALBAD	Output	Alarm output reflecting the state of XTAL. LVCMOS/LVTTL interface levels. 0 = crystal is switching within specifications 1 = crystal is out of specification

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			3.5		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance	HOLDOVER, CLK_ACTIVE, CLK0BAD, CLK1BAD, XTALBAD, LOCK_IND	V <sub>CC</sub> = 3.465V	25		Ω
		HOLDOVER, CLK_ACTIVE, CLK0BAD, CLK1BAD, XTALBAD, LOCK_IND	V <sub>CC</sub> = 2.625V	25		Ω

## Functional Description

The IDT8T49N222I is designed to provide two output frequencies almost anywhere within its supported output frequency range (7.29MHz to 1200MHz) from any input source in the supported input frequency range (8kHz to 710MHz). It is capable of synthesizing frequencies from a crystal or crystal oscillator source. The output frequency is generated regardless of the relationship to the input frequency. The output frequency will be exactly the required frequency in most cases. In most others, it will only differ from the desired frequency by a few ppb. IDT configuration software will indicate the frequency error, if any. The IDT8T49N222I can translate the desired output frequency from one of two input clocks. Again, no relationship is required between the input and output frequencies in order to translate to the output clock rate. In this frequency translation mode, a low-bandwidth, jitter attenuation option is available that makes use of an external fixed-frequency crystal or crystal oscillator to translate from a noisy input source. If the input clock is known to be fairly clean or if some modulation on the input needs to be tracked, then the high-bandwidth frequency translation mode can be used, without the need for the external crystal.

The input clock references and crystal input are monitored continuously and appropriate alarms are raised both as register bits and hard-wired pins in the event of any out-of-specification conditions arising. Clock switching is supported in manual, revertive & non-revertive modes.

The IDT8T49N222I has one factory-programmed configuration that sets the default operating state after reset. These defaults may be over-written by I<sup>2</sup>C register access at any time, but those over-written settings will be lost on power-down. Please contact IDT if a specific set of power-up default settings is desired. Users that have a custom configuration programmed may not require I<sup>2</sup>C access.

Please make use of IDT-provided configuration tools to determine the best operating settings for the desired configurations of the device. Please refer to the Universal Frequency Translator Family Programming Guide if further details are required.

## Operating Modes

The IDT8T49N222I has three operating modes which are set by the MODE\_SEL[1:0] bits. There are two frequency translator modes - low bandwidth and high bandwidth and a frequency synthesizer mode.

Please make use of IDT-provided configuration applications to determine the best operating settings for the desired configurations of the device.

## Output Dividers & Supported Output Frequencies

The internal VCO is capable of operating in a range from 1.850GHz up to 2.5GHz. The output divider stages N0[7:0] and N1[7:0] are limited to selection of integers from 2 to 254. Please refer to Table 3A for the recommended values of N applicable to the desired output frequency.

**Table 3A. Output Divider Settings & Frequency Ranges\***

Register Setting	Frequency Divider	Minimum f <sub>OUT</sub> (MHz)	Maximum f <sub>OUT</sub> (MHz)
Nn[7:0]	Nn		
0000000x	Not Supported		
00000010	2	925.00	1200.00
00000011	3	616.67	833.33
00000100	4	462.50	625.00
00000101	5	370.00	500.00
00000110	6	308.33	416.67
00000111	7	264.29	357.14
00001000	8	231.25	312.50
00001001	9	205.56	277.78
00001010	10	185.00	250.00
...			
11111110	254	7.29	9.84

\*NOTE: Frequency ranges for other N output dividers are possible. Contact IDT Factory for special cases.

In addition to the above output divider settings, it is possible for either or both of the outputs to present a copy of the currently active input reference frequency by asserting the appropriate BYPn register bit.

Below are some example configurations for some common frequency combinations. Please use the IDT Configuration SW or consult with IDT to select other options.

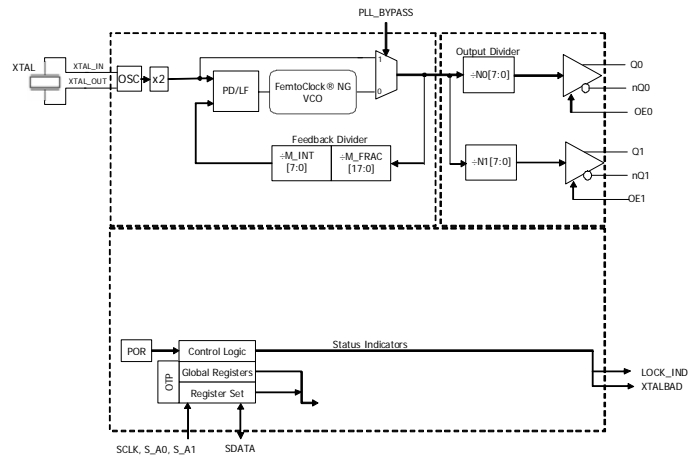
**Table 3B. Common Frequency Combination Examples**

Output Frequency (MHz)	Output Divider Ratio	VCO Operating Frequency (MHz)
125	15	1875
156.25	12	
25	75	1875
156.25	12	
25	80	2000
125	16	
155.52	12	1866.24
622.08	3	
19.44	96	1866.24
622.08	3	
161.1328125	12	1933.59375
644.53125	3	
156.25	12	1875
625	3	
122.88	20	2457.6
614.4	4	
245.76	10	2457.6
614.4	4	
30.72	80	2457.6
614.4	4	
153.6	16	2457.6
614.4	4	
15.36	144	2211.84
737.28	3	
125	16	2000
133.3333	15	
32.76	60	1965.6
131.04	15	
26.5625	80	2125
212.5	10	
106.25	18	1912.5
318.75	6	

**Frequency Synthesizer Mode**

This mode of operation allows an arbitrary output frequency to be generated from a fundamental mode crystal input. For improved phase noise performance, the crystal input frequency may be doubled. As can be seen from the block diagram in Figure 1, only the upper feedback loop is used in this mode of operation. It is recommended that CLK0 and CLK1 be left unused in this mode of operation.

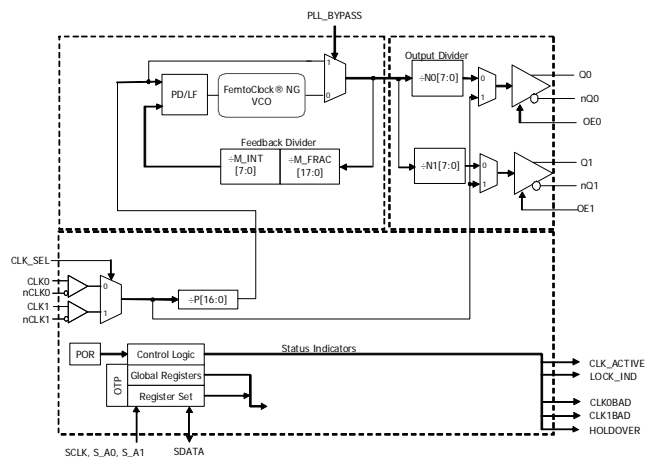
The upper feedback loop supports a delta-sigma fractional feedback divider. This allows the VCO operating frequency to be a non-integer multiple of the crystal frequency. By using an integer multiple only, lower phase noise jitter on the output can be achieved, however the use of the delta-sigma divider logic will provide excellent performance on the output if a fractional divisor is used.



**Figure 1. Frequency Synthesizer Mode Block Diagram**

**High-Bandwidth Frequency Translator Mode**

This mode of operation is used to translate one of two input clocks of the same nominal frequency into an output frequency with little jitter attenuation. As can be seen from the block diagram in Figure 2, similarly to the Frequency Synthesizer mode, only the upper feedback loop is used.



**Figure 2. High Bandwidth Frequency Translator Mode Block Diagram**



attention to the non-selected input reference until a locked state has been achieved. This is necessary to prevent 'hunting' behavior during the locking phase.

Once the IDT8T49N222I has achieved a stable lock, it will remain locked to the preferred input reference as long as there is a valid clock on it. If at some point, that clock fails, then the device will automatically switch to the other input reference as long as there is a valid clock there. If there is not a valid clock on either input reference, the IDT8T49N222I will go into holdover state and the HOLDOVER alarm will be raised.

The device will recover from holdover state once a valid clock is re-established on either reference input. If clocks are valid on both input references, the device will choose the reference indicated by the CLK\_SEL register bit.

If running from the non-preferred input reference and a valid clock returns, there is a difference in behavior between Revertive and Non-revertive modes. In Revertive mode, the device will switch back to the reference indicated by the CLK\_SEL register bit even if there is still a valid clock on the non-preferred reference input. In Non-revertive mode, the IDT8T49N222I will not switch back as long as the non-preferred input reference still has a valid clock on it.

### Switchover Behavior of the PLL

Even though the two input references have the same nominal frequency, there may be minor differences in frequency and potentially large differences in phase between them. The IDT8T49N222I will adjust its output to the new input reference. It will use Phase Slope Limiting to adjust the output phase at a fixed maximum rate until the output phase and frequency are now aligned to the new input reference. Phase will always be adjusted by extending the clock period of the output so that no unacceptably short clock periods are generated on the output IDT8T49N222I.

### Holdover / Free-run Behavior

When both input references have failed (Automatic mode) or the selected input has failed (Manual mode), the IDT8T49N222I will enter holdover (Low Bandwidth Frequency Translator mode) or free-run (High Bandwidth Frequency Translator mode) state if. In both cases, once the input reference is lost, the PLL will stop making adjustments to the output phase.

If operating in Low Bandwidth Frequency Translation mode, the PLL will continue to reference itself to the local oscillator and will hold its output phase and frequency in relation to that source. Output stability is determined by the stability of the local oscillator in this case.

However, if operating in High Bandwidth Frequency Translation mode, the PLL no longer has any frequency reference to use and output stability is now determined by the stability of the internal VCO.

If the device is programmed to perform Manual switching, once the selected input reference recovers, the IDT8T49N222I will switch back to that input reference. If programmed for either Automatic mode, the device will switch back to whichever input reference has a valid clock first.

The switchover that results from returning from holdover or free-run is handled in the same way as a switch between two valid input references as described in the previous section.



## Output Configuration

The two outputs of the IDT8T49N222I provide separate output frequencies. Each output may have a different output voltage level of 3.3V or 2.5V, although this output voltage must be less than or equal to the core voltage (3.3V or 2.5V) the rest of the device is operating from. The output voltage level used on each output is supplied on their respective V<sub>CCO</sub> pin.

The two outputs are individually selectable as LVDS or LVPECL output types via the Qn\_TYPE register bits (where n = 0 for Q0 / nQ0 and n = 1 for the Q1 / nQ1 output pair).

The two outputs can be enabled individually also via both register control bits and input pins. When both the OEn register bit and OEn pin are enabled, then the appropriate output is enabled. The OEn register bits default to enabled so that by default the outputs can be directly controlled by the input pins. Similarly, the input pins are provisioned with weak pull-ups so that if they are left unconnected, the output state can be directly controlled by the register bits. When the differential output is in the disabled state, it will show a high impedance condition.

**Table 4A. I<sup>2</sup>C Device Slave Address**

1	1	0	1	1	S_A1	S_A0	R/W
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## Serial Interface Configuration Description

The IDT8T49N222I has an I<sup>2</sup>C-compatible configuration interface to access any of the internal registers (Table 4D) for frequency and PLL parameter programming. The IDT8T49N222I acts as a slave device on the I<sup>2</sup>C bus and has the address 0b11011xx, where xx is set by the values on the S\_A0 & S\_A1 pins (see Table 4A for details). The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 4D) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see table 4B, 4C). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate I<sup>2</sup>C the read or write transfer after accessing byte #23.

For full electrical I<sup>2</sup>C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

Note: if a different device slave address is desired, please contact IDT.

**Table 4B. Block Write Operation**

Bit	1	2:8	9	10	11:18	19	20:27	28	29-36	37	...	...	...
Description	START	Slave Address	W (0)	ACK	Address Byte (P)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

**Table 4C. Block Read Operation**

Bit	1	2:8	9	10	11:18	19	20	21:27	28	29	30:37	38	39-46	47	...	...	...
Description	START	Slave Address	W (0)	ACK	Address Byte (P)	ACK	Repeated START	Slave Address	R (1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

## Register Descriptions

Please consult IDT for configuration software and/or programming guides to assist in selection of optimal register settings for the desired configurations.

**Table 4D. I<sup>2</sup>C Register Map**

Reg	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	MFRAC0[17]	MFRAC0[16]	MFRAC0[15]	MFRAC0[14]	MFRAC0[13]	MFRAC0[12]	MFRAC0[11]	MFRAC0[10]
1	00001	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	00010	MFRAC0[9]	MFRAC0[8]	MFRAC0[7]	MFRAC0[6]	MFRAC0[5]	MFRAC0[4]	MFRAC0[3]	MFRAC0[2]
3	00011	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
4	00100	MFRAC0[1]	MFRAC0[0]	MINT[7]	MINT[6]	MINT[5]	MINT[4]	MINT[3]	MINT[2]
5	00101	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
6	00110	MINT[1]	MINT[0]	P[16]	P[15]	P[14]	P[13]	P[12]	P[11]
7	00111	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
8	01000	P[10]	P[9]	P[8]	P[7]	P[6]	P[5]	P[4]	P[3]
9	01001	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	01010	P[2]	P[1]	P[0]	M1[16]	M1[15]	M1[14]	M1[13]	M1[12]
11	01011	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
12	01100	M1[11]	M1[10]	M1[9]	M1[8]	M1[7]	M1[6]	M1[5]	M1[4]
13	01101	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
14	01110	M1[3]	M1[2]	M1[1]	M1[0]	Rsvd	Rsvd	Rsvd	Rsvd
15	01111	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
16	10000	N0[7]	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]
17	10001	N1[7]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
18	10010	Rsvd	BW[6]	BW[5]	BW[4]	BW[3]	BW[2]	BW[1]	BW[0]
19	10011	DBL_XTAL	Re-Calibrate	OE1	OE0	Q1_TYPE	Q0_TYPE	BYP1	BYP0
20	10100	MODE_SEL1	MODE_SELO	0	0	Rsvd	Rsvd	Rsvd	Rsvd
21	10101	CLK_SEL	AUTO_MAN[1]	AUTO_MAN[0]	0	ADC_RATE[1]	ADC_RATE[0]	LCK_WIN[1]	LCK_WIN[0]
22	10110	1	0	1	0	0	0	0	0
23	10111	CLK_ACTIVE	HOLDOVER	CLK1BAD	CLK0BAD	XTAL_BAD	LOCK_IND	Rsvd	Rsvd

**Table 4E. Control Bits**

Register Bits	Function
Q0_TYPE	Determines the output type for output pair Q0, nQ0. 0 = LVPECL (Default) 1 = LVDS
Q1_TYPE	Determines the output type for output pair Q1, nQ1. 0 = LVPECL (Default) 1 = LVDS
BYP0	Bypass Input to output Q0. 0 = Use result of output divider N0 (Default) 1 = Drive currently active input reference frequency on output
BYP1	Bypass Input to output Q1. 0 = Use result of output divider N1 (Default) 1 = Drive currently active input reference frequency on output
P[16:0]	Reference Pre-Divider.
M1[16:0]	Integer Feedback Divider in Lower Feedback Loop.
M_INT[7:0]	Feedback Divider, Integer Value in Upper Feedback Loop.
M_FRAC[17:0]	Feedback Divider, Fractional Value in Upper Feedback Loop.
N0[7:0]	Output Divider for Q0, nQ0.
N1[7:0]	Output Divider for Q1, nQ1.
BW[6:0]	Internal Operation Settings. Please use IDT IDT8T49N222I Configuration Software to determine the correct settings for these bits for the specific configuration. Alternatively, please consult with IDT directly for further information on the functions of these bits. The function of these bits is explained in Tables 4H and 4I.
Re-calibrate	This bit is asserted to force a VCO calibration cycle. The bit needs to be returned to '0' to resume normal operation. This is only needed if the P[16:0], M_INT[7:0] or M_FRAC[17:0] registers are changed after power-up. The device automatically calibrates the VCO on power-up.
Rsvd	Reserved bits - user should write a '0' to these bit positions if a write to these registers is needed.

**Table 4F. Global Control Bits**

Register Bits	Function
OE0	Output Enable Control for Output 0. Both this register bit and the corresponding Output Enable pin OE0 must be asserted to enable the Q0, nQ0 output. 0 = Output Q0, nQ0 disabled 1 = Output Q0, nQ0 under control of the OE0 pin (Default)
OE1	Output Enable Control for Output 1. Both this register bit and the corresponding Output Enable pin OE1 must be asserted to enable the Q1, nQ1 output. 0 = Output Q1, nQ1 disabled 1 = Output Q1, nQ1 under control of the OE1 pin (Default)
AUTO_MAN[1:0]	Selects how input clock selection is performed. 00 = Manual Selection via pin only (Default) 01 = Automatic, non-revertive 10 = Automatic, revertive 11 = Manual Selection via register only
CLK_SEL	In manual clock selection via register mode, this bit will command which input clock is selected. In the automatic modes, this indicates the primary clock input. In manual selection via pin mode, this bit has no effect. 0 = CLK0 (Default) 1 = CLK1
DBL_XTAL	When set, enables the crystal frequency doubler circuit.
ADC_RATE[1:0]	Sets the ADC sampling as a fraction of the crystal input frequency. 00 = Crystal Frequency $\div 16$ 01 = Crystal Frequency $\div 8$ 10 = Crystal Frequency $\div 4$ (recommended) 11 = Crystal Frequency $\div 2$
LCK_WIN[1:0]	Sets the width of the window in which a new reference edge must fall relative to the feedback edge: 00 = 2 $\mu$ S (default), 01 = 4 $\mu$ S, 10 = 8 $\mu$ S, 11 = 16 $\mu$ S
MODE_SEL[1:0]	PLL mode select. 00 = Low Bandwidth Mode (default) 01 = Frequency Synthesizer Mode 10 = High Bandwidth Mode 11 = High Bandwidth Mode

**Table 4G. Global Status Bits**

Register Bits	Function
CLK0BAD	Status Bit for input CLK0. This function is mirrored in the CLK0BAD pin. 0 = input CLK0 is good 1 = input CLK0 is bad. Self clears when input clock returns to good status
CLK1BAD	Status Bit for input CLK1. This function is mirrored in the CLK1BAD pin. 0 = input CLK1 is good 1 = input CLK1 is bad. Self clears when input clock returns to good status
XTALBAD	Status Bit. This function is mirrored on the XTALBAD pin. 0 = crystal input is good 1 = crystal input is bad. Self-clears when the XTAL clock returns to good status
LOCK_IND	Status bit. This function is mirrored on the LOCK_IND pin. 0 = PLL is unlocked 1 = PLL is locked
HOLDOVER	Status Bit. This function is mirrored on the HOLDOVER pin. 0 = Input to phase detector is within specifications and device is tracking to it 1 = Phase detector input is not within specifications and DCXO is frozen at last value
CLK_ACTIVE	Status Bit. Indicates which input clock is active. Automatically updates during fail-over switching. Status also indicated on CLK_ACTIVE pin.

**Table 4H. BW[6:0] Bits**

Mode	BW[6]	BW[5]	BW[4]	BW[3]	BW[2]	BW[1]	BW[0]
Synthesizer Mode	PLL2_LF[1]	PLL2_LF[0]	DSM_ORD	DSM_EN	PLL2_CP[1]	PLL2_CP[0]	PLL2_LOW_ICP
High-Bandwidth Mode	PLL2_LF[1]	PLL2_LF[0]	DSM_ORD	DSM_EN	PLL2_CP[1]	PLL2_CP[0]	PLL2_LOW_ICP
Low-Bandwidth Mode	ADC_GAIN[3]	ADC_GAIN[2]	ADC_GAIN[1]	ADC_GAIN[0]	PLL1_CP[1]	PLL1_CP[0]	PLL2_LOW_ICP

**Table 4I. Functions of Fields in BW[6:0]**

Register Bits	Function
PLL2_LF[1:0]	Sets loop filter values for upper loop PLL in Frequency Synthesizer & High-Bandwidth modes. Defaults to setting of 00 when in Low Bandwidth Mode. See Table 4L for settings.
DSM_ORD	Sets Delta-Sigma Modulation to 2nd (0) or 3rd order (1) operation.
DSM_EN	Enables Delta-Sigma Modulator. 0 = Disabled - feedback in integer mode only 1 = Enabled - feedback in fractional mode
PLL2_CP[1:0]	Upper loop PLL charge pump current settings. 00 = 173 $\mu$ A (defaults to this setting in Low Bandwidth Mode) 01 = 346 $\mu$ A 10 = 692 $\mu$ A 11 = reserved
PLL2_LOW_ICP	Reduces Charge Pump current by 1/3 to reduce bandwidth variations resulting from higher feedback register settings or high VCO operating frequency (>2.4GHz).
ADC_GAIN[3:0]	Gain setting for ADC in Low Bandwidth Mode.
PLL1_CP[1:0]	Lower loop PLL charge pump current settings (lower loop is only used in Low Bandwidth Mode). 00 = 800 $\mu$ A 01 = 400 $\mu$ A 10 = 200 $\mu$ A 11 = 100 $\mu$ A

**Table 4J. High Bandwidth Frequency and Frequency Synthesizer Bandwidth Settings**

Desired Bandwidth	PLL2_CP	PLL2_LOW_ICP	PLL2_LF
<b>Frequency Synthesizer Mode</b>			
200kHz	00	1	00
400kHz	01	1	01
800kHz	10	1	10
2MHz	10	1	11
<b>High Bandwidth Frequency Translator Mode</b>			
200kHz	00	1	00
400kHz	01	1	01
800kHz	10	1	10
4MHz	10	0	11

NOTE: To achieve 4MHz bandwidth, reference to the phase detector should be 80MHz.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	3.6V
Inputs, $V_I$ XTAL_IN OEx Other Inputs	0V to 2V -0.5V to $V_{CC0x} + 0.5V$ -0.5V to $V_{CC} + 0.5V$
Outputs, $V_O$ (LVCMOS)	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	10mA 15mA
Outputs, $I_O$ (SDATA)	10mA
Package Thermal Impedance, $\theta_{JA}$	29°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 5A. Power Supply DC Characteristics,  $V_{CC} = V_{CC00} = V_{CC01} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.30$	3.3	$V_{CC}$	V
$V_{CC00}$ , $V_{CC01}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				358	mA
$I_{CCA}$	Analog Supply Current	With $V_{CCA}$ pin connected to power supply via 10Ω resistor			30	mA

**Table 5B. LVPECL Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CC00} = V_{CC01} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.30$	3.3	$V_{CC}$	V
$V_{CC00}$ , $V_{CC01}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				357	mA
$I_{CCA}$	Analog Supply Current	With $V_{CCA}$ pin connected to power supply via 10Ω resistor			30	mA

**Table 5C. Power Supply DC Characteristics,  $V_{CC} = V_{CC00} = V_{CC01} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.26$	2.5	$V_{CC}$	V
$V_{CC00}$ , $V_{CC01}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				328	mA
$I_{CCA}$	Analog Supply Current	With $V_{CCA}$ pin connected to power supply via $10\Omega$ resistor			26	mA

**Table 5D. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = V_{CC00} = V_{CC01} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3V$	-0.3		0.8	V
		$V_{CC} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	CLK_SEL, PLL_BYPASS, S_A[0:1] $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
		SCLK, SDATA $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			10	$\mu A$
		OE0 $V_{CC00} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
		OE1 $V_{CC01} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	CLK_SEL, PLL_BYPASS, S_A[0:1] $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$
		OE0, OE1, SCLK, SDATA $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{OH}$	Output High Voltage	HOLDOVER, SDATA CLK_ACTIVE, LOCK_IND, XTALBAD, CLK0BAD, CLK1BAD $V_{CC} = 3.465V$ , $I_{OH} = -8mA$	2.6			V
		$V_{CC} = 2.625V$ , $I_{OH} = -8mA$	1.8			V
$V_{OL}$	Output Low Voltage	HOLDOVER, SDATA CLK_ACTIVE, LOCK_IND, XTALBAD, CLK0BAD, CLK1BAD $V_{CC} = 3.465V$ or $2.625V$ , $I_{OH} = 8mA$			0.5	V

**Table 5E. Differential Input DC Characteristics,  $V_{CC} = V_{CC00} = V_{CC01} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK0, nCLK0, CLK1, nCLK1 $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1 $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$
		nCLK0, nCLK1 $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1		$V_{EE} + 0.5$		$V_{CC} - 1.0$	V

NOTE 1: Common mode input voltage is defined at the crosspoint.



**Table 5F. LVPECL DC Characteristics,  $V_{CC} = V_{CC00} = V_{CC01} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ; or  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CC00} = V_{CC01} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC0x} - 1.1$		$V_{CC0x} - 0.7$	V
$V_{OL}$	Output Low Voltage NOTE 1		$V_{CC0x} - 2.0$		$V_{CC0x} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE:  $V_{CC0x}$  denotes  $V_{CC00}$  (Q0, nQ0) and  $V_{CC01}$  (Q1, nQ1).

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC0x} - 2V$ .

**Table 5G. LVDS DC Characteristics,  $V_{CC} = V_{CC00} = V_{CC01} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.125		1.375	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**Table 6. Input Frequency Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{IN}$	Input Frequency	XTAL_IN, XTAL_OUT; NOTE 1	16		40	MHz	
		CLK0, nCLK0, CLK1, nCLK1	High Bandwidth Mode	16		710	MHz
			Low Bandwidth Mode	0.008		710	MHz
		SCLK				50	MHz

NOTE 1: For the input crystal and CLKx, nCLKx frequency range, the M value must be set for the VCO to operate within the 1.850GHz to 2.500GHz range.

**Table 7. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		16		40	MHz
Load Capacitance ( $C_L$ )			12		pF
Shunt Capacitance				7	pF

## AC Electrical Characteristics

**Table 8. AC Characteristics**,  $V_{CC} = V_{CC00} = V_{CC01} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ; or  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CC00} = V_{CC01} = 2.5V \pm 5\%$  (LVPECL Only),  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		7.29		1200	MHz
$f_{VCO}$	VCO Frequency		1850		2500	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random), Integer Divide Ratio	Synth Mode (Integer FB), $f_{OUT} = 125MHz$ , 25MHz XTAL, Integration Range: 12kHz – 20MHz		278	350	fs
		Synth Mode (FracN FB), $f_{OUT} = 698.81MHz$ , 40MHz XTAL, Integration Range: 12kHz – 20MHz		481	590	fs
		HBW Mode, (NOTE 3) $f_{IN} = 133.33MHz$ , $f_{OUT} = 400MHz$ , Integration Range: 12kHz – 20MHz		306	570	fs
		LBW Mode (FracN), 40MHz XTAL, $f_{IN} = 19.44MHz$ , $f_{OUT} = 622.08MHz$ , Integration Range: 12kHz – 20MHz		425	540	fs
		LBW Mode (FracN), 40MHz XTAL, $f_{IN} = 25MHz$ , $f_{OUT} = 156.25MHz$ , Integration Range: 12kHz – 20MHz		508	680	fs
$f_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 1, 2	LBW Mode, 40MHz XTAL, $f_{IN} = 25MHz$ , $f_{OUT} = 156.25MHz$			40	ps
$f_{jit}(per)$	RMS Period Jitter; NOTE 2	LVPECL Outputs	LBW Mode, 40MHz XTAL, $f_{IN} = 25MHz$ , $f_{OUT} = 156.25MHz$		3.5	ps
		LVDS Outputs			4	ps
$t_R / t_F$	Output Rise/Fall Time	LVPECL Outputs	20% to 80%	80	350	ps
		LVDS Outputs	20% to 80%	90	400	ps
odc	Output Duty Cycle; NOTE 5		45		55	%
$t_{SET}$	Output Re-configuration Settling Time	from falling edge of the 8th SCLK for a register change (NOTE 4)		200		ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Using 40MHz, fundamental mode crystal with 12pF ( $C_L$ ) and the doubler circuit enabled.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

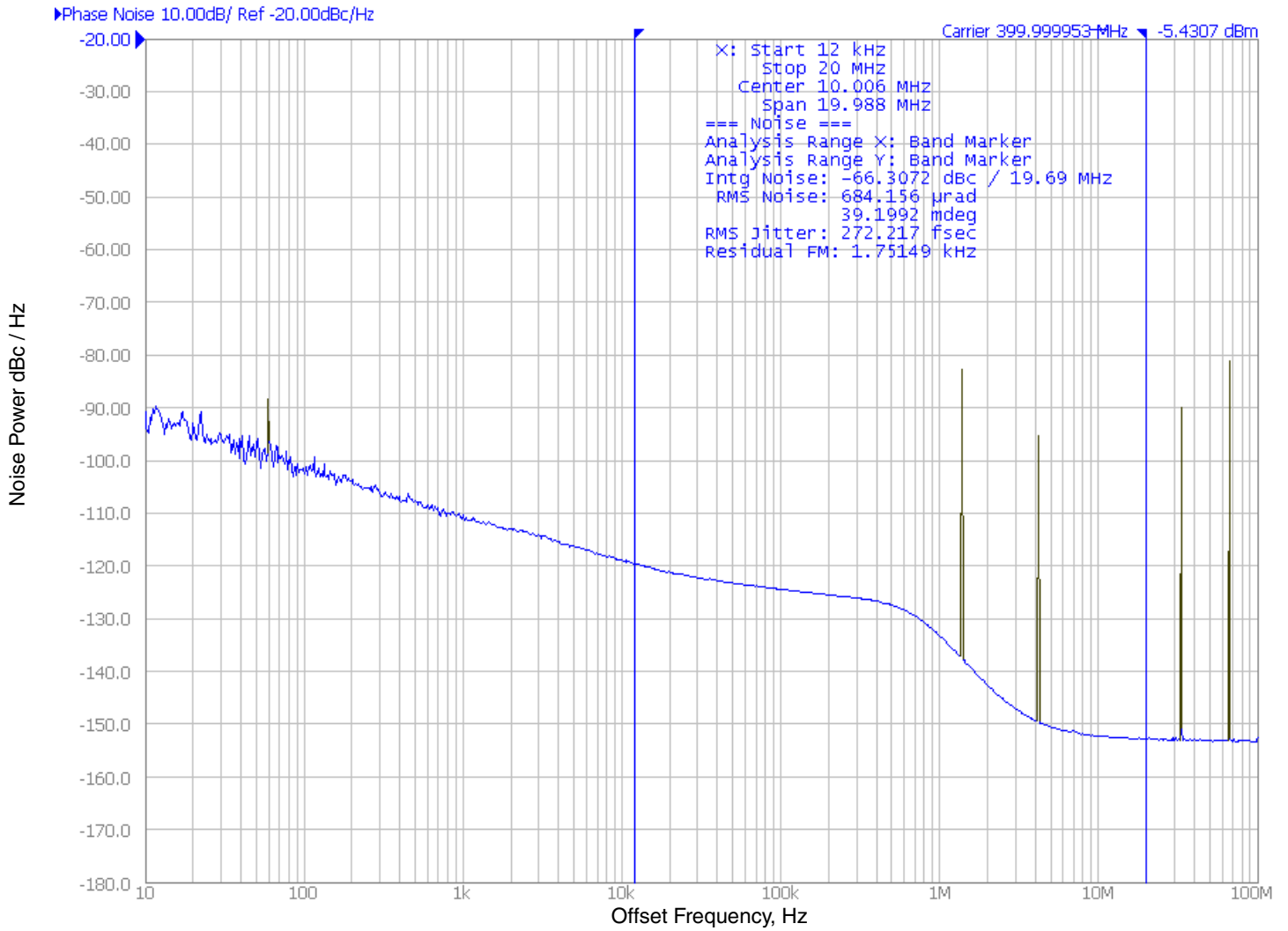
NOTE 2: This configuration corresponds to dash code -000.

NOTE 3: Measured using a Rohde & Schwarz SMA100 Signal Generator, 9kHz to 6GHz as the input source.

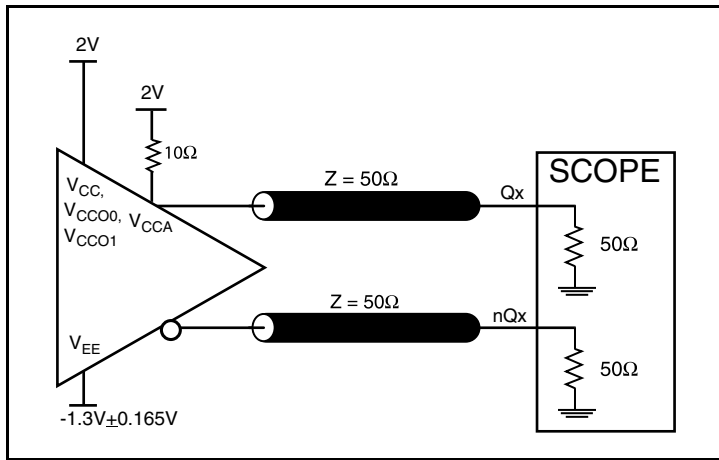
NOTE 4: This settling time does not include PLL re-calibration and locking if required. Since those times are highly dependent on the specific configuration, please contact IDT for times if PLL re-configuration is performed as part of the configuration change.

NOTE 5: Measurements are collected with the following output frequencies: 19.44MHz, 25MHz, 100MHz, 125MHz, 156.25MHz, 311.04MHz, 480MHz, 531.25MHz, 600MHz, 622.08MHz, 1062.5MHz, 1200MHz.

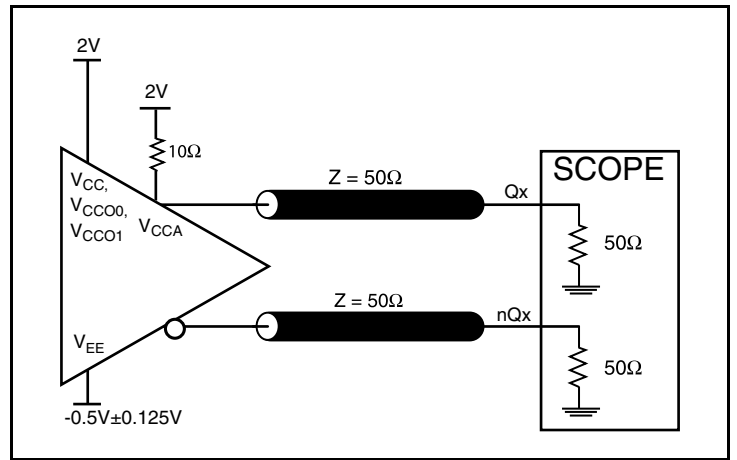
### Typical Phase Noise at 400MHz (HBW Mode)



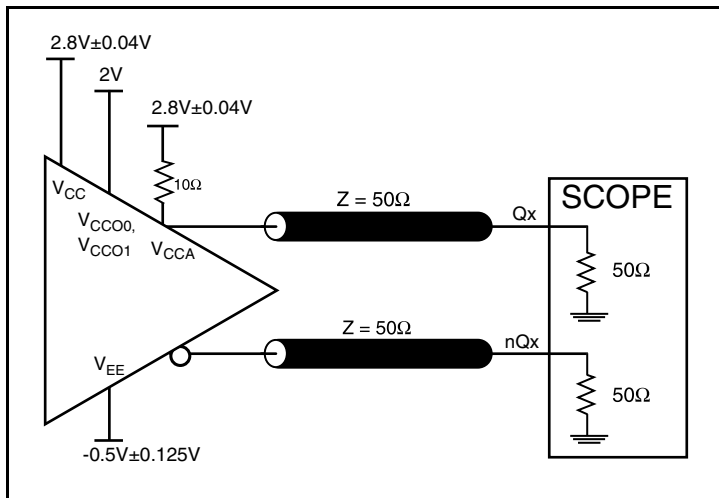
## Parameter Measurement Information



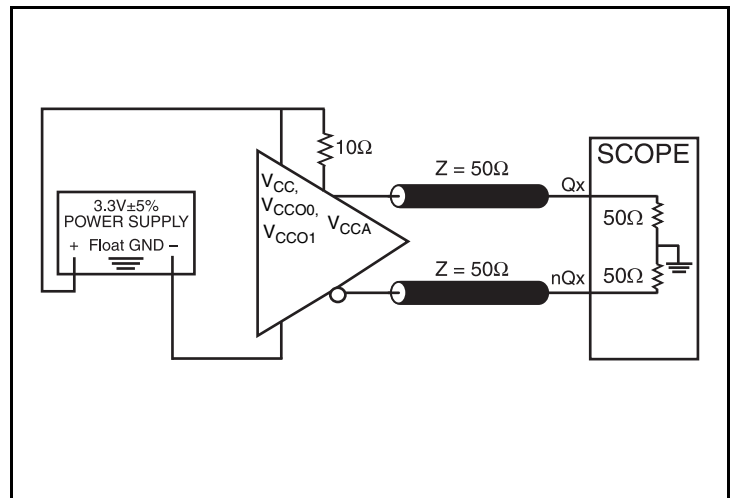
**3.3V Core/3.3V LVPECL Output Load Test Circuit**



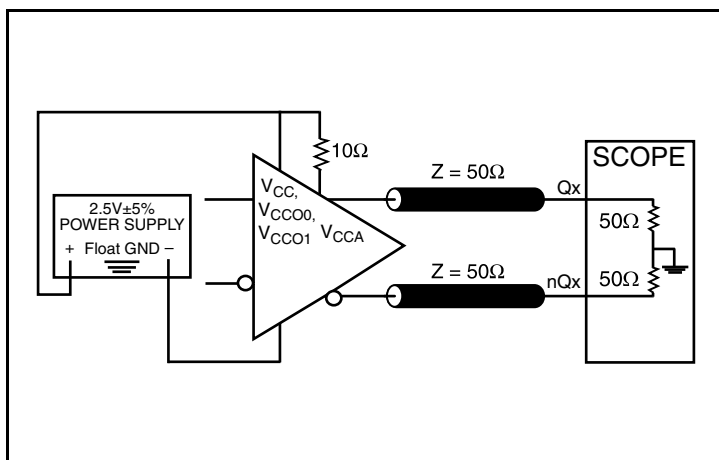
**2.5V Core/2.5V LVPECL Output Load Test Circuit**



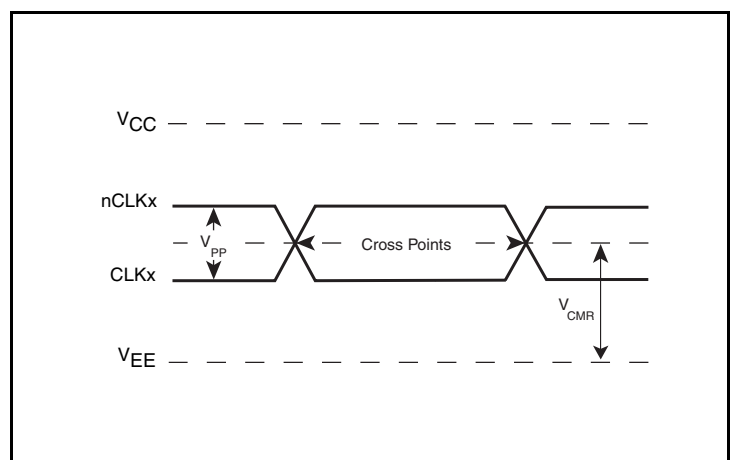
**3.3V Core/2.5V LVPECL Output Load Test Circuit**



**3.3V Core/3.3V LVDS Output Load Test Circuit**

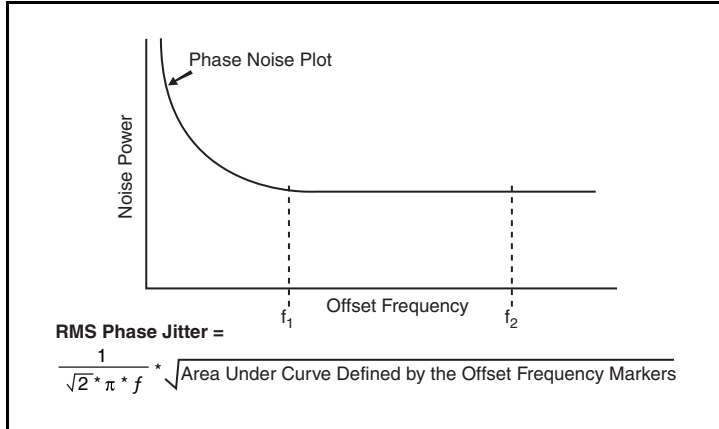


**2.5V Core/2.5V LVDS Output Load Test Circuit**

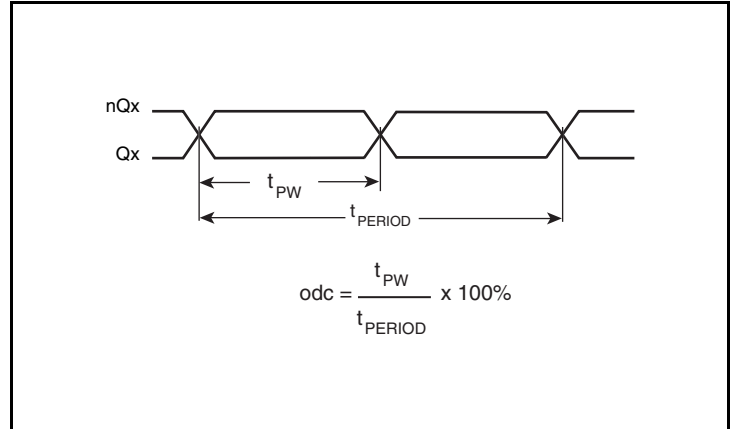


**Differential Input Levels**

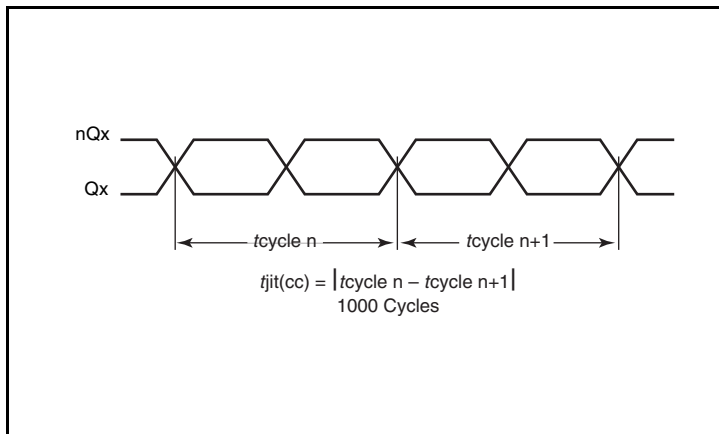
### Parameter Measurement Information, continued



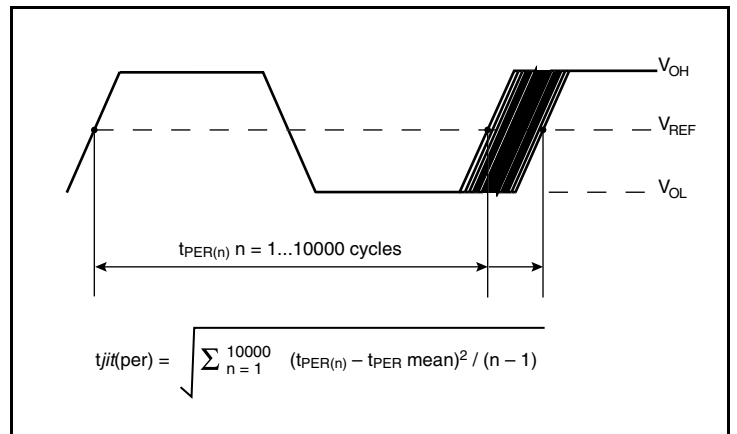
**RMS Phase Jitter**



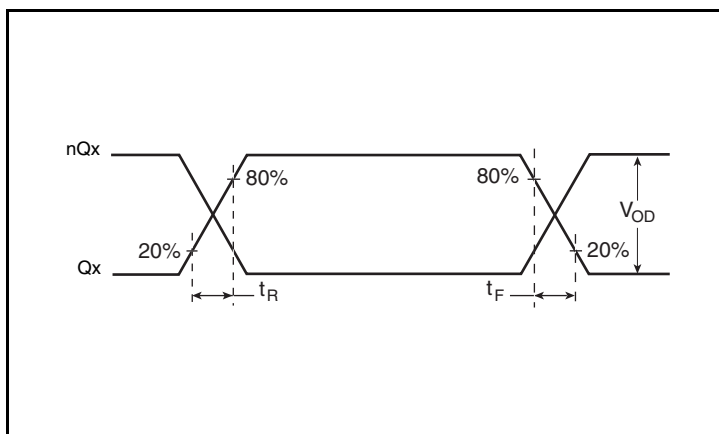
**Differential Output Duty Cycle/Output Pulse Width/Period**



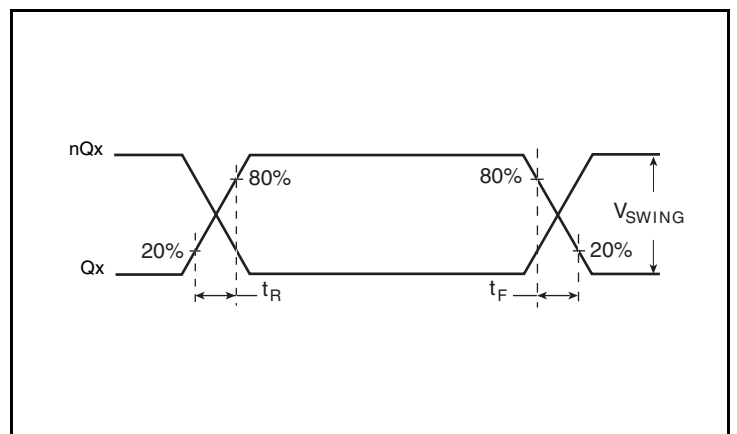
**Cycle-to-Cycle Jitter**



**RMS Period Jitter**

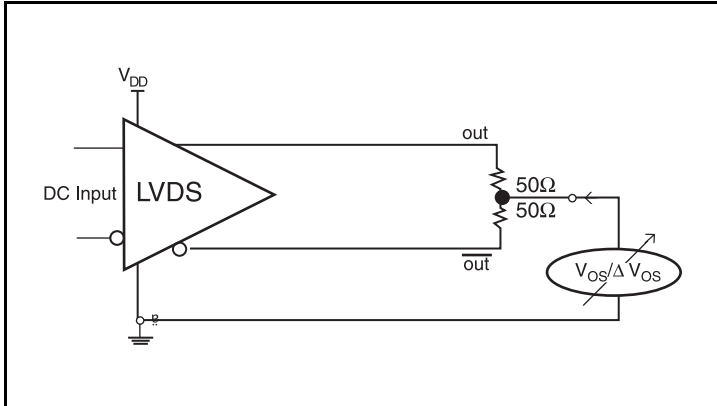


**LVDS Output Rise/Fall Time**

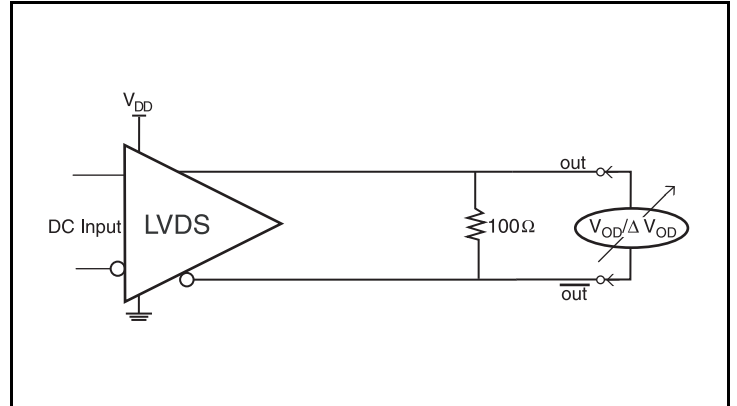


**LVPECL Output Rise/Fall Time**

### Parameter Measurement Information, continued



Offset Voltage Setup



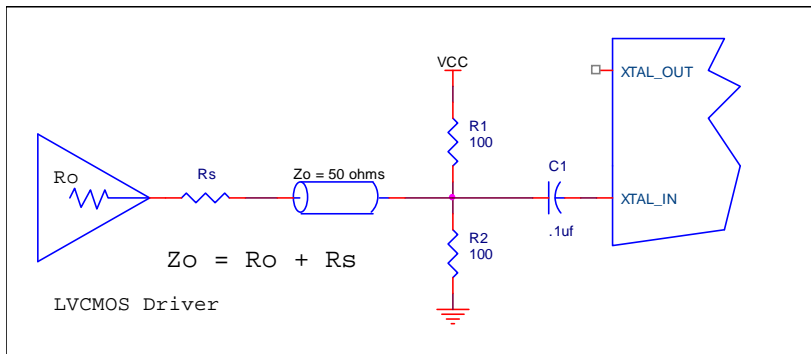
Differential Output Voltage Setup

## Applications Information

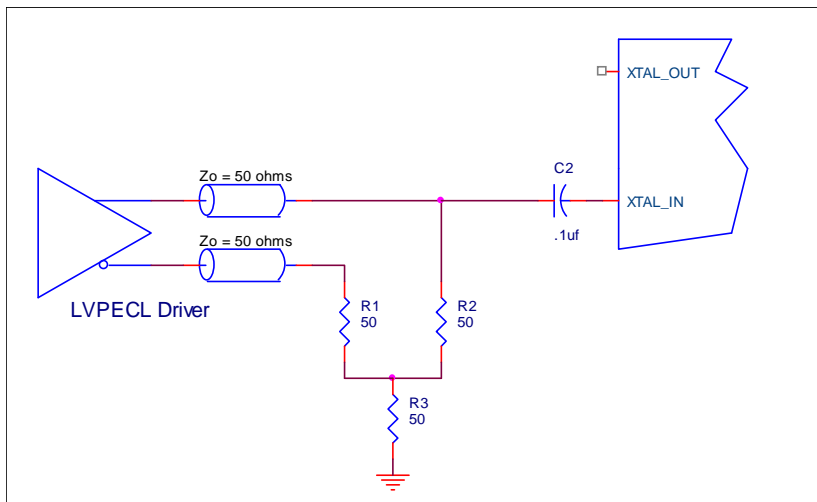
### Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.



**Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line

impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3V$  and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

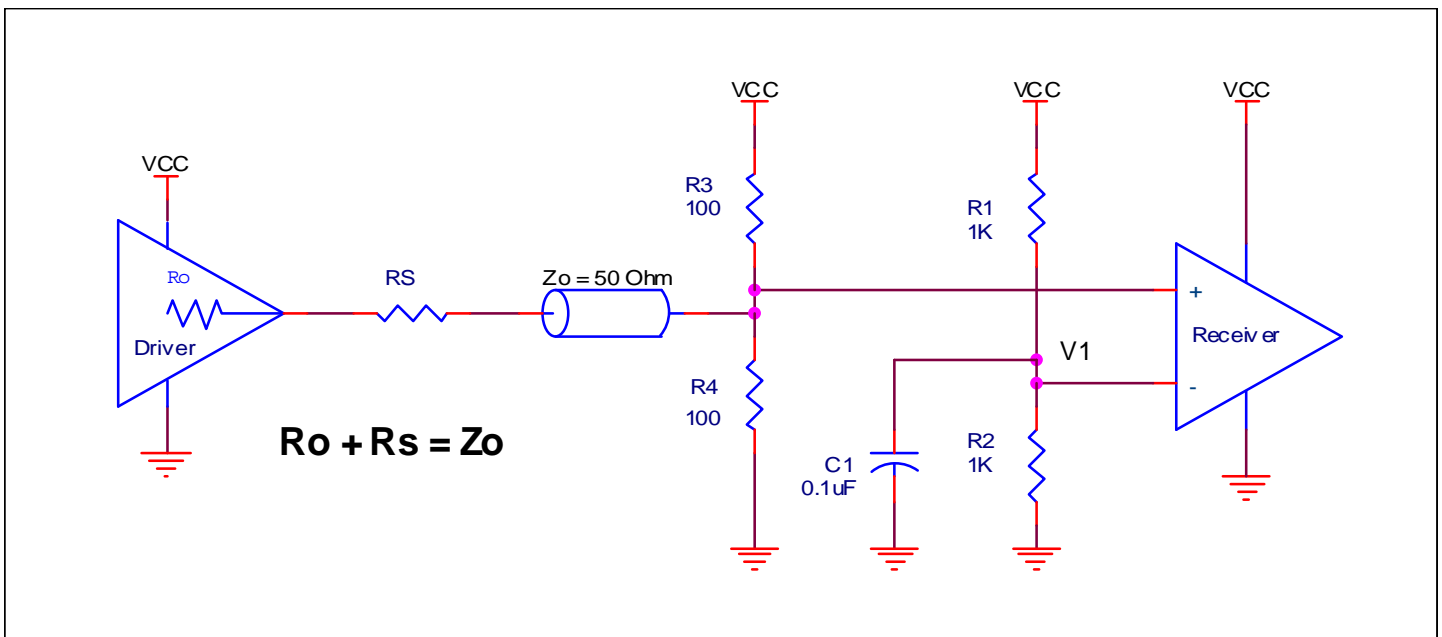


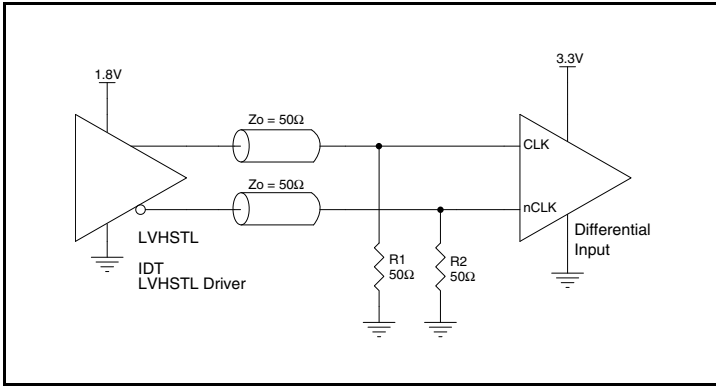
Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



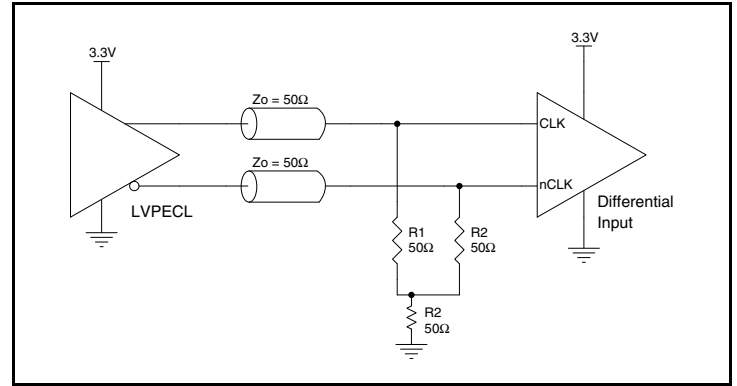
### 3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 3A to 3E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult

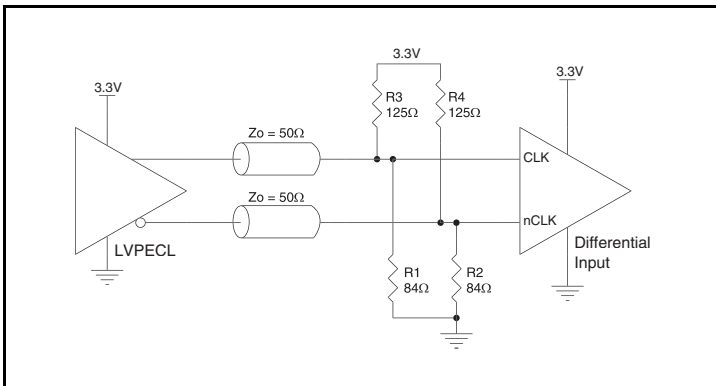
with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



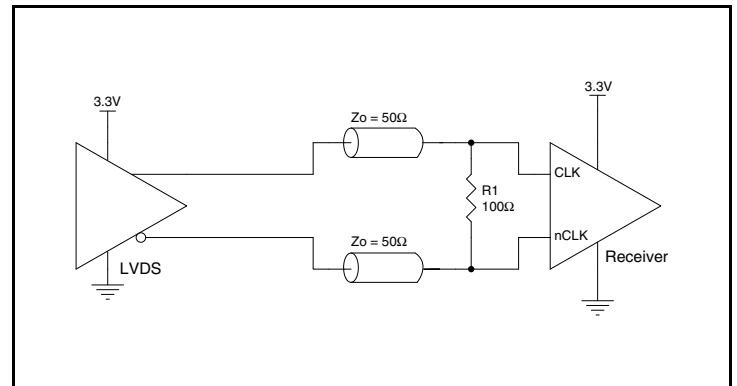
**Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**



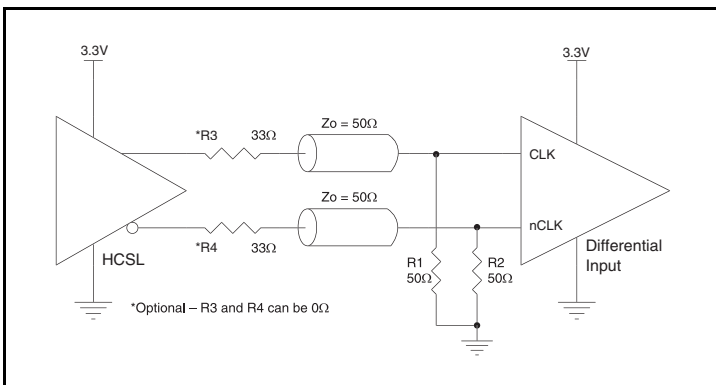
**Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

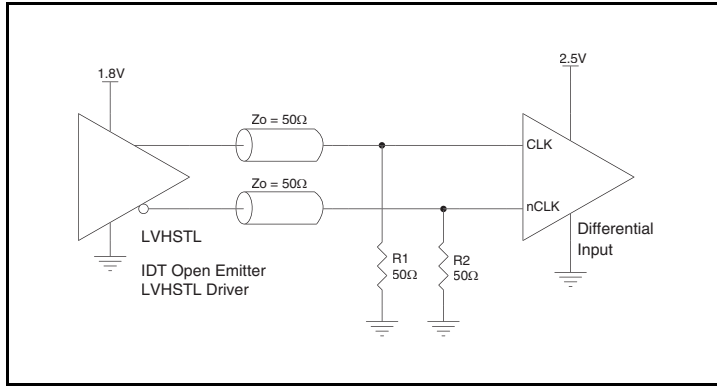


**Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

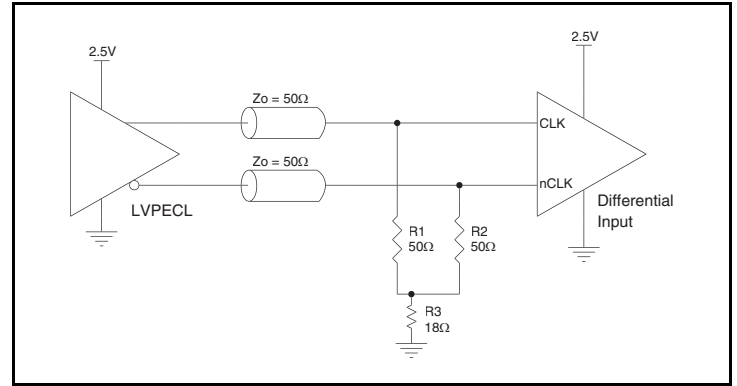
## 2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 4A to 4E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult

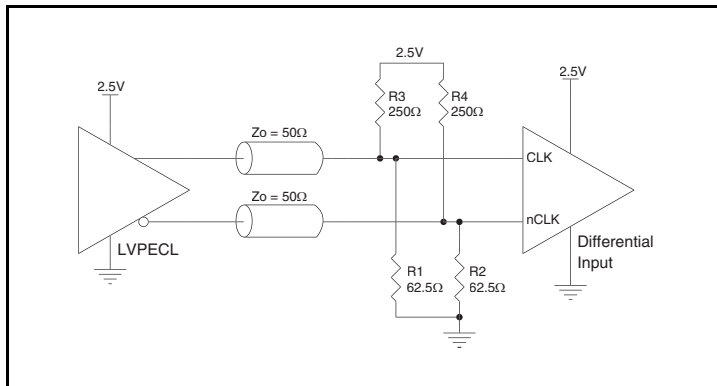
with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



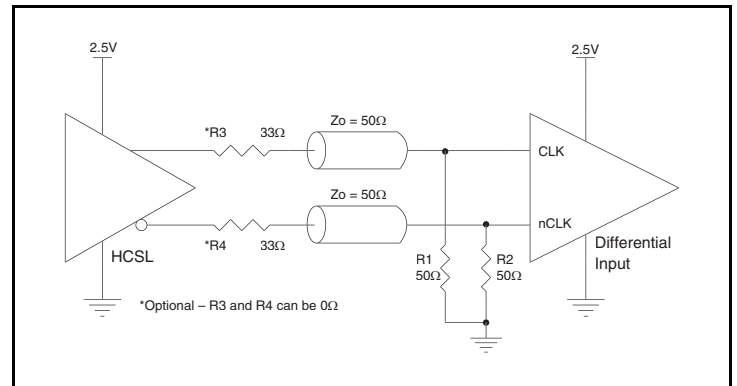
**Figure 4A.** CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver



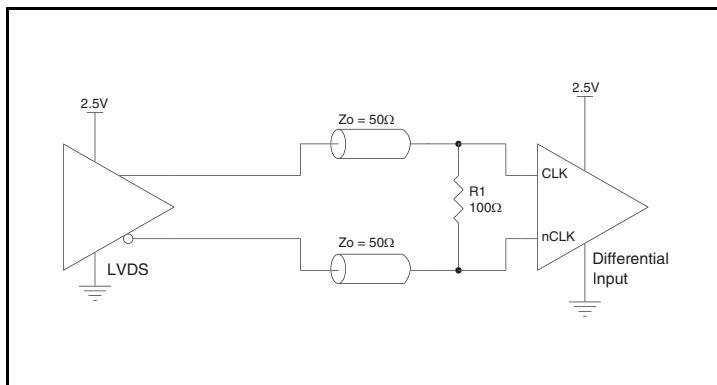
**Figure 4B.** CLK/nCLK Input Driven by a 2.5V LVPECL Driver



**Figure 4C.** CLK/nCLK Input Driven by a 2.5V LVPECL Driver



**Figure 4D.** CLK/nCLK Input Driven by a 2.5V HCSL Driver

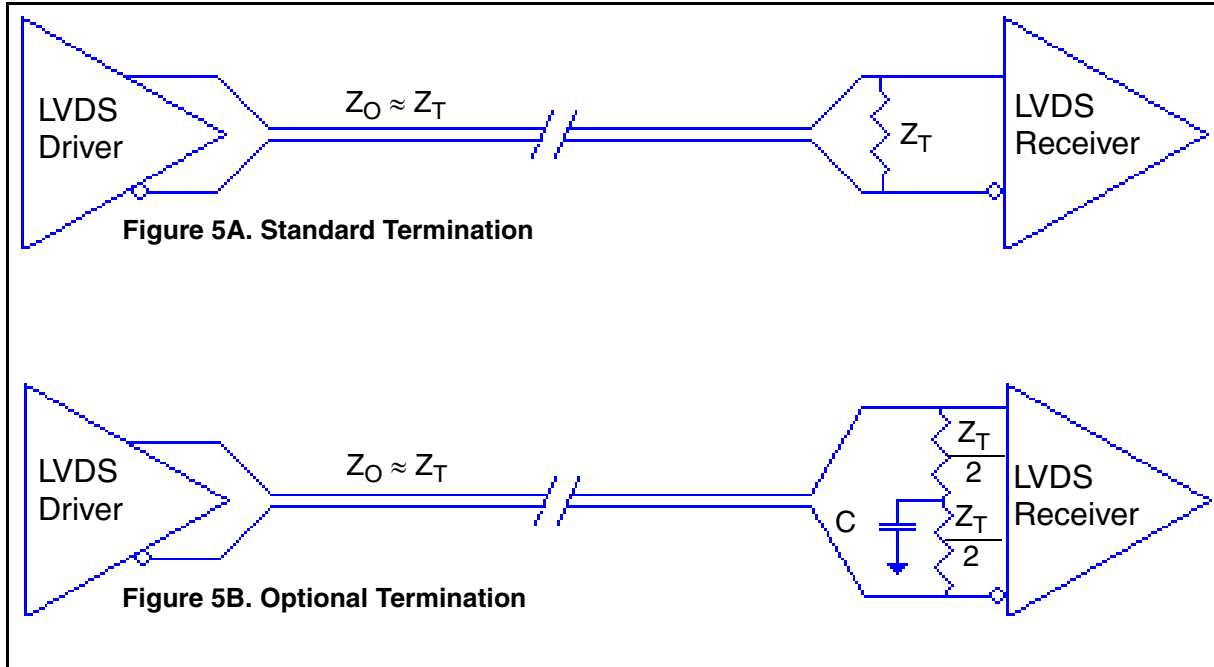


**Figure 4E.** CLK/nCLK Input Driven by a 2.5V LVDS Driver

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source type. The

standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



### LVDS Termination

## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

#### CLKx/nCLKx Inputs

For applications not requiring the use of either differential input, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from CLKx to ground.

#### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating there should be no trace attached.

#### LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 6A and 6B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

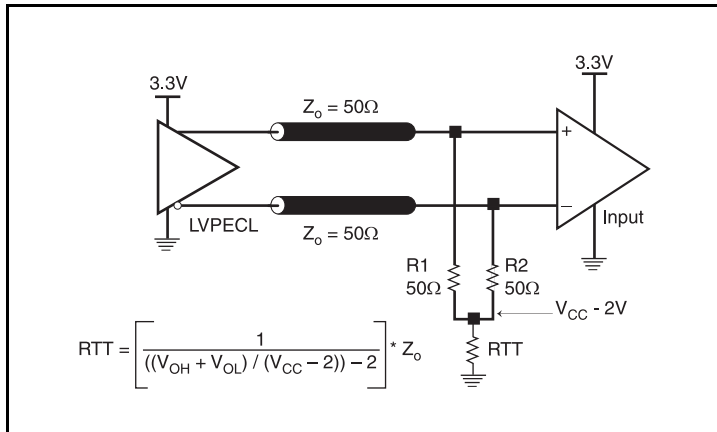


Figure 6A. 3.3V LVPECL Output Termination

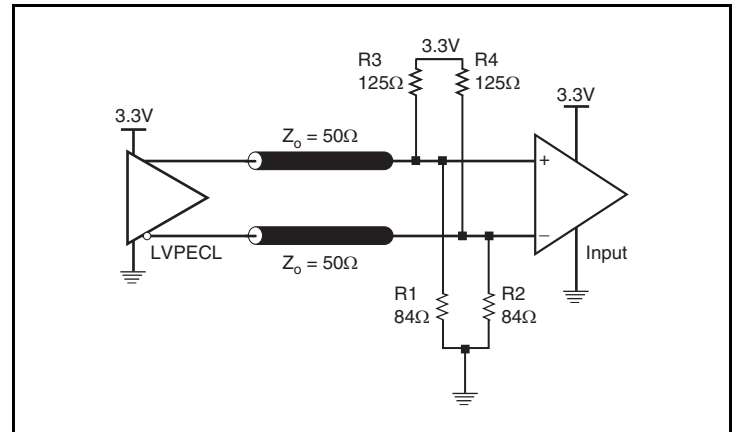


Figure 6B. 3.3V LVPECL Output Termination

### Termination for 2.5V LVPECL Outputs

Figure 7A and Figure 7B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC0} - 2V$ . For  $V_{CC0} = 2.5V$ , the  $V_{CC0} - 2V$  is very close to ground

level. The R3 in Figure7B can be eliminated and the termination is shown in Figure 7C.

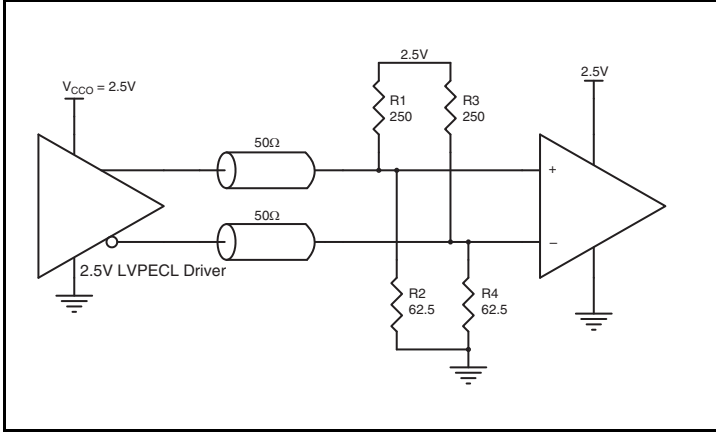


Figure 7A. 2.5V LVPECL Driver Termination Example

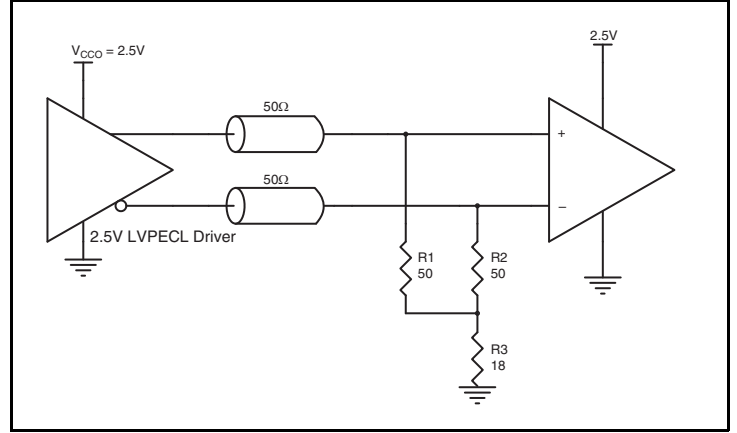


Figure 7B. 2.5V LVPECL Driver Termination Example

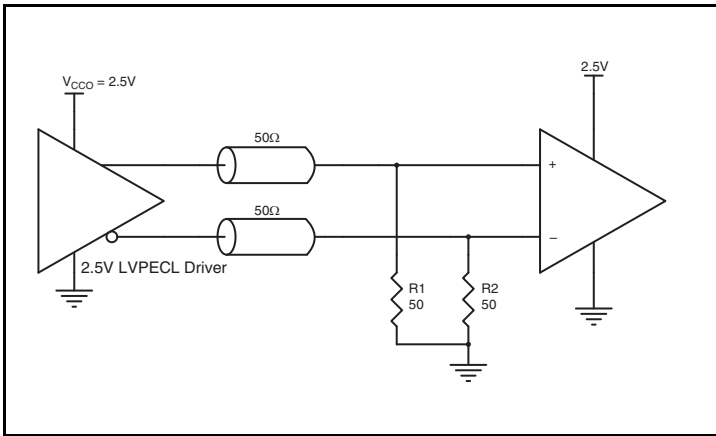


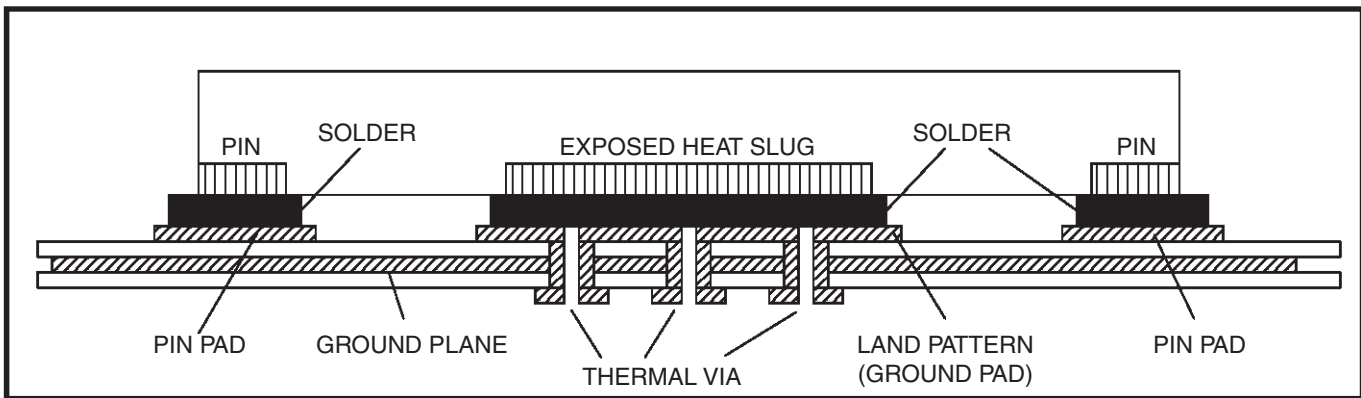
Figure 7C. 2.5V LVPECL Driver Termination Example

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 8*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Lead frame Base Package, Amkor Technology.



**Figure 8. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Schematic Layout

Figure 9 (next page) shows an example IDT8T49N222I application schematic. Input and output terminations shown are intended as examples only and may not represent the exact user configuration. In this example, the device is operated at  $V_{CC} = V_{CCO} = 3.3V$ . A Fox FX325BS Series 12pF parallel resonant 40MHz crystal is used in this example, though different crystal frequencies may be used. Load caps  $C1 = C2 = 2pF$  are recommended for frequency accuracy, but these may be adjusted for different board layouts. If different crystal types are used, please consult IDT for recommendations.

It is recommended that the loop filter components be laid out for the 3-pole option which can be adjusted for spur reduction and also allow for a simpler 2-pole filter when the internal phase detector frequency is high by setting R3 to  $0\Omega$  and not populating C3.

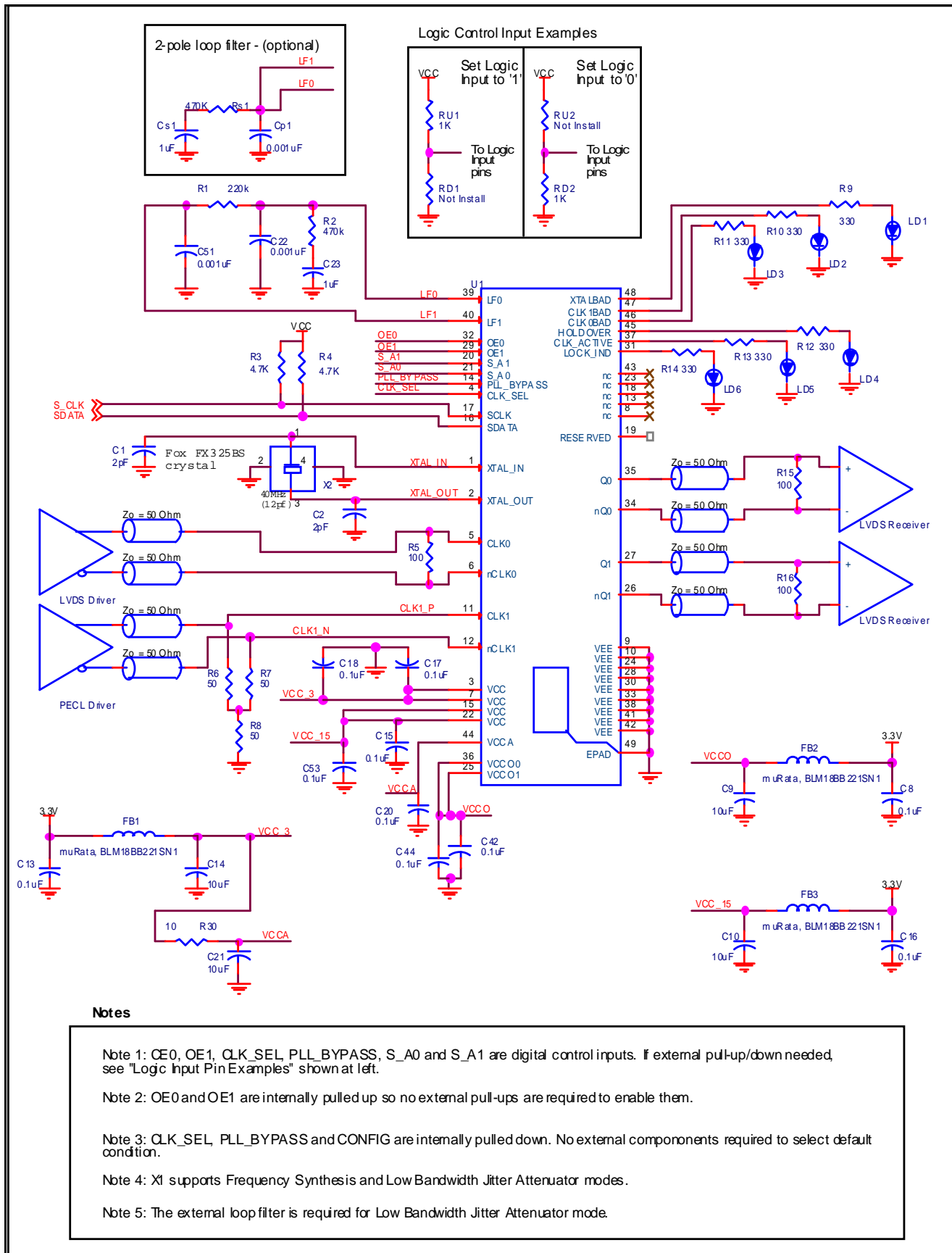
As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N222I provides separate  $V_{CC}$ ,  $V_{CCA}$  and  $V_{CCO}$  power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the

ferrite beads be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uF and 0.1uF capacitor connected to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.



**Notes**

Note 1: OE0, OE1, CLK\_SEL, PLL\_BYPASS, S\_A0 and S\_A1 are digital control inputs. If external pull-up/down needed, see "Logic Input Pin Examples" shown at left.

Note 2: OE0 and OE1 are internally pulled up so no external pull-ups are required to enable them.

Note 3: CLK\_SEL, PLL\_BYPASS and CONFIG are internally pulled down. No external components required to select default condition.

Note 4: X1 supports Frequency Synthesis and Low Bandwidth Jitter Attenuator modes.

Note 5: The external loop filter is required for Low Bandwidth Jitter Attenuator mode.

**Figure 9. IDT8T49N222I Application Schematic**



## LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N222I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8T49N222I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 358mA = 1240.47mW$
- Power (outputs)<sub>MAX</sub> = **33.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 33.2mW = 66.4mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $1240.47W + 66.4mW = 1306.8W$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 29°C/W per Table 9 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 1.307W * 29^\circ C/W = 122.9^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

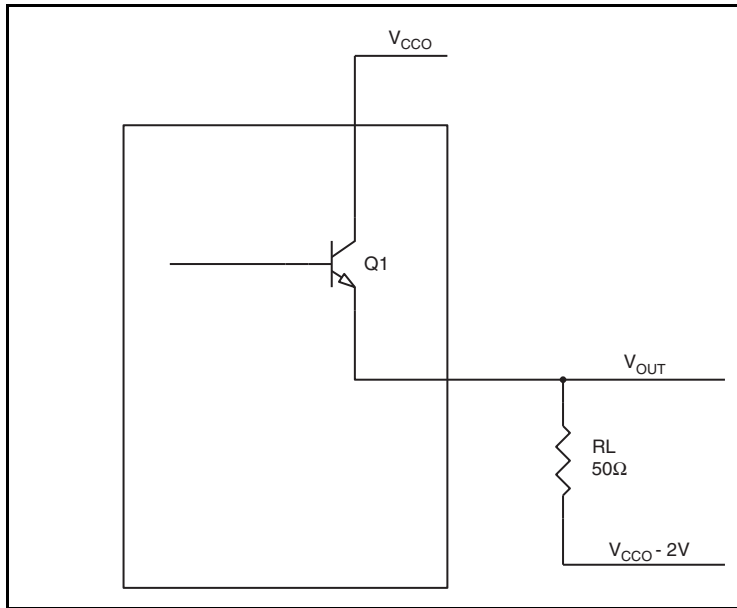
**Table 9. Thermal Resistance  $\theta_{JA}$  for 48 Lead VFQFN, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	22.88°C/W	20.62°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 10*.



**Figure 10. LVPECL Driver Circuit and Termination**

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.7V$   
 $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.7V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.5V$   
 $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.5V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.7V)/50\Omega] * 0.7V = \mathbf{18.2mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.5V)/50\Omega] * 1.5V = \mathbf{15mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{33.2mW}$$

## LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N222I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8T49N222I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{EE\_MAX} + I_{CCA\_MAX}) = 3.465V * (358mA + 30mA) = 1344.42mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 29°C/W per Table 10 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 1.344W * 29^\circ C/W = 124^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 10. Thermal Resistance  $\theta_{JA}$  for 48 Lead VFQFN, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	22.88°C/W	20.62°C/W

## Reliability Information

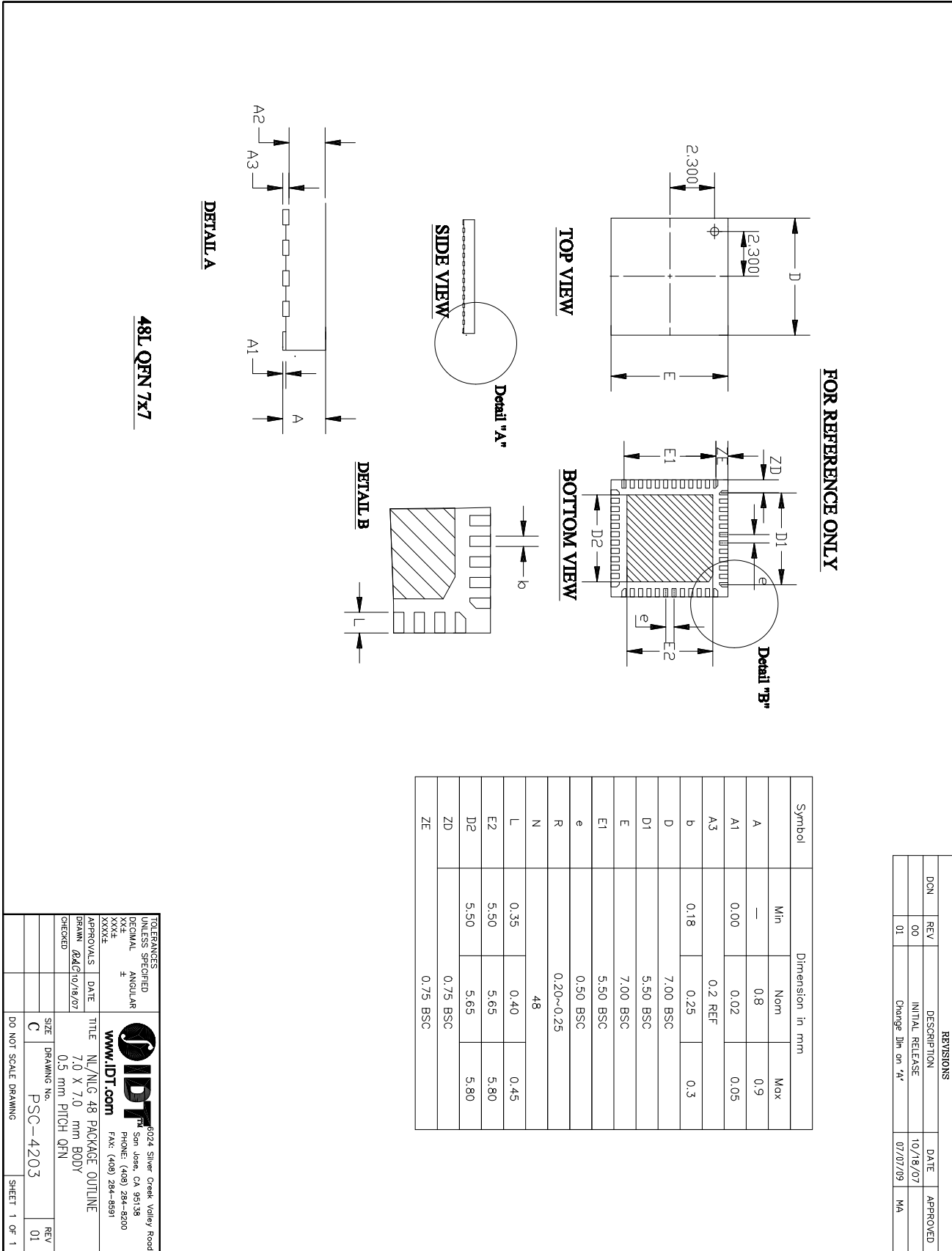
**Table 11.  $\theta_{JA}$  vs. Air Flow Table for a 48 Lead VFQFN**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	<b>0</b>	<b>1</b>	<b>2</b>
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	22.88°C/W	20.62°C/W

## Transistor Count

The transistor count for IDT8T49N222I is: 50,749

# 48 Lead VFQFN Package Outline and Package Dimensions



## Ordering Information

**Table 12. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N222B-dddNLGI	IDT8T49N222B-dddNLGI	"Lead-Free" 48 Lead VFQFN	Tray	-40°C to +85°C
8T49N222B-dddNLGI8	IDT8T49N222B-dddNLGI	"Lead-Free" 48 Lead VFQFN	Tape & Reel	-40°C to +85°C

NOTE: For the specific -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		32 - 32	Schematic Layout - Reference schematic was changed to show correct polarity on capacitors C17 & C18 and to add Recommended Crystal information.	5/13/2013

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