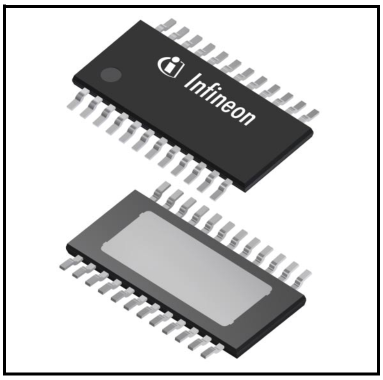
BTS71220-4ESE

SPOC™+2	**2x 9.5 mΩ**
SPI Power Controller	**2x 22.5 mΩ**

Package	PG-TSDSO-24-32
Marking	71220-4ESE



1 Overview

Potential Applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Driving capability suitable for 5 A and 3 A loads and high inrush current loads such as 55W bulb, HID or LED equivalent and 27W bulb or LED equivalent

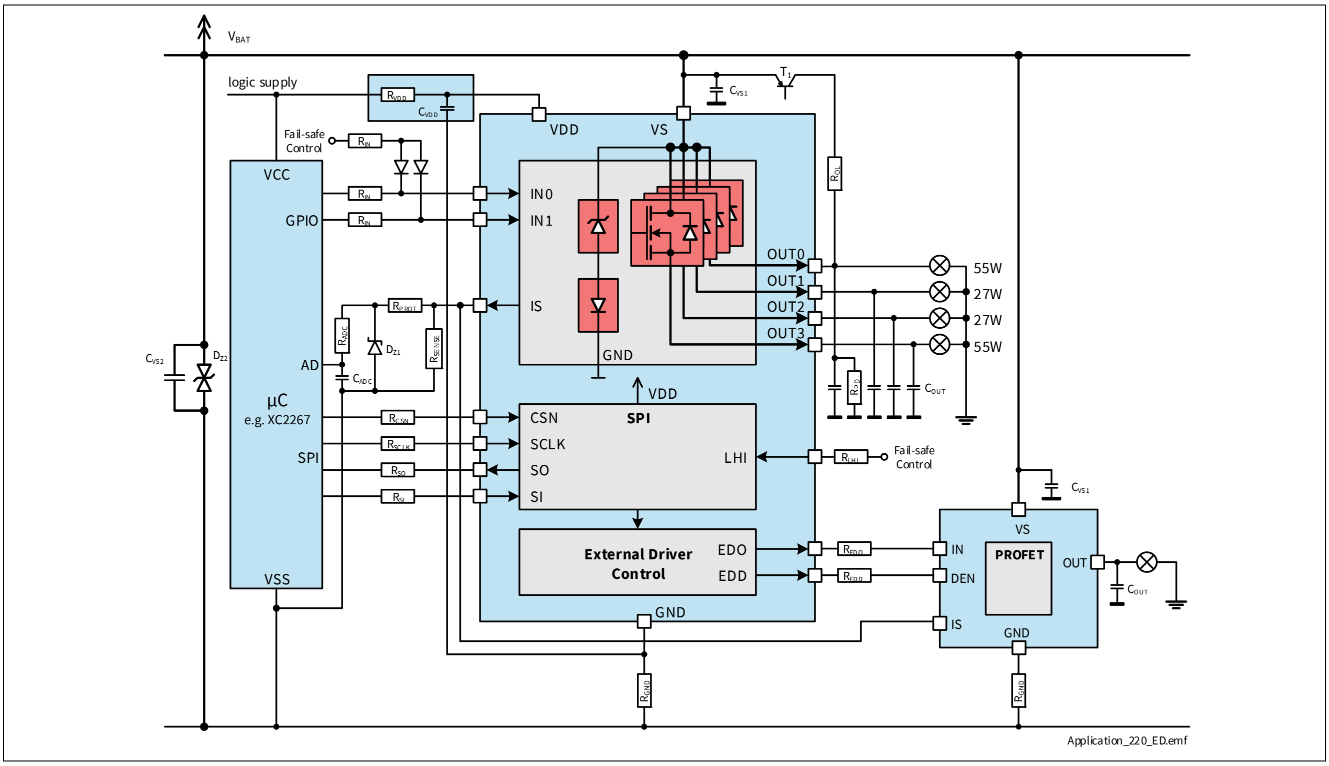

V_BAT
logic supply
R_VDD
C_VDD
Fail-safe Control
R_IN
VCC
GPIO
AD
μC
e.g. XC2267
SPI
VSS
C_VS2
D_Z2
R_ADC
D_Z1
C_ADC
R_PROT
R_SENSE
R_CSN
R_SCLK
R_SO
R_SI
VDD
VS
C_VS1
T_1
R_OL
IN0
IN1
IS
GND
OUT0
OUT1
OUT2
OUT3
55W
27W
27W
55W
R_PD
C_OUT
VDD
CSN
SPI
SCLK
SO
SI
LHI
R_LHI
Fail-safe Control
External Driver Control
EDO
EDD
R_EDO
R_EDD
GND
R_GND
VS
IN
DEN
IS
PROFET
OUT
GND
C_VS1
C_OUT
R_GND
Application_220_ED.emf

Figure 1 Application Diagram. Further information in Chapter 11

Overview

Basic Features

- High-Side Switch with Diagnosis and Embedded Protection
- Part of SPOC™+2 Family
- Daisy Chain capable SPI interface
- 3.3 V and 5 V compatible logic pins
- Slew rate control for internal Channels
- Integrated control for one external smart power switch
- ReverSave™ for low power dissipation in Reverse Polarity
- Switch ON capability while Inverse Current condition (InverseON)
- Green Product (RoHS compliant)
- Qualified in accordance with AEC Q100 grade 1

Protection Features

- Absolute and dynamic temperature limitation with controlled restart
- Overcurrent protection (tripping) with Programmable Restart Control and Current Threshold
- Undervoltage shutdown
- Overvoltage protection with external components

Diagnostic Features

- Proportional load current sense multiplexed
- Open Load in ON and OFF state
- Short circuit to ground and battery
- Diagnosis feedback via SPI

Functional Safety Features

- Limp Home mode
- Monitoring of Input pin status (IN and LHI)
- Checksum verification of Configuration Registers
- Current Sense verification mode

Description

The BTS71220-4ESE is a SPI Power Controller, providing protection functions and diagnosis. The device is integrated in SMART7 technology.

Table 1 Product Summary

Parameter	Symbol	Values
Minimum Operating voltage (at switch ON)	$V_{S(OP)}$	4.1 V
Minimum Operating voltage (cranking)	$V_{S(UV)}$	3.1 V
Maximum Operating voltage	V_S	28 V
Digital Supply voltage	V_{DD}	3.3 V or 5 V
Minimum Overvoltage protection ($T_J = 25$ °C)	$V_{DS(CLAMP)\_25}$	35 V
Maximum current in Sleep mode ($T_J \leq 85$ °C)	$I_{VS(SLEEP)\_85}$	0.7 µA

Table 1 Product Summary (continued)

Parameter	**Symbol**	**Values**
Maximum operative current	$I_{GND(ACTIVE)}$	7 mA
Maximum ON-state resistance (T_J = 150 °C) channels 0 and 3	$R_{DS(ON)\_150}$	16.5 mΩ
Maximum ON-state resistance (T_J = 150 °C) channels 1 and 2	$R_{DS(ON)\_150}$	38 mΩ
Nominal load current (T_A = 85 °C) channels 0 and 3	$I_{L(NOM)}$	5 A
Nominal load current (T_A = 85 °C) channels 1 and 2	$I_{L(NOM)}$	3 A
Typical current sense ratio at $I_L = I_{L(NOM)}$ channels 0 and 3	k_{ILIS}	5000
Typical current sense ratio at $I_L = I_{L(NOM)}$ channels 1 and 2	k_{ILIS}	2000
SPI clock frequency	$f_{SCLK(max)}$	5 MHz

2 Block Diagram and Terms

2.1 Block Diagram

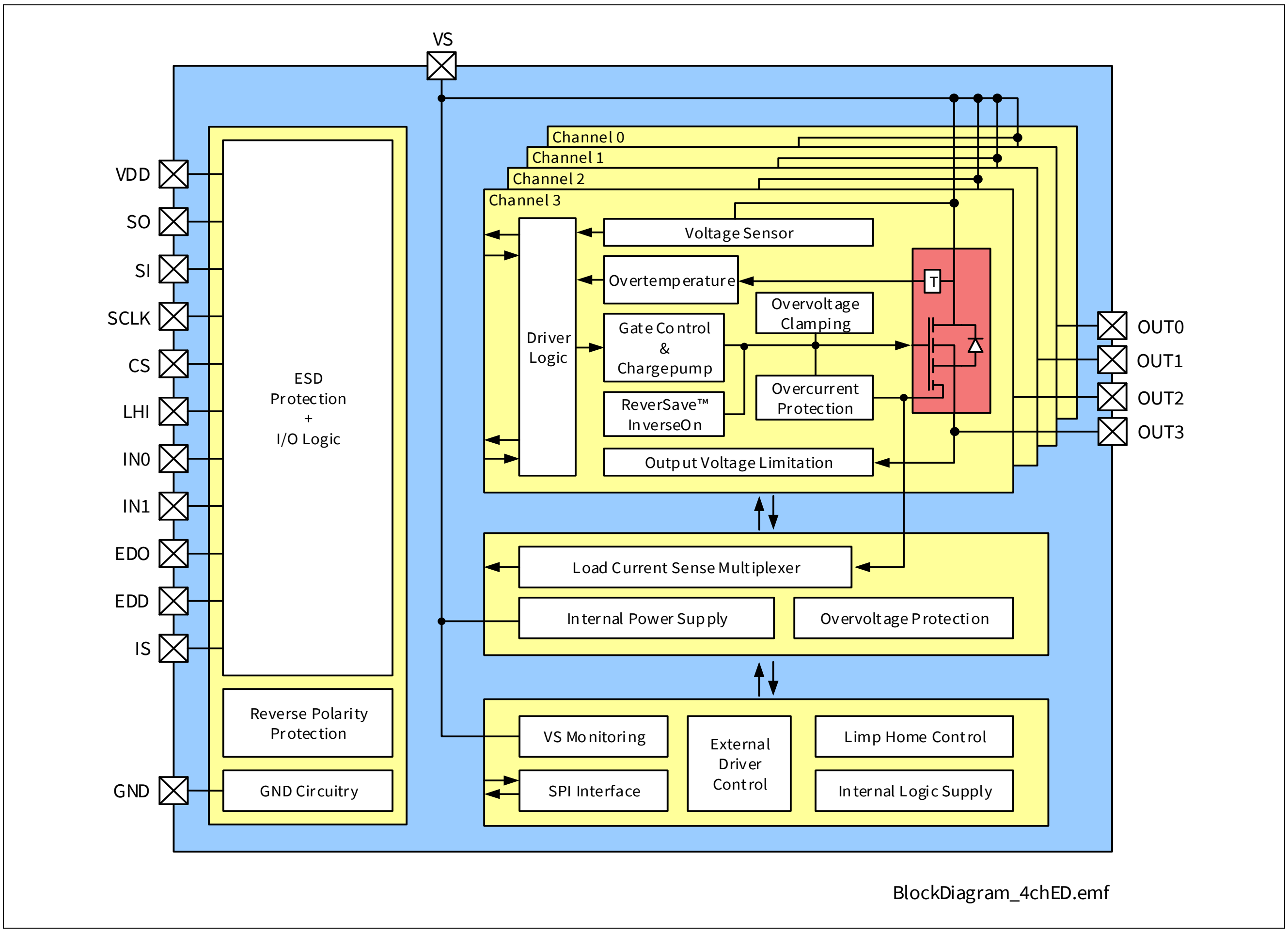

VS
VDD
SO
SI
SCLK
CS
LHI
IN0
IN1
EDO
EDD
IS
GND
ESD
Protection
+
I/O Logic
Reverse Polarity
Protection
GND Circuitry
Channel 0
Channel 1
Channel 2
Channel 3
Driver
Logic
Voltage Sensor
Overtemperature
Overvoltage
Clamping
Gate Control
&
Chargepump
ReverSave™
InverseOn
Overcurrent
Protection
Output Voltage Limitation
T
OUT0
OUT1
OUT2
OUT3
Load Current Sense Multiplexer
Internal Power Supply
Overvoltage Protection
VS Monitoring
External
Driver
Control
Limp Home Control
SPI Interface
Internal Logic Supply
BlockDiagram_4chED.emf

Figure 2 **Block Diagram of BTS71220-4ESE**

2.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

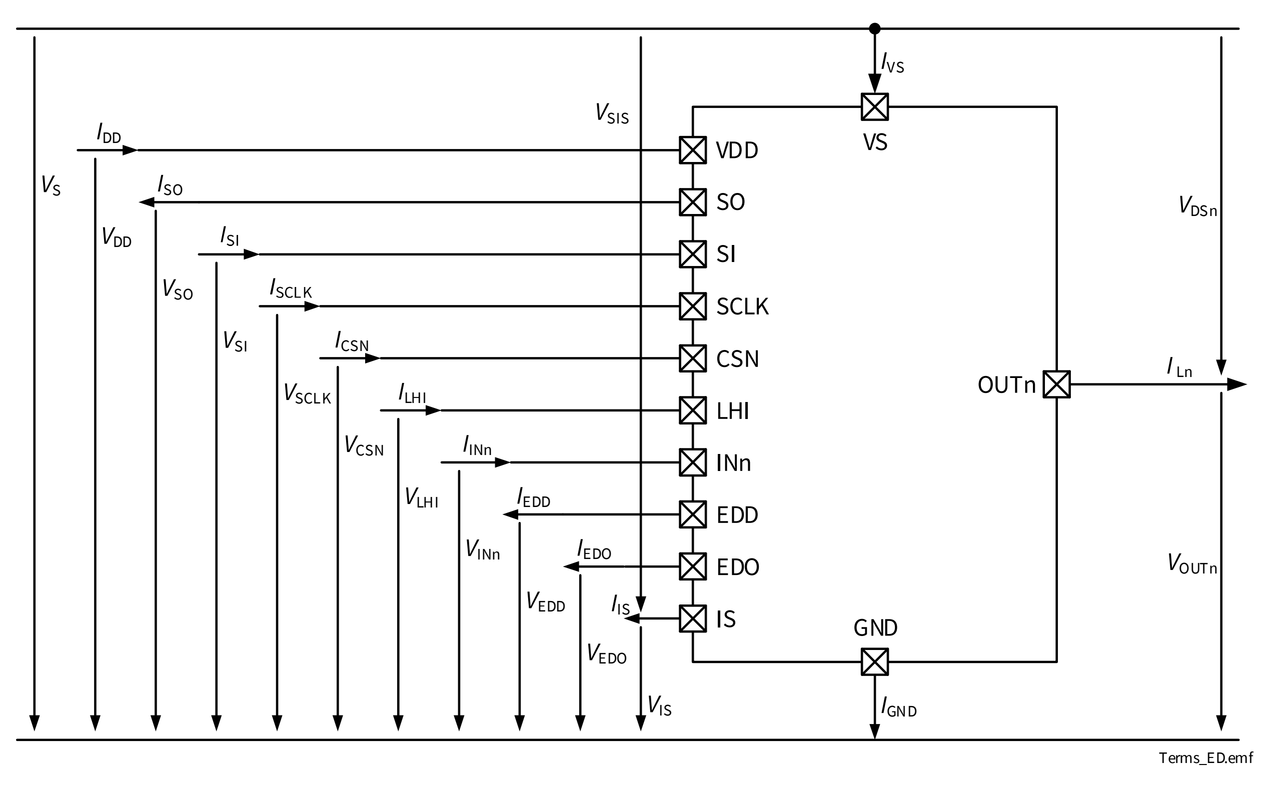

I_{VS}
V_{SIS}
I_{DD}
VDD
VS
V_S
I_{SO}
SO
V_{DSn}
V_{DD}
I_{SI}
SI
V_{SO}
I_{SCLK}
SCLK
V_{SI}
I_{CSN}
CSN
OUTn
I_{Ln}
V_{SCLK}
I_{LHI}
LHI
V_{CSN}
I_{INn}
INn
V_{LHI}
I_{EDD}
EDD
V_{INn}
I_{EDO}
EDO
V_{OUTn}
V_{EDD}
I_{IS}
IS
GND
V_{EDO}
V_{IS}
I_{GND}
Terms_ED.emf

Figure 3 **Voltage and Current Convention**

3 Pin Configuration

3.1 Pin Assignment

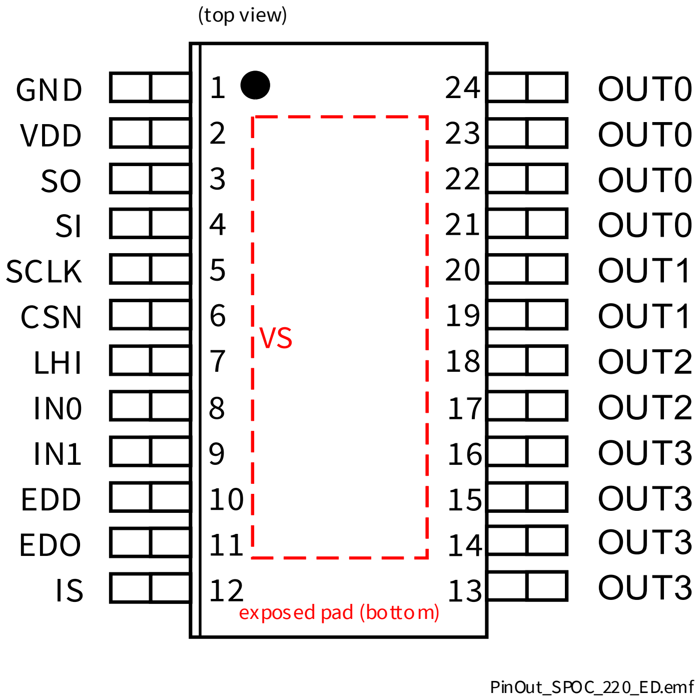

(top view)
GND
VDD
SO
SI
SCLK
CSN
LHI
IN0
IN1
EDD
EDO
IS
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
OUT0
OUT0
OUT0
OUT0
OUT1
OUT1
OUT2
OUT2
OUT3
OUT3
OUT3
OUT3
VS
exposed pad (bottom)
PinOut_SPOC_220_ED.emf

Figure 4 Pin Configuration

3.2 Pin Definitions and Functions

Table 2 Pin Definition

Pin	Symbol	I/O	Function
EP	VS (exposed pad)	-	**Power Supply Voltage** Battery voltage
1	GND	-	**Ground**
2	VDD	-	**Digital Supply Voltage**
3	SO	O	**Serial output of SPI interface**
4	SI	I	**Serial input of SPI interface (“high” active)**
5	SCLK	I	**Serial clock of SPI interface (“high” active)**
6	CSN	I	**Chip select of SPI interface (“low” active); integrated pull up to VDD**
7	LHI	I	**Limp Home activation signal (“high” active)**
8, 9	INn	I	**Input Channel n** Digital signal to switch ON the channel n (“high” active) If not used: connect with a 10 kΩ resistor either to GND pin or to module ground
10	EDD	O	**External driver diagnosis enable signal** Digital signal to activate the diagnosis of an external controlled device
11	EDO	O	**External driver output enable signal** Digital signal to activate the output of an external controlled device
12	IS	O	**Current sense output signal**
21-24 19-20 17-18 13-16	OUTn	O	**Output n** Protected high-side power output of channel n(1)

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

4 General Product Characteristics

4.1 Absolute Maximum Ratings - General

Table 3 Absolute Maximum Ratings[1]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply pins							
Power Supply Voltage	V_S	-0.3	–	28	V	–	P_4.1.0.1
Digital Supply Voltage	V_{DD}	-0.3	–	5.5	V	–	P_4.1.0.29
Load Dump Voltage	$V_{BAT(LD)}$	–	–	35	V	suppressed Load Dump acc. to ISO16750-2 (2010). R_i = 2 Ω	P_4.1.0.3
Supply Voltage for Short Circuit Protection	$V_{BAT(SC)}$	0	–	24	V	Setup acc. to AEC-Q100-012	P_4.1.0.25
Reverse Polarity Voltage	$-V_{BAT(REV)}$	–	–	16	V	$t \leq 2$ min T_A = +25 °C Setup as described in **Chapter 11**	P_4.1.0.5
Current through GND Pin	I_{GND}	-50	–	50	mA	R_{GND} according to **Chapter 11**	P_4.1.0.9
Current through VDD Pin	$I_{VDD(REV)}$	-10	–	30	mA	$t \leq 2$ min	P_4.1.0.10
Counter Reset Delay Time after Fault Condition	t_{RETRY}	50	–	–	ms	–	P_4.1.0.35
Logic & control pins (Digital Input = DI) **DI = INn, CS, SCLK, SI, LHI**							
Current through DI Pin	I_{DI}	-1	–	2	mA	[2]	P_4.1.0.14
Current through DI Pin Reverse Battery Condition	$I_{DI(REV)}$	-1	–	10	mA	[2] $t \leq 2$ min	P_4.1.0.36
Logic & control pins (Digital Output = DO) **DO = SO, EDO, EDD**							
Current through DO Pin	I_{DO}	-2	–	1	mA	[2]	P_4.1.0.33
Current through DO Pin Reverse Battery Condition	$I_{DO(REV)}$	-10	–	1	mA	[2] $t \leq 2$ min	P_4.1.0.37

Table 3 Absolute Maximum Ratings[1] (continued)

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
IS pin							
Voltage at IS Pin	V_{IS}	-1.5	–	V_S	V	I_{IS} = 10 µA	P_4.1.0.16
Current through IS Pin	I_{IS}	-25	–	$I_{IS(SAT),MAX}$	mA	–	P_4.1.0.18
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.0.19
Storage Temperature	T_{STG}	-55	–	150	°C	–	P_4.1.0.20
ESD Susceptibility							
ESD Susceptibility all Pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	HBM[3]	P_4.1.0.21
ESD Susceptibility OUTn vs GND and VS connected (HBM)	$V_{ESD(HBM)\_OUT}$	-4	–	4	kV	HBM[3]	P_4.1.0.22
ESD Susceptibility all Pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	CDM[4]	P_4.1.0.23
ESD Susceptibility Corner Pins (pins 1, 12, 13, 24)	$V_{ESD(CDM)\_CRN}$	-750	–	750	V	CDM[4]	P_4.1.0.24

1) Not subject to production test - specified by design.
2) Maximum V_{DI} to be considered for Latch-Up tests: 5.5 V.
3) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002.
4) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Absolute Maximum Ratings - Power Stages

4.2.1 Power Stages - 55 W channels

Table 4 Absolute Maximum Ratings - 55 W channels[1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum Energy Dissipation Single Pulse Channel 0, 3	E_{AS}	–	–	55	mJ	$I_L = 2^*I_{L(NOM)}$ $T_{J(0)}$ = 150 °C V_S = 28 V	P_4.2.15.1
Maximum Energy Dissipation Repetitive Pulse Channel 0, 3	E_{AR}	–	–	24	mJ	$I_L = I_{L(NOM)}$ $T_{J(0)}$ = 85 °C V_S = 13.5 V 1M cycles	P_4.2.15.2
Load Current	$\|I_L\|$	–	–	$I_{L(OVL),MAX}$	A	–	P_4.2.15.3

1) Not subject to production test - specified by design.

4.2.2 Power Stages - 27 W channels

Table 5 Absolute Maximum Ratings - 27 W channels[1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum Energy Dissipation Single Pulse Channel 1, 2	E_{AS}	–	–	28	mJ	$I_L = 2^*I_{L(NOM)}$ $T_{J(0)}$ = 150 °C V_S = 28 V	P_4.2.16.1
Maximum Energy Dissipation Repetitive Pulse Channel 1, 2	E_{AR}	–	–	8.5	mJ	$I_L = I_{L(NOM)}$ $T_{J(0)}$ = 85 °C V_S = 13.5 V 1M cycles	P_4.2.16.2
Load Current	$\|I_L\|$	–	–	$I_{L(OVL),MAX}$	A	–	P_4.2.16.3

1) Not subject to production test - specified by design.

4.3 Functional Range

Table 6 Functional Range - Supply Voltages and Temperature[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	6	13.5	18	V	–	P_4.3.0.1
Lower Extended Power Supply Voltage Range for Operation	$V_{S(EXT,LOW)}$	3.1	–	6	V	[2)3)] (parameter deviations possible)	P_4.3.0.2
Upper Extended Power Supply Voltage Range for Operation	$V_{S(EXT,UP)}$	18	–	28	V	[3)] (parameter deviations possible)	P_4.3.0.3
Digital Supply Voltage Range	$V_{DD(NOR)}$	3.0	–	5.5	V	–	P_4.3.0.4
Junction Temperature	T_J	-40	–	150	°C	–	P_4.3.0.5

1) Not subject to production test - specified by design.
2) In case of V_S voltage decreasing: $V_{S(EXT,LOW),MIN}$ = 3.1 V. In case of V_S voltage increasing: $V_{S(EXT,LOW),MIN}$ = 4.1 V.
3) Protection functions still operative.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics tables.

4.4 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Table 7 Thermal Resistance[1]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Characterization Parameter Junction-Top	Ψ_{JTOP}	–	3	5	K/W	[2]	P_4.4.0.4
Thermal Resistance Junction-to-Case	R_{thJC}	–	3	5	K/W	[2] simulated at exposed pad	P_4.4.0.5
Thermal Resistance Junction to Ambient	R_{thJA}	–	26	–	K/W	[2]	P_4.4.0.6

1) Not subject to production test - specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_A = 105°C, $P_{DISSIPATION}$ = 1 W.

4.4.1 PCB Setup

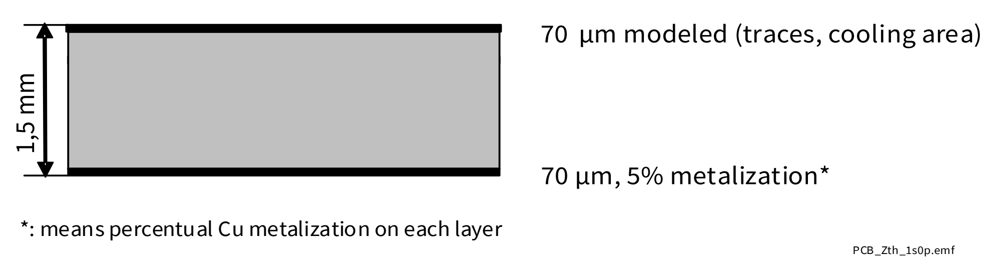

1,5 mm
70 µm modeled (traces, cooling area)
70 µm, 5% metalization*
*: means percentual Cu metalization on each layer
PCB_Zth_1s0p.emf

Figure 5 1s0p PCB Cross Section

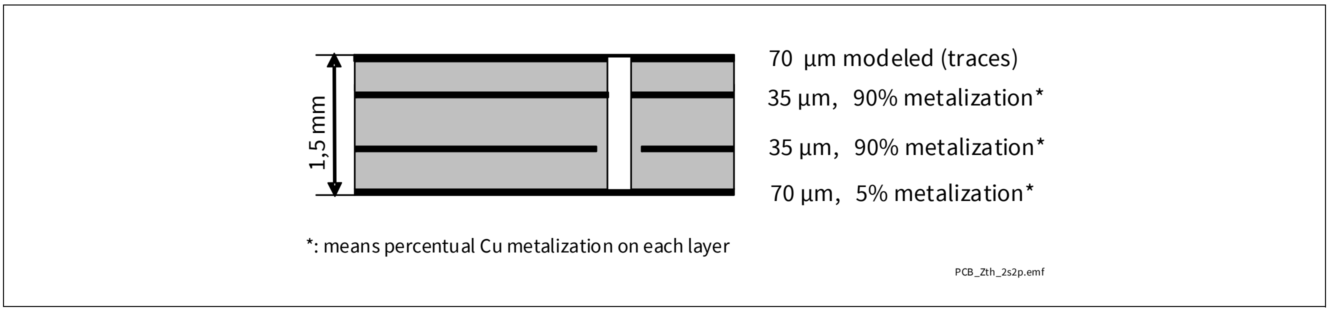
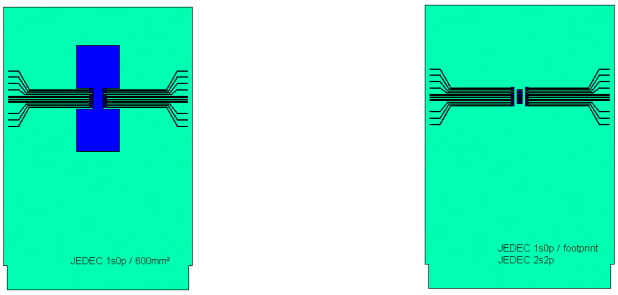

1,5 mm
70 µm modeled (traces)
35 µm, 90% metalization*
35 µm, 90% metalization*
70 µm, 5% metalization*
*: means percentual Cu metalization on each layer
PCB_Zth_2s2p.emf

Figure 6 2s2p PCB Cross Section


JEDEC 1s0p / 600mm²
JEDEC 1s0p / footprint
JEDEC 2s2p

PCB 1s0p + 600 mm² cooling

PCB 2s2p / 1s0p footprint

PCB_sim_setup_TSDSO24.emf

Figure 7 PCB setup for thermal simulations

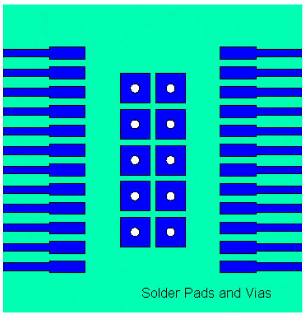

Solder Pads and Vias
PCB_2s2p_vias_TSDSO24.emf

Figure 8 Thermal vias on PCB for 2s2p PCB setup

4.4.2 Thermal Impedance

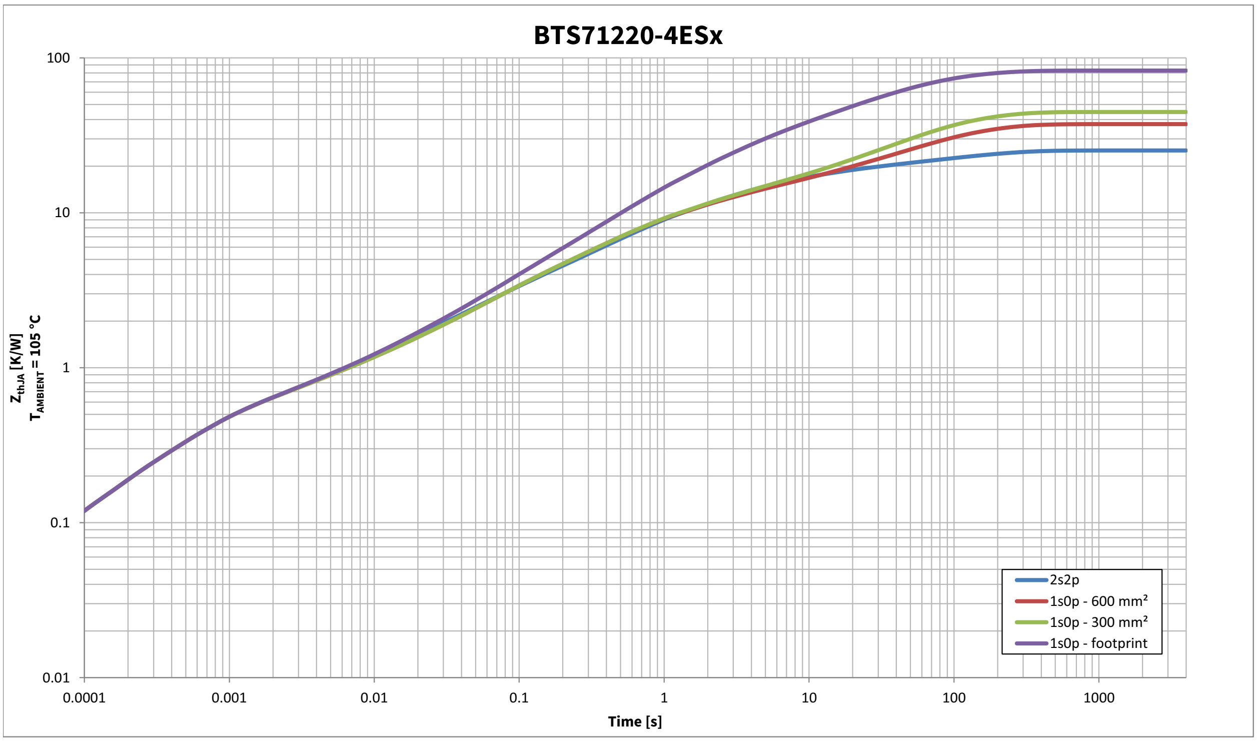


Figure 9 Typical Thermal Impedance. PCB setup according Chapter 4.4.1

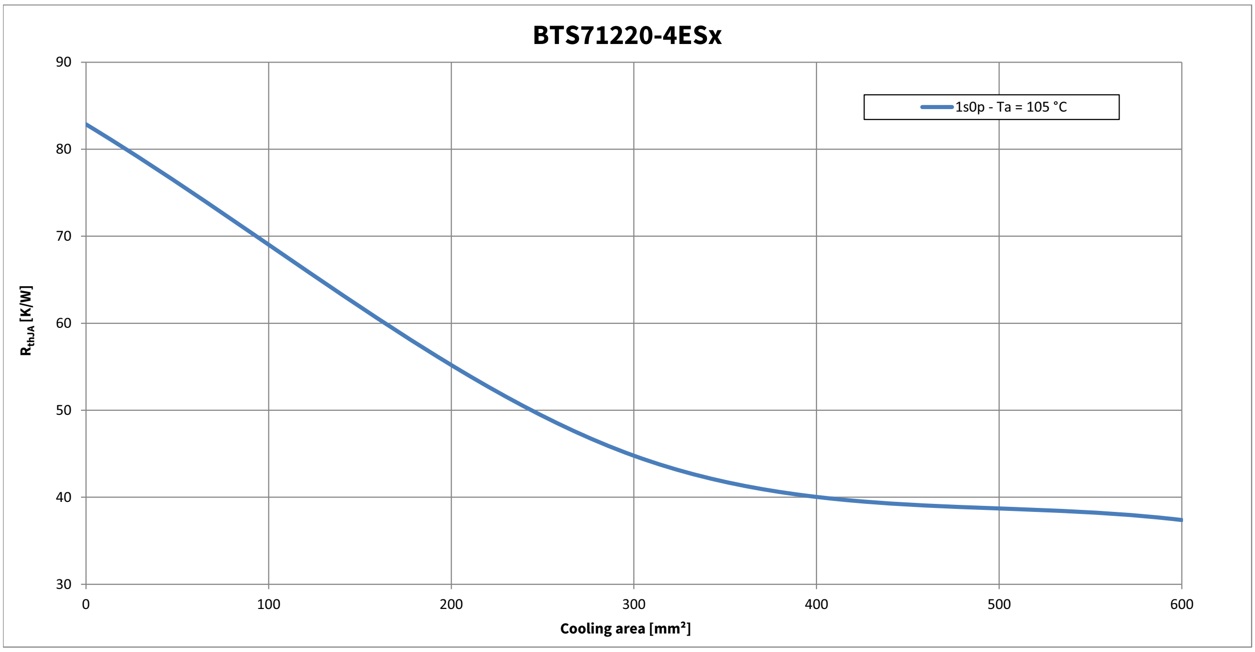


Figure 10 Thermal Resistance on 1s0p PCB with various cooling surfaces

5 Logic Pins

The device has 9 digital pins to configure and control the device. They can be grouped based on their function into input pins, SPI pins, external driver pins and Limp Home pin.

5.1 Input Pins (INn)

The input pins IN0 and IN1 activate the corresponding output channel, if the device is either in Sleep, Stand-by, Ready or in Limp Home mode. The input circuitry is compatible with 3.3V and 5V microcontroller. The electrical equivalent of the input circuitry is shown in **Figure 11**. In case the pin is not used, it must be connected with a 10 kΩ resistor either to GND pin or to module ground.

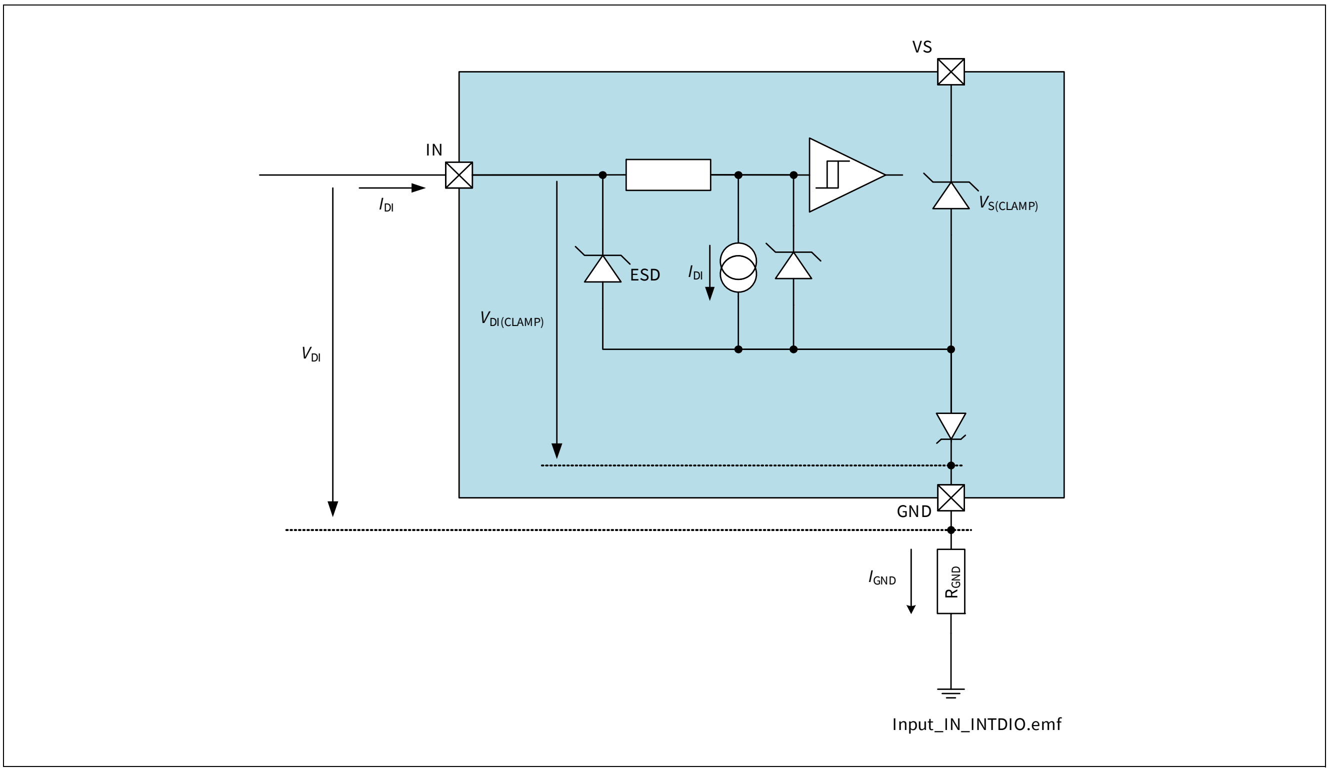


Figure 11 **Input circuitry**

The logic thresholds for “low” and “high” states are defined by parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in **Figure 12**. The voltage V_{IN} needed to ensure a “high” state is always higher than the voltage needed to ensure a “low” state.

Logic Pins

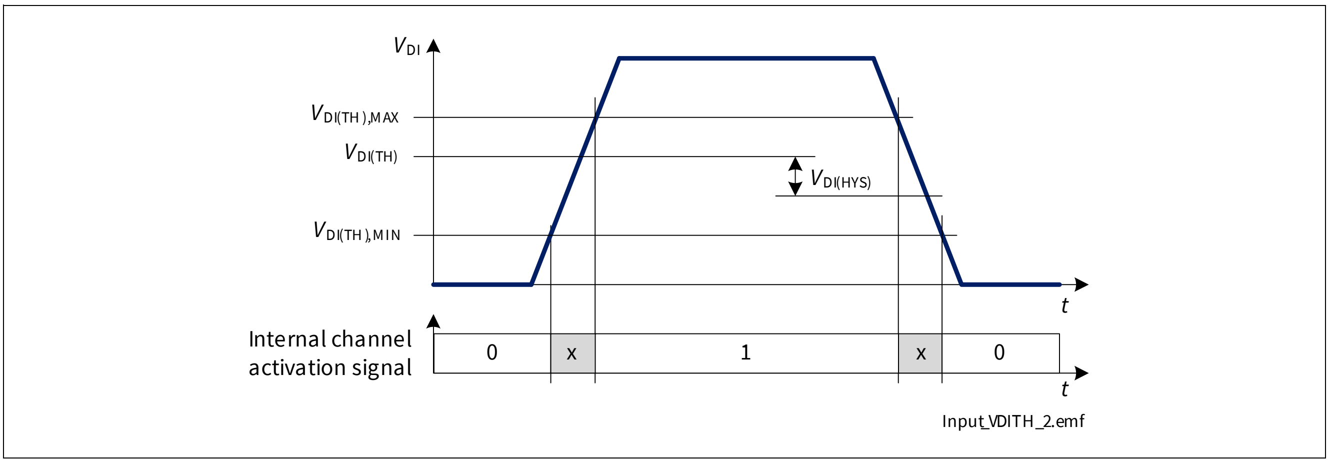


Figure 12 Input Threshold voltages and hysteresis

There are two ways of using the input pins in combination with the register **OUT** by programming bit **HWCR.COL** in register **HWCR** (see **Table 35**).

- **HWCR.COL** = 0_B: A channel is switched ON either by the according **OUT.OUTn** bit or by the input pin.
- **HWCR.COL** = 1_B: A channel is switched ON by the according **OUT.OUTn** bit only, when the input pin is "high". In this configuration, a PWM signal can be applied to the input pin and the channel is activated by the SPI register **OUT** (see **Table 35**).

The default state (**HWCR.COL** = 0_B) is the OR-combination of the input signal and the SPI-bit. In Limp Home mode (LHI pin set to "high") the combinatorial logic is in default state to enable a channel activation via the input pins only. **Figure 13** shows the complete input switch matrix.

The logic level of the input pins can be monitored via the input status monitor. In case of a "high" level on an input pin, the corresponding **ICS.INSTn** bit is set and cleared on read.

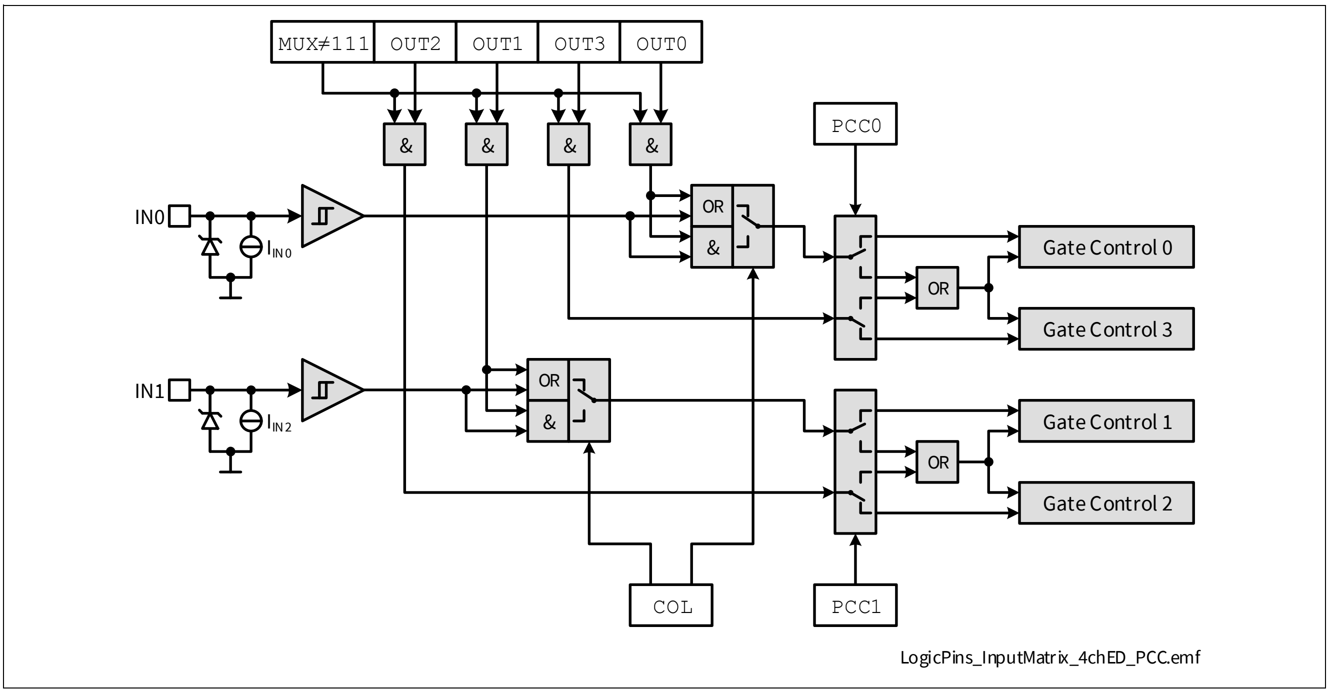

MUX≠111
OUT2
OUT1
OUT3
OUT0
&
PCC0
IN0
I_{IN0}
OR
&
Gate Control 0
OR
Gate Control 3
IN1
I_{IN2}
OR
&
Gate Control 1
OR
Gate Control 2
COL
PCC1
LogicPins_InputMatrix_4chED_PCC.emf

Figure 13 Input Switch Matrix

5.2 Advanced Features Pins

5.2.1 SPI Pins

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN. See **Chapter 10** for further information.

5.2.2 Limp Home Input (LHI) Pin

For activating the fail-safe state, the device features a Limp Home Input pin. When the pin is set to “high” for a time longer than $t_{LHI(AC)}$, the Limp Home mode will be activated. See **Chapter 6.1.7** and **Chapter 6.1.8** for further information.

5.2.3 External Driver Pins

One external smart power driver can be controlled by the BTS71220-4ESE via the external driver control block. There are two control outputs available: one output for controlling the input (EDO) and one output for diagnosis enable input (EDD). The current sense output of the external smart power driver can be connected to the IS pin. For details please refer to the Application Circuit Example in **Chapter 11**. The external driver output signals can be used in Stand-by and Active mode.

The external driver can be activated via SPI bit **`OUT.OUT4`**.

Note: The usable duty cycle range and diagnostic timings depend on the external driver’s characteristics.

5.3 Electrical Characteristics Logic Pins

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Digital Input (DI) pins = IN

Table 8 Electrical Characteristics: Logic Pins - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Input Voltage Threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See **Figure 11** and **Figure 12**	P_5.4.0.1
Digital Input Clamping Voltage	$V_{DI(CLAMP1)}$	–	7	–	V	[1)] I_{DI} = 1 mA See **Figure 11** and **Figure 12**	P_5.4.0.2
Digital Input Clamping Voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	I_{DI} = 2 mA See **Figure 11** and **Figure 12**	P_5.4.0.3
Digital Input Hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	[1)] See **Figure 11** and **Figure 12**	P_5.4.0.4
Digital Input Current (“high”)	$I_{DI(H)}$	2	10	25	µA	V_{DI} = 2 V See **Figure 11** and **Figure 12**	P_5.4.0.5
Digital Input Current (“low”)	$I_{DI(L)}$	2	10	25	µA	V_{DI} = 0.8 V See **Figure 11** and **Figure 12**	P_5.4.0.6

1) Not subject to production test - specified by design.

5.4 Electrical Characteristics Logic Pins - Advanced Features

Table 9 Electrical Characteristics: Logic Pins - Advanced

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI pins							
Digital Input Voltage Threshold of Pin CSN	$V_{CSN(TH)}$	0.8	1.3	2	V	–	P_5.5.0.1
Digital Input Voltage Threshold of Pin SCLK	$V_{SCLK(TH)}$	0.8	1.3	2	V	[1)]	P_5.5.0.2
Digital Input Voltage Threshold of Pin SI	$V_{SI(TH)}$	0.8	1.3	2	V	–	P_5.5.0.3
Digital Input Clamping Voltage of Pin CSN	$V_{CSN(CLAMP1)}$	–	7	–	V	[2)] I_{CSN} = 1 mA	P_5.5.0.4
Digital Input Clamping Voltage of Pin CSN	$V_{CSN(CLAMP2)}$	6.5	7.5	8.5	V	I_{CSN} = 2 mA	P_5.5.0.5

Table 9 Electrical Characteristics: Logic Pins - Advanced (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Input Clamping Voltage of Pin SCLK	$V_{SCLK(CLAMP1)}$	–	7	–	V	[2] I_{SCLK} = 1 mA	P_5.5.0.6
Digital Input Clamping Voltage of Pin SCLK	$V_{SCLK(CLAMP2)}$	6.5	7.5	8.5	V	I_{SCLK} = 2 mA	P_5.5.0.7
Digital Input Clamping Voltage of Pin SI	$V_{SI(CLAMP1)}$	–	7	–	V	[2] I_{SI} = 1 mA	P_5.5.0.8
Digital Input Clamping Voltage of Pin SI	$V_{SI(CLAMP2)}$	6.5	7.5	8.5	V	I_{SI} = 2 mA	P_5.5.0.9
Digital Input Hysteresis of Pin CSN	$V_{CSN(HYS)}$	–	0.25	–	V	[2] See **Figure 12**	P_5.5.0.11
Digital Input Hysteresis of Pin SCLK	$V_{SCLK(HYS)}$	–	0.25	–	V	[2] See **Figure 12**	P_5.5.0.13
Digital Input Hysteresis of Pin SI	$V_{SI(HYS)}$	–	0.25	–	V	[2] See **Figure 12**	P_5.5.0.15
Digital Input Current ("low") of Pin CSN	$-I_{CSN(L)}$	2	10	25	µA	V_{CSN} = 0.5 V	P_5.5.0.10
Digital Input Current ("high") of Pin CSN	$-I_{CSN(H)}$	2	10	25	µA	V_{CSN} = 2.6 V	P_5.5.0.12
Digital Input Current ("low") of Pin SCLK	$I_{SCLK(L)}$	2	10	25	µA	V_{SCLK} = 0.5 V	P_5.5.0.14
Digital Input Current ("high") of Pin SCLK	$I_{SCLK(H)}$	2	10	25	µA	V_{SCLK} = 2.6 V	P_5.5.0.16
Digital Input Current ("low") of Pin SI	$I_{SI(L)}$	2	10	25	µA	V_{SI} = 0.5 V	P_5.5.0.18
Digital Input Current ("high") of Pin SI	$I_{SI(H)}$	2	10	25	µA	V_{SI} = 2.6 V	P_5.5.0.20
Digital Output Voltage ("low") of Pin SO	$V_{SO(L)}$	0	–	0.5	V	I_{SO} = -0.5 mA	P_5.5.0.22
Digital Output Voltage ("high") of Pin SO	$V_{SO(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{SO} = 0.5 mA	P_5.5.0.23
Output Tristate Leakage Current of Pin SO	$I_{SO(OFF)}$	-1	–	1	µA	$V_{CSN} = V_{DD}$ V_{SO} = 0 V or $V_{CSN} = V_{DD}$ $V_{SO} = V_{DD}$	P_5.5.0.24
LHI pin							
Digital Input Voltage Threshold of Pin LHI	$V_{LHI(TH)}$	1.4	1.9	2.6	V	–	P_5.5.0.25
Digital Input Clamping Voltage of Pin LHI	$V_{LHI(CLAMP1)}$	–	7	–	V	[2] I_{LHI} = 1 mA	P_5.5.0.27
Digital Input Clamping Voltage of Pin LHI	$V_{LHI(CLAMP2)}$	6.5	7.5	8.5	V	I_{LHI} = 2 mA	P_5.5.0.28

Table 9 Electrical Characteristics: Logic Pins - Advanced (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Input Hysteresis of Pin LHI	$V_{LHI(HYS)}$	–	0.25	–	V	[2]	P_5.5.0.29
Digital Input Current (“high”) of Pin LHI	$I_{LHI(H)}$	10	32	65	µA	V_{LHI} = 5 V V_{DD} = 0 V	P_5.5.0.30
Digital Input Current (“low”) of Pin LHI	$I_{LHI(L)}$	10	24	45	µA	V_{LHI} = 0.8 V V_{DD} = 0 V	P_5.5.0.32
External Driver Pins							
Digital Output Voltage (“low”) of Pin EDO	$V_{EDO(L)}$	0	–	0.5	V	I_{EDO} = -0.2 mA	P_5.5.0.33
Digital Output Voltage (“high”) of Pin EDO	$V_{EDO(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{EDO} = 0.2 mA	P_5.5.0.34
Digital Output Voltage (“low”) of Pin EDD	$V_{EDD(L)}$	0	–	0.5	V	I_{EDD} = -0.2 mA	P_5.5.0.36
Digital Output Voltage (“high”) of Pin EDD	$V_{EDD(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{EDD} = 0.2 mA	P_5.5.0.37

1) Functional test only.

2) Not subject to production test - specified by design.

6 Power Supply

The BTS71220-4ESE is supplied by two supply voltages:

- Power Supply Voltage (V_S)
- Digital Supply Voltage (V_{DD})

The V_S supply line is connected to a battery feed and used for the driving circuitry of the power stages, while V_{DD} is used for the SPI logic and for driving SO pin. V_S and V_{DD} supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the undervoltage threshold. More in detail:

- An undervoltage on V_{DD} supply prevents SPI communication. SPI registers are reset to their default values
- An undervoltage on V_S supply switches OFF all channels, even in Limp Home mode. The channels are enabled again as soon as $V_S \geq V_{S(OP)}$

The voltage at pin V_S is also monitored. In case of a negative voltage transient on V_S resulting in $V_S < V_{S(TP)}$ when the device is out of Sleep mode, any SPI command sent by the microcontroller is not accepted (see **Chapter 6.2** and **Chapter 10.5** for further information). An overview of channel behavior according to different V_S and V_{DD} supply voltages is shown in **Table 10**.

Table 10 Device capability as function of V_S and V_{DD}[1]

	$V_{DD} \leq V_{DD(PO)}$ ($V_{DD(PO)}$ see P_6.4.1.1)	$V_{DD} > V_{DD(PO)}$
$V_S \leq V_{S(TP)}$ ($V_{S(TP)}$ see P_6.4.0.5)	Channels are OFF	Channels are OFF
	SPI registers reset	SPI registers protected
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication available[2] (f_{SCLK} = 5 MHz)
	Limp Home mode not available	Limp Home mode not available
$V_{S(TP)} < V_S \leq V_{S(UV)}$ ($V_{S(UV)}$ see P_6.4.0.1)	Channels are OFF	Channels are OFF
	SPI registers reset	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication available (f_{SCLK} = 5 MHz)
	Limp Home mode available (channels are OFF)	Limp Home mode available (channels are OFF)
$V_S > V_{S(UV)}$[3]	Channels cannot be controlled by SPI	Channels can be controlled by SPI
	SPI registers reset	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication available (f_{SCLK} = 5 MHz)
	Limp Home mode available	Limp Home mode available

1) Valid after a successful supply voltage ramp-up.

2) Write commands are ignored. Furthermore the device responds with `STDDIAG` only.

3) The undervoltage condition on VS supply must be considered. See **Chapter 6.2**.

6.1 Operation Modes

BTS71220-4ESE has the following operation modes:

- Sleep mode
- Active mode
- Stand-by mode
- Ready mode
- Limp Home mode
- Limp Home Active mode

The transition between operation modes is determined according to these variables:

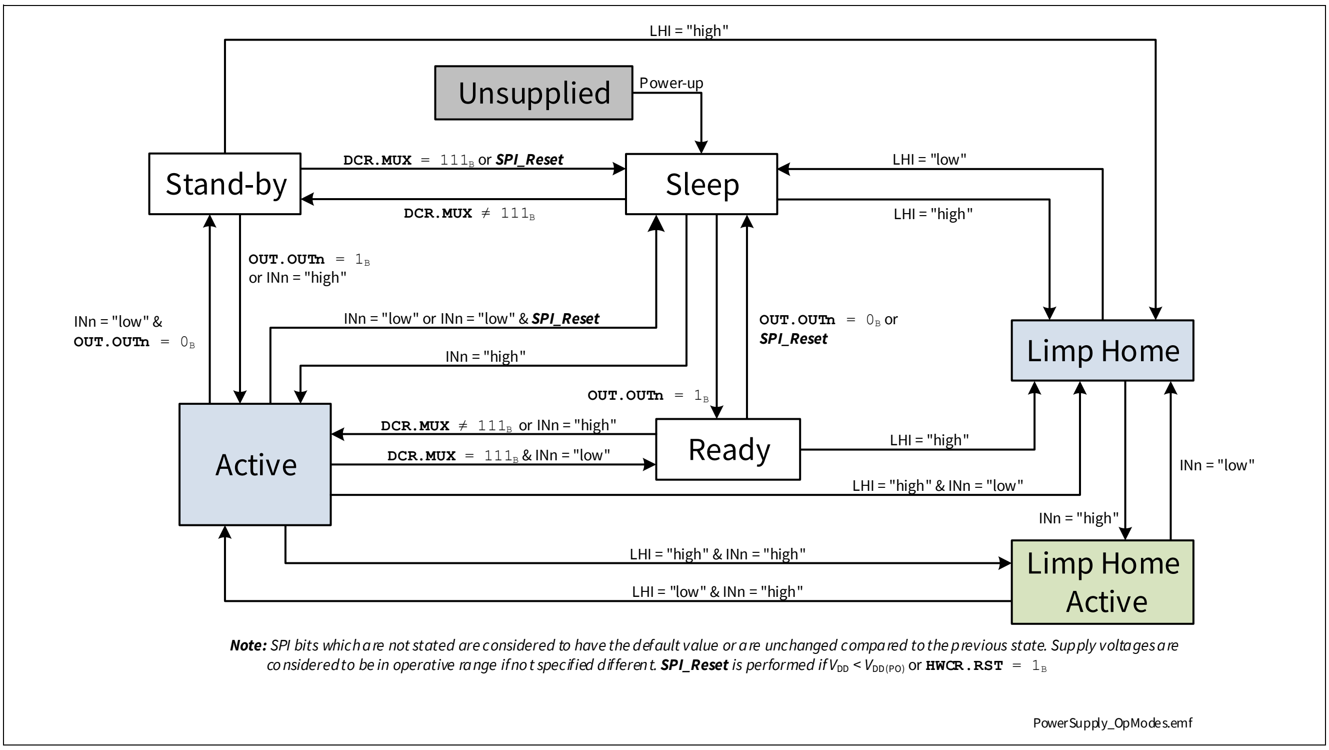
- Digital supply level (V_{DD})
- Logic level at INn pins
- Logic level at LHI pin
- Current sense multiplexer state (**`DCR.MUX`**)
- Output register state (**`OUT.OUTn`**)
- Configuration registers state

The state diagram including the possible transitions is shown in **Figure 14**. The behavior of BTS71220-4ESE as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S supply voltage, some changes within the same operation mode can be seen accordingly.

There are five parameters describing each operation mode of BTS71220-4ESE:

- Status of the output channels
- Status of SPI registers
- Status of SPI communication
- Current consumption at VS pin (measured by I_{VS} in Sleep mode, I_{GND} in all other operative modes)
- Current consumption at VDD pin (I_{VDD})

Table 11 shows the correlation between operation modes, V_S and V_{DD} supply voltages, and the state of the most important functions (channel status, SPI communication and SPI registers).


LHI = "high"
Unsupplied
Power-up
Stand-by
DCR.MUX = 111B or SPI_Reset
Sleep
DCR.MUX ≠ 111B
LHI = "low"
LHI = "high"
OUT.OUTn = 1B or INn = "high"
INn = "low" & OUT.OUTn = 0B
INn = "low" or INn = "low" & SPI_Reset
INn = "high"
OUT.OUTn = 0B or SPI_Reset
Limp Home
OUT.OUTn = 1B
DCR.MUX ≠ 111B or INn = "high"
DCR.MUX = 111B & INn = "low"
Active
Ready
LHI = "high"
LHI = "high" & INn = "low"
INn = "low"
INn = "high"
LHI = "high" & INn = "high"
LHI = "low" & INn = "high"
Limp Home Active
PowerSupply_OpModes.emf

Note: *SPI bits which are not stated are considered to have the default value or are unchanged compared to the previous state. Supply voltages are considered to be in operative range if not specified different.* ***SPI_Reset*** *is performed if* $V_{DD} < V_{DD(PO)}$ or **HWCR.RST** = 1_B

Figure 14 Operation Mode state diagram

Table 11 Device function in relation to operation modes, V_{DD} and V_S voltages

Operative Mode	Function	$V_S \leq V_{S(TP)}$	$V_{S(TP)} \leq V_S \leq V_{S(UV)}$	$V_S > V_{S(UV)}$
Sleep	Channels	OFF	OFF	OFF
	SPI registers	available[1]	available[1]	available[1]
	SPI comm.	available[1]	available[1]	available[1]
Stand-by	Channels	OFF	OFF	OFF
	SPI registers	protected[1]	available[1]	available[1]
	SPI comm.	all commands rejected[1]	available[1]	available[1]
Ready	Channels	OFF	OFF	OFF
	SPI registers	protected[1]	available[1]	available[1]
	SPI comm.	all commands rejected[1]	available[1]	available[1]
Active	Channels	OFF	OFF	follow SPI and/or Input pins
	SPI registers	protected[1]	available[1]	available[1]
	SPI comm.	all commands rejected[1]	available[1]	available[1]
Limp Home / Limp Home Active	Channels	OFF	OFF	follow Input pins
	SPI registers	protected[1]	reset (Diagnosis available)[1]	reset (Diagnosis available)[1]
	SPI comm.	all commands rejected[1][2]	read-only[1]	read-only[1]

1) In case $V_{DD} > V_{DD(PO)}$ otherwise not available or in reset.

2) In case all input pins are set to “low”, SPI communication is in read-only mode.

6.1.1 Unsupplied

In this state, the device is either unsupplied (no voltage applied to VS pin and VDD pin) or the supply voltages are both below the corresponding undervoltage threshold.

6.1.2 Power-up

The Power-up condition is entered when one of the supply voltages (V_S or V_{DD}) is applied to the device. Both supplies are rising until they are above the undervoltage thresholds $V_{S(OP)}$ and $V_{DD(PO)}$ therefore the internal Power-On signals are set. The SPI interface can be accessed after wake up time $t_{WU(PO)}$.

6.1.3 Sleep mode

The device is in Sleep mode when all Digital Input pins (INn, LHI) are set to “low” and **DCR.MUX** is still set to 111_B. When BTS71220-4ESE is in Sleep mode, all outputs are OFF. The SPI registers can be programmed if $V_{DD} > V_{DD(PO)}$. The current consumption is minimum (see parameter $I_{VS(SLEEP)}$). No Overtemperature or Overload protection mechanism is active when the device is in Sleep mode. The circuitry that monitors V_S versus $V_{S(UV)}$ and V_S versus $V_{S(TP)}$ is disabled. This allows the programming of the registers even if $V_S < V_{S(TP)}$.

6.1.4 Stand-by mode

The device is in Stand-by mode when **DCR.MUX** $\neq 111_B$ and no command to switch ON a channel was received (either via SPI or via Input pins). All channels are OFF but the internal supply circuitry is working and therefore the device current consumption is increased. A command to switch ON one or more outputs is accepted and executed, bringing the device into Active mode. SPI communication is possible.

6.1.5 Ready mode

In Ready mode, one or more outputs received a command to switch ON (either via SPI or via Input pins if **HWCR.COL** = 1_B). Nevertheless, all outputs are OFF because of **DCR.MUX** bits still set to 111_B. It is necessary to change the value of those bits to bring the device into Active mode and switch ON the channels.

*Note: Since **OUT** register is blanked with **DCR.MUX** = 111_B it is not possible to enter Active mode when **HWCR.COL** bit is set to 1_B.*

6.1.6 Active mode

Active mode is the normal operation mode of BTS71220-4ESE when no Limp Home condition is set and one or more outputs are switched ON. Device current consumption is specified by parameter $I_{GND(ACTIVE)}$. An undervoltage condition on V_{DD} supply voltage brings the device into Sleep mode in case all Input pins are set to “low”.

6.1.7 Limp Home mode

The device enters Limp Home mode when LHI pin is set to “high” for $t > t_{LHI(AC)}$. SPI registers are reset to the default values when Limp Home mode is entered. The corresponding bit in the standard diagnosis (**STDDIAG.LHI**) will be set to 1_B once the LHI pin is set to “high” and latched until next **STDDIAG** transmission. See **Figure 15** for further information. SPI registers are available for read access. ERRDIAG, STDDIAG, WRNDIAG and ICS can be used for diagnosis in Limp Home.

When the device is in transient protection ($V_S \leq V_{S(TP)}$) and the LHI pin is set to "high", the **STDDIAG.LHI** bit will be set but the device will not change its state to Limp Home mode. Furthermore **STDDIAG.VSMON** and **STDDIAG.TER** bits will be set to report the battery transient protection.

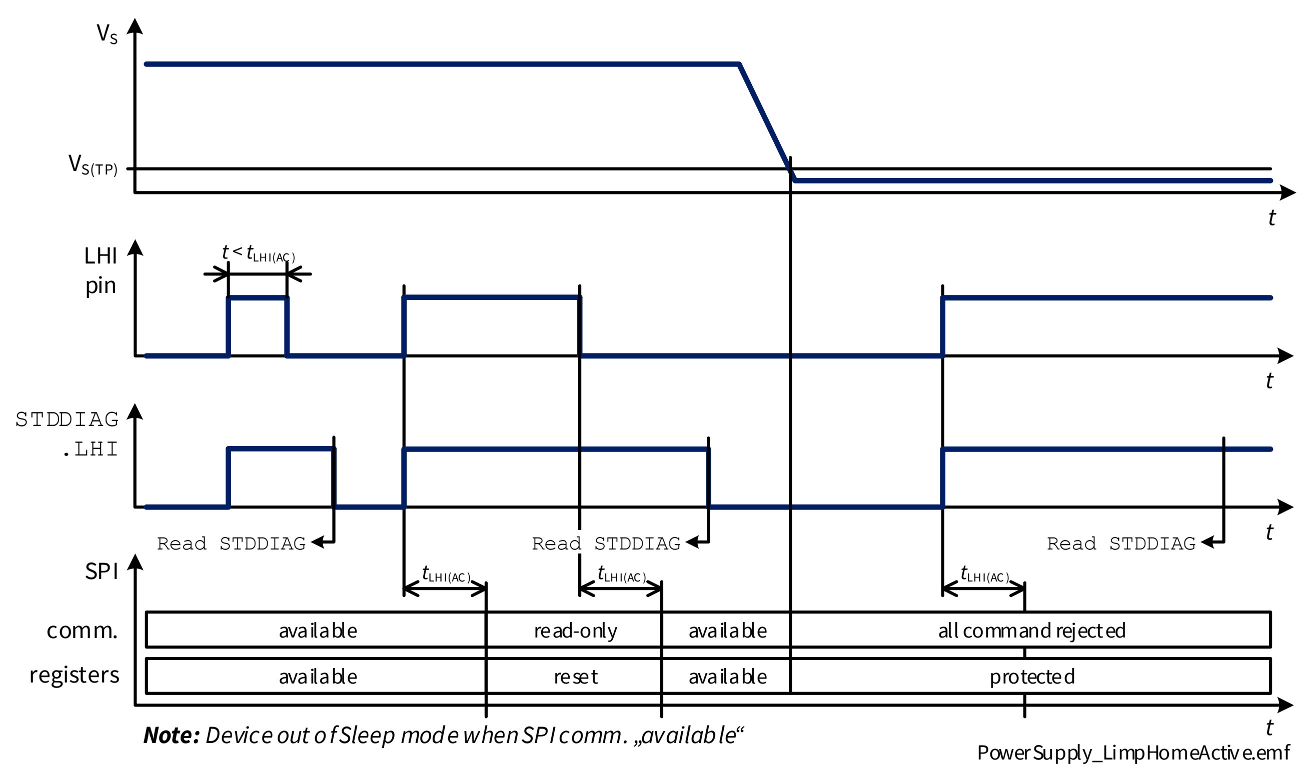

V_S
$V_{S(TP)}$
t
LHI pin
$t < t_{LHI(AC)}$
t
STDDIAG .LHI
Read STDDIAG
Read STDDIAG
Read STDDIAG
t
SPI
$t_{LHI(AC)}$
$t_{LHI(AC)}$
$t_{LHI(AC)}$
comm.
available
read-only
available
all command rejected
registers
available
reset
available
protected
t
Note: Device out of Sleep mode when SPI comm. „available“
PowerSupply_LimpHomeActive.emf

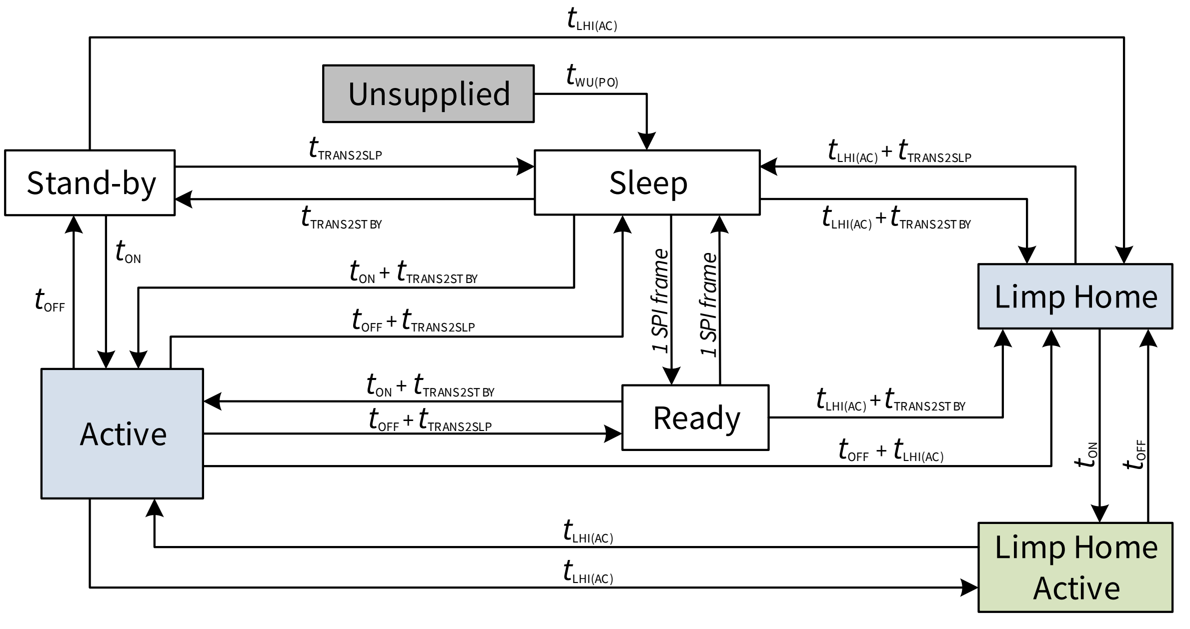
Figure 15 Limp Home Activation as function of V_S

6.1.8 Limp Home Active mode

Limp Home Active mode is entered when the device is in Limp Home mode and one of the IN pins is set to "high". Overload, Overtemperature and Overvoltage protections are active. Since SPI registers cannot be written current sensing is not available.

6.1.9 Definition of Operation modes transition times

The channel turn-ON time is as defined by parameter t_{ON} when BTS71220-4ESE is in Active mode or in Limp Home mode. In all other cases, it is necessary to add the transition time required to reach one of the two aforementioned operation modes (as shown in **Figure 16**).


$t_{LHI(AC)}$
Unsupplied
$t_{WU(PO)}$
Stand-by
$t_{TRANS2SLP}$
Sleep
$t_{LHI(AC)} + t_{TRANS2SLP}$
$t_{TRANS2STBY}$
$t_{LHI(AC)} + t_{TRANS2STBY}$
t_{ON}
t_{OFF}
$t_{ON} + t_{TRANS2STBY}$
Limp Home
$t_{OFF} + t_{TRANS2SLP}$
1 SPI frame
1 SPI frame
Active
$t_{ON} + t_{TRANS2STBY}$
$t_{OFF} + t_{TRANS2SLP}$
Ready
$t_{LHI(AC)} + t_{TRANS2STBY}$
$t_{OFF} + t_{LHI(AC)}$
t_{ON}
t_{OFF}
$t_{LHI(AC)}$
$t_{LHI(AC)}$
Limp Home Active

PowerSupply_OpModes_Timings.emf

Figure 16 **Transition Time diagram**

6.2 Undervoltage on V_S

Between $V_{S(OP)}$ and $V_{S(UV)}$ the undervoltage mechanism is triggered. If the device is operative (in Active or Limp Home Active mode) and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the internal logic switches OFF the output channels. When the device is either in Stand-by, Active or Limp Home mode the bit `STDDIAG.VSMON` is set and latched until readout. When the state is changed from Sleep to any other state, a delay of $t \geq t_{TRANS2STBY}$ has to be considered until `STDDIAG.VSMON` is valid.

As soon as the supply voltage V_S is above the operative threshold $V_{S(OP)}$, the channels having the corresponding input pin set to "high" or the bit in the `OUT` register set to 1_B are switched ON again. The restart is delayed with a time $t_{DELAY(UV)}$ which protects the device in case the undervoltage condition is caused by a short circuit event (according to AEC-Q100-012), as shown in **Figure 17**.

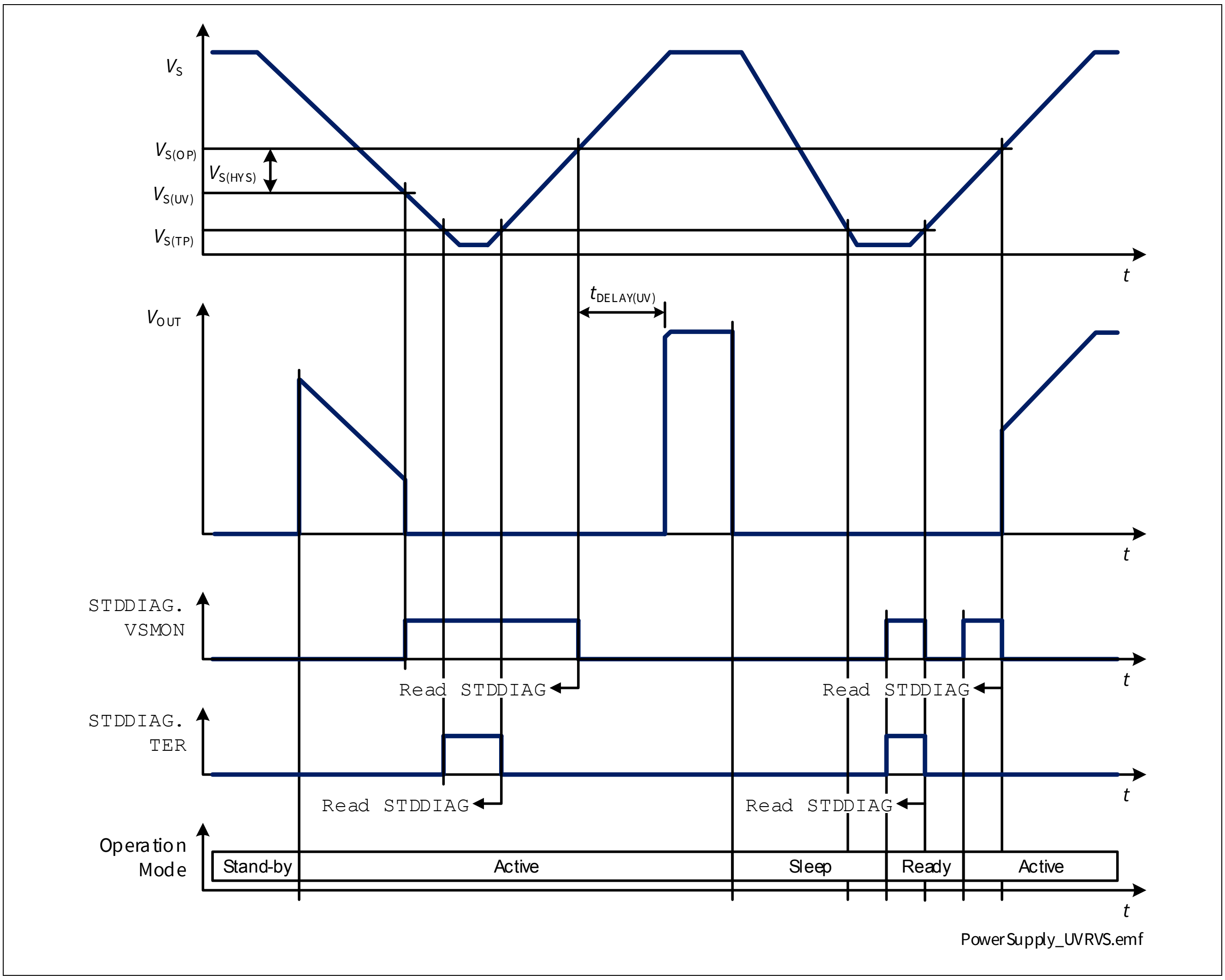


Figure 17 V_S **undervoltage behavior**

6.3 Reset Condition

One of the following conditions reset the SPI registers to their default value:

- V_{DD} is not present or below the undervoltage threshold $V_{DD(PO)}$
  - SPI registers will be reset to their default values (in the first communication after reset the **STDDIAG.TER** will be set to 1_B).
  - Restart counters will not be reset if V_S is available or LHI is "high".
- LHI pin is set to “high” for $t > t_{LHI(AC)}$ and $V_S > V_{S(TP)}$
  - Configuration registers will be reset to their default values. **ERRDIAG** and **WRNDIAG** will be reset.
  - Restart counters will be reset.
- Reset command (**HWCR.RST** = 1_B) is executed and $V_S > V_{S(TP)}$
  - Configuration registers will be reset to their default values. **ERRDIAG**, **WRNDIAG** and **STDDIAG** will not be reset.
  - Restart counters will not be reset.

In case all Input pins are set to “low” after any reset condition, all channels are switched OFF.

6.4 Electrical Characteristics Power Supply

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: R_L = 2.6 Ω

27W output: R_L = 4.8 Ω

Table 12 Electrical Characteristics: Power Supply - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS pin							
Power Supply Undervoltage Shutdown	$V_{S(UV)}$	1.8	2.3	3.1	V	V_S decreasing IN = “high” or **OUT.OUTn** = 1_B From $V_{DS} \leq 0.5$ V to $V_{DS} = V_S$ See **Figure 17**	P_6.4.0.1
Power Supply Minimum Operating Voltage	$V_{S(OP)}$	2.0	3.0	4.1	V	V_S increasing IN = “high”or **OUT.OUTn** = 1_B From $V_{DS} = V_S$ to $V_{DS} \leq 0.5$ V See **Figure 17**	P_6.4.0.3
Power Supply Voltage Threshold for Battery Transients Protection	$V_{S(TP)}$	0.6	1.0	1.8	V	V_S decreasing **STDDIAG.VSMON** = 1_B **STDDIAG.TER** = 1_B **DCR.MUX** ≠ 111_B See **Figure 17**	P_6.4.0.5
Power Supply Undervoltage Shutdown Hysteresis	$V_{S(HYS)}$	–	0.7	–	V	1) $V_{S(OP)} - V_{S(UV)}$ See **Figure 17**	P_6.4.0.6
Power Supply Undervoltage Recovery Time	$t_{DELAY(UV)}$	2.5	4	5.5	ms	1) See **Figure 17**	P_6.4.0.10
Breakdown Voltage between GND and VS Pins in Reverse Battery	$-V_{S(REV)}$	16	–	30	V	1) $I_{GND(REV)}$ = 14 mA T_J = 150 °C	P_6.4.0.9

1) Not subject to production test - specified by design.

6.4.1 Electrical Characteristics Power Supply - SPOC™

Table 13 Electrical Characteristics: Power Supply - SPOC™

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDD pin							
Digital Supply Operating Voltage	$V_{DD(OP)}$	2.45	4.3	5.5	V	[1] f_{SCLK} = 5 MHz	P_6.4.1.1
Digital Supply Power-On Reset Threshold Voltage	$V_{DD(PO)}$	1.4	1.9	2.3	V	[1] V_{DD} increasing	P_6.4.1.9
Digital Supply Undervoltage Shutdown	$V_{DD(UV)}$	1.3	1.8	2.2	V	V_{DD} decreasing **OUT.OUTn** = 1_B From $V_{DS} \leq 0.5$ V to $V_{DS} = V_S$	P_6.4.1.2
Digital Supply Undervoltage Shutdown Hysteresis	$V_{DD(HYS)}$	–	0.1	–	V	[1]	P_6.4.1.3
Digital Supply Clamping Voltage	$V_{DD(CLAMP1)}$	–	6.5	–	V	[1] I_{DD} = 1 mA	P_6.4.1.11
Digital Supply Clamping Voltage	$V_{DD(CLAMP2)}$	6	7	8	V	I_{DD} = 20 mA	P_6.4.1.12
Power-On Wake Up Time	$t_{WU(PO)}$	–	10	30	µs	[1]	P_6.4.1.13
Transition Time to Stand-by Mode	$t_{TRANS2STBY}$	5	10	30	µs	[1]	P_6.4.1.4
Transition Time to Sleep Mode	$t_{TRANS2SLP}$	1	5	20	µs	[1]	P_6.4.1.5
Limp Home Acknowledgement Time	$t_{LHI(AC)}$	10	20	40	µs	[1]	P_6.4.1.6

1) Not subject to production test - specified by design.

6.5 Electrical Characteristics Power Supply - Product Specific

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: R_L = 2.6 Ω

27W output: R_L = 4.8 Ω

6.5.1 BTS71220-4ESE

Table 14 Electrical Characteristics: Power Supply BTS71220-4ESE

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Supply Current Consumption in Normal Operation	I_{DD}	–	80	200	µA	$f_{SCLK} = 0$ MHz $V_S > V_{S(UV)}$ $V_{CSN} = V_{DD} = 5$ V DCR.MUX ≠ 111_B	P_6.5.31.1
Digital Supply Current Consumption in Sleep Mode	$I_{DD(SLEEP)}$	–	17	50	µA	$f_{SCLK} = 0$ MHz $V_S > V_{S(UV)}$ $V_{CSN} = V_{DD} = 5$ V DCR.MUX = 111_B	P_6.5.31.3
Digital Supply Current Consumption in Sleep Mode	$I_{DD(SLEEP)}$	–	17	35	µA	$f_{SCLK} = 0$ MHz $V_S > V_{S(UV)}$ $V_{CSN} = V_{DD} = 5$ V DCR.MUX = 111_B $T_J \leq 85$ °C	P_6.5.31.12
Power Supply Current Consumption in Sleep Mode with Loads at $T_J \leq 85$ °C	$I_{VS(SLEEP)\_85}$	–	0.05	0.7	µA	[1][2] $V_S = 18$ V $V_{OUT} = 0$ V INx = “low” $T_J \leq 85$ °C	P_6.5.31.4
Power Supply Current Consumption in Sleep Mode with Loads at $T_J = 150$ °C	$I_{VS(SLEEP)\_150}$	–	2	100	µA	$V_S = 18$ V $V_{OUT} = 0$ V INx = “low” $T_J = 150$ °C	P_6.5.31.5
Operating Current in Active Mode (all Channels ON)	$I_{GND(ACTIVE)}$	–	5	7	mA	$V_S = 18$ V $V_{DD} = 5$ V INx = “high” or OUT.OUTn = 1_B	P_6.5.31.6
Operating Current in Ready Mode	$I_{GND(READY)}$	–	80	200	µA	$V_S = 18$ V $V_{CSN} = V_{DD} = 5$ V $f_{SCLK} = 0$ MHz DCR.MUX = 111_B OUT.OUTn = 1_B	P_6.5.31.8
Operating Current in Stand-by Mode	$I_{GND(STBY)}$	–	1.25	2	mA	$V_S = 18$ V $V_{DD} = 5$ V DCR.MUX ≠ 111_B	P_6.5.31.9

[1] Not subject to production test - specified by design.

[2] If $V_{DD} < V_{DD(PO)}$, LHI = ”low” and any restart counter > 0, $I_{GND(STBY)}$ has to be considered.

7 Power Stages

The high-side power stages are built using a N-channel vertical Power MOSFET with charge pump.

7.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature T_J. **Figure 18** shows the variation of $R_{DS(ON)}$ across the whole T_J range. The value "2" on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at T_J = 150 °C.

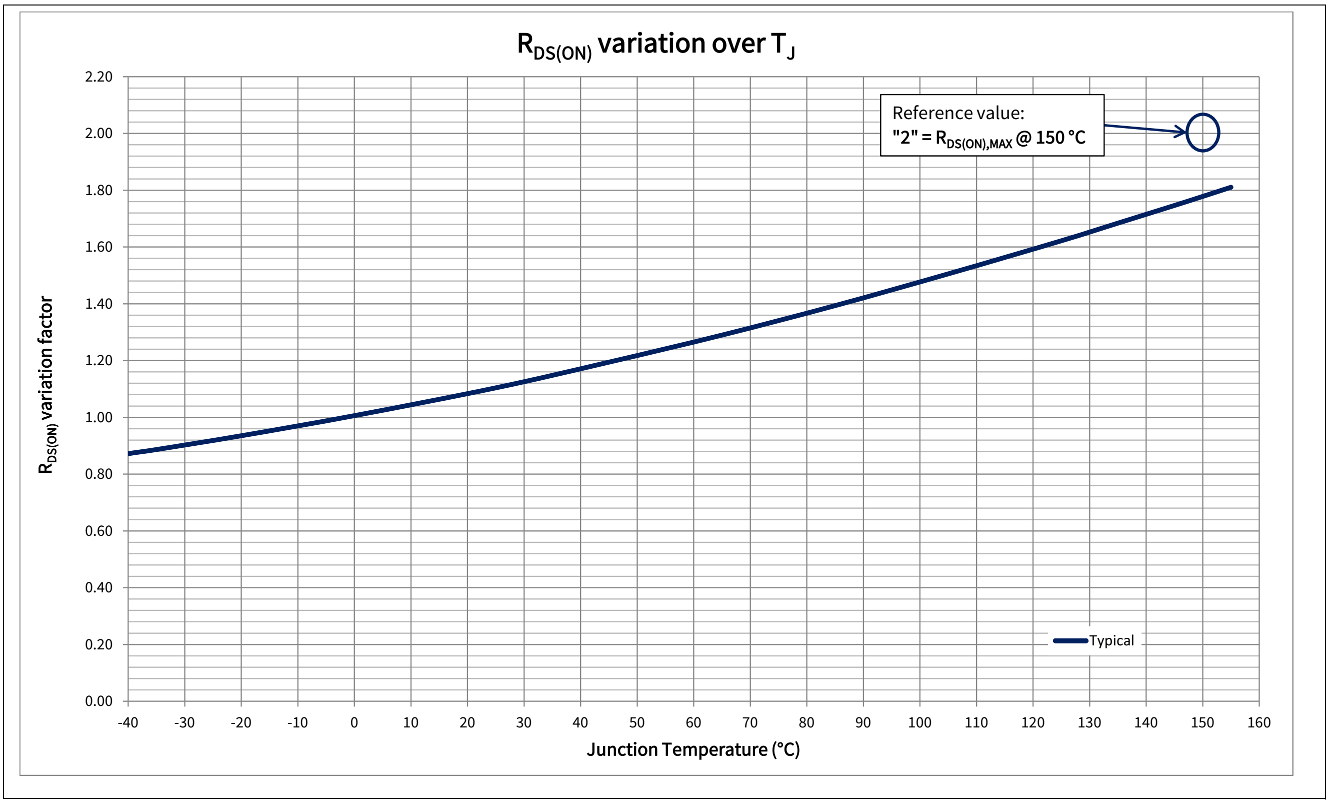


Figure 18 $R_{DS(ON)}$ **variation factor**

The behavior in Reverse Polarity is described in **Chapter 8.4.1**.

7.2 Switching loads

7.2.1 Switching Resistive Loads

When switching resistive loads, the switching times and slew rates shown in **Figure 19** can be considered. The switch energy values E_{ON} and E_{OFF} are proportional to load resistance and times t_{ON} and t_{OFF}.

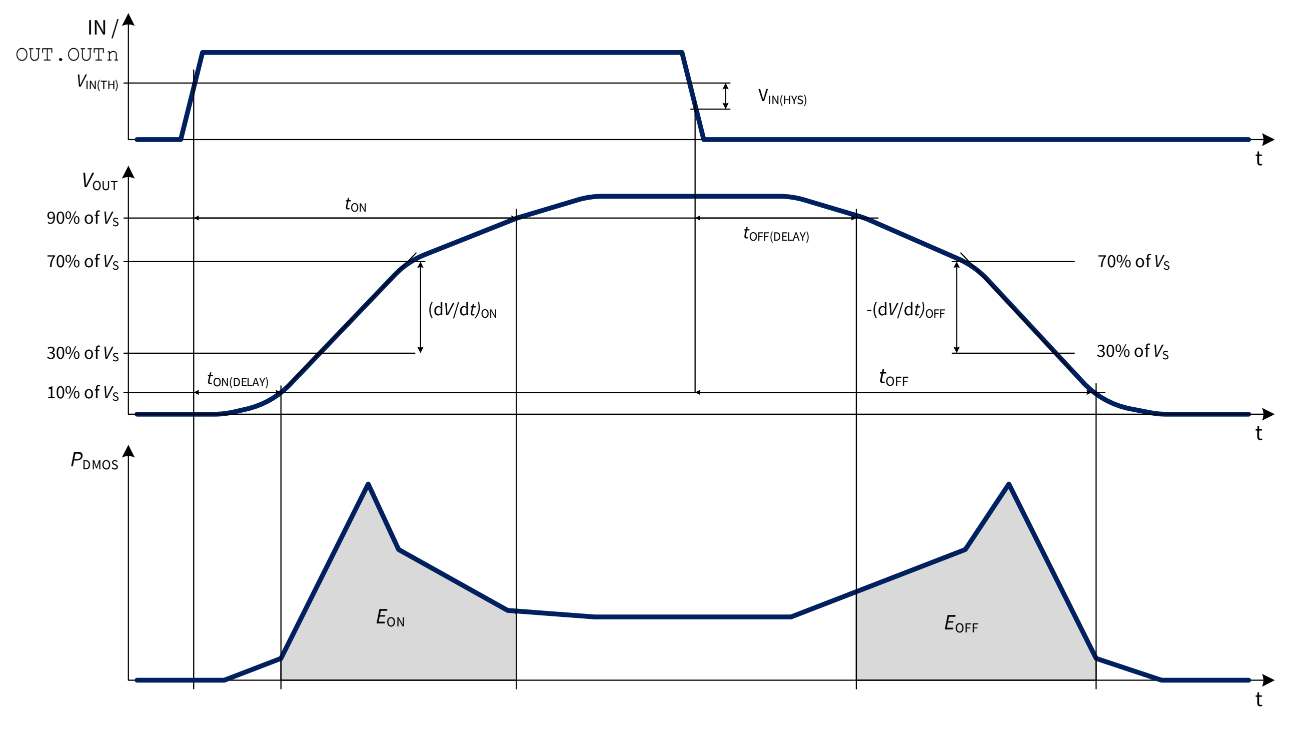


Figure 19 Switching a Resistive Load

7.2.2 Switching Inductive Loads

When switching OFF inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the negative output voltage so that V_{DS} = $V_{DS(CLAMP)}$. **Figure 20** shows a concept drawing of the implementation. The clamping structure protects the device in all operation modes listed in **Chapter 6.1**.

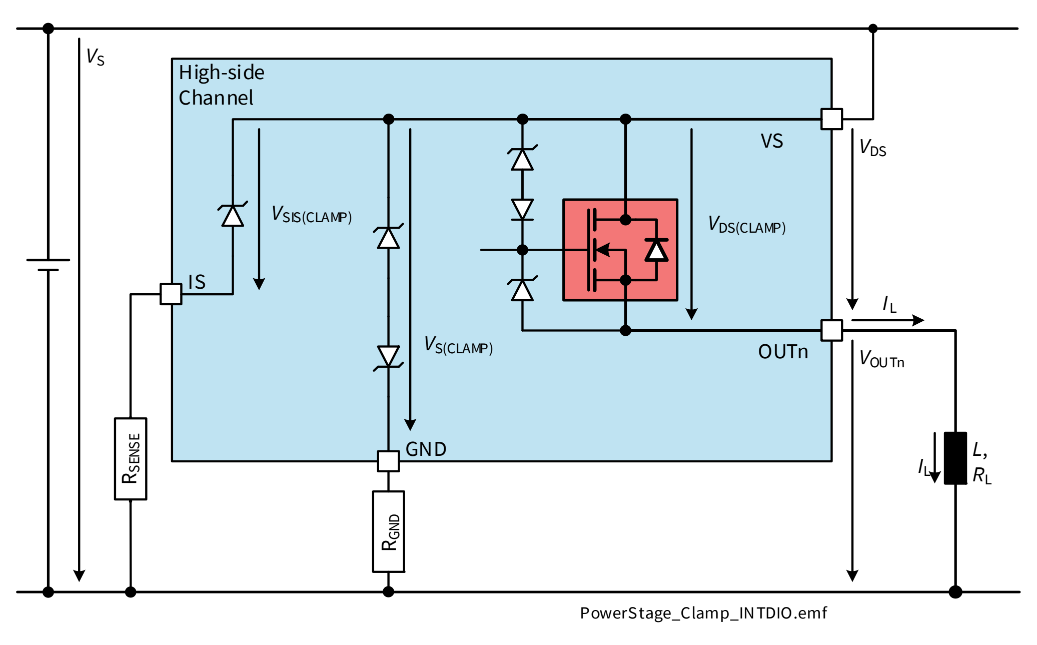

V_S
High-side
Channel
VS
V_{DS}
V_{SIS(CLAMP)}
V_{DS(CLAMP)}
IS
I_L
V_{S(CLAMP)}
OUTn
V_{OUTn}
GND
R_{SENSE}
R_{GND}
I_L
L,
R_L
PowerStage_Clamp_INTDIO.emf

Figure 20 Output Clamp concept

During demagnetization of inductive loads, energy has to be dissipated in BTS71220-4ESE. The energy can be calculated with **Equation (7.1)**:

$$E = V_{DS(CLAMP)} \cdot \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}}\right) + I_L\right] \cdot \frac{L}{R_L} \qquad (7.1)$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component.

7.2.3 Output Voltage Limitation

To increase the current sense accuracy, V_{DS} voltage is monitored. When the output current I_L decreases while the channel is diagnosed (channel selected via **`DCR.MUX`** - see **Figure 21**) bringing V_{DS} equal or lower than $V_{DS(SLC)}$, the output DMOS gate is partially discharged. This increases the output resistance so that $V_{DS} = V_{DS(SLC)}$ even for very small output currents. The V_{DS} increase allows the current sensing circuitry to work more efficiently, providing better k_{ILIS} accuracy for output current in the low range.

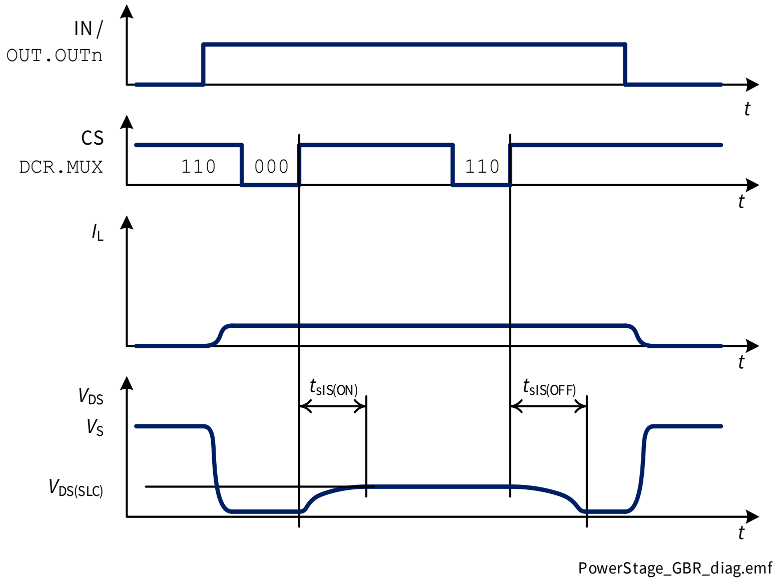


Figure 21 Output Voltage Limitation activation during diagnosis

7.2.4 Switching Capacitive Loads

When switching ON a capacitive load, the capacitance is causing a high inrush current. The current is depending on the value of the capacitance, the ESR, the impedance of the system and the slew rate of the driver. To improve the load driving capability, BTS71220-4ESE offers a slew rate control feature. When the slew rate bit **`SRC.SRCn`** is set, the slew rate of the respective channel is reduced to the half (see **Chapter 7.4.1**).

7.3 Advanced Switching Characteristics

7.3.1 Inverse Current behavior

When $V_{OUT} > V_S$, a current I_{INV} flows into the power output transistor (see **Figure 22**). This condition is known as “Inverse Current”.

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses therefore an increase of overall device temperature. This may lead to a switch OFF of unaffected channels due to Overtemperature. If the channel is in ON state, $R_{DS(INV)}$ can be expected and power dissipation in the output stage is comparable to normal operation in $R_{DS(ON)}$.

During Inverse Current condition, the channel remains in ON or OFF state as long as $I_{INV} < I_{L(INV)}$.

With InverseON, it is possible to switch ON the channel during Inverse Current condition as long as $I_{INV} < I_{L(INV)}$ (see **Figure 23**).

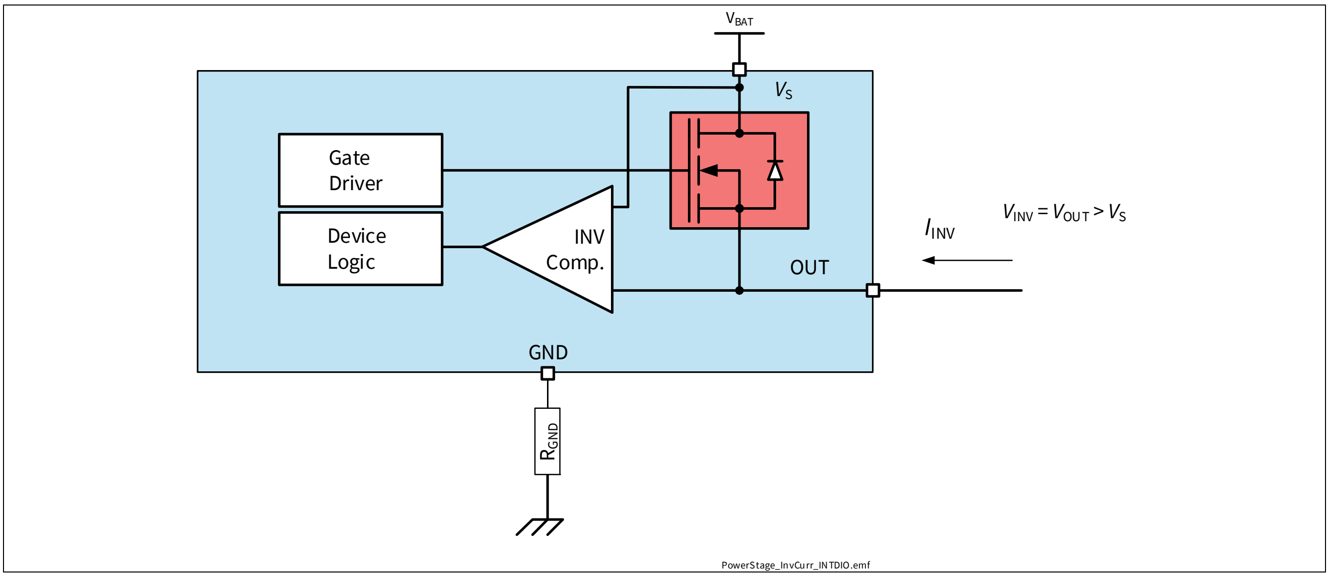

V_BAT
V_S
Gate Driver
Device Logic
INV Comp.
OUT
I_INV
V_INV = V_OUT > V_S
GND
R_GND
PowerStage_InvCurr_INTDIO.emf

Figure 22 Inverse Current Circuitry

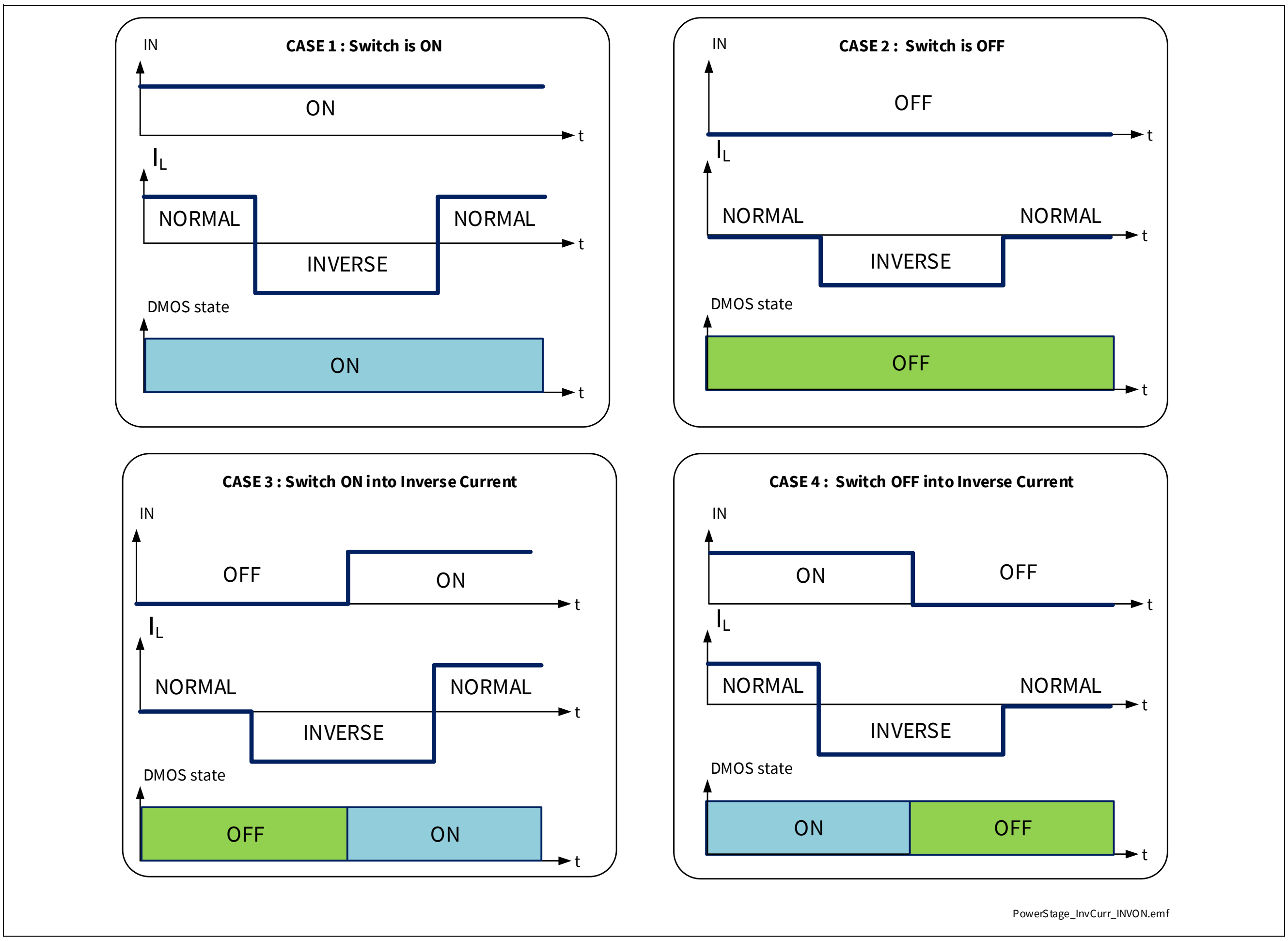

CASE 1 : Switch is ON
IN
ON
t
I_L
NORMAL
INVERSE
NORMAL
t
DMOS state
ON
t
CASE 2 : Switch is OFF
IN
OFF
t
I_L
NORMAL
INVERSE
NORMAL
t
DMOS state
OFF
t
CASE 3 : Switch ON into Inverse Current
IN
OFF
ON
t
I_L
NORMAL
INVERSE
NORMAL
t
DMOS state
OFF
ON
t
CASE 4 : Switch OFF into Inverse Current
IN
ON
OFF
t
I_L
NORMAL
INVERSE
NORMAL
t
DMOS state
ON
OFF
t
PowerStage_InvCurr_INVON.emf

Figure 23 **InverseON - Channel behavior in case of applied Inverse Current**

Note: No protection mechanism like Overtemperature or Overload protection is active during applied Inverse Currents.

7.3.2 Switching Channels in Parallel

When switching channels in parallel to drive a single load it may happen that the two channels switch OFF asynchronously in case of a fault condition which brings additional stress to the channel that switches OFF last. In order to avoid this condition, it is possible to synchronize the protection of two channels when used in parallel. There are 2 bits in the SPI (**PCS.PCCn**), which allow to synchronize channel 0&3 and 1&2. When the corresponding **PCS.PCCn** bit is set, the switch-OFF and restart of the channels are synchronized and the current trip levels will be reduced to $I_{L(OVL3)}$. In case the current trip level for one channel is set to the low level (**OCR.OCTn** = 1_B), the current for both channels will be reduced to $I_{L(OVL2)}$. Since the restart counters of the channels in parallel are synchronized, both channels will latch-OFF as soon one counter has reached $n_{RESTART(CR)}$. Due to this reason it is recommended to clear counters before switching channels in parallel. In case the slew rate adjustment for one channels is used, (**SRC.SRCn** = 1_B), both channels operating in parallel mode will use the adjusted slew rate. When channels are switched in parallel (**PCS.PCCn** = 1_B), the Output Voltage Drop Limitation at Small Load Currents is disabled. Therefore the current sense ratio specifications at lower currents are not valid. See **Chapter 9.7** for further information. To improve current sense accuracy in parallel channel operation, parallel mode has to be deactivated (**PCS.PCCn** = 0_B). Since the current sense of the two channels used in parallel is not synchronized, the total current has to be calculated out of the current sense reading of each single channel. Unless otherwise specified parameter deviations are possible when parallel mode is activated.

When two channels are used in parallel, the total current capability $I_{L(NOM)}$ is doubled. It has to be ensured that the outputs used in parallel mode are connected together with a symmetric and low impedance connection either on the PCB or in the wire harness.

7.3.3 Cross Current robustness with H-Bridge configuration

When BTS71220-4ESE is used as high-side switch e.g. in a bridge configuration (therefore paired with a low-side switch as shown in **Figure 24**), the maximum slew rate applied to the output by the low-side switch must be lower than | dV_{OUT} / dt |. Otherwise the output stage may turn ON in linear mode (not in $R_{DS(ON)}$) while the low-side switch is commutating. This creates an unprotected overheating for the DMOS due to the cross-conduction current.

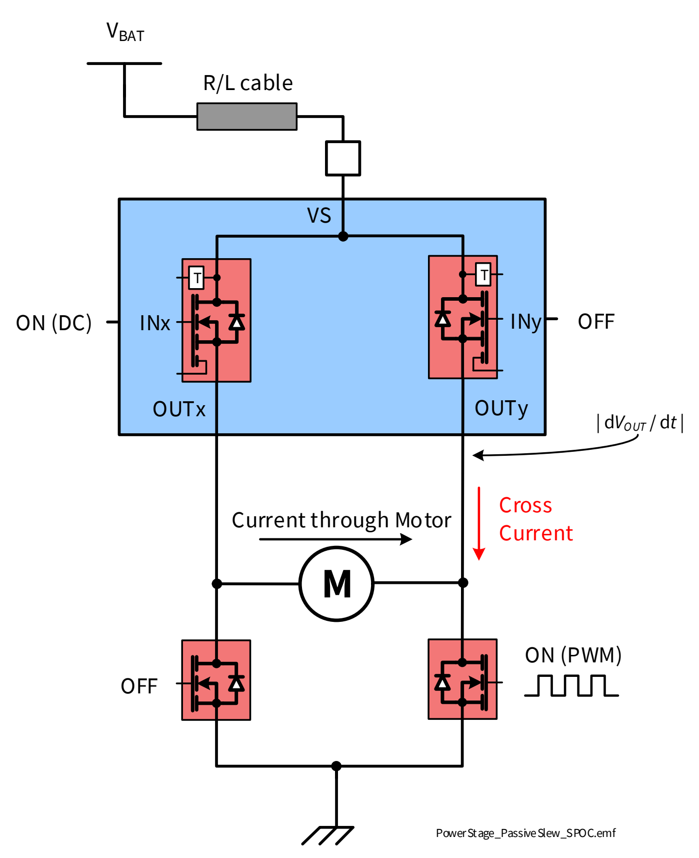

V_BAT
R/L cable
VS
ON (DC)
INx
INy
OFF
OUTx
OUTy
| dV_OUT / dt |
Cross Current
Current through Motor
M
OFF
ON (PWM)
PowerStage_PassiveSlew_SPOC.emf

Figure 24 High-Side switch used in Bridge configuration

7.4 Electrical Characteristics Power Stages

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: R_L = 2.6 Ω

27W output: R_L = 4.8 Ω

Table 15 Electrical Characteristics: Power Stages - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Drain to Source Clamping Voltage at T_J = -40 °C	$V_{DS(CLAMP)\_-40}$	33	36.5	42	V	I_L = 5 mA T_J = -40°C See **Figure 20**	P_7.4.0.1
Drain to Source Clamping Voltage at T_J ≥ 25 °C	$V_{DS(CLAMP)\_25}$	35	38	44	V	[1] I_L = 5 mA T_J ≥ 25°C See **Figure 20**	P_7.4.0.2

1) Tested at T_J = 150°C.

7.4.1 Electrical Characteristics Power Stages - SPOC™

Table 16 Electrical Characteristics: Power Stages - SPOC™

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Timings							
Switch-ON Delay	$t_{ON(DELAY)}$	10	30	60	µs	V_S = 13.5 V V_{OUT} = 10% V_S **PCS . PCCn** = 0_B	P_7.4.2.1
Switch-ON Delay (parallel mode)	$t_{ON(DELAY)}$	10	40	80	µs	[2] V_S = 13.5 V V_{OUT} = 10% V_S **PCS . PCCn** = 1_B	P_7.4.2.16
Switch-OFF Delay	$t_{OFF(DELAY)}$	10	30	60	µs	V_S = 13.5 V V_{OUT} = 90% V_S	P_7.4.2.2
Switch-ON Time	t_{ON}	20	55	100	µs	V_S = 13.5 V V_{OUT} = 90% V_S **SRC . SRCn** = 0_B **PCS . PCCn** = 0_B	P_7.4.2.3
Switch-ON Time (parallel mode)	t_{ON}	20	70	125	µs	[2] V_S = 13.5 V V_{OUT} = 90% V_S **SRC . SRCn** = 0_B **PCS . PCCn** = 1_B	P_7.4.2.20

Table 16 Electrical Characteristics: Power Stages - SPOC™ (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Switch-ON Time	t_{ON}	30	75	150	µs	V_S = 13.5 V V_{OUT} = 90% V_S **SRC . SRCn** = 1_B	P_7.4.2.4
Switch-OFF Time	t_{OFF}	20	55	100	µs	V_S = 13.5 V V_{OUT} = 10% V_S **SRC . SRCn** = 0_B	P_7.4.2.6
Switch-OFF Time	t_{OFF}	30	75	150	µs	V_S = 13.5 V V_{OUT} = 10% V_S **SRC . SRCn** = 1_B	P_7.4.2.7
Switch-ON/OFF Matching t_{ON} - t_{OFF}	Δt_{SW}	-50	0	50	µs	V_S = 13.5 V **PCS . PCCn** = 0_B	P_7.4.2.9
Voltage Slope							
Switch-ON Slew Rate	$(dV/dt)_{ON}$	0.3	0.6	0.9	V/µs	V_S = 13.5 V V_{OUT} = 30% to 70% of V_S **SRC . SRCn** = 0_B	P_7.4.2.11
Switch-ON Slew Rate	$(dV/dt)_{ON}$	0.15	0.3	0.45	V/µs	V_S = 13.5 V V_{OUT} = 30% to 70% of V_S **SRC . SRCn** = 1_B	P_7.4.2.12
Switch-OFF Slew Rate	$-(dV/dt)_{OFF}$	0.3	0.6	0.9	V/µs	V_S = 13.5 V V_{OUT} = 70% to 30% of V_S **SRC . SRCn** = 0_B	P_7.4.2.14
Switch-OFF Slew Rate	$-(dV/dt)_{OFF}$	0.125	0.3	0.45	V/µs	V_S = 13.5 V V_{OUT} = 70% to 30% of V_S **SRC . SRCn** = 1_B	P_7.4.2.15
Slew Rate Matching	$\Delta(dV/dt)_{SW}$	-30	0	30	%	[1] V_S = 13.5 V	P_7.4.2.17
Voltages							
Output Voltage Drop Limitation at Small Load Currents	$V_{DS(SLC)}$	2	10	18	mV	[2] I_L = $I_{L(OL)}$ = 20 mA	P_7.4.2.18

1) $\Delta(dV/dt)_{SW} = ((dV/dt)_{ON} - (dV/dt)_{OFF}) / (((dV/dt)_{ON} + (dV/dt)_{OFF}) / 2)$.

2) Not subject to production test - specified by design.

7.5 Electrical Characteristics - Power Output Stages

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: R_L = 2.6 Ω

27W output: R_L = 4.8 Ω

7.5.1 Power Output Stage - 55 W

Table 17 Electrical Characteristics: Power Stages - 55 W

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output characteristics							
ON-State Resistance at T_J = 25 °C	$R_{DS(ON)\_25}$	–	9.5	–	mΩ	[1] T_J = 25 °C	P_7.5.15.1
ON-State Resistance at T_J = 150 °C	$R_{DS(ON)\_150}$	–	–	16.5	mΩ	T_J = 150 °C	P_7.5.15.2
ON-State Resistance in Cranking	$R_{DS(ON)\_CRANK}$	–	–	20.5	mΩ	T_J = 150 °C V_S = 3.1 V	P_7.5.15.3
ON-State Resistance in Inverse Current at T_J = 25 °C	$R_{DS(INV)\_25}$	–	9.5	–	mΩ	[1] T_J = 25 °C $I_L = -I_{L(NOM)}$	P_7.5.15.4
ON-State Resistance in Inverse Current at T_J = 150 °C	$R_{DS(INV)\_150}$	–	–	20.5	mΩ	[1] T_J = 150 °C $I_L = -I_{L(NOM)}$	P_7.5.15.5
ON-State Resistance in Reverse Polarity at T_J = 25 °C	$R_{DS(REV)\_25}$	–	19	–	mΩ	[1] T_J = 25 °C V_S = -13.5 V $I_L = -I_{L(NOM)}$ R_{SENSE} = 1.2 kΩ	P_7.5.15.6
ON-State Resistance in Reverse Polarity at T_J = 150 °C	$R_{DS(REV)\_150}$	–	–	33	mΩ	[1] T_J = 150 °C V_S = -13.5 V $I_L = -I_{L(NOM)}$ R_{SENSE} = 1.2 kΩ	P_7.5.15.7
Nominal Load Current per Channel (all Channels Active)	$I_{L(NOM)}$	–	5	–	A	[1] T_A = 85 °C $T_J \leq$ 150 °C	P_7.5.15.8
Output Leakage Current at $T_J \leq$ 85 °C	$I_{L(OFF)\_85}$	–	0.06	0.3	µA	[1] V_{OUT} = 0 V V_{IN} = “low” and `OUT.OUTn` = 0_B $T_A \leq$ 85 °C	P_7.5.15.9

Table 17 Electrical Characteristics: Power Stages - 55 W (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Leakage Current at $T_J = 150\ °C$	$I_{L(OFF)\_150}$	–	–	12	µA	$V_{OUT} = 0\ V$ V_{IN} = "low" and **OUT.OUTn** = 0_B $T_A = 150\ °C$	P_7.5.15.10
Inverse Current Capability	$I_{L(INV)}$	–	5	–	A	[1] $V_S < V_{OUT}$ IN = "high" or **OUT.OUTn** = 1_B	P_7.5.15.11
Voltage Slope							
Passive Slew Rate (e.g. for Half Bridge Configuration)	$\lvert dV_{OUT} / dt \rvert$	–	–	10	V/µs	[1] $V_S = 13.5\ V$	P_7.5.15.12
Voltages							
Drain Source Diode Voltage	$\lvert V_{DS(DIODE)} \rvert$	–	500	600	mV	[1] $I_L = -190\ mA$ $T_J = 150\ °C$	P_7.5.15.13
Switching Energy							
Switch-ON Energy	E_{ON}	–	0.53	–	mJ	[1] $V_S = 18\ V$ **SRC.SRCn** = 0_B **PCS.PCCn** = 0_B	P_7.5.15.14
Switch-OFF Energy	E_{OFF}	–	0.68	–	mJ	[1] $V_S = 18\ V$ **SRC.SRCn** = 0_B **PCS.PCCn** = 0_B	P_7.5.15.15

[1] Not subject to production test - specified by design.

7.5.2 Power Output Stage - 27 W

Table 18 Electrical Characteristics: Power Stages - 27 W

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output characteristics							
ON-State Resistance at $T_J = 25\ °C$	$R_{DS(ON)\_25}$	–	22.5	–	mΩ	[1] $T_J = 25\ °C$	P_7.5.16.1
ON-State Resistance at $T_J = 150\ °C$	$R_{DS(ON)\_150}$	–	–	38	mΩ	$T_J = 150\ °C$	P_7.5.16.2
ON-State Resistance in Cranking	$R_{DS(ON)\_CRANK}$	–	–	44	mΩ	$T_J = 150\ °C$ $V_S = 3.1\ V$	P_7.5.16.3
ON-State Resistance in Inverse Current at $T_J = 25\ °C$	$R_{DS(INV)\_25}$	–	22.5	–	mΩ	[1] $T_J = 25\ °C$ $I_L = -I_{L(NOM)}$	P_7.5.16.4

Table 18 Electrical Characteristics: Power Stages - 27 W (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-State Resistance in Inverse Current at $T_J = 150$ °C	$R_{DS(INV)\_150}$	–	–	44	mΩ	1) $T_J = 150$ °C $I_L = -I_{L(NOM)}$	P_7.5.16.5
ON-State Resistance in Reverse Polarity at $T_J = 25$ °C	$R_{DS(REV)\_25}$	–	45	–	mΩ	1) $T_J = 25$ °C $V_S = -13.5$ V $I_L = -I_{L(NOM)}$ $R_{SENSE} = 1.2$ kΩ	P_7.5.16.6
ON-State Resistance in Reverse Polarity at $T_J = 150$ °C	$R_{DS(REV)\_150}$	–	–	70	mΩ	1) $T_J = 150$ °C $V_S = -13.5$ V $I_L = -I_{L(NOM)}$ $R_{SENSE} = 1.2$ kΩ	P_7.5.16.7
Nominal Load Current per Channel (all Channels Active)	$I_{L(NOM)}$	–	3	–	A	1) $T_A = 85$ °C $T_J \leq 150$ °C	P_7.5.16.8
Output Leakage Current at $T_J \leq 85$ °C	$I_{L(OFF)\_85}$	–	0.03	0.15	µA	1) $V_{OUT} = 0$ V V_{IN} = “low” and `OUT.OUTn` = 0_B $T_A \leq 85$ °C	P_7.5.16.9
Output Leakage Current at $T_J = 150$ °C	$I_{L(OFF)\_150}$	–	–	10	µA	$V_{OUT} = 0$ V V_{IN} = “low” and `OUT.OUTn` = 0_B $T_A = 150$ °C	P_7.5.16.10
Inverse Current Capability	$I_{L(INV)}$	–	3	–	A	1) $V_S < V_{OUT}$ IN = “high” or `OUT.OUTn` = 1_B	P_7.5.16.11
Voltage Slope							
Passive Slew Rate (e.g. for Half Bridge Configuration)	$\lvert dV_{OUT} / dt \rvert$	–	–	10	V/µs	1) $V_S = 13.5$ V	P_7.5.16.12
Voltages							
Drain Source Diode Voltage	$\lvert V_{DS(DIODE)} \rvert$	–	500	600	mV	1) $I_L = -190$ mA $T_J = 150$ °C	P_7.5.16.13

Table 18 Electrical Characteristics: Power Stages - 27 W (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Switching Energy							
Switch-ON Energy	E_{ON}	–	0.30	–	mJ	[1)] $V_S = 18$ V **SRC . SRCn** = 0_B **PCS . PCCn** = 0_B	P_7.5.16.14
Switch-OFF Energy	E_{OFF}	–	0.38	–	mJ	[1)] $V_S = 18$ V **SRC . SRCn** = 0_B **PCS . PCCn** = 0_B	P_7.5.16.15

1) Not subject to production test - specified by design.

8 Protection

The BTS71220-4ESE is protected against Overtemperature, Overload, Reverse Battery (with ReverSave™) and Overvoltage. Overtemperature and Overload protections are working when the device is not in Sleep mode. Overvoltage protection works in all operation modes. Reverse Battery protection works when the GND and VS pins are reverse supplied.

8.1 Overtemperature Protection

The device incorporates both an absolute ($T_{J(ABS)}$) and a dynamic ($T_{J(DYN)}$) temperature protection circuitry for each channel. An increase of junction temperature T_J above either one of the two thresholds ($T_{J(ABS)}$ or $T_{J(DYN)}$) switches OFF the overheated channel to prevent destruction. The corresponding **`WRNDIAG.WRNn`** bits are set and cleared on read. The channel remains switched OFF until junction temperature has reached the "Restart" condition described in **Table 19**. The behavior is shown in **Figure 25** (absolute Overtemperature Protection) and **Figure 26** (dynamic Overtemperature Protection). $T_{J(REF)}$ is the reference temperature used for dynamic temperature protection.

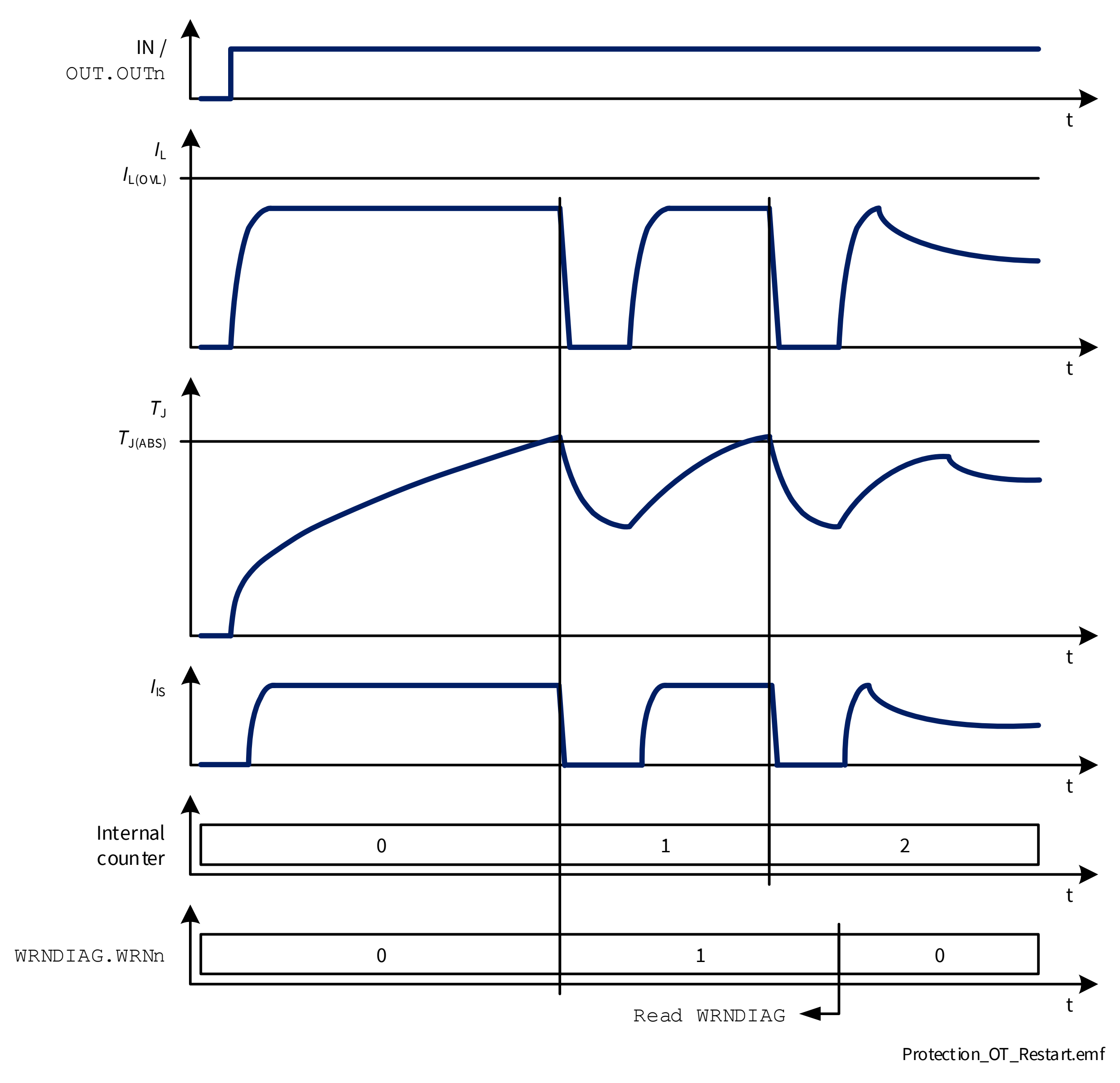
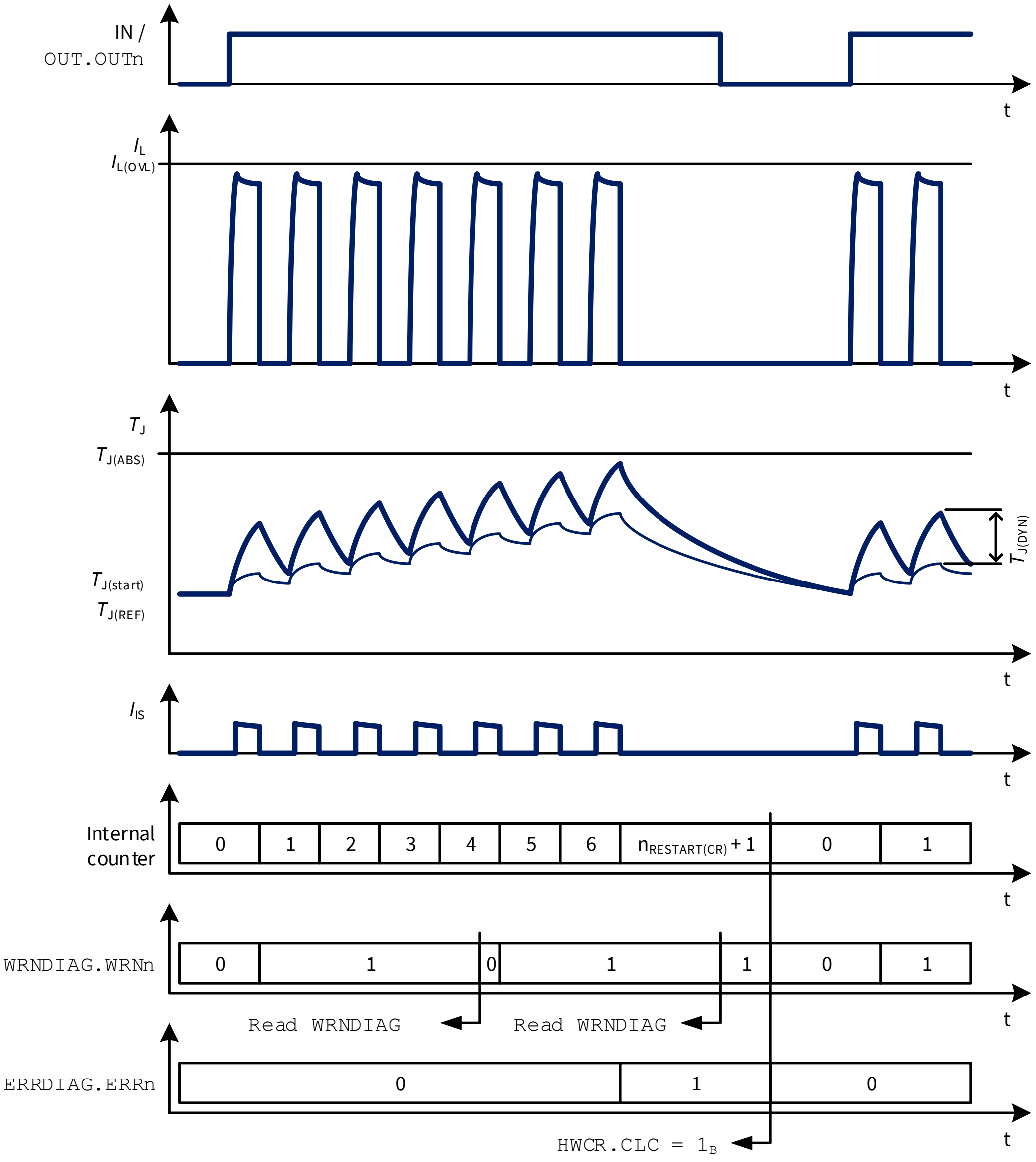


Figure 25 Overtemperature Protection (Absolute)


IN /
OUT.OUTn
t
I_L
$I_{L(OVL)}$
t
T_J
$T_{J(ABS)}$
$T_{J(start)}$
$T_{J(REF)}$
$T_{J(DYN)}$
t
I_{IS}
t
Internal
counter
0
1
2
3
4
5
6
$n_{RESTART(CR)} + 1$
0
1
t
WRNDIAG.WRNn
0
1
0
1
1
0
1
t
Read WRNDIAG
Read WRNDIAG
ERRDIAG.ERRn
0
1
0
t
HWCR.CLC = 1_B

Protection_dT_Restart.emf

Figure 26 Overtemperature Protection (Dynamic)

When the Overtemperature protection circuitry allows the channel to be switched ON again, the restart strategy described in **Chapter 8.3.1** is followed.

8.2 Overload Protection

The BTS71220-4ESE is protected in case of Overload or short circuit to ground. Two Overload thresholds are defined (see **Figure 27**) and selected automatically depending on the voltage V_{DS} across the power DMOS:

- $I_{L(OVL0)}$ when $V_{DS} < 13$ V
- $I_{L(OVL1)}$ when $V_{DS} > 22$ V

In addition, the Overload threshold can be reduced by setting `OCR.OCTn`.

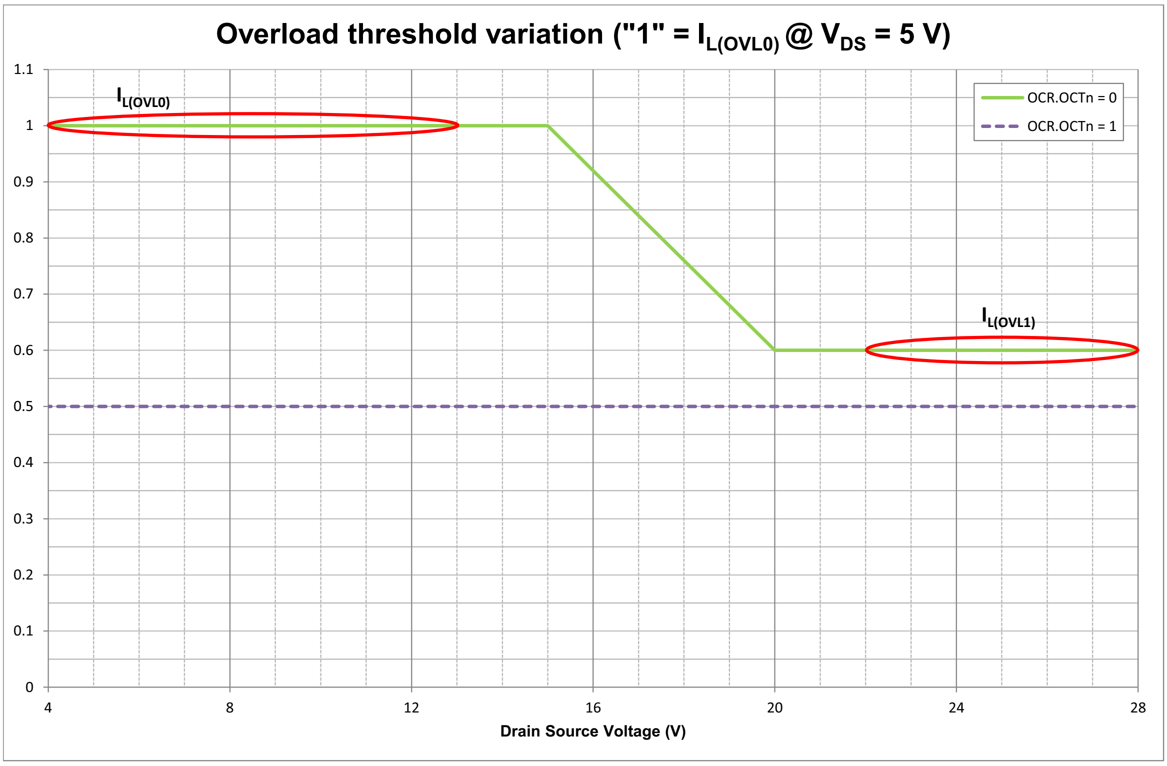


Figure 27 Overload current thresholds

When $I_L \geq I_{L(OVL)}$ (either $I_{L(OVL0)}$ or $I_{L(OVL1)}$), the channel is switched OFF. The channel is allowed to restart according to the restart strategy described in **Chapter 8.3.1**.

8.3 Protection and Diagnosis in case of Fault

Any event that triggers a protection mechanism (either Overtemperature or Overload) has 3 consequences:

- The affected channel switches OFF and the internal counter is incremented
- The current sense of the affected channel is set to high impedance
- The corresponding `WRNDIAG.WRNn` are set to 1_B and latched until readout.

The channel can be switched ON again if all the protection mechanisms fulfill the “restart” conditions described in **Table 19** and the internal restart counter is enabled (`RCD.RCDn` set to 0_B).

Table 19 Protection “Restart” Condition

Fault condition	Switch OFF event	“Restart” Condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis) $n_{RESTART} < n_{RESTART(CR)}$ **RCD.RCDn** = 0
Overload	$I_L \geq I_{L(OVL)}$	I_L < 50 mA T_J within $T_{J(ABS)}$ and $T_{J(DYN)}$ ranges (including hysteresis) $n_{RESTART} < n_{RESTART(CR)}$ **RCD.RCDn** = 0

8.3.1 Restart Strategy

When INx or **OUT.OUTn** is set to “high”, the corresponding channel is switched ON. In case of fault condition the output stage is switched OFF. The channel is allowed to restart only in case the “restart” conditions for the protection mechanisms are fulfilled (see **Table 19**). The **WRNDIAG.WRNn** is set during Overcurrent shutdown. It is reset when the internal fault signal is cleared and the **WRNDIAG** is transmitted, unless latched state is reached by exceeding $n_{RESTART(CR)}$. The next Overcurrent event set the **WRNDIAG.WRNn** again. In case the automatic restarts are not required, they can be deactivated by setting **RCD.RCDn** to 1_B. When **RCD.RCDn** is set to 1_B, the restart counter will be reset. When a channel reaches latched state, the corresponding **ERRDIAG.ERRn** bit is set. The restart latch and counter are cleared by setting the SPI bit **HWCR.CLC** to 1_B. If the input pin is “high” or **OUT.OUTn** is still set to 1_B, the channel is switched ON immediately after the command that set **HWCR.CLC** bit to 1_B. To ensure an adequate cool down after latch-OFF condition, application software needs to wait for $t > t_{RETRY}$ before restarting the channel.

The restart strategy is shown in **Figure 28**.

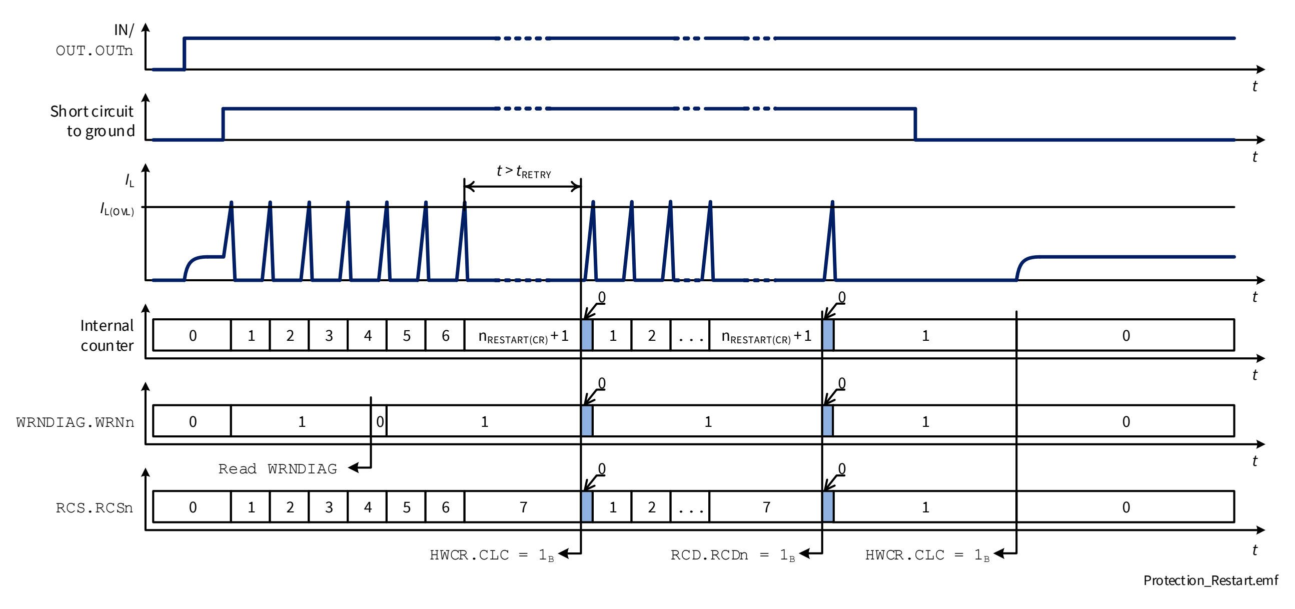

IN/
OUT.OUTn
t
Short circuit
to ground
t
I_L
$I_{L(OVL)}$
$t > t_{RETRY}$
t
Internal
counter
0
1
2
3
4
5
6
$n_{RESTART(CR)}+1$
1
2
...
$n_{RESTART(CR)}+1$
1
0
t
WRNDIAG.WRNn
0
1
0
1
1
1
0
t
Read WRNDIAG
RCS.RCSn
0
1
2
3
4
5
6
7
1
2
...
7
1
0
t
HWCR.CLC = 1_B
RCD.RCDn = 1_B
HWCR.CLC = 1_B
Protection_Restart.emf

Figure 28 Restart Strategy timing diagram

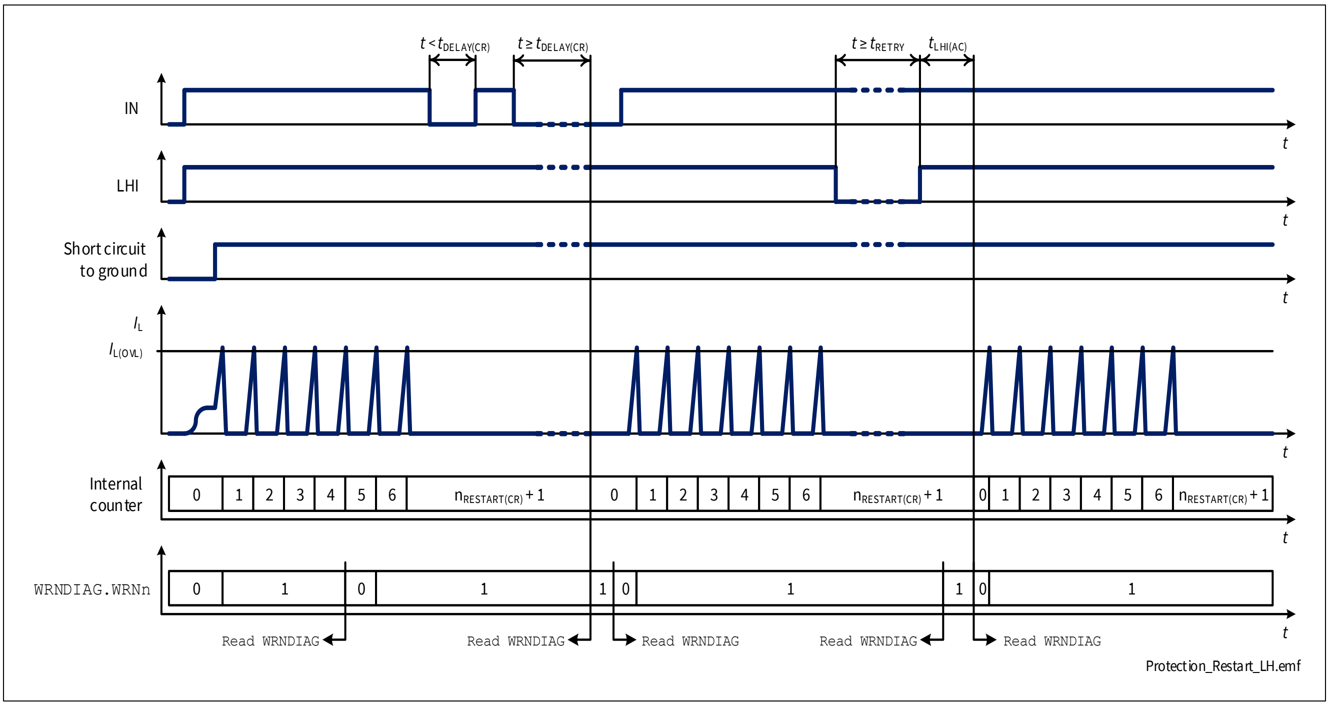

t < t_DELAY(CR)
t ≥ t_DELAY(CR)
t ≥ t_RETRY
t_LHI(AC)
IN
LHI
Short circuit to ground
I_L
I_L(OVL)
Internal counter
0 1 2 3 4 5 6 n_RESTART(CR) + 1
WRNDIAG.WRNn
Read WRNDIAG
t
Protection_Restart_LH.emf

Figure 29 Restart Strategy timing diagram in Limp Home

8.4 Additional protections

8.4.1 Reverse Polarity Protection

In Reverse Polarity condition (also known as Reverse Battery), the output stages are switched ON (see parameter $R_{DS(REV)}$) because of ReverSave™ feature which limits the power dissipation in the output stages. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stages must be limited by the connected loads. The current through digital power supply V_{DD} and Digital Input pins has to be limited as well by an external resistor (please refer to the Absolute Maximum Ratings listed in **Chapter 4.1** and to Application Information in **Chapter 11**).

Figure 30 shows a typical application including a device with ReverSave™. A current flowing into GND pin ($-I_{GND}$) during Reverse Polarity condition is necessary to activate ReverSave™, therefore a resistive path between module ground and device GND pin must be present.

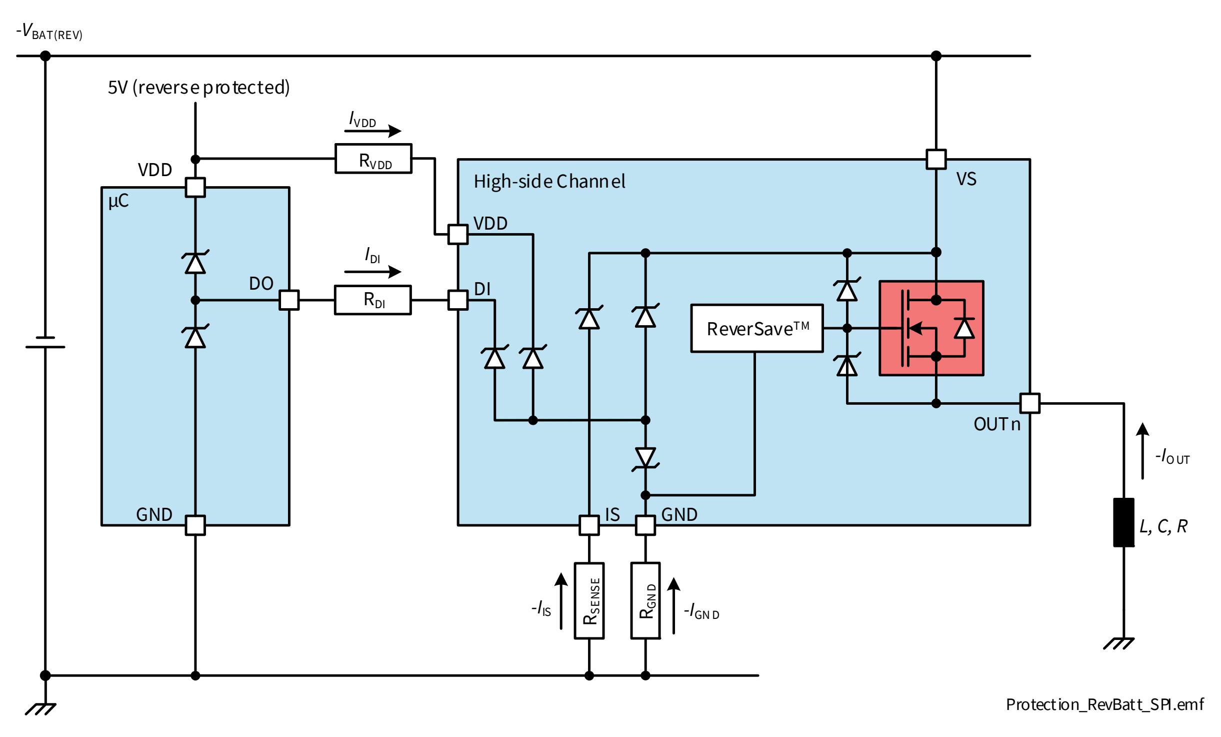

-V_BAT(REV)
5V (reverse protected)
I_VDD
R_VDD
VDD
µC
I_DI
R_DI
DO
DI
High-side Channel
VDD
VS
ReverSave™
OUT n
-I_OUT
L, C, R
GND
IS
GND
-I_IS
R_SENSE
R_GND
-I_GND
Protection_RevBatt_SPI.emf

Figure 30 Reverse Battery Protection (application example)

8.4.2 Overvoltage Protection

In the case of supply voltages between $V_{S(EXT,UP)}$ and $V_{BAT(LD)}$, the output transistors are still operational and follow the input pins or the `OUT` register. In addition to the output clamp for inductive loads as described in **Chapter 7.2.2**, there is a clamp mechanism available for Overvoltage protection for the logic and the output channels, monitoring the voltage between VS and GND pins ($V_{S(CLAMP)}$).

8.5 Protection against loss of connection

8.5.1 Loss of Battery and Loss of Load

The loss of connection to battery or to the load has no influence on device robustness when load and wire harness are purely resistive. In case of driving an inductive load, the energy stored in the inductance must be handled. BTS71220-4ESE can handle the inductivity of the wire harness up to 10 µH with $I_{L(NOM)}$. In case of applications where currents and/or the aforementioned inductivity are exceeded, an external suppressor diode (like diode D_{Z2} shown in **Chapter 11**) is recommended to handle the energy and to provide a well-defined path to the load current.

Note: In case of a lost battery connection the VS monitoring function protects the SPI registers as soon the device is out of Sleep mode. This means that any command sent to the device will be ignored and the device will just send back the ***`STDDIAG`****. Furthermore, the status of the LHI pin is blanked, which means that it is not possible to enter Limp Home mode.*

8.5.2 Loss of Ground

In case of loss of device ground, it is recommended to have a resistor connected between any Digital Input pin and the microcontroller to ensure a channel switch OFF (as described in **Chapter 11**).

Note: In case any Digital Input pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground. The same behavior applies for the SPI functionality.

8.6 Electrical Characteristics Protection

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: $R_L = 2.6\ \Omega$

27W output: $R_L = 4.8\ \Omega$

Table 20 Electrical Characteristics: Protection - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Shutdown Temperature (Absolute)	$T_{J(ABS)}$	150	175	200	°C	[1][2] See **Figure 25**	P_8.6.0.1
Thermal Shutdown Hysteresis (Absolute)	$T_{HYS(ABS)}$	–	30	–	K	[3] See **Figure 25**	P_8.6.0.2
Thermal Shutdown Temperature (Dynamic)	$T_{J(DYN)}$	–	80	–	K	[3] See **Figure 26**	P_8.6.0.3
Power Supply Clamping Voltage at T_J = -40 °C	$V_{S(CLAMP)\_-40}$	33	36.5	42	V	I_{VS} = 5 mA T_J = -40 °C See **Figure 20**	P_8.6.0.6
Power Supply Clamping Voltage at $T_J \geq 25$ °C	$V_{S(CLAMP)\_25}$	35	38	44	V	[2] I_{VS} = 5 mA $T_J \geq 25$ °C See **Figure 20**	P_8.6.0.7
Power Supply Voltage Threshold for Overcurrent Threshold Reduction in case of Short Circuit	$V_{S(JS)}$	20.5	22.5	24.5	V	[3] Setup acc. to AEC-Q100-012	P_8.6.0.8

1) Functional test only.
2) Tested at T_J = 150°C only.
3) Not subject to production test - specified by design.

8.6.1 Electrical Characteristics Protection - SPOC™

Table 21 Electrical Characteristics: Protection - SPOC™

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Counter Reset Delay Time after Fault Condition in Limp Home	$t_{DELAY(CR)}$	40	70	100	ms	[1] LHI = "high" INx = "low"	P_8.6.2.1
Automatic Restarts in Case of Fault after a Counter Reset	$n_{RESTART(CR)}$	–	6	–	–	[1]	P_8.6.2.2

1) Not subject to production test - specified by design.

8.7 Electrical Characteristics Protection - Power Output Stages

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: R_L = 2.6 Ω

27W output: R_L = 4.8 Ω

8.7.1 Protection Power Output Stage - 55 W channels

Table 22 Electrical Characteristics: Protection - 55 W channels

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload Detection Current High Level	$I_{L(OVL0)}$	79	89	99	A	1) OCR.OCTn= 0_B T_J = -40 °C to 50 °C dI/dt = 0.4 A/µs	P_8.7.15.3
Overload Detection Current High Level	$I_{L(OVL0)}$	65	72	79	A	2) OCR.OCTn= 0_B T_J = 150 °C dI/dt = 0.4 A/µs	P_8.7.15.4
Overload Detection Current Low Level	$I_{L(OVL2)}$	36	45	54	A	2) OCR.OCTn= 1_B dI/dt = 0.4 A/µs	P_8.7.15.2
Overload Detection Current High Level (parallel mode)	$I_{L(OVL3)}$	38	54	62	A	2)3) OCR.OCTn= 0_B PCS.PCCn= 1_B dI/dt = 0.4 A/µs	P_8.7.15.6
Overload Detection Current at High V_{DS}	$I_{L(OVL1)}$	–	54	–	A	2) dI/dt = 0.4 A/µs	P_8.7.15.5
Overload Detection Current Jump Start Condition	$I_{L(OVL\_JS)}$	–	54	–	A	2) OCR.OCTn= 0_B $V_S > V_{S(JS)}$ dI/dt = 0.4 A/µs	P_8.7.15.7

1) Tested at T_J = -40 °C.

2) Not subject to production test - specified by design.

3) $I_{L(OVL3)}$ applies for one channel. Total current for two channels in parallel $I_{L(OVL)} \leq 2 \times I_{L(OVL3)}$.

8.7.2 Protection Power Output Stage - 27 W channels

Table 23 Electrical Characteristics: Protection - 27 W channels

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload Detection Current High Level	$I_{L(OVL0)}$	44	48	53	A	[1] `OCR.OCTn`= 0_B T_J = -40 °C to 50 °C dI/dt = 0.2 A/µs	P_8.7.16.3
Overload Detection Current High Level	$I_{L(OVL0)}$	35	39	44	A	[2] `OCR.OCTn`= 0_B T_J = 150 °C dI/dt = 0.2 A/µs	P_8.7.16.4
Overload Detection Current Low Level	$I_{L(OVL2)}$	19	24	29	A	[2] `OCR.OCTn`= 1_B dI/dt = 0.2 A/µs	P_8.7.16.2
Overload Detection Current High Level (parallel mode)	$I_{L(OVL3)}$	22	31	36	A	[2][3] `OCR.OCTn`= 0_B `PCS.PCCn`= 1_B dI/dt = 0.2 A/µs	P_8.7.16.6
Overload Detection Current at High V_{DS}	$I_{L(OVL1)}$	–	29	–	A	[2] dI/dt = 0.2 A/µs	P_8.7.16.5
Overload Detection Current Jump Start Condition	$I_{L(OVL\_JS)}$	–	29	–	A	[2] `OCR.OCTn`= 0_B $V_S > V_{S(JS)}$ dI/dt = 0.2 A/µs	P_8.7.16.7

1) Tested at T_J = -40 °C.

2) Not subject to production test - specified by design.

3) $I_{L(OVL3)}$ applies for one channel. Total current for two channels in parallel $I_{L(OVL)} \leq 2 \times I_{L(OVL3)}$.

9 Diagnosis

For diagnosis purpose, the BTS71220-4ESE provides a current sense at pin IS as well as a diagnosis feedback via SPI. In case of disabled diagnostic, IS pin becomes high impedance. The integrated current sense multiplexer is controlled via SPI.

A sense resistor R_{SENSE} must be connected between IS pin and module ground if the current sense diagnosis is used. R_{SENSE} value has to be higher than 820 Ω (or 400 Ω when a central Reverse Battery protection is present on the battery feed) to limit the power losses in the sense circuitry. A typical value is R_{SENSE} = 1.2 kΩ.

Due to the internal connection between IS pin and V_S supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices, if they are supplied by a different battery feed or using a different sense concept.

See **Figure 31** for details as an overview. For diagnosis feedback at different operation modes, please see **Chapter 9.2**.

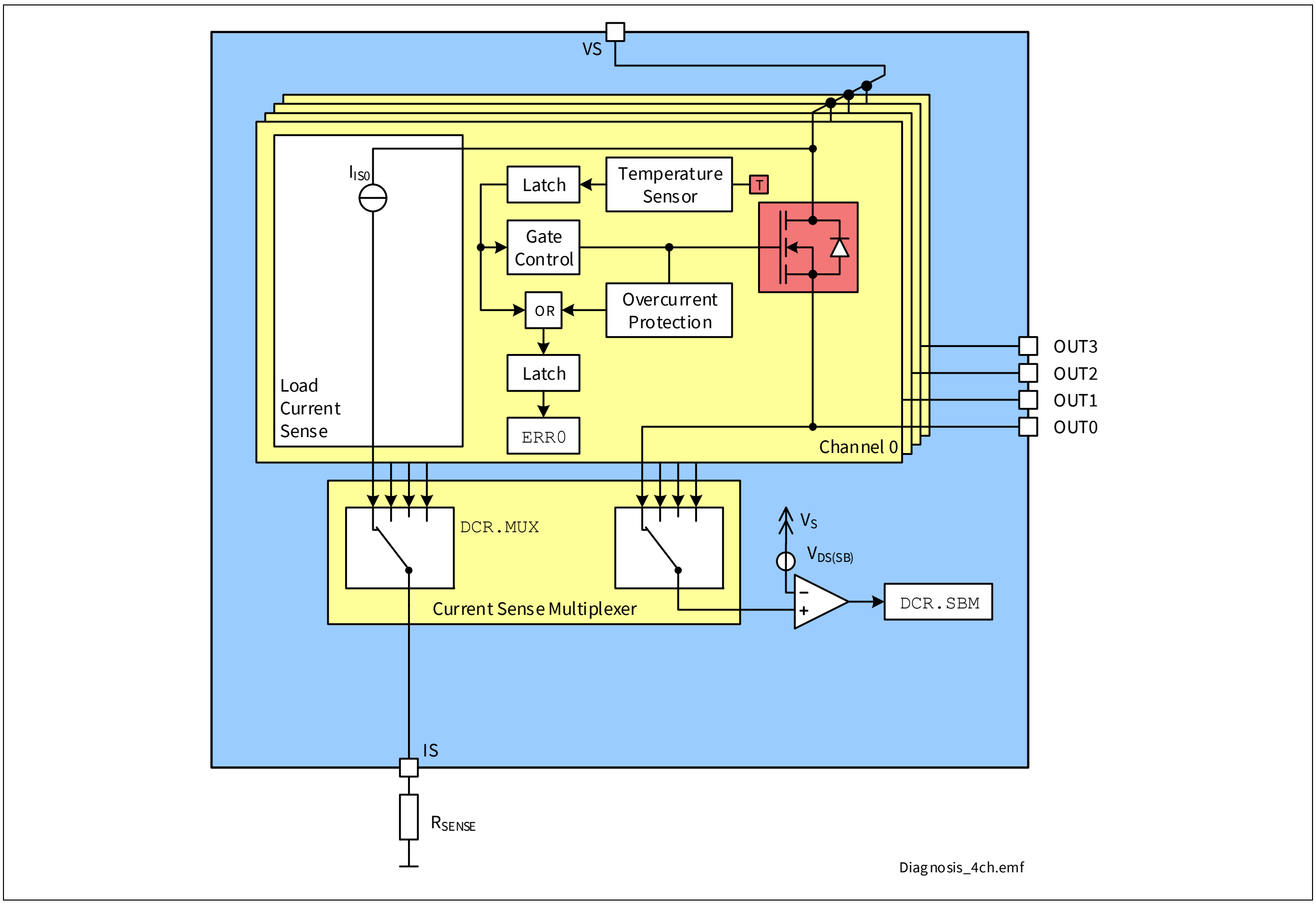

VS
I_{IS0}
Latch
Temperature Sensor
T
Gate Control
OR
Overcurrent Protection
Latch
ERR0
Load Current Sense
Channel 0
OUT3
OUT2
OUT1
OUT0
DCR.MUX
Current Sense Multiplexer
V_S
$V_{DS(SB)}$
DCR.SBM
IS
R_{SENSE}
Diagnosis_4ch.emf

Figure 31 Diagnosis block diagram

9.1 Overview

Table 24 gives a quick reference to the state of the IS pin during BTS71220-4ESE operation.

Table 24 Diagnosis feedback, Function of Operation Mode

Operation Mode	Input level `OUT.OUTn`	V_{OUT}	Current sense I_{IS}	`WRNDIAG.WRNn`	`STDDIAG.SBM`
Normal operation	Low / 0_B OFF	~ GND	Z	0	1
Short circuit to GND		~ GND	Z	0	1
Overtemperature		Z	Z	1	x
Short circuit to V_S		V_S	Z	0	0
Open Load		$< V_S - V_{DS(SB)}$ $> V_S - V_{DS(SB)}$[1]	Z Z	0 0	1 0
Sense verification[2]		x	$I_{IS(VER)}$	x	0
Normal operation	High / 1_B ON	$\sim V_S$	$I_{IS} = I_{L(NOM)} / k_{ILIS}$	0	0
Overload		$< V_S$	$I_{IS} = I_L / k_{ILIS}$	0	x
Short circuit to GND		~ GND	Z	1	1
Overtemperature		Z	Z	1	x
Short circuit to V_S		V_S	$I_{IS} < I_L / k_{ILIS}$	0	0
Open Load		$\sim V_S$[3]	$I_{IS} = I_{IS(EN)}$	0	0
Sense verification[2]		x	$I_{IS(VER)}$	x	0
Under load (e.g. Output Voltage Limitation condition)		$\sim V_S$[4]	$I_{IS(EN)} < I_{IS} < I_{L(NOM)} / k_{ILIS}$	0	0

[1] With additional pull-up resistor.

[2] `DCR.MUX` = 101_B.

[3] The output current has to be smaller than $I_{L(OL)}$.

[4] The output current has to be higher than $I_{L(OL)}$.

9.2 Diagnosis Word at SPI

Diagnostic information about the status of each channel is provided through SPI. The fault flags, an OR combination of the overtemperature flags and the Overload monitoring signals are provided in the **`WRNDIAG`** register.

The Overload monitoring signals are latched in the **`WRNDIAG.WRNn`** bits and cleared each time the **`WRNDIAG`** is transmitted via SPI unless the maximum number of restarts is reached and the channel protects itself. The protection latches are cleared by SPI command **`HWCR.CLC`**.

9.3 Diagnosis in ON state

A current proportional to the load current (ratio $k_{ILIS} = I_L / I_{IS}$) is provided at pin IS when the following conditions are fulfilled:

- A power output stage is switched ON with $V_{DS} < V_{DS(SB)}$
- The diagnosis is enabled for that channel
- No fault (as described in **Chapter 8.3**) is present

If a “hard” failure mode is present or occurs for the channel selected using the **`DCR.MUX`** bits, the IS pin remains in or changes to “high impedance” state.

9.3.1 Current Sense (k_{ILIS})

The accuracy of the sense current depends on temperature and load current. I_{IS} increases linearly with I_L output current until it reaches the saturation current $I_{IS(SAT)}$. In case of Open Load at the output stage (I_L close to 0 A), the maximum sense current $I_{IS(EN)}$ (no load, diagnosis enabled) is specified. This condition is shown in **Figure 33**. The blue line represents the ideal k_{ILIS} line, while the red lines show the behavior of a typical product.

An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1 µs for the RC filter is recommended).

The k_{ILIS} factor is specified with limits that take into account effects due to temperature, supply voltage and manufacturing process. Tighter limits are possible (within a defined current window) with calibration:

- A well-defined and precise current ($I_{L(CAL)}$) is applied at the output during End of Line test at customer side
- The corresponding current at IS pin is measured and the k_{ILIS} is calculated (k_{ILIS} @ $I_{L(CAL)}$)
- Within the current range going from $I_{L(CAL)\_L}$ to $I_{L(CAL)\_H}$ the k_{ILIS} is equal to k_{ILIS} @ $I_{L(CAL)}$ with limits defined by Δk_{ILIS}

The derating of k_{ILIS} after calibration is calculated using the formulas in **Figure 32** and it is specified by Δk_{ILIS}

$$\Delta k_{ILIS,MAX} = 100 \cdot MAX\left(\frac{k_{ILIS}@I_{L(CAL)\_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)\_H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

$$\Delta k_{ILIS,MIN} = 100 \cdot MIN\left(\frac{k_{ILIS}@I_{L(CAL)\_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)\_H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

Diagnosis_dKILIS.emf

Figure 32 Δk_{ILIS} calculation formulas

The calibration is intended to be performed at $T_{A(CAL)}$ = 25°C. The parameter Δk_{ILIS} includes the drift overtemperature as well as the drift over the current range from $I_{L(CAL)\_L}$ to $I_{L(CAL)\_H}$.

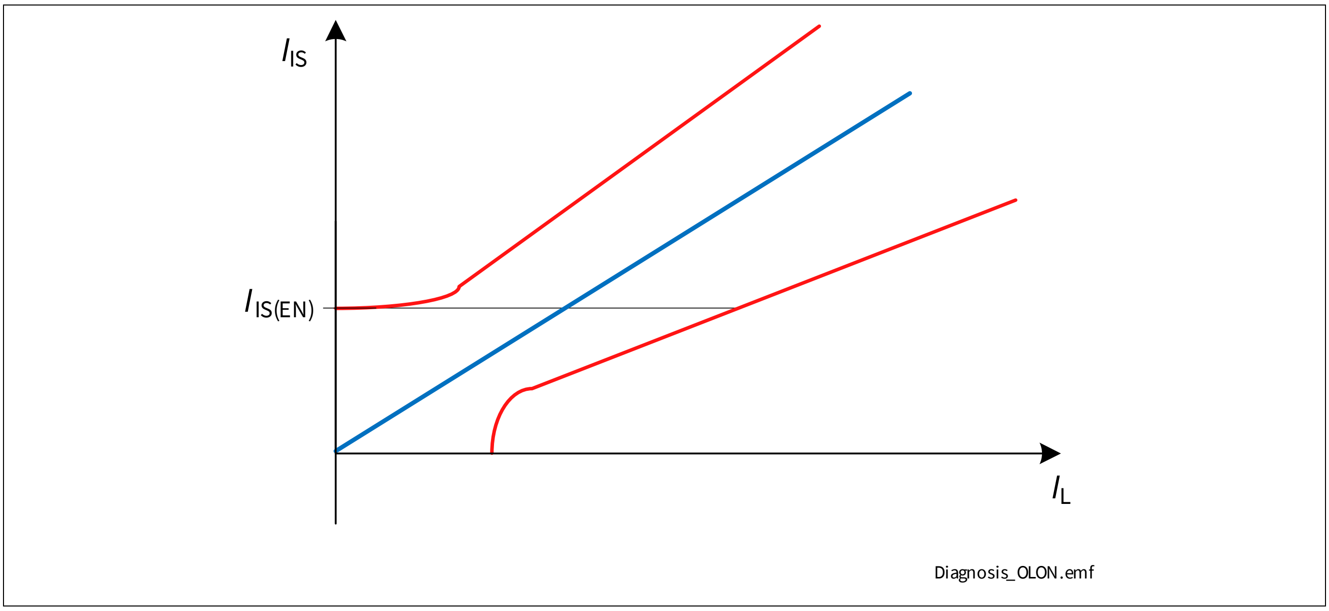


Figure 33 Current Sense Ratio in Open Load at ON condition

9.3.2 Current Sense Multiplexer

There is a current sense multiplexer implemented in the BTS71220-4ESE that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register **DCR.MUX**. The sense current can also be disabled by SPI register **DCR.MUX**. For details on timing of the current sense multiplexer, refer to **Figure 34**. In addition **DCR.MUX** is used in combination with other SPI bits to address further functions of the device. To verify the function of the current sensing path in ON and OFF state, the device offers a sense verification mode. In this mode a predefined current $I_{IS(VER)}$ is provided on the current sense pin independent on the load condition of any channel. This enables the microcontroller to verify the sense path at any time. The sense verification mode is enabled when **DCR.MUX** = 101_B.

All commands and functions involving the **DCR.MUX** bits are listed below:

- The main function of **DCR.MUX** is to switch the current sense multiplexer
- Executing **PCS.CLCS** = 1_B clears the counter and latches OFF the channel selected by **DCR.MUX**
- Executing **PCS.SRCS** = 1_B the slew rate of the channel selected by **DCR.MUX** will be changed. See **Chapter 7.4.1** for further information
- When reading **RCS.RCSn** bits, the status of the internal counter of the channel selected by **DCR.MUX** is responded
- When setting **DCR.MUX** = 101_B the sense verification mode is enabled
- When setting **PCS.SRCS** = 1b, the slew rate of the channel selected by **DCR.MUX** will be adjusted

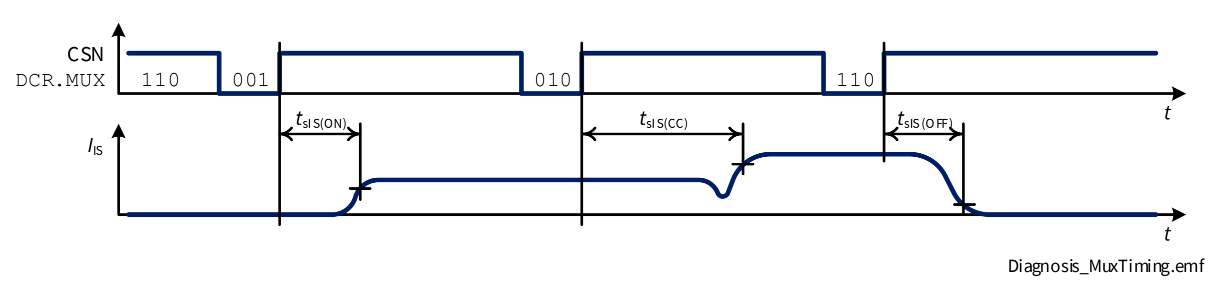

CSN
DCR.MUX
110
001
010
110
$t_{\mathrm{sIS(ON)}}$
$t_{\mathrm{sIS(CC)}}$
$t_{\mathrm{sIS(OFF)}}$
I_{IS}
t
t
Diagnosis_MuxTiming.emf

Figure 34 Current Sense Multiplexer Timings

9.4 Diagnosis in OFF state

When a power output stage is in OFF state, the BTS71220-4ESE can measure the output voltage and compare it with a threshold voltage. In this way, using some additional external components (a pull-down resistor and a switchable pull-up current source), it is possible to detect if the load is missing or if there is a short circuit to battery.

9.4.1 Switch Bypass Monitor

To detect short circuit to V_S, there is a switch bypass monitor implemented. In case of short circuit between the output pin OUT and VS in ON state, the current flows through the power transistor as well as through the short circuit (bypass) with undefined share between the two. As a result, the current sense signal shows lower values than expected by the load current. In OFF state, the output voltage remains close to V_S potential which leads to a small V_{DS}. The switch bypass monitor compares the threshold $V_{DS(SB)}$ with the voltage V_{DS} across the power transistor of that channel which is selected by the current sense multiplexer (**`DCR.MUX`**). The result of the comparison can be read in the standard diagnosis **`STDDIAG.SBM`**. In addition the switch bypass monitor can be used to detect an Open Load in OFF state. In this case a switchable pull-up resistor has to be placed to pull the OUT to VS potential.

9.5 SENSE Timings

Figure 35 shows the timing during settling $t_{\mathrm{sIS(ON)}}$ and disabling $t_{\mathrm{sIS(OFF)}}$ of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before t_{ON}), $t_{\mathrm{sIS(DIAG)}} = t_{\mathrm{sIS(ON)}} + t_{\mathrm{ON}}$.

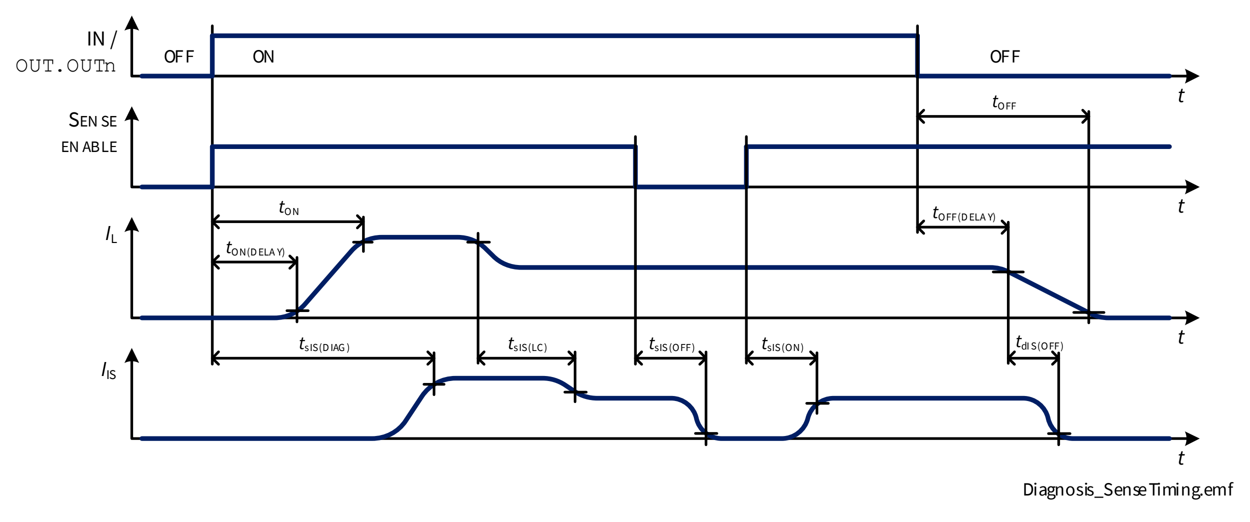

IN /
OUT.OUTn
OFF
ON
OFF
t_{OFF}
t
SENSE
ENABLE
t
t_{ON}
$t_{\mathrm{ON(DELAY)}}$
$t_{\mathrm{OFF(DELAY)}}$
I_L
t
$t_{\mathrm{sIS(DIAG)}}$
$t_{\mathrm{sIS(LC)}}$
$t_{\mathrm{sIS(OFF)}}$
$t_{\mathrm{sIS(ON)}}$
$t_{\mathrm{dIS(OFF)}}$
I_{IS}
t
Diagnosis_SenseTiming.emf

Figure 35 SENSE Settling / Disabling Timing

9.6 Electrical Characteristics Diagnosis

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: R_L = 2.6 Ω

27W output: R_L = 4.8 Ω

Table 25 Electrical Characteristics: Diagnosis - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SENSE Saturation Current	$I_{IS(SAT)}$	4.2	–	15	mA	[1] R_{SENSE} = 1.2 kΩ	P_9.6.0.12
SENSE Leakage Current when Disabled	$I_{IS(OFF)}$	–	0.01	0.5	µA	$I_L \geq I_{L(NOM)}$ V_{IS} = 0 V **DCR.MUX** = 110_B	P_9.6.0.2
SENSE Leakage Current when Enabled at $T_J \leq 85$ °C	$I_{IS(EN)\_85}$	–	0.2	1	µA	[1] $T_J \leq 85$ °C **DCR.MUX** ≠ <110_B,111_B> See **Figure 33**	P_9.6.0.3
SENSE Leakage Current when Enabled at T_J = 150 °C	$I_{IS(EN)\_150}$	–	1	2	µA	T_J = 150 °C **DCR.MUX** ≠ <110_B,111_B> See **Figure 33**	P_9.6.0.11
SENSE Operative Range for k_{ILIS} Operation (V_S - V_{IS})	V_{SIS_k}	–	0.5	1	V	[1] V_S = 6 V INx = "high" or **OUT.OUTn** = 1_B $I_L \leq 2 * I_{L(NOM)}$	P_9.6.0.6
Power Supply to IS Pin Clamping Voltage at T_J = -40 °C	$V_{SIS(CLAMP)\_-40}$	33	36.5	42	V	I_{IS} = 1 mA T_J = -40 °C See **Figure 20**	P_9.6.0.9
Power Supply to IS Pin Clamping Voltage at $T_J \geq 25$ °C	$V_{SIS(CLAMP)\_25}$	35	38	44	V	[2] I_{IS} = 1 mA $T_J \geq 25$ °C See **Figure 20**	P_9.6.0.10

1) Not subject to production test - specified by design.
2) Tested at T_J = 150°C.

9.6.1 Electrical Characteristics Diagnosis - SPOC™

Table 26 Electrical Characteristics: Diagnosis - Thresholds, Timings

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Switch Bypass Monitor Threshold	$V_{DS(SB)}$	1.3	1.9	2.5	V	OFF state	P_9.6.2.1
SENSE Settling Time with Nominal Load Current Stable	$t_{sIS(ON)}$	–	8	20	µs	V_S = 13.5 V $I_L = I_{L(NOM)}$ **DCR.MUX**: 110_B → 001_B	P_9.6.2.2
SENSE Settling Time with Small Load Current Stable	$t_{sIS(ON)\_SLC}$	–	–	60	µs	2) V_S = 13.5 V $I_L = I_{L(CAL)\_OL}$ **DCR.MUX**: 110_B → 001_B	P_9.6.2.10
SENSE Settling Time after Channel Change	$t_{sIS(CC)}$	–	–	20	µs	1) V_S = 13.5 V $I_L = I_{L(NOM)}$ **DCR.MUX**: 001_B → 010_B	P_9.6.2.4
SENSE Settling Time after Channel Change with Small Load Current	$t_{sIS(CC)\_SLC}$	–	–	60	µs	1)2) V_S = 13.5 V Start channel: $I_L = I_{L(CAL)}$ End channel: $I_L = I_{L(CAL)\_OL}$ **DCR.MUX**: 001_B → 010_B	P_9.6.2.11
SENSE Disable Time	$t_{sIS(OFF)}$	–	–	20	µs	1) V_S = 13.5 V $I_L = I_{L(NOM)}$ **DCR.MUX**: 010_B → 110_B	P_9.6.2.5
SENSE Settling Time after Load Change	$t_{sIS(LC)}$	–	–	20	µs	2)	P_9.6.2.6
SENSE Settling Time after Load Change with Small Load Current	$t_{sIS(LC)\_SLC}$	–	250	400	µs	2) V_S = 13.5 V from $I_L = I_{L(CAL)}$ to $I_L = I_{L(CAL)\_OL}$	P_9.6.2.12
SENSE Disable Time after Channel Deactivation	$t_{dIS(OFF)}$	–	–	20	µs	2)	P_9.6.2.7
SENSE Current in Sense Verification Mode	$I_{IS(VER)}$	400	500	600	µA	**DCR.MUX** = 101_B	P_9.6.2.8

1) Production test for functionality within parameter limits.

2) Not subject to production test - specified by design.

9.7 Electrical Characteristics Diagnosis - Power Output Stages

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 5.0 V, V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

55W output: $R_L = 2.6\ \Omega$

27W output: $R_L = 4.8\ \Omega$

9.7.1 Diagnosis Power Output Stage 55 W Channels

Table 27 Electrical Characteristics: Diagnosis - 55 W channels

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Open Load Output Current at $I_{IS} = 4\ \mu A$	$I_{L(OL)\_4u}$	5	18	50	mA	1) $I_{IS} = I_{IS(OL)} = 4\ \mu A$	P_9.7.15.1
Current Sense Ratio at $I_L = I_{L02}$	k_{ILIS02}	-65%	5000	+65%		1) `KRC.KRCn` = 0_B I_{L02} = 20 mA	P_9.7.15.4
Current Sense Ratio at $I_L = I_{L05}$	k_{ILIS05}	-60%	5000	+60%		1) `KRC.KRCn` = 0_B I_{L05} = 100 mA	P_9.7.15.7
Current Sense Ratio at $I_L = I_{L07}$	k_{ILIS07}	-55%	5000	+55%		1) `KRC.KRCn` = 0_B I_{L07} = 250 mA	P_9.7.15.9
Current Sense Ratio at $I_L = I_{L10}$	k_{ILIS10}	-40%	5000	+40%		1) `KRC.KRCn` = 0_B I_{L10} = 1 A	P_9.7.15.12
Current Sense Ratio at $I_L = I_{L13}$	k_{ILIS13}	-24%	5000	+24%		`KRC.KRCn` = 0_B I_{L13} = 2.8 A	P_9.7.15.15
Current Sense Ratio at $I_L = I_{L15}$	k_{ILIS15}	-8%	5000	+8%		`KRC.KRCn` = 0_B I_{L15} = 5.5 A	P_9.7.15.17
Current Sense Ratio at $I_L = I_{L17}$	k_{ILIS17}	-8%	5000	+8%		`KRC.KRCn` = 0_B I_{L17} = 10 A	P_9.7.15.19
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	-30	0	+30	%	1)2) $I_{L(CAL)\_OL} = I_{L05}$ $I_{L(CAL)\_OL\_H} = I_{L07}$ $I_{L(CAL)\_OL\_L} = I_{L02}$ $T_{A(CAL)}$ = 25 °C	P_9.7.15.40
SENSE Current Derating with Nominal Current Calibration	$\Delta k_{ILIS(NOM)}$	-9	0	+9	%	1)2) $I_{L(CAL)} = I_{L15}$ $I_{L(CAL)\_H} = I_{L17}$ $I_{L(CAL)\_L} = I_{L13}$ $T_{A(CAL)}$ = 25 °C	P_9.7.15.41

1) Parameter valid only if `PCS.PCCn` = 0_B.

2) Not subject to production test - specified by design.

Table 28 Electrical Characteristics: Diagnosis - 55 W channels

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Open Load Output Current at I_{IS} = 4 µA	$I_{L(OL)\_4u}$	2	9	15	mA	[1][2] $I_{IS} = I_{IS(OL)}$ = 4 µA	P_9.7.15.20
Current Sense Ratio at $I_L = I_{L01}$	k_{ILIS01}	-65%	1660	+65%		[1] **KRC.KRCn** = 1_B I_{L01} = 10 mA	P_9.7.15.22
Current Sense Ratio at $I_L = I_{L03}$	k_{ILIS03}	-60%	1660	+60%		[1][2] **KRC.KRCn** = 1_B I_{L03} = 30 mA	P_9.7.15.24
Current Sense Ratio at $I_L = I_{L05}$	k_{ILIS05}	-55%	1660	+55%		[1][2] **KRC.KRCn** = 1_B I_{L05} = 100 mA	P_9.7.15.27
Current Sense Ratio at $I_L = I_{L07}$	k_{ILIS07}	-45%	1660	+45%		[1][2] **KRC.KRCn** = 1_B I_{L07} = 250 mA	P_9.7.15.30
Current Sense Ratio at $I_L = I_{L08}$	k_{ILIS08}	-35%	1660	+35%		[1] **KRC.KRCn** = 1_B I_{L08} = 450 mA	P_9.7.15.32
Current Sense Ratio at $I_L = I_{L10}$	k_{ILIS10}	-24%	1660	+24%		[2] **KRC.KRCn** = 1_B I_{L10} = 1 A	P_9.7.15.34
Current Sense Ratio at $I_L = I_{L12}$	k_{ILIS12}	-8%	1660	+8%		[2] **KRC.KRCn** = 1_B I_{L12} = 2 A	P_9.7.15.36
Current Sense Ratio at $I_L = I_{L15}$	k_{ILIS15}	-8%	1660	+8%		[2] **KRC.KRCn** = 1_B I_{L15} = 5.5 A	P_9.7.15.39
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	-30	0	+30	%	[1][3] $I_{L(CAL)\_OL} = I_{L03}$ $I_{L(CAL)\_OL\_H} = I_{L05}$ $I_{L(CAL)\_OL\_L} = I_{L01}$ $T_{A(CAL)}$ = 25 °C	P_9.7.15.42
SENSE Current Derating with Nominal Current Calibration	$\Delta k_{ILIS(NOM)}$	-9	0	+9	%	[1][3] $I_{L(CAL)} = I_{L10}$ $I_{L(CAL)\_H} = I_{L12}$ $I_{L(CAL)\_L} = I_{L08}$ $T_{A(CAL)}$ = 25 °C	P_9.7.15.43

1) Parameter valid only if **PCS.PCCn** = 0_B.

2) k_{ILIS} accuracy valid if 1 µs RC filter is placed at ADC input.

3) Not subject to production test - specified by design.

9.7.2 Diagnosis Power Output Stage 27 W Channels

Table 29 Electrical Characteristics: Diagnosis - 27 W channels

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Open Load Output Current at I_{IS} = 4 µA	$I_{L(OL)\_4u}$	2	7	15	mA	1) $I_{IS} = I_{IS(OL)}$ = 4 µA	P_9.7.16.1
Current Sense Ratio at $I_L = I_{L01}$	k_{ILIS01}	-65%	2000	+65%		1) `KRC.KRCn` = 0_B I_{L01} = 10 mA	P_9.7.16.3
Current Sense Ratio at $I_L = I_{L03}$	k_{ILIS03}	-60%	2000	+60%		1) `KRC.KRCn` = 0_B I_{L03} = 30 mA	P_9.7.16.5
Current Sense Ratio at $I_L = I_{L05}$	k_{ILIS05}	-55%	2000	+55%		1) `KRC.KRCn` = 0_B I_{L05} = 100 mA	P_9.7.16.7
Current Sense Ratio at $I_L = I_{L07}$	k_{ILIS07}	-45%	2000	+45%		1) `KRC.KRCn` = 0_B I_{L07} = 250 mA	P_9.7.16.9
Current Sense Ratio at $I_L = I_{L10}$	k_{ILIS10}	-24%	2000	+24%		`KRC.KRCn` = 0_B I_{L10} = 1 A	P_9.7.16.12
Current Sense Ratio at $I_L = I_{L12}$	k_{ILIS12}	-8%	2000	+8%		`KRC.KRCn` = 0_B I_{L12} = 2 A	P_9.7.16.14
Current Sense Ratio at $I_L = I_{L15}$	k_{ILIS15}	-8%	2000	+8%		`KRC.KRCn` = 0_B I_{L15} = 5.5 A	P_9.7.16.17
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	-30	0	+30	%	1)2) $I_{L(CAL)\_OL} = I_{L03}$ $I_{L(CAL)\_OL\_H} = I_{L05}$ $I_{L(CAL)\_OL\_L} = I_{L01}$ $T_{A(CAL)}$ = 25 °C	P_9.7.16.37
SENSE Current Derating with Nominal Current Calibration	$\Delta k_{ILIS(NOM)}$	-9	0	+9	%	2) $I_{L(CAL)} = I_{L12}$ $I_{L(CAL)\_H} = I_{L15}$ $I_{L(CAL)\_L} = I_{L10}$ $T_{A(CAL)}$ = 25 °C	P_9.7.16.38

1) Parameter valid only if `PCS.PCCn` = 0_B.

2) Not subject to production test - specified by design.

Table 30 Electrical Characteristics: Diagnosis - 27 W channels

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Open Load Output Current at I_{IS} = 4 µA	$I_{L(OL)\_4u}$	0.5	3.2	6	mA	1)2) $I_{IS} = I_{IS(OL)}$ = 4 µA	P_9.7.16.18
Current Sense Ratio at $I_L = I_{L00}$	k_{ILIS00}	-65%	660	+65%		1) **KRC.KRCn** = 1_B I_{L00} = 5 mA	P_9.7.16.19
Current Sense Ratio at $I_L = I_{L01}$	k_{ILIS01}	-60%	660	+60%		1)2) **KRC.KRCn** = 1_B I_{L01} = 10 mA	P_9.7.16.20
Current Sense Ratio at $I_L = I_{L03}$	k_{ILIS03}	-55%	660	+55%		1)2) **KRC.KRCn** = 1_B I_{L03} = 30 mA	P_9.7.16.23
Current Sense Ratio at $I_L = I_{L05}$	k_{ILIS05}	-45%	660	+45%		1)2) **KRC.KRCn** = 1_B I_{L05} = 100 mA	P_9.7.16.26
Current Sense Ratio at $I_L = I_{L07}$	k_{ILIS07}	-30%	660	+30%		1)2) **KRC.KRCn** = 1_B I_{L07} = 250 mA	P_9.7.16.29
Current Sense Ratio at $I_L = I_{L08}$	k_{ILIS08}	-20%	660	+20%		**KRC.KRCn** = 1_B I_{L08} = 450 mA	P_9.7.16.31
Current Sense Ratio at $I_L = I_{L10}$	k_{ILIS10}	-8%	660	+8%		2) **KRC.KRCn** = 1_B I_{L10} = 1 A	P_9.7.16.33
Current Sense Ratio at $I_L = I_{L12}$	k_{ILIS12}	-8%	660	+8%		**KRC.KRCn** = 1_B I_{L12} = 2 A	P_9.7.16.35
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	-30	0	+30	%	1)3) $I_{L(CAL)\_OL} = I_{L01}$ $I_{L(CAL)\_OL\_H} = I_{L03}$ $I_{L(CAL)\_OL\_L} = I_{L00}$ $T_{A(CAL)}$ = 25 °C	P_9.7.16.39
SENSE Current Derating with Nominal Current Calibration	$\Delta k_{ILIS(NOM)}$	-9	0	+9	%	1)3) $I_{L(CAL)} = I_{L10}$ $I_{L(CAL)\_H} = I_{L12}$ $I_{L(CAL)\_L} = I_{L08}$ $T_{A(CAL)}$ = 25 °C	P_9.7.16.40

1) Parameter valid only if **PCS.PCCn** = 0_B.
2) k_{ILIS} accuracy valid if 1 µs RC filter is placed at ADC input.
3) Not subject to production test - specified by design.

10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CSN indicates the beginning of an access. Data is sampled-in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CSN. A modulo 8 counter ensures that data is taken only when a multiple of 8 bit has been transferred. The interface provides daisy chain capability with modulo 8 bit SPI devices.

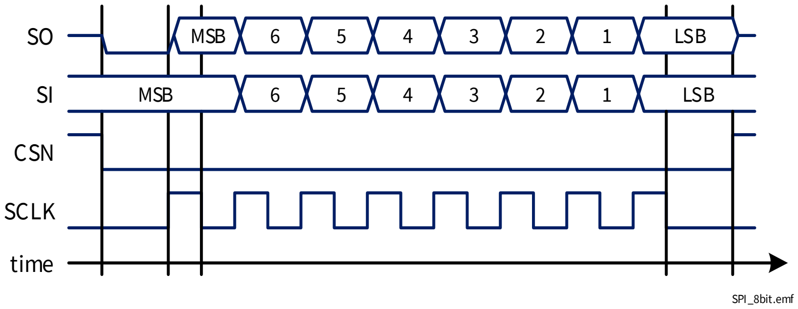


Figure 36 Serial Peripheral Interface

10.1 SPI Signal Description

CSN - Chip Select Negated

The system microcontroller selects the BTS71220-4ESE by means of the CSN pin. Whenever the pin is in “low” state, data transfer can take place. When CSN is in “high” state, any signals at the SCLK and SI pins are ignored and SO is forced into a “high impedance” state.

CSN “high” to “low” Transition

- The requested information is transferred into the shift register.
- SO changes from “high impedance” state to “low” state.

CSN “low” to “high” Transition

- Command decoding is only done, when after the falling edge of CSN exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of an incorrect SCLK count, the transmission error flag (`STDDIAG.TER`) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in “low” state whenever chip select CSN makes any transition, otherwise the command may not be accepted.

SI - Serial Input

Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Chapter 10.5** for further information.

SO Serial Output

Data is shifted out serially at this pin, the most significant bit first. SO is in “high impedance” state until the CSN pin goes to “low” state. New data will appear at the SO pin following the rising edge of SCLK.

Please refer to **Chapter 10.5** for further information.

10.2 Daisy Chain Capability

The SPI of BTS71220-4ESE provides daisy chain capability for modulo 8 bit SPI devices. In this configuration several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device (see **Figure 37**), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

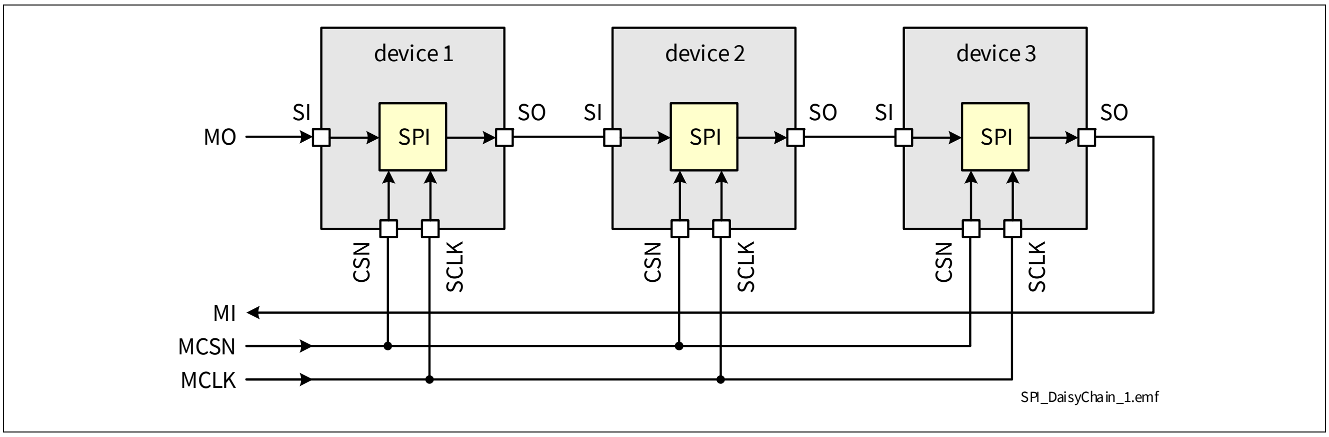

device 1
device 2
device 3
SI
SO
SPI
MO
CSN
SCLK
MI
MCSN
MCLK
SPI_DaisyChain_1.emf

Figure 37 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from SI line is shifted in each SCLK. The bit is shifted out on SO pin. After eight SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CSN line must turn “high” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted into device 2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the MCSN line must turn “high” (see **Figure 38**).

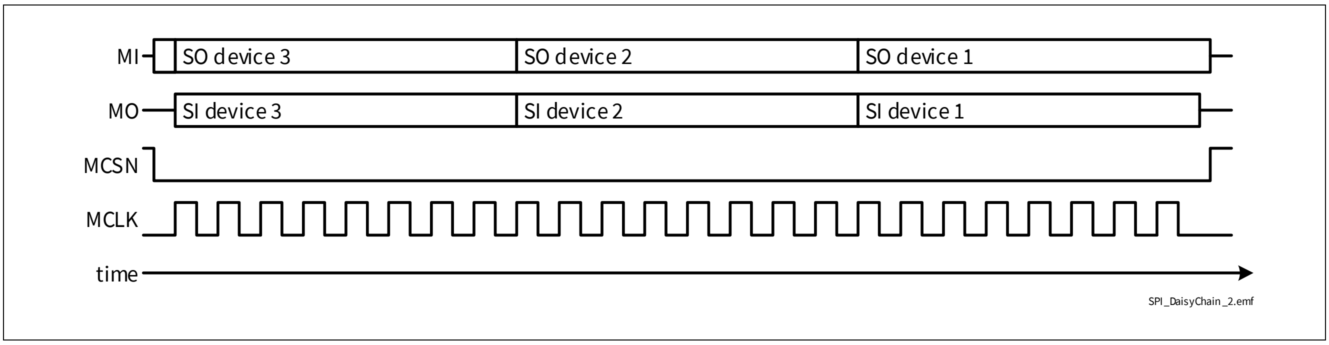

MI
SO device 3
SO device 2
SO device 1
MO
SI device 3
SI device 2
SI device 1
MCSN
MCLK
time
SPI_DaisyChain_2.emf

Figure 38 Data Transfer in Daisy Chain Configuration

10.3 Timing Diagrams

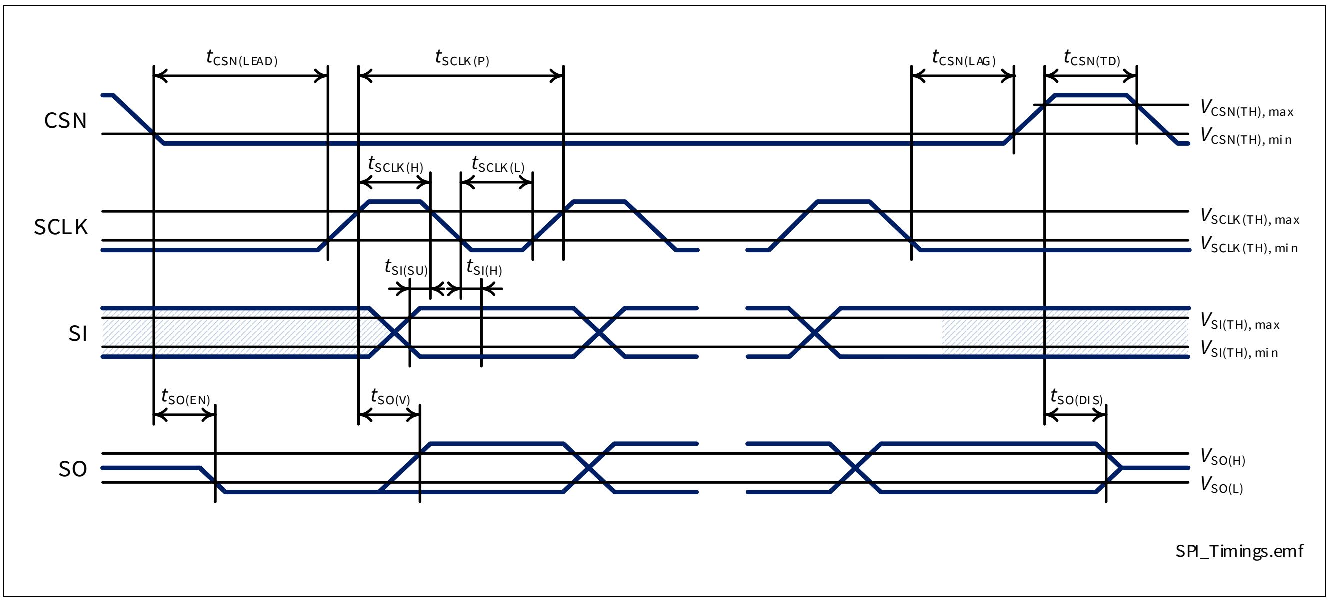

CSN
SCLK
SI
SO
$t_{CSN(LEAD)}$
$t_{SCLK(P)}$
$t_{CSN(LAG)}$
$t_{CSN(TD)}$
$t_{SCLK(H)}$
$t_{SCLK(L)}$
$t_{SI(SU)}$
$t_{SI(H)}$
$t_{SO(EN)}$
$t_{SO(V)}$
$t_{SO(DIS)}$
$V_{CSN(TH), max}$
$V_{CSN(TH), min}$
$V_{SCLK(TH), max}$
$V_{SCLK(TH), min}$
$V_{SI(TH), max}$
$V_{SI(TH), min}$
$V_{SO(H)}$
$V_{SO(L)}$
SPI_Timings.emf

Figure 39 Timing Diagram SPI Access

10.4 Electrical Characteristics

V_{DD} = 3.0 V to 5.5 V, V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_{DD} = 4.3 V, V_S = 13.5 V, T_J = 25 °C

Table 31 Electrical Characteristics Serial Peripheral Interface (SPI)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Timings							
Enable Lead Time (falling CSN to rising SCLK)	$t_{CSN(LEAD)}$	200	–	–	ns	[1]	P_10.4.0.1
Enable Lag Time (falling SCLK to rising CSN)	$t_{CSN(LAG)}$	200	–	–	ns	[1]	P_10.4.0.2
Transfer Delay Time (rising CSN to falling CSN)	$t_{CSN(TD)}$	500	–	–	ns	[1]	P_10.4.0.3
Output Enable Time (falling CSN to SO valid)	$t_{SO(EN)}$	–	30	100	ns	[1] $C_{L(SO)}$ = 50 pF	P_10.4.0.4
Output Disable Time (rising CSN to SO tristate)	$t_{SO(DIS)}$	–	30	100	ns	[1] $C_{L(SO)}$ = 50 pF	P_10.4.0.5
Serial Clock Frequency	f_{SCLK}	0	–	5	MHz	[1]	P_10.4.0.6
Serial Clock Period	$t_{SCLK(P)}$	200	–	–	ns	[1]	P_10.4.0.7
Serial Clock “High” Time	$t_{SCLK(H)}$	90	–	–	ns	[1]	P_10.4.0.8
Serial Clock “Low” Time	$t_{SCLK(L)}$	90	–	–	ns	[1]	P_10.4.0.9
Data Setup Time (required Time SI to falling SCLK)	$t_{SI(SU)}$	20	–	–	ns	[1]	P_10.4.0.10
Data Hold Time (falling SCLK to SI)	$t_{SI(H)}$	20	–	–	ns	[1]	P_10.4.0.11
Output Data Valid Time with Capacitive Load	$t_{SO(V)}$	–	–	60	ns	[1] $C_{L(SO)}$ = 50 pF	P_10.4.0.12

1) Not subject to production test - specified by design.

10.5 SPI Protocol

The relationship between SI and SO content during SPI communication is shown in **Figure 40**. SI line represents the frame sent from the µC and SO line is the answer provided by BTS71220-4ESE. The "previous response" means that the frame sent back depends on the command frame sent from the µC before.

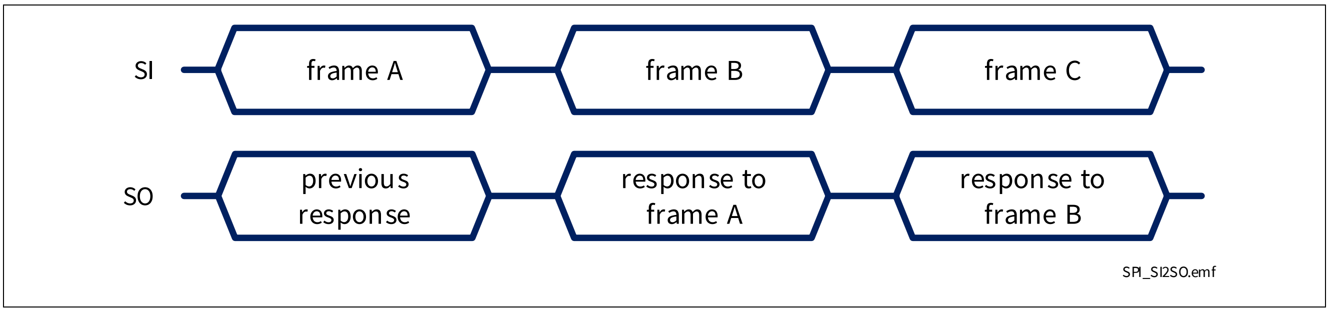

SI
frame A
frame B
frame C
SO
previous response
response to frame A
response to frame B
SPI_SI2SO.emf

Figure 40 Relationship between SI and SO during SPI communication

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the µC. The responses of write commands are deterministic and can be decoded as STDDIAG or WRNDIAG frame. For responses of read commands previous transmission has to be considered for decoding.

More in detail, the sequence of commands to "read" and "write" the content of a register will look as follows:

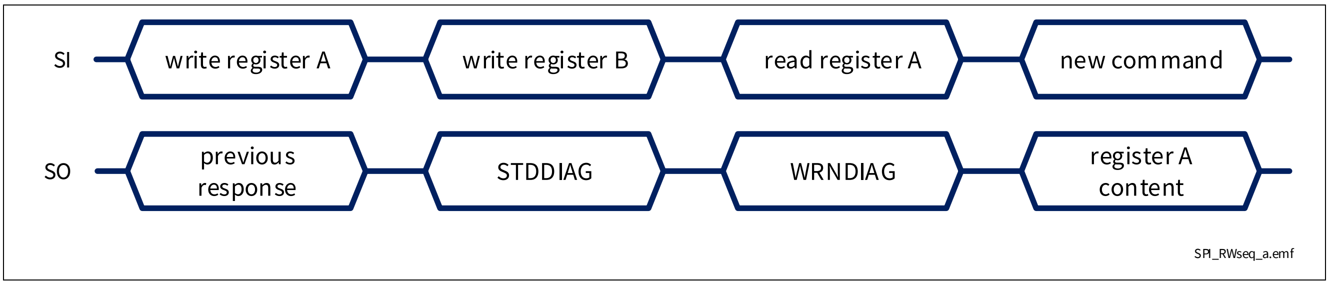

SI
write register A
write register B
read register A
new command
SO
previous response
STDDIAG
WRNDIAG
register A content
SPI_RWseq_a.emf

Figure 41 Register content sent back to µC (a)

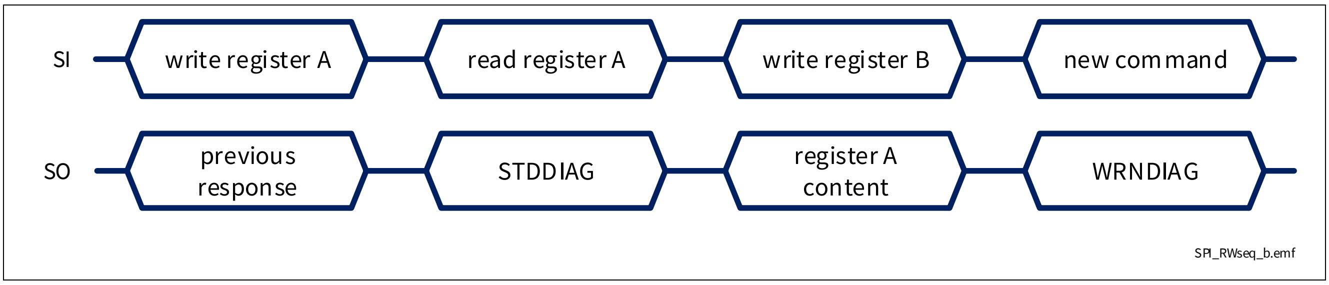

SI
write register A
read register A
write register B
new command
SO
previous response
STDDIAG
register A content
WRNDIAG
SPI_RWseq_b.emf

Figure 42 Register content sent back to µC (b)

There are 3 special situations where the frame sent back to the µC doesn't depend on the previous received frame:

- In case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8), shown in **Figure 43**
- When BTS71220-4ESE digital supply comes out of Power-On reset condition, as shown in **Figure 44**
- When $V_S < V_{S(TP)}$ and `DCR.MUX` $\neq 111_B$, as shown in **Figure 45**

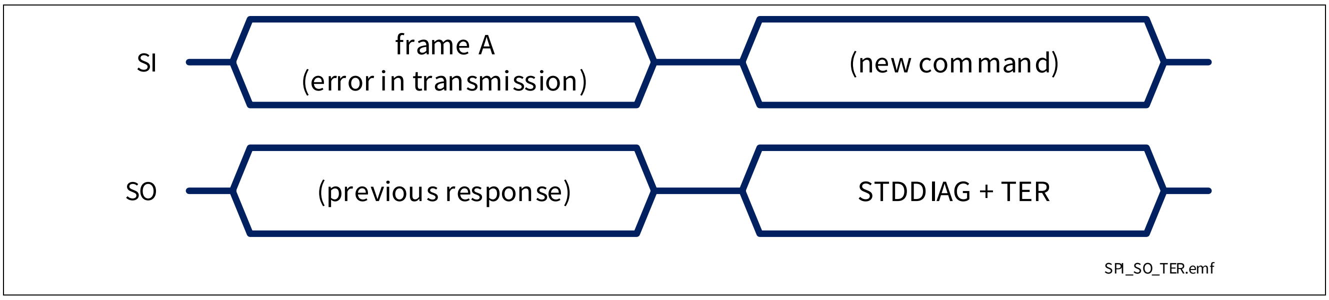

SI
frame A
(error in transmission)
(new command)
SO
(previous response)
STDDIAG + TER
SPI_SO_TER.emf

Figure 43 SPI response after an error in transmission

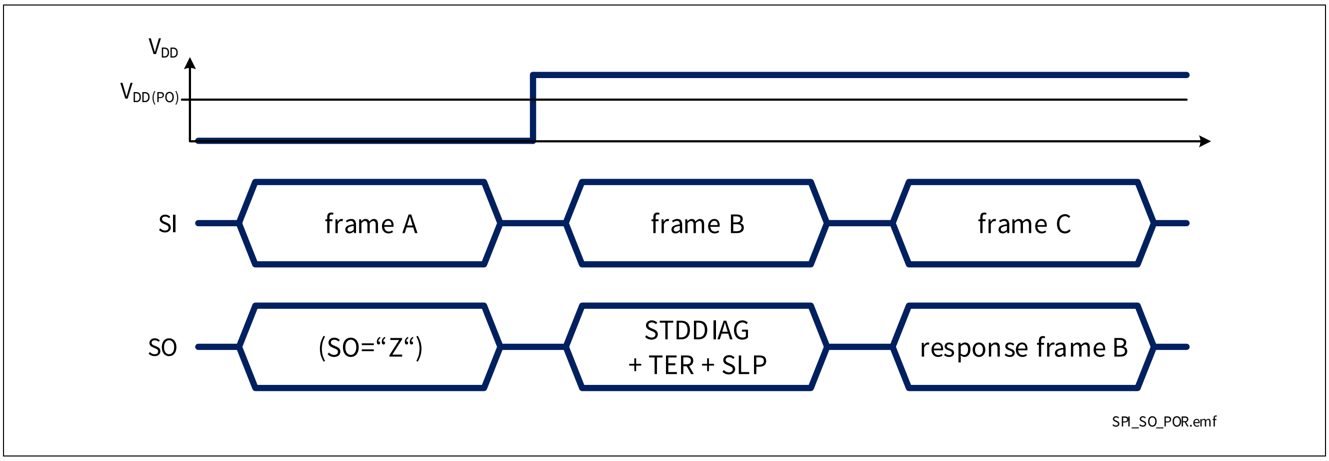

V_DD
V_DD(PO)
SI
frame A
frame B
frame C
SO
(SO="Z")
STDDIAG
+ TER + SLP
response frame B
SPI_SO_POR.emf

Figure 44 SPI response after coming out of Power-On reset at V_{DD}

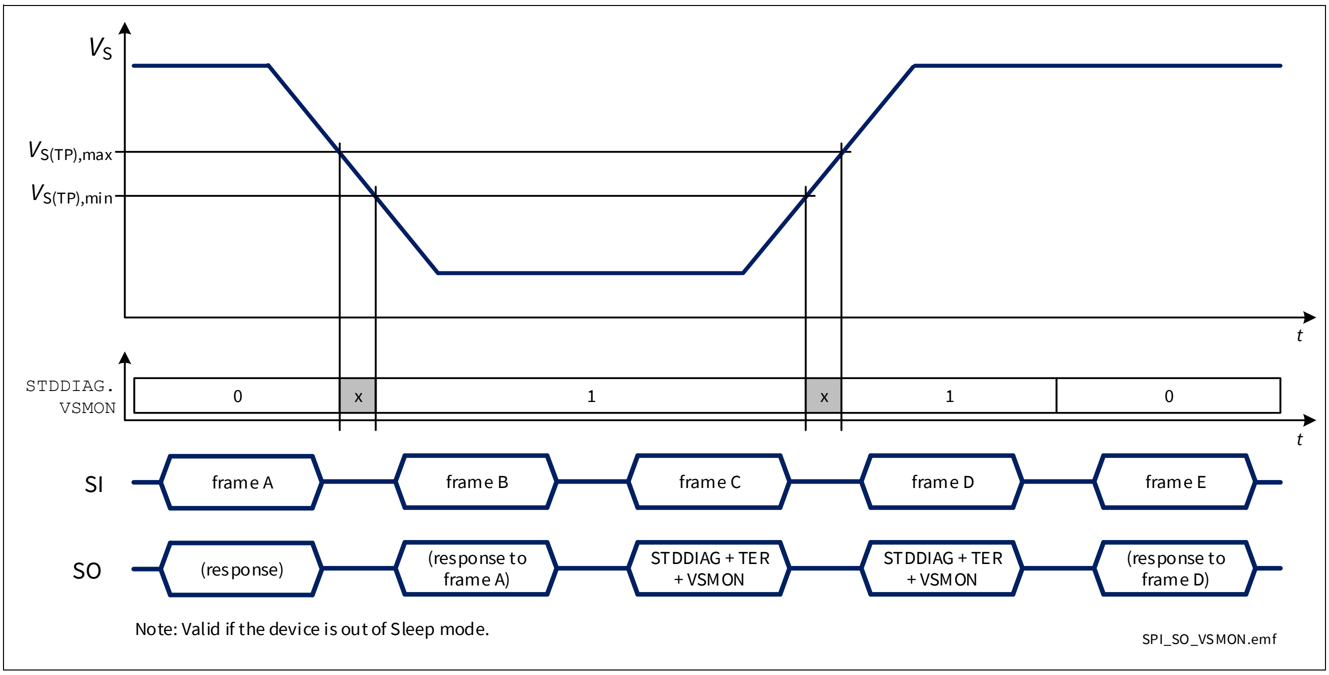

V_S
V_S(TP),max
V_S(TP),min
t
STDDIAG.
VSMON
0
x
1
x
1
0
t
SI
frame A
frame B
frame C
frame D
frame E
SO
(response)
(response to
frame A)
STDDIAG + TER
+ VSMON
STDDIAG + TER
+ VSMON
(response to
frame D)
Note: Valid if the device is out of Sleep mode.
SPI_SO_VSMON.emf

Figure 45 SPI response in case of voltage drop on battery

A summary of all possible SPI commands is presented in **Table 32**, including the answer that BTS71220-4ESE will send back at the next transmission.

Table 32 SPI Command Summary

Requested Operation	Frame sent to SPOC™ (SI pin)	Frame received from SPOC™ (SO pin) with the next command
Write **OUT** register **DCR.SWR** = x_B	`100ddddd`$_B$ where: “`ddddd`$_B$” = new **OUT** register content	`00dddddd`$_B$ - `STDDIAG` or `01dddddd`$_B$ - `WRNDIAG` (Standard Diagnosis or Warning Diagnosis will be sent alternating)
Read **OUT** register	`0xxxaaaa`$_B$ where: “aaaa$_B$” = `ADDR1` [1] (“`x`$_B$” = don't care)	`100ddddd`$_B$ (“`ddddd`$_B$” = **OUT** register content)
Read **RCS** register	`0xxxaaaa`$_B$ where: “aaaa$_B$” = `ADDR1` [1] (“`x`$_B$” = don't care)	`10000ddd`$_B$ (“`ddd`$_B$” = **RCS** register content)

Write Configuration registers	`11aadddd`$_B$
	where:
	“`aa`$_B$” = `ADDR0` [1]
	“`dddd`$_B$” = new register content
		`00dddddd`$_B$ - `STDDIAG`
		`01dddddd`$_B$ - `WRNDIAG`
		(Standard Diagnosis or Warning Diagnosis will be sent alternating)

Read Configuration registers	`0xxxaaaa`$_B$ where: “aaaa$_B$” = `ADDR1` [1] (“`x`$_B$” = don't care)	`11aadddd`$_B$ where: “`aa`$_B$” = `ADDR0` [1] “`dddd`$_B$” = register content
Read Warning Diagnosis	`0xxxx001`$_B$ (“`x`$_B$” = don't care)	`0100dddd`$_B$ - `WRNDIAG` (Warning Diagnosis)
Read Standard Diagnosis	`0xxxx010`$_B$ (“`x`$_B$” = don't care)	`00dddddd`$_B$ - `STDDIAG` (Standard Diagnosis)
Read Error Diagnosis	`0xxxx011`$_B$ (“`x`$_B$” = don't care)	`0100dddd`$_B$ - `ERRDIAG` (Error Diagnosis)

[1] **ADDR0** and **ADDR1** are defined according to **Table 33**.

10.6 SPI Diagnosis Registers

10.6.1 Diagnosis Registers - Read Commands

Name	7	6	5	4	3	2	1	0
`WRNDIAG`	0	x	x	x	0	0	0	1
`STDDIAG`	0	x	x	x	0	0	1	0
`ERRDIAG`	0	x	x	x	0	0	1	1

10.6.2 Diagnosis Registers - Responses

Name	7	6	5	4	3	2	1	0	Default
`WRNDIAG`	0	1	0	0	`WRNDIAG.WRNn`				40_H
`STDDIAG`	0	0	`STDDIAG.TER`	`STDDIAG.CSV`	`STDDIAG.LHI`	`STDDIAG.SLP`	`STDDIAG.SBM`	`STDDIAG.VSMON`	24_H
`ERRDIAG`	0	1	0	0	`ERRDIAG.ERRn`				40_H

Field	Bits	Type	Description
STDDIAG.TER	5	r	**Transmission Error** 0_B Previous transmission was successful (modulo 8 clocks received) 1_B (default) Previous transmission failed or first transmission after Power-On reset or $V_S < V_{S(TP)}$ if `STDDIAG.VSMON` = 1_B
STDDIAG.CSV	4	r	**Checksum Verification**[1] 0_B (default) Checksum verification was pass or no checksum calculated 1_B Previous checksum verification was fail
STDDIAG.LHI	3	r	**Limp Home monitor** 0_B (default) “Low” level at pin LHI 1_B “High” level at pin LHI
STDDIAG.SLP	2	r	**Sleep mode monitor** 0_B Device out of Sleep mode 1_B (default) Device is in Sleep mode
STDDIAG.SBM	1	r	**Switch Bypass Monitor**[2] 0_B $V_{DS} < V_{DS(SB)}$ 1_B $V_{DS} > V_{DS(SB)}$
STDDIAG.VSMON	0	r	**V_S monitor** 0_B (default) V_S always > $V_{S(UV)}$ since last Standard Diagnosis readout 1_B $V_S < V_{S(UV)}$ at least once or $V_S < V_{S(TP)}$ if `STDDIAG.TER` = 1_B

Field	Bits	Type	Description
`WRNDIAG.WRNn` n = 3 to 0	3:0	r	**Warning Diagnosis of Channel n** 0_B (default) No failure 1_B Overcurrent, Overtemperature or delta T detected
`ERRDIAG.ERRn` n = 3 to 0	3:0	r	**Error Diagnosis of Channel n** 0_B (default) No failure 1_B Channel latched OFF

1) See **Chapter 10.8** for details on checksum calculation.

2) The switch bypass monitor compares the threshold $V_{DS(SB)}$ with the voltage V_{DS} across the power transistor of that channel which is selected by the current sense multiplexer (**`DCR.MUX`**).

10.7 SPI Configuration Registers

The following table provides an overview on the registers available and the available address space.

Table 33 Register Overview

Name	SWR 1)	RB	ADDR0	ADDR1	Content
`OUT`	x/0 2)	0	(na)	0000	Output configuration
`RCS`	1	0	(na)	1000	Restart counter status (read-only)
`SRC`	1	0	(na)	1001	Slew Rate Control register (read-only)
`OCR`	0	1	00	0100	Overcurrent threshold configuration
`RCD`	1	1	00	1100	Restart counter disable
`KRC`	0	1	01	0101	KILIS range control
`PCS`	1	1	01	1101	Parallel channel and Slew Rate control
`HWCR`	0	1	10	0110	Hardware configuration
`ICS`	1	1	10	1110	Input status & checksum input
`DCR`	x	1	11	x111	Diagnostic configuration and Swap bit

1) **`DCR.SWR`** bit is only changed for write commands. For read commands it is used as part of the read address.

2) For writing to **`OUT`** register **`DCR.SWR`** = x, for read address **`DCR.SWR`** = 0_B.

Table 34 Configuration Registers - Write Commands RB-0

Bit		**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**SWR**	**7**	**RB**	**5**	**4**	**3**	**2**	**1**	**0**
`OUT`	x	1	0	0	**`OUT.OUTn`** 1)				

1) `OUT.OUT4` controls the logic state of EDO pin.

Table 35 Configuration Registers - Write Commands RB-1

Bit		**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**SWR**	**7**	**RB**	**ADDR0**		**3**	**2**	**1**	**0**
`OCR`	0	1	1	0	0	**`OCR.OCTn`**			
`RCD`	1	1	1	0	0	**`RCD.RCDn`**			
`KRC`	0	1	1	0	1	**`KRC.KRCn`**			

Table 35 Configuration Registers - Write Commands RB-1

Bit		7	6	5	4	3	2	1	0
Name	**SWR**	**7**	**RB**	**ADDR0**		**3**	**2**	**1**	**0**
PCS	1	1	1	0	1	PCS.PCCn		PCS.CLCS	PCS.SRCS
HWCR	0	1	1	1	0	0	HWCR.COL	HWCR.RST	HWCR.CLC
ICS	1	1	1	1	0	ICS.CSRn [1]			
DCR	x	1	1	1	1	DCR.SWR	DCR.MUX		

[1] See **Chapter 10.8** for details on checksum calculation.

Table 36 Configuration Registers - Read Commands

Bit	7	6	5	4	3	2	1	0
Name	**7**	**6**	**5**	**4**	**ADDR1**			
OUT	0	x	x	x	0	0	0	0
RCS	0	x	x	x	1	0	0	0
SRC	0	x	x	x	1	0	0	1
OCR	0	x	x	x	0	1	0	0
RCD	0	x	x	x	1	1	0	0
KRC	0	x	x	x	0	1	0	1
PCS	0	x	x	x	1	1	0	1
HWCR	0	x	x	x	0	1	1	0
ICS	0	x	x	x	1	1	1	0
DCR	0	x	x	x	x	1	1	1

Table 37 Configuration Registers - Responses

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
Name	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Default**
`OUT`	1	0	0	`OUT.OUTn` 1)					80_H
`RCS`	1	0	0	0	0	`RCS.RCSn`			80_H
`SRC`	1	0	0	1	`SRC.SRCn`				90_H
`OCR`	1	1	0	0	`OCR.OCTn`				$C0_H$
`RCD`	1	1	0	0	`RCD.RCDn`				$C0_H$
`KRC`	1	1	0	1	`KRC.KRCn`				$D0_H$
`PCS`	1	1	0	1	`PCS.PCCn`		0	0	$D0_H$
`HWCR`	1	1	1	0	0	`HWCR.COL`	`HWCR.SLP`	0	$E2_H$
`ICS`	1	1	1	0	0	0	`ICS.INSTn`		$E0_H$
`DCR`	1	1	1	1	`DCR.SWR`	`DCR.MUX`			$F7_H$

1) `OUT.OUT4` controls the logic state of EDO pin.

Field	**Bits**	**Type**	**Description**
`RB`	6	rw	**Register Bank** 0_B (default) Read/write to `OUT`/`RCS` register 1_B Read/write to other registers
`OUT.OUTn` n = 4 to 0	4:0	rw	**Output Control Register of Channel n** 0_B (default) channel is OFF 1_B Channel is ON
`RCS.RCSn` n = 2 to 0	2:0	r	**Restart Counter Status of Channel selected via MUX** 000_B (default) Restart counter value = 0 001_B Restart counter value = 1 010_B Restart counter value = 2 011_B Restart counter value = 3 100_B Restart counter value = 4 101_B Restart counter value = 5 110_B Restart counter value = 6 111_B Restart counter value = 7
`SRC.SRCn` n = 3 to 0	3:0	r	**Set Slew Rate control for Channel n (read only)** 0_B (default) Normal Slew Rate 1_B Adjusted Slew Rate
`OCR.OCTn` n = 3 to 0	3:0	rw	**Set Overcurrent Level for Channel n** 0_B (default) High level of overcurrent threshold $I_{L(OVL0)}$ 1_B Low level of overcurrent threshold $I_{L(OVL2)}$
`RCD.RCDn` n = 3 to 0	3:0	rw	**Set Restart Strategy for Channel n** 0_B (default) Automatic restart mode 1_B Latch mode
`KRC.KRCn` n = 3 to 0	3:0	rw	**Set Current Sense Ratio Range for Channel n** 0_B (default) High range of current sense ratio 1_B Low range of current sense ratio

Field	Bits	Type	Description
`PCS.SRCS`	0	w	**Set Slew Rate control for Channel selected by DCR.MUX** 0_B (default) Normal Slew Rate 1_B Adjusted Slew Rate
`PCS.CLCS`	1	w	**Clear Restart Counters and Latches for Channel selected by DCR.MUX** 0_B (default) Restart counters and latches are untouched 1_B Restart counters and latches are reset
`PCS.PCCn` n = 1 to 0	3:2	rw	**Parallel Channel Configuration** 00_B (default) Channels are operating independent 01_B OUT0 + OUT3 are in parallel configuration 10_B OUT1 + OUT2 are in parallel configuration 11_B OUT0 + OUT3 and OUT1 + OUT2 are in parallel configuration
`HWCR.CLC`	0	w	**Clear Restart Counters and Latches** 0_B (default) Restart counters and latches are untouched 1_B Restart counters and latches are reset for all channels
`HWCR.RST`	1	w	**Reset Command** 0_B (default) Normal operation 1_B Execute reset command
`HWCR.SLP`	1	r	**Sleep Mode** 0_B Device is awake 1_B (default) DCR.MUX = 111_B
`HWCR.COL`	2	rw	**Input Combinatorial Logic Configuration** 0_B (default) Input signal OR-combined with according OUT register bit[1)] 1_B Input signal AND-combined with according OUT register bit
`ICS.CSRn` n = 3 to 0	3:0	w	**Checksum Input Register** 4 bit Checksum is written to this register
`ICS.INSTn` n = 1 to 0	1:0	r	**Input Status Monitor Channel n** 0_B (default) Input signal is “low” 1_B Input signal is “high”

Field	**Bits**	**Type**	**Description**
`DCR.MUX`	2:0	rw	**Set Current Sense Multiplexer Configuration in OFF state** 000_B IS pin is "high impedance" 001_B IS pin is "high impedance" 010_B IS pin is "high impedance" 011_B IS pin is "high impedance" 100_B Diagnosis enable of external driver activated (EDD set to "high") 101_B Current sense verification mode 110_B IS pin is "high impedance" 111_B Sleep mode (IS pin is "high impedance") **Set Multiplexer Configuration in ON state** 000_B Current sense of channel 0 is routed to IS pin 001_B Current sense of channel 1 is routed to IS pin 010_B Current sense of channel 2 is routed to IS pin 011_B Current sense of channel 3 is routed to IS pin 100_B Diagnosis enable of external driver activated (EDD set to "high") 101_B Current sense verification mode 110_B IS pin is "high impedance" 111_B Sleep mode (IS pin is "high impedance")
`DCR.SWR`	3	rw	**Switch Register** 0_B (default) Registers **`OUT`**, **`OCR`**, **`KRC`**, **`HWCR`** and **`DCR`** can be written 1_B Registers **`OUT`**, **`RCD`**, **`PCS`**, **`ICS`** and **`DCR`** can be written

1) In Limp Home mode (LHI pin set to "high") the combinatorial logic is switched to OR-mode.

10.8 SPI Checksum Verification

BTS71220-4ESE offers a simple parity check to identify unexpected content or unintended changes of configuration registers. For the checksum calculation a subset of the configuration bits is used, which is expected not to be changed periodically. The checksum calculation is an easy column parity calculation. The configuration bits which are used for the calculation are shown in **Table 39**. The SPI master writes the result to **ICS.CSRn**. After the 4bit checksum is written to **ICS** register, the device is doing once the comparison and the result can be read within the next **STDDIAG** frame in the bit **STDDIAG.CSV**. The **STDDIAG.CSV** bit is cleared with the next **STDDIAG** readout. In case the **ICS** register is not written, the checksum comparison is disabled and the bit **STDDIAG.CSV** = 0_B. If Limp Home mode is entered after **ICS.CSRn** is written but before **STDDIAG.CSV** is read, the checksum verification is not valid. Same applies in case **STDDIAG.TER** and **STDDIAG.VSMON** are set to 1_B. In these cases checksum verification result shall be discarded.

Table 38 Conventions for parity calculation

Number of ‘1’ in a column	Result with EVEN-parity	Result with ODD-parity
EVEN	0	1
ODD	1	0

Table 39 Checksum calculation bit matrix

Name	3	2	1	0
OCR	OCT3	OCT2	OCT1	OCT0
RCD	RCD3	RCD2	RCD1	RCD0
KRC	KRC3	KRC2	KRC1	KRC0
SRC	SRC3	SRC2	SRC1	SRC0
HWCR/**PCS**	0	COL	PCC	PCC0
Parity	even	odd	even	odd
ICS	CSR3	CSR2	CSR1	CSR0

Table 40 Checksum calculation bit matrix example

Name	3	2	1	0
OCR	0	1	0	0
RCD	1	0	0	0
KRC	0	1	1	0
SRC	0	0	1	0
HWCR/**PCS**	0	0	0	0
Parity	even	odd	even	odd
ICS	1	1	0	1

10.9 SPI command quick list

A summary of the most used SPI commands (read and write operations) is shown in Table 154.

Table 41 SPI command quick list

Name	"read" command [1]	"write" command [2]	SWR [3]
OUT	$0xxx0000_B$	$10dddddd_B$	x
RCS	$0xxx1000_B$		
SRC	$0xxx1001_B$		
OCR	$0xxx0100_B$	$1100dddd_B$	0
RCD	$0xxx1100_B$	$1100dddd_B$	1
KRC	$0xxx0101_B$	$1101dddd_B$	0
PCS	$0xxx1101_B$	$1101dddd_B$	1
HWCR	$0xxx0110_B$	$1110dddd_B$	0
ICS	$0xxx1110_B$	$1110dddd_B$	1
DCR	$0xxxx111_B$	$1111dddd_B$	x
WRNDIAG	$0xxx0001_B$		
STDDIAG	$0xxx0010_B$		
ERRDIAG	$0xxx0011_B$		

1) x = don't care bits.

2) d = data bits.

3) DCR.SWR bit needs to be set for writing a register. For reading a register the DCR.SWR bit is part of the read address.

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

11.1 Application setup - SPOC™

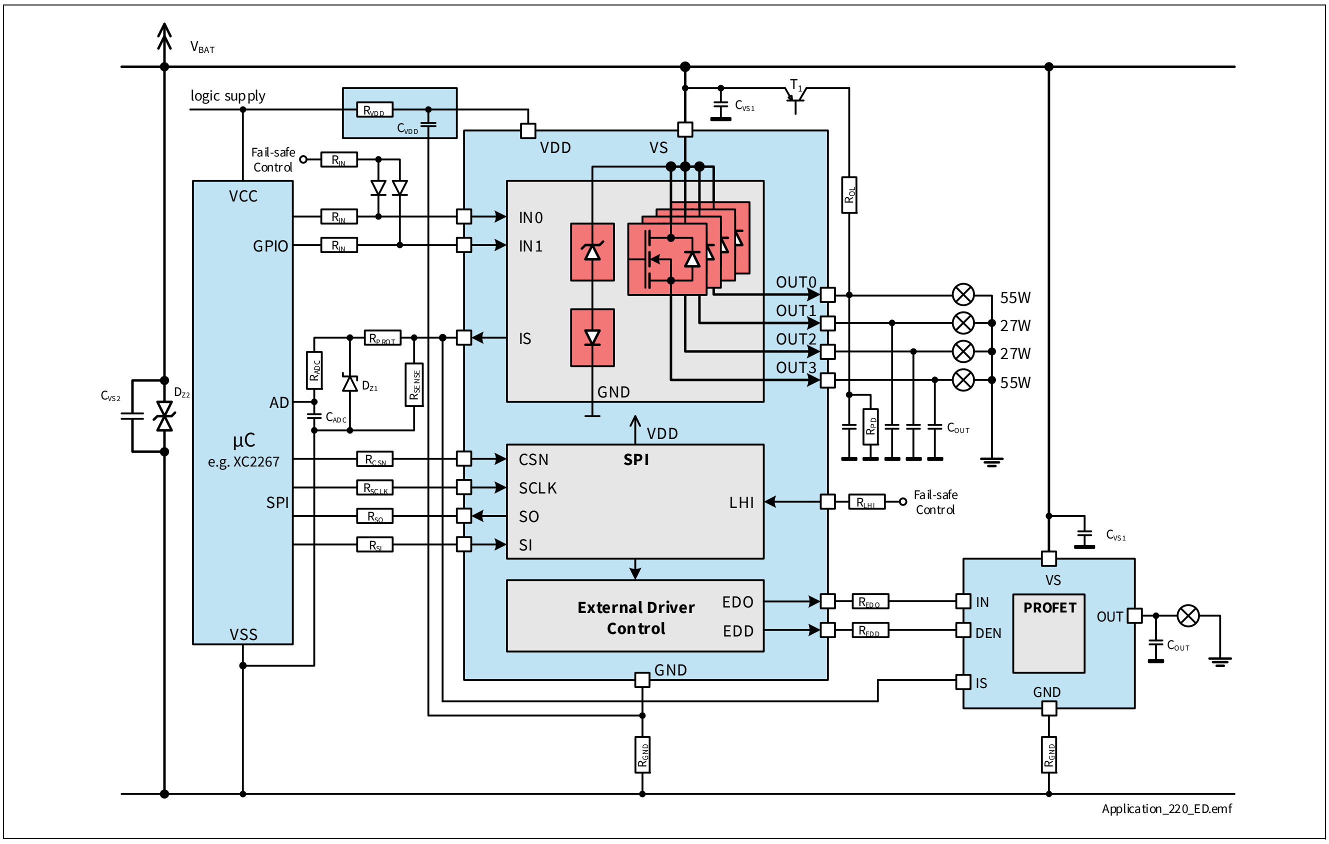

V_BAT
logic supply
R_VDD
C_VDD
Fail-safe Control
R_IN
VCC
GPIO
R_IN
R_IN
R_PROT
R_ADC
D_Z1
R_SENSE
C_ADC
AD
µC
e.g. XC2267
SPI
VSS
C_VS2
D_Z2
R_CSN
R_SCLK
R_SO
R_SI
VDD
VS
C_VS1
T_1
R_OL
IN0
IN1
IS
GND
OUT0
OUT1
OUT2
OUT3
55W
27W
27W
55W
R_PD
C_OUT
VDD
CSN
SPI
SCLK
SO
SI
LHI
R_LHI
Fail-safe Control
External Driver Control
EDO
EDD
R_EDO
R_EDD
GND
C_VS1
VS
IN
DEN
IS
PROFET
OUT
C_OUT
GND
R_GND
R_GND
Application_220_ED.emf

Figure 46 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

11.2 External Components

Table 42 Suggested Component values

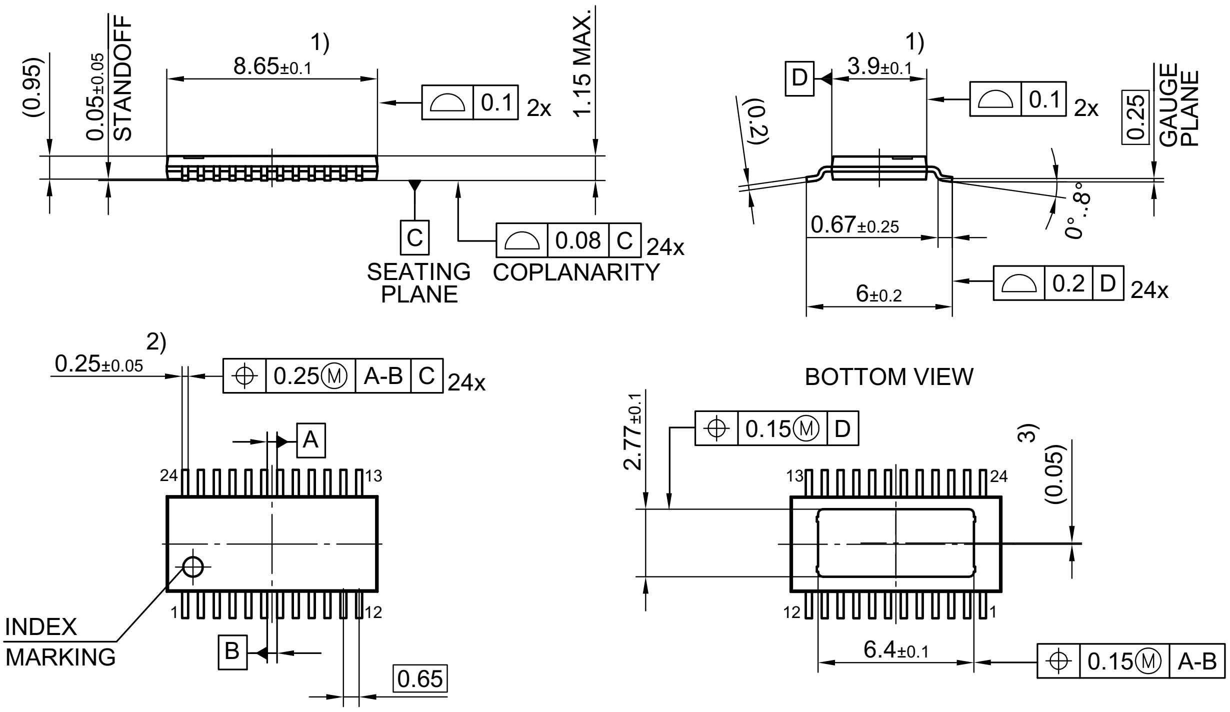
Reference	Value	Purpose
R_{VDD}	470 Ω	Device logic protection
R_{IN}	4.7 kΩ	Protection of the microcontroller during overvoltage, reverse polarity Guarantee BTS71220-4ESE output OFF during Loss of Ground
R_{PROT}	4.7 kΩ	Protection resistor for overvoltage, reverse polarity and Loss of Ground Value to be tuned with µC specification
R_{SENSE}	1.2 kΩ	Sense resistor
R_{ADC}	1.0 kΩ	µC-ADC voltage spikes filtering
R_{CSN}	1.2 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SCLK}	1.2 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SO}	1.2 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SI}	1.2 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{LHI}	4.7 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{EDO}	4.7 kΩ	Protection of the device during overvoltage, reverse polarity of external driver
R_{EDD}	4.7 kΩ	Protection of the device during overvoltage, reverse polarity of external driver
C_{ADC}	1.0 nF	µC-ADC voltage spikes filtering
C_{VDD}	470 nF	Digital supply voltage spikes filtering and for improved robustness against battery voltage transients
C_{VS1}	100 nF	Battery voltage spikes filtering
C_{VS2}	100 nF	Battery voltage spikes filtering
C_{OUT}	10 nF	For improved electromagnetic compatibility (EMC)
R_{GND}	47 Ω (1/16 W)	Ground voltage spikes filtering for improved robustness against battery voltage transients
T_1	BC 807	Switch the battery voltage for Open Load in OFF diagnosis
R_{PD}	47 kΩ	Output polarization (pull-down) Ensure polarization of BTS71220-4ESE output to distinguish between Open Load and Short to V_S in OFF diagnosis
R_{OL}	1.5 kΩ	Output polarization (pull-up) Ensure polarization of BTS71220-4ESE output during Open Load in OFF diagnosis

Note: The suggested component values above are determined for typical applications. Based on the application circuit and the used components connected to BTS71220-4ESE, it could be necessary to adjust the recommended values to stay below the maximum ratings for all components (e.g. reverse battery, transients on battery, etc.).

11.3 Further Application Information

- Please contact us for information regarding the Pin FMEA
- For further information you may contact **http://www.infineon.com/**

12 Package Outlines


(0.95)
0.05±0.05
STANDOFF
1)
8.65±0.1
0.1 2x
1.15 MAX.
C
SEATING PLANE
0.08 C 24x
COPLANARITY
1)
D
3.9±0.1
(0.2)
0.1 2x
0.25
GAUGE PLANE
0°...8°
0.67±0.25
6±0.2
0.2 D 24x
2)
0.25±0.05
0.25Ⓜ A-B C 24x
A
24
13
1
12
INDEX MARKING
B
0.65
BOTTOM VIEW
2.77±0.1
0.15Ⓜ D
3)
(0.05)
13
24
12
1
6.4±0.1
0.15Ⓜ A-B

1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE
2) DAMBAR PROTUSION SHALL BE MAXIMUM 0.1MM TOTAL IN EXCESS OF LEAD WIDTH
3) DISTANCE FROM CENERLINE EXPOSED PAD TO PACKAGE CENTERLINE
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [⊲⊕]

Figure 47 **PG-TSDSO-24-32** (Thin (Slim) Dual Small Outline 24 pins) **Package drawing**

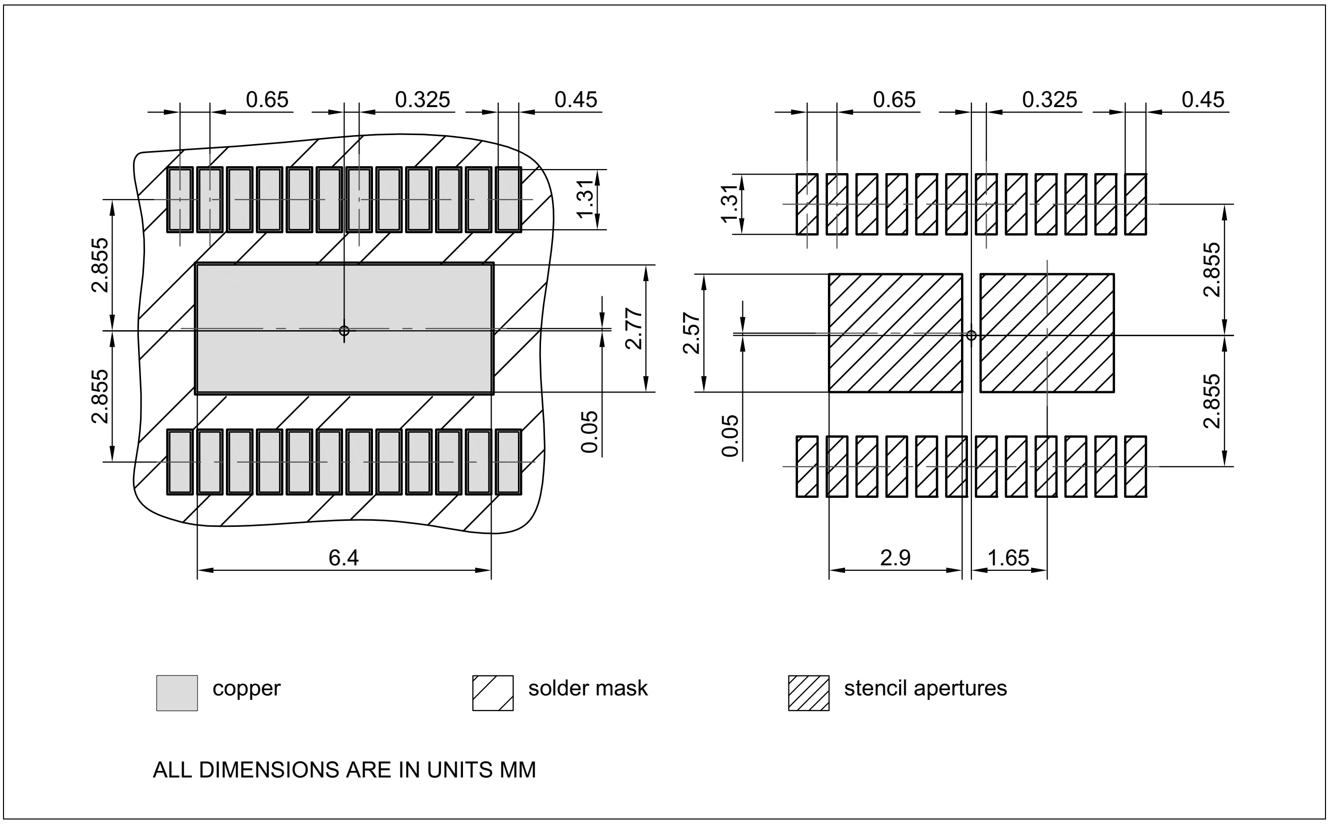

0.65
0.325
0.45
1.31
2.855
2.855
2.77
0.05
6.4
0.65
0.325
0.45
1.31
2.57
0.05
2.855
2.855
2.9
1.65
copper
solder mask
stencil apertures
ALL DIMENSIONS ARE IN UNITS MM

Figure 48 **PG-TSDSO-24-32** (Thin (Slim) Dual Small Outline 24 pins) **Package pads and stencil**

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

13 Revision History

Table 43 BTS71220-4ESE - List of changes

Revision	Changes
1.00, 2018-06-11	Data Sheet available

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Edition 2018-06-11
Published by
Infineon Technologies AG
81726 Munich, Germany

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