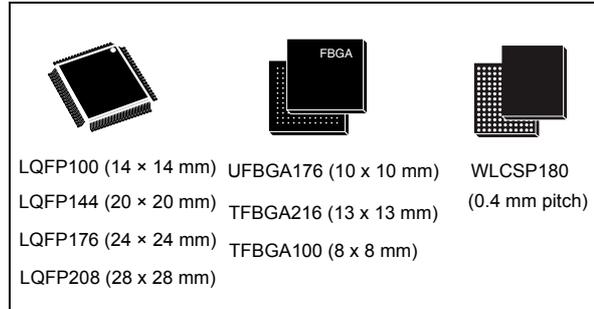


Arm® Cortex®-M7 32b MCU+FPU, 462DMIPS, up to 2MB Flash/
512+16+4KB RAM, USB OTG HS/FS, 28 com IF, LCD, DSI

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M7 CPU with DPFPU, ART Accelerator™ and L1-cache: 16 Kbytes I/D cache, allowing 0-wait state execution from embedded Flash and external memories, up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions.
- Memories
 - Up to 2 Mbytes of Flash memory organized into two banks allowing read-while-write
 - SRAM: 512 Kbytes (including 128 Kbytes of data TCM RAM for critical real-time data) + 16 Kbytes of instruction TCM RAM (for critical real-time routines) + 4 Kbytes of backup SRAM
 - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPDDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- Graphics
 - Chrom-ART Accelerator™ (DMA2D), graphical hardware accelerator enabling enhanced graphical user interface
 - Hardware JPEG codec
 - LCD-TFT controller supporting up to XGA resolution
 - MIPI® DSI host controller supporting up to 720p 30 Hz resolution
- Clock, reset and supply management
 - 1.7 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - Dedicated USB power
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration



- Low-power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 32×32 bit backup registers + 4 Kbytes backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels
- Digital filters for sigma delta modulator (DFSDM), 8 channels / 4 filters
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer
- Debug mode
 - SWD & JTAG interfaces
 - Cortex®-M7 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
 - Up to 164 fast I/Os up to 108 MHz
 - Up to 166 5 V-tolerant I/Os

- Up to 28 communication interfaces
 - Up to 4 I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs/4 UARTs (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
 - Up to 6 SPIs (up to 54 Mbit/s), 3 with muxed simplex I²S for audio
 - 2 x SAIs (serial audio interface)
 - 3 x CANs (2.0B Active) and 2x SDMMCs
 - SPDIFRX interface
 - HDMI-CEC
 - MDIO slave interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit camera interface up to 54 Mbyte/s
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F765xx	STM32F765BI, STM32F765BG, STM32F765NI, STM32F765NG, STM32F765II, STM32F765IG, STM32F765ZI, STM32F765ZG, STM32F765VI, STM32F765VG
STM32F767xx	STM32F767BG, STM32F767BI, STM32F767IG, STM32F767II, STM32F767NG, STM32F767NI, STM32F767VG, STM32F767VI, STM32F767ZG, STM32F767ZI
STM32F768Ax	STM32F768AI
STM32F769xx	STM32F769AG, STM32F769AI, STM32F769BG, STM32F769BI, STM32F769IG, STM32F769II, STM32F769NG, STM32F769NI

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1 Description

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a floating point unit (FPU) which supports Arm® double-precision and single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices incorporate high-speed embedded memories with a Flash memory up to 2 Mbytes, 512 Kbytes of SRAM (including 128 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces:

- Up to four I2Cs
- Six SPIs, three I2Ss in half-duplex mode. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI)
- Three CANs
- Two SAI serial audio interfaces
- Two SDMMC host interfaces
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface, a camera interface for CMOS sensors.

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices operate in the -40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for USB (OTG_FS and OTG_HS) and SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices offer devices in 11 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smartwatches

The following table lists the peripherals available on each part number.



Table 2. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts

Peripherals		STM32F765Vx		STM32F767/769Vx		STM32F765Zx		STM32F767/769Zx		STM32F769Ax		STM32F768Ax		STM32F765Ix		STM32F767/769Ix		STM32F765Bx		STM32F767/769Bx		STM32F765Nx		STM32F767/769Nx		
Flash memory in Kbytes		1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System	512(368+16+128)																								
	Instruction	16																								
	Backup	4																								
FMC memory controller		Yes ⁽¹⁾																								
Quad-SPI		Yes																								
Ethernet		Yes								No				Yes												
Timers	General-purpose	10																								
	Advanced-control	2																								
	Basic	2																								
	Low-power	1																								
Random number generator		Yes																								
Communication interfaces	SPI / I ² S	4/3 (simplex) ⁽²⁾						6/3 (simplex) ⁽²⁾																		
	I ² C	4																								
	USART/UART	4/4																								
	USB OTG FS	Yes																								
	USB OTG HS	Yes																								
	CAN	3																								
	SAI	2																								
	SPDIFRX	4 inputs																								
	SDMMC1	Yes																								
	SDMMC2	Yes ⁽³⁾																								
Camera interface		Yes																								
MIPI-DSI Host ⁽⁴⁾		No								Yes				No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	
LCD-TFT		No	Yes	No	Yes								No	Yes	No	Yes	No	Yes	No	Yes	No	Yes				



Table 2. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts (continued)

Peripherals	STM32F765Vx	STM32F767/769Vx	STM32F765Zx	STM32F767/769Zx	STM32F769Ax	STM32F768Ax	STM32F765Ix	STM32F767/769Ix	STM32F765Bx	STM32F767/769Bx	STM32F765Nx	STM32F767/769Nx
Chrom-ART Accelerator™ (DMA2D)	Yes											
JPEG codec	No	Yes	No	Yes		No	Yes	No	Yes	No	Yes	
GPIOs	82		114		129		140	132	168	159	168	159
DFSDM1	Yes (4 filters)											
12-bit ADC	3											
Number of channels	16		24									
12-bit DAC	Yes											
Number of channels	2											
Maximum CPU frequency	216 MHz ⁽⁵⁾											
Operating voltage	1.7 to 3.6 V ⁽⁶⁾											
Operating temperatures	Ambient temperatures: -40 to +85 °C / -40 to +105 °C											
	Junction temperature: -40 to + 125 °C											
Package	LQFP100 TFBGA100		LQFP144		WLCSP180		UFBGA176 ⁽⁷⁾ LQFP176		LQFP208		TFBGA216	

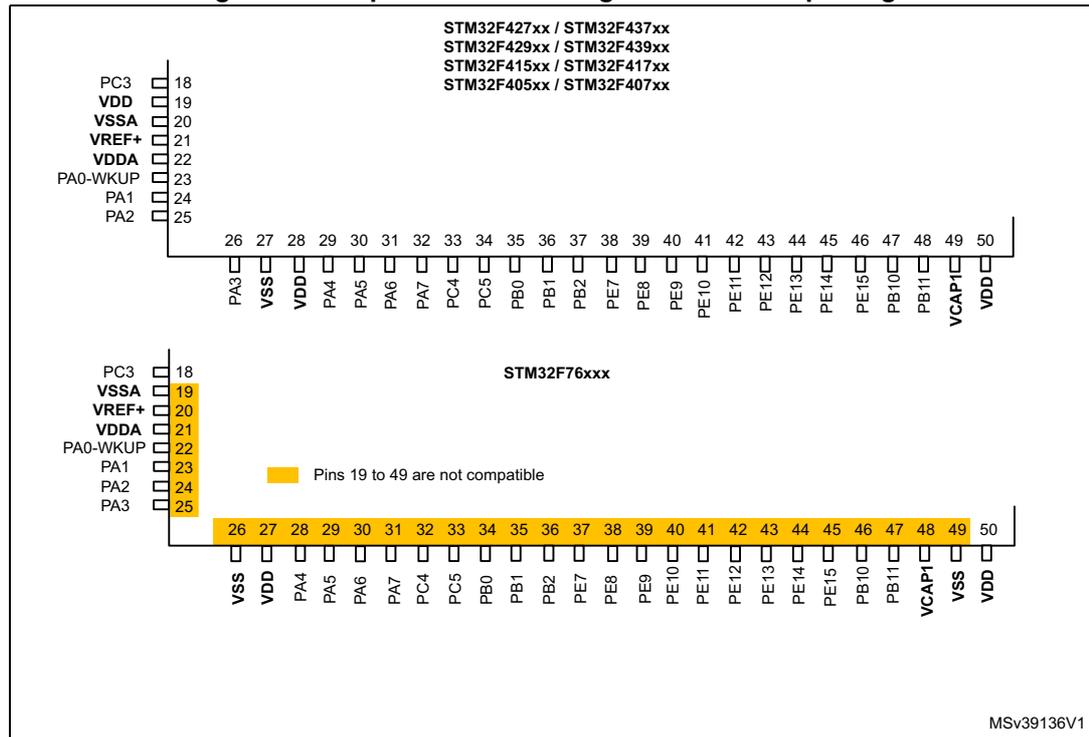
1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
4. DSI host interface is only available on STM32F769x sales types.
5. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
6. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 2.18.2: Internal reset OFF](#)).
7. UFBGA176 is not available for STM32F769x sales types.

Full compatibility throughout the family

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices are fully pin-to-pin, compatible with the STM32F4xxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

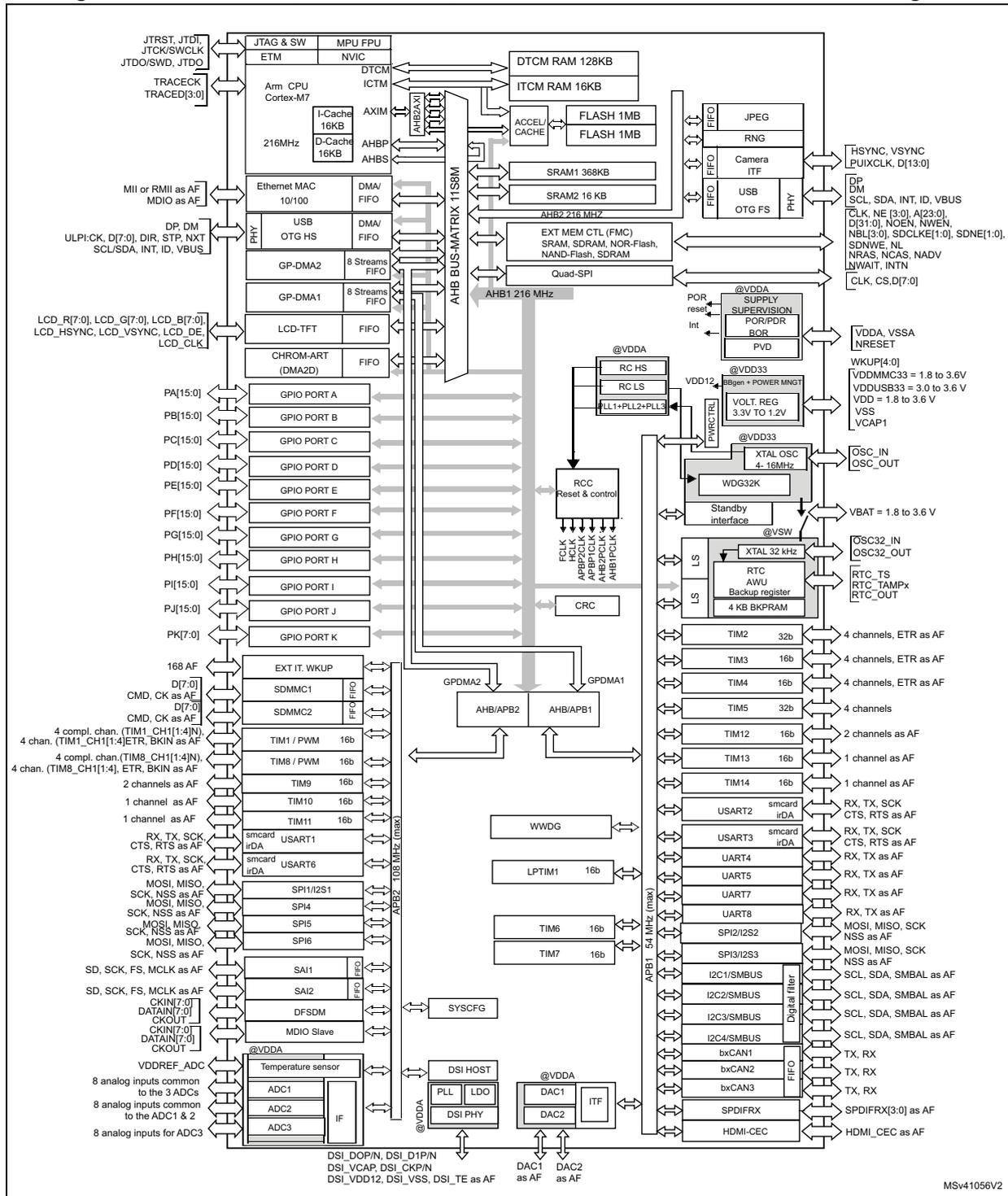
Figure 1 gives compatible board designs between the STM32F7xx and STM32F4xx families.

Figure 1. Compatible board design for LQFP100 package



The STM32F76x LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176 packages are fully pin to pin compatible with STM32F4xx devices.

Figure 2. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2 Functional overview

2.1 Arm[®] Cortex[®]-M7 with FPU

The Arm[®] Cortex[®]-M7 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex[®]-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow an efficient signal processing and a complex algorithm execution.

It supports single and double precision FPU (floating point unit), speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 2 shows the general block diagram of the STM32F76xxx family.

Note: The Cortex[®]-M7 with FPU core is binary compatible with the Cortex[®]-M4 core.

2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3 Embedded Flash memory

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx devices embed a Flash memory of up to 2 Mbytes available for storing programs and data. The Flash interface features:

- Single /or Dual bank operating modes,
- Read-While-Write (RWW) in Dual bank mode.

2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.5 Embedded SRAM

All the devices feature:

- System SRAM up to 512 Kbytes:
 - SRAM1 on AHB bus Matrix: 368 Kbytes
 - SRAM2 on AHB bus Matrix: 16 Kbytes
 - DTCM-RAM on TCM interface (Tightly Coupled Memory interface): 128 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
 - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMA's and peripherals DMA's through specific AHB slave of the CPU. The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

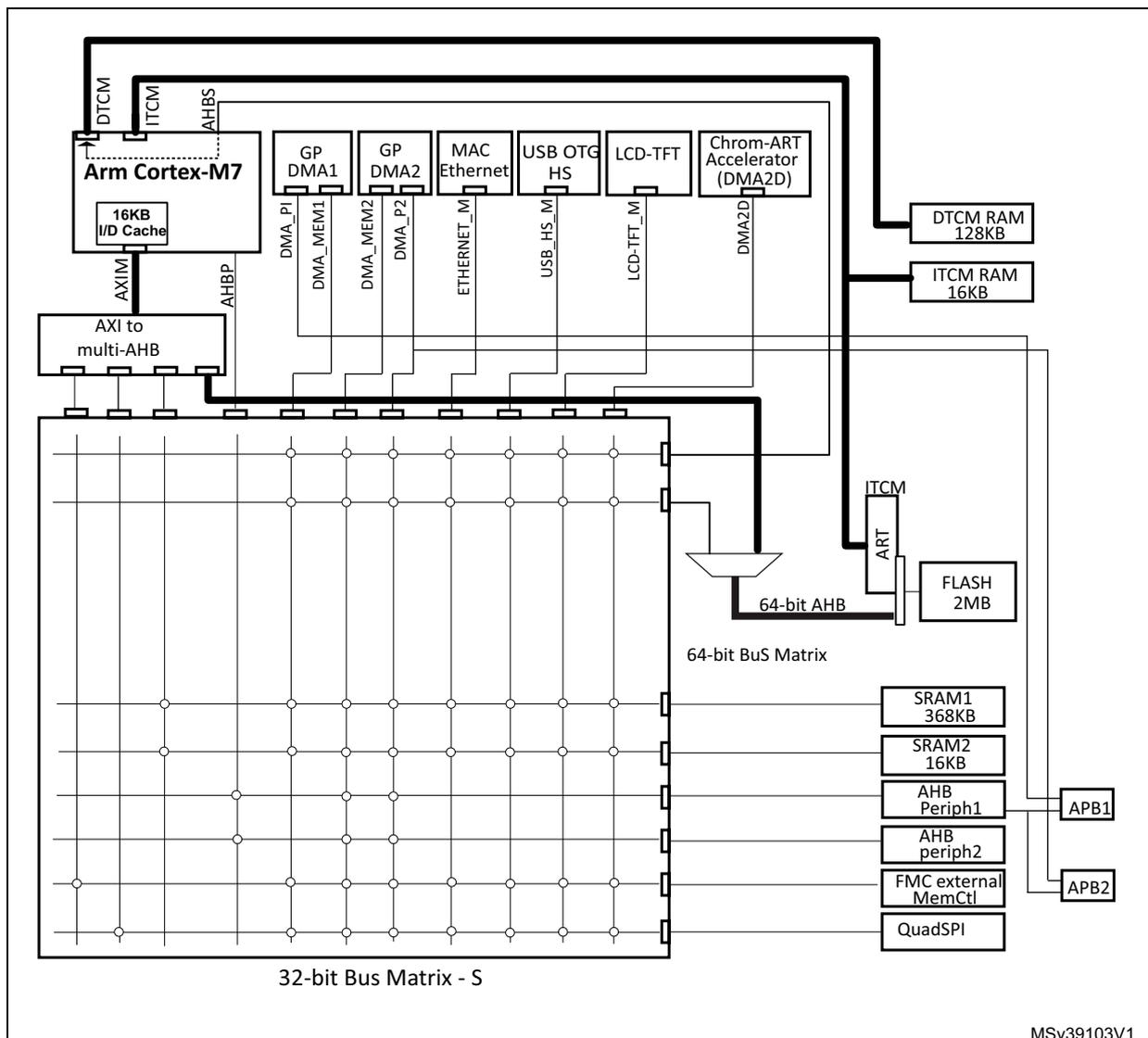
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

2.6 AXI-AHB bus matrix

The STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
 - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
 - 1x AXI to 64-bit AHB bridge connected to the embedded Flash memory
- A multi-AHB Bus-Matrix
 - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 3. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx AXI-AHB bus matrix architecture⁽¹⁾



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. The configuration is made by software and the transfer sizes between the source and the destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- Camera interface (DCMI)
- ADC
- SAI
- SPDIFRX
- Quad-SPI
- HDMI-CEC
- JPEG codec
- DFSDM1

2.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
 - Static random access memory (SRAM)
 - NOR Flash memory/OneNAND Flash memory
 - PSRAM (4 memory banks)
 - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) memories
- 8-, 16-, 32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.9 Quad-SPI memory interface (QUADSPI)

All the devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It can work in:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes external Flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. The communication can be either in Single Data Rate or Dual Data Rate.

2.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events

2.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format codings are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

2.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 110 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.13 JPEG codec (JPEG)

The JPEG codec provides a fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Stallable design
- Support for single, greyscale component
- Functionality to enable/disable header processing
- Internal register interface
- Fully synchronous design
- Configured for high-speed decode mode

2.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 25 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

2.15 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 216 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 216 MHz while the maximum frequency of the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz.

The devices embed two dedicated PLL (PLLI2S and PLLSAI) which allow to achieve audio class performance. In this case, the I²S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.16 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to *STM32 microcontroller system memory boot mode* application note (AN2606) for details.

2.17 Power supply schemes

- $V_{DD} = 1.7$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.7$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 2.18.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

- $V_{DDSDMMC}$ can be connected either to V_{DD} or an external independent power supply (1.8 to 3.6V) for SDMMC2 pins (clock, command, and 4-bit data). For example, when the device is powered at 1.8V, an independent power supply 2.7V can be connected to $V_{DDSDMMC}$. When the $V_{DDSDMMC}$ is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions $V_{DDSDMMC}$ must be respected:
 - During the power-on phase ($V_{DD} < V_{DD_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
 - During the power-down phase ($V_{DD} < V_{DD_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
 - The $V_{DDSDMMC}$ rising and falling time rate specifications must be respected
 - In operating mode phase, $V_{DDSDMMC}$ could be lower or higher than V_{DD} : All associated GPIOs powered by $V_{DDSDMMC}$ are operating between $V_{DDSDMMC_MIN}$ and $V_{DDSDMMC_MAX}$.
- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to [Figure 4](#) and [Figure 5](#)). For example, when the device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB} . When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to

disappear. The following conditions V_{DDUSB} must be respected:

- During the power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During the power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- The V_{DDUSB} rising and falling time rate specifications must be respected (see [Table 20](#) and [Table 21](#))
- In operating mode phase, V_{DDUSB} could be lower or higher than V_{DD} :
 - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX} .
 - The V_{DDUSB} supply both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB} .
 - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX} .

Figure 4. V_{DDUSB} connected to V_{DD} power supply

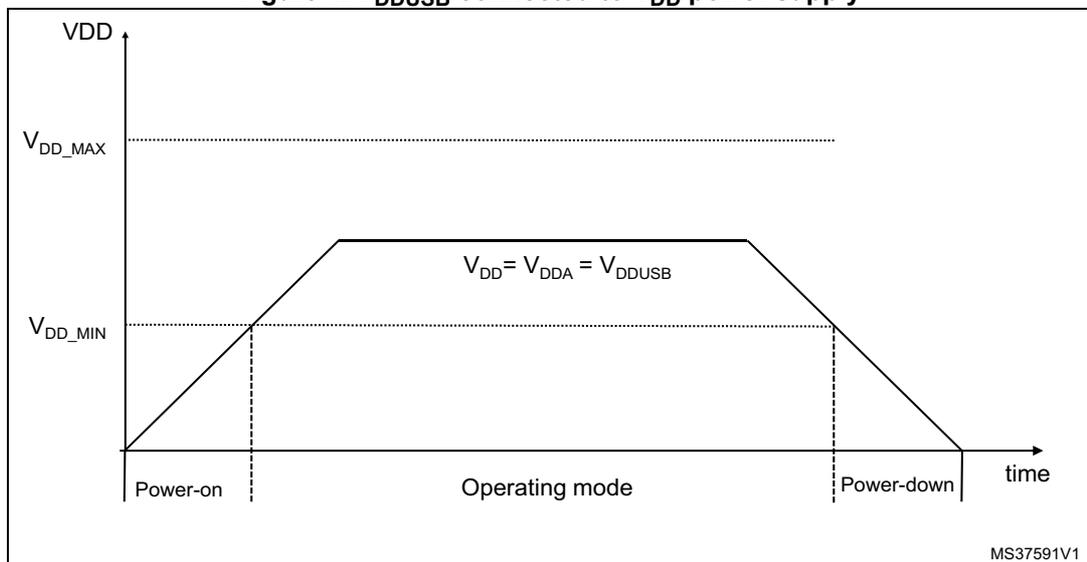
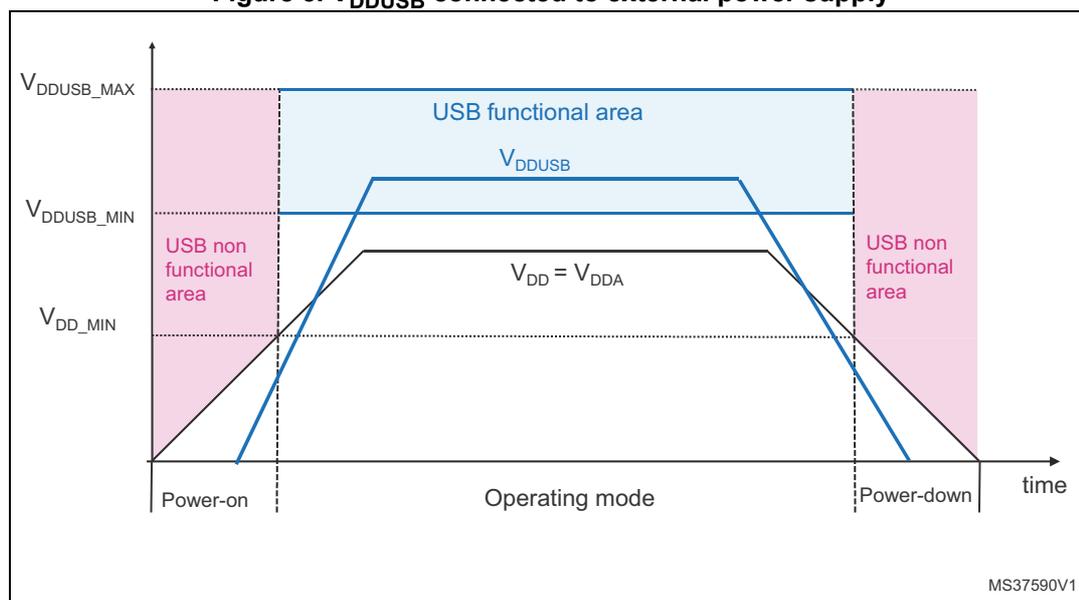


Figure 5. V_{DDUSB} connected to external power supply

The DSI (Display Serial Interface) sub-system uses several power supply pins which are independent from the other supply pins:

- V_{DDDSI} is an independent DSI power supply dedicated for DSI Regulator and MIPI D-PHY. This supply must be connected to global V_{DD} .
- The V_{CAPDSI} pin is the output of DSI Regulator (1.2V) which must be connected externally to $V_{DD12DSI}$.
- The $V_{DD12DSI}$ pin is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. An external capacitor of 2.2 μF must be connected on the $V_{DD12DSI}$ pin.
- The V_{SSDSI} pin is an isolated supply ground used for DSI sub-system.
- If the DSI functionality is not used at all, then:
 - The V_{DDDSI} pin must be connected to global V_{DD} .
 - The V_{CAPDSI} pin must be connected externally to $V_{DD12DSI}$ but the external capacitor is no more needed.
 - The V_{SSDSI} pin must be grounded.

2.18 Power supply supervisor

2.18.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through

option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit.

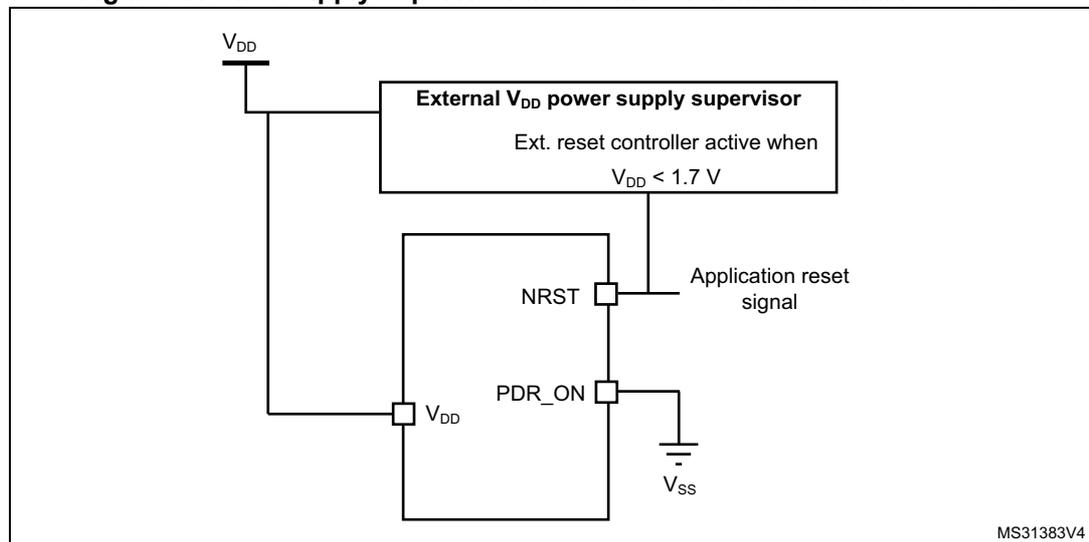
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.18.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to V_{SS} . Refer to [Figure 6: Power supply supervisor interconnection with internal reset OFF](#).

Figure 6. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see [Figure 7](#)).

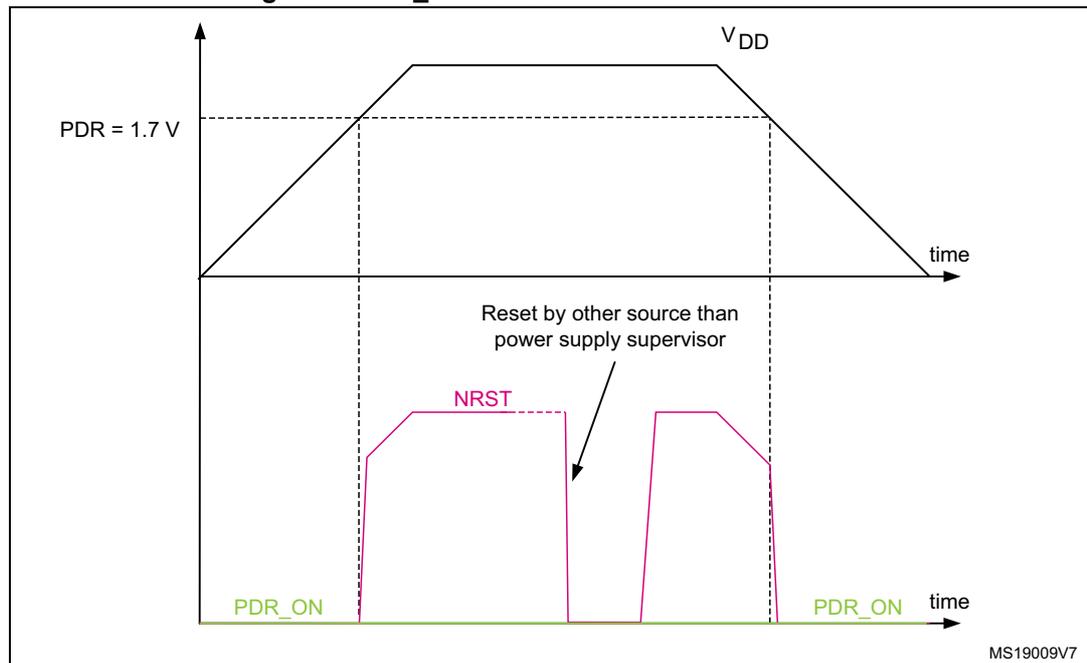
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD} .

All the packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal when connected to V_{SS} .

Figure 7. PDR_ON control with internal reset OFF



2.19 Voltage regulator

The regulator has four operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low power regulator (LPR)
 - Power-down
- Regulator OFF

2.19.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
 - In Run/Sleep modes

The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
 - In Stop modes

The MR can be configured in two ways during stop mode:
 MR operates in normal mode (default mode of MR in stop mode)
 MR operates in under-drive mode (reduced leakage mode).

- LPR is used in the Stop modes:
 The LP regulator mode is configured by software when entering Stop mode.
 Like the MR mode, the LPR can be configured in two ways during stop mode:
 - LPR operates in normal mode (default mode when LPR is ON)
 - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.
 The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to [Table 3](#) for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode⁽¹⁾

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode ⁽²⁾	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.

2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

2.19.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V₁₂ voltage source through V_{CAP_1} and V_{CAP_2} pins.

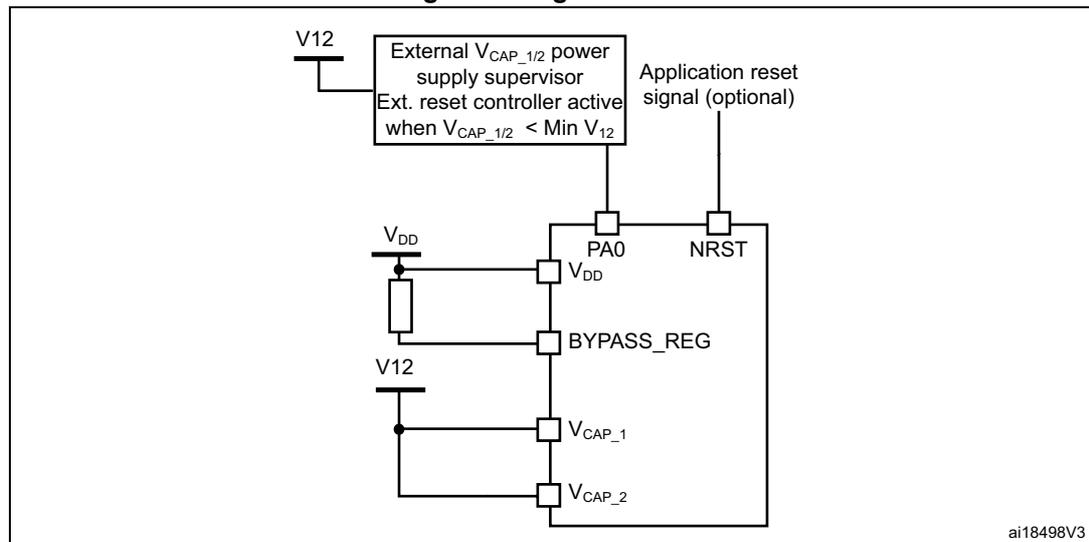
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V₁₂. An external power supply supervisor should be used to monitor the V₁₂ of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V₁₂ power domain.

In the regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V₁₂ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 8. Regulator OFF

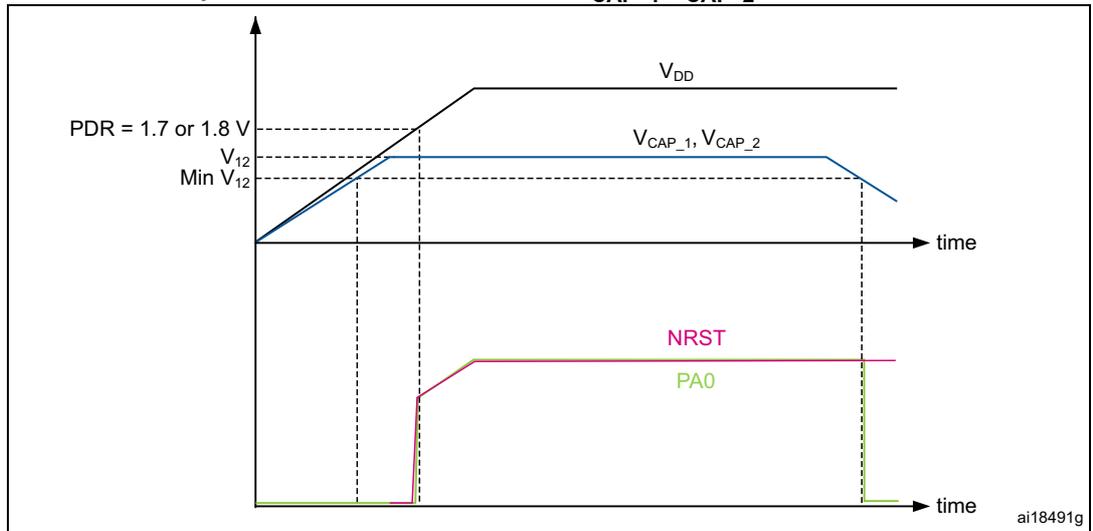


The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see [Figure 9](#)).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 10](#)).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

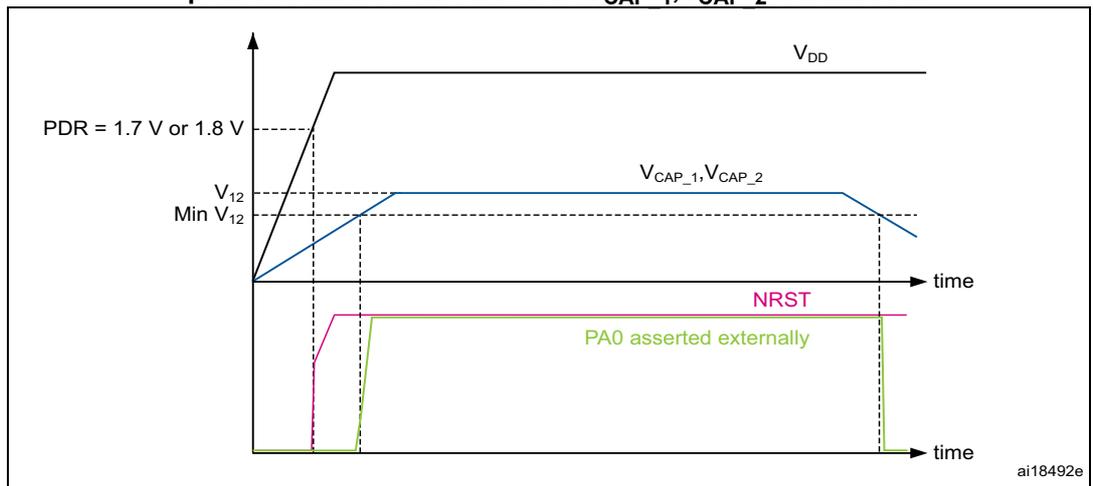
Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

Figure 9. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1} , V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 10. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1} , V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

2.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP100	Yes	No	Yes	No
LQFP144, LQFP208			Yes PDR_ON set to V _{DD}	Yes PDR_ON set to V _{SS}
LQFP176, UFBGA176, TFBGA100, TFBGA216	Yes BYPASS_REG set to V _{SS}	Yes BYPASS_REG set to V _{DD}		
WLCSP180	Yes ⁽¹⁾			

1. Available only on dedicated part number. Refer to [Section 7: Ordering information](#).

2.20 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator(LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.21 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup and LPTIM1 asynchronous interrupt).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering

Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

2.22 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT} , external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When the PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and the V_{BAT} pin should be connected to V_{DD} .

2.23 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

[Table 6](#) compares the features of the advanced-control, general-purpose and basic timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) ⁽¹⁾
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	108	216
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	108	216
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	108	216
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	54	108/216
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	54	108/216
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	54	108/216

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2.23.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.23.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F76xxx devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F76xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

2.23.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

2.23.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
 - Internal clock source: LSE, LSI, HSI or APB clock
 - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

2.23.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

2.23.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.23.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.24 Inter-integrated circuit interface (I²C)

The devices embed 4 I2C. Refer to table [Table 7: I2C implementation](#) for the features implementation.

The I²C bus interface handles communications between the microcontroller and the serial I²C bus. It controls all I²C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
 - Slave and master modes, multimaster capability
 - Standard-mode (Sm), with a bitrate up to 100 kbit/s
 - Fast-mode (Fm), with a bitrate up to 400 kbit/s
 - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
 - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
 - Programmable setup and hold times
 - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
 - Hardware PEC (Packet Error Checking) generation and verification with ACK control
 - Address resolution protocol (ARP) support
 - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

I2C features ⁽¹⁾	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X

1. X: supported.

2.25 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed USART. Refer to [Table 8: USART implementation](#) for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when the USART clock source is system clock frequency (max is 216 MHz) and oversampling by 8 is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Programmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode (T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard)
- Support for Modbus communication

[Table 8](#) summarizes the implementation of all U(S)ARTs instances

Table 8. USART implementation

features ⁽¹⁾	USART1/2/3/6	UART4/5/7/8
Data Length	7, 8 and 9 bits	
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	-

Table 8. USART implementation (continued)

features ⁽¹⁾	USART1/2/3/6	UART4/5/7/8
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X

1. X: supported.

2.26 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 54 Mbits/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation. All the SPIs can be served by the DMA controller.

Three standard I²S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

2.27 Serial audio interface (SAI)

The devices embed two serial audio interfaces.

The serial audio interface is based on two independent audio subblocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both subblocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 and SAI2 can be served by the DMA controller

2.28 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main features of the SPDIFRX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named `spdif_frame_sync`, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

2.29 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S and SAI applications. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S/SAI flow with an external PLL (or Codec output).

2.30 Audio and LCD PLL (PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

2.31 SD/SDIO/MMC card host interface (SDMMC)

SDMMC host interfaces are available, that support the MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

2.32 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.33 Controller area network (bxCAN)

The three CANs are compliant with the 2.0A and B (active) specifications with a bit rate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for CAN1 and CAN2. 512 bytes of SRAM are dedicated for CAN3.

2.34 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For the OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.35 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support

- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.36 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

2.37 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbytes/s in 8-bit mode at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.38 Management Data Input/Output (MDIO) slaves

The devices embed a MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
 - 32 x 16-bit firmware read/write, MDIO read-only output data registers
 - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
 - MDIO Register write
 - MDIO Register read
 - MDIO protocol error
- Able to operate in and wake up from STOP mode

2.39 Random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.40 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

A fast I/O handling allows a maximum I/O toggling up to 108 MHz.

2.41 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

2.42 Digital filter for Sigma-Delta Modulators (DFSDM)

The devices embed one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support. The DFSDM peripheral is dedicated to interface the external $\Sigma\Delta$ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on $\Sigma\Delta$ modulators inputs). The DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM). The DFSDM transceivers support several serial interface formats (to support various $\Sigma\Delta$ modulators). The DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
 - Configurable SPI interface to connect various SD modulator(s)
 - Configurable Manchester coded 1 wire interface support
 - PDM (Pulse Density Modulation) microphone input support
 - Maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
 - Clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
 - internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
 - Sincxfilter: filter order/type (1..5), oversampling ratio (up to 1..1024)
 - integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
 - Software trigger
 - Internal timers
 - External events
 - Start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
 - Low value and high value data threshold registers
 - Dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
 - Input from final output data or from selected input digital serial channels
 - Continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
 - Up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
 - Monitoring continuously each input serial channel
- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
 - Storage of minimum and maximum values of final conversion data

- Refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “regular” or “injected” conversions:
 - “regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
 - “injected” conversions for precise timing and with high conversion priority

Table 9. DFSDM implementation

DFSDM features	DFSDM1
Number of filters: x (DFSDM_FLTx)	4
Number of input transceivers/channels: y (DFSDM_CHy)	8
Internal ADC parallel input support	-
Number of external triggers (JEXTSEL size)	32
ID register support	-

2.43 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with the temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT} , ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.44 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.45 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.46 Embedded Trace Macrocell™

The Arm embedded trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F76xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or

any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

2.47 DSI Host (DSIHOST)

The DSI Host is a dedicated peripheral for interfacing with MIPI[®] DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

These interfaces are as follows:

- LTDC interface:
 - Used to transmit information in Video mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).
 - Through a customized for mode, this interface can be used to transmit information in full bandwidth in the Adapted Command mode (DBI).
- APB slave interface:
 - Allows the transmission of generic information in Command mode, and follows a proprietary register interface.
 - Can operate concurrently with either LTDC interface in either Video mode or Adapted Command mode.
- Video mode pattern generator:
 - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.

The DSI Host main features:

- Compliant with MIPI[®] Alliance standards
- Interface with MIPI[®] D-PHY
- Supports all commands defined in the MIPI[®] Alliance specification for DCS:
 - Transmission of all Command mode packets through the APB interface
 - Transmission of commands in low-power and high-speed during Video mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-power mode with PLL disabled
- ECC and Checksum capabilities
- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes
- 3D transmission support
- Configurable selection of system interfaces:
 - AMBA APB for control and optional support for Generic and DCS commands
 - Video Mode interface through LTDC
 - Adapted Command mode interface through LTDC
- Independently programmable Virtual Channel ID in

- Video mode
- Adapted Command mode
- APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:
 - 16-bit RGB, configurations 1, 2, and 3
 - 18-bit RGB, configurations 1 and 2
 - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Maximum resolution is limited by available DSI physical link bandwidth:
 - Number of lanes: 2
 - Maximum speed per lane: 500 Mbps1Gbps

Adapted interface features

Support for sending large amounts of data through the memory_write_start(WMS) and memory_write_continue(WMC) DCS commands

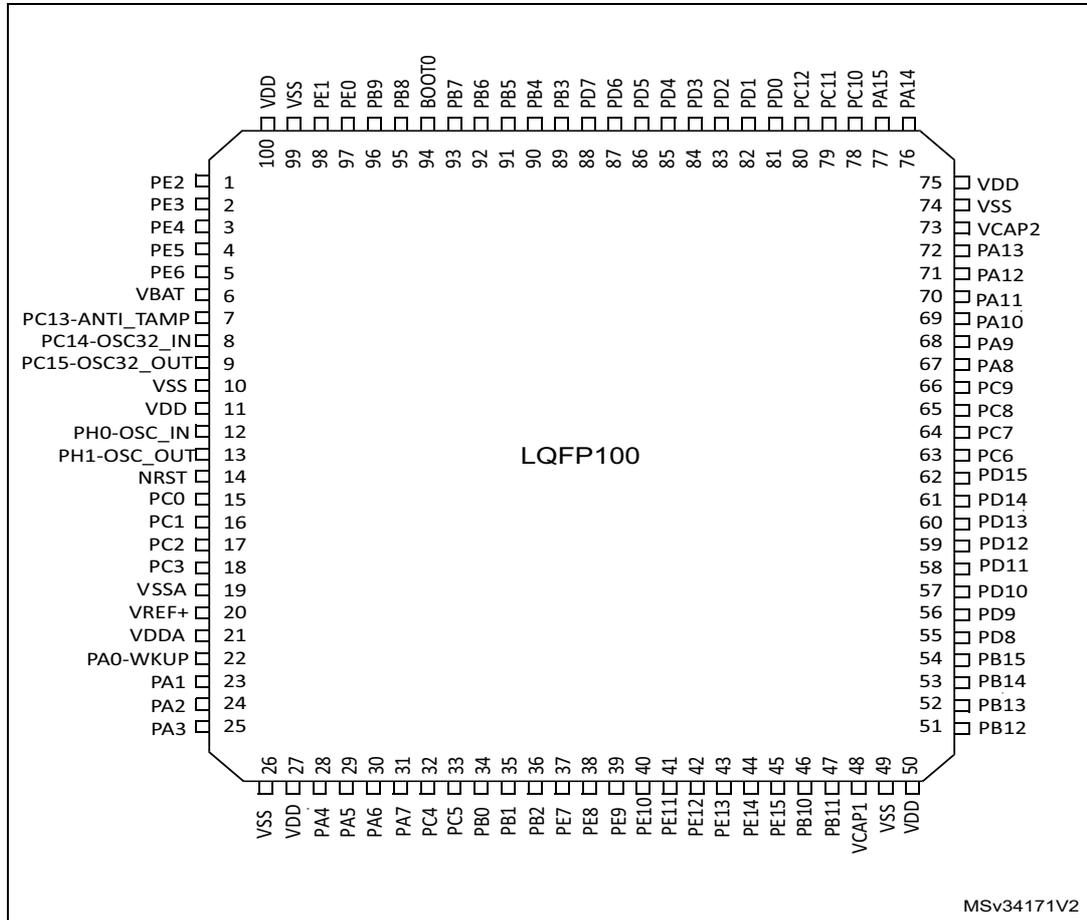
- LTDC interface color coding mappings into 24-bit interface:
 - 16-bit RGB, configurations 1, 2, and 3
 - 18-bit RGB, configurations 1 and 2
 - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

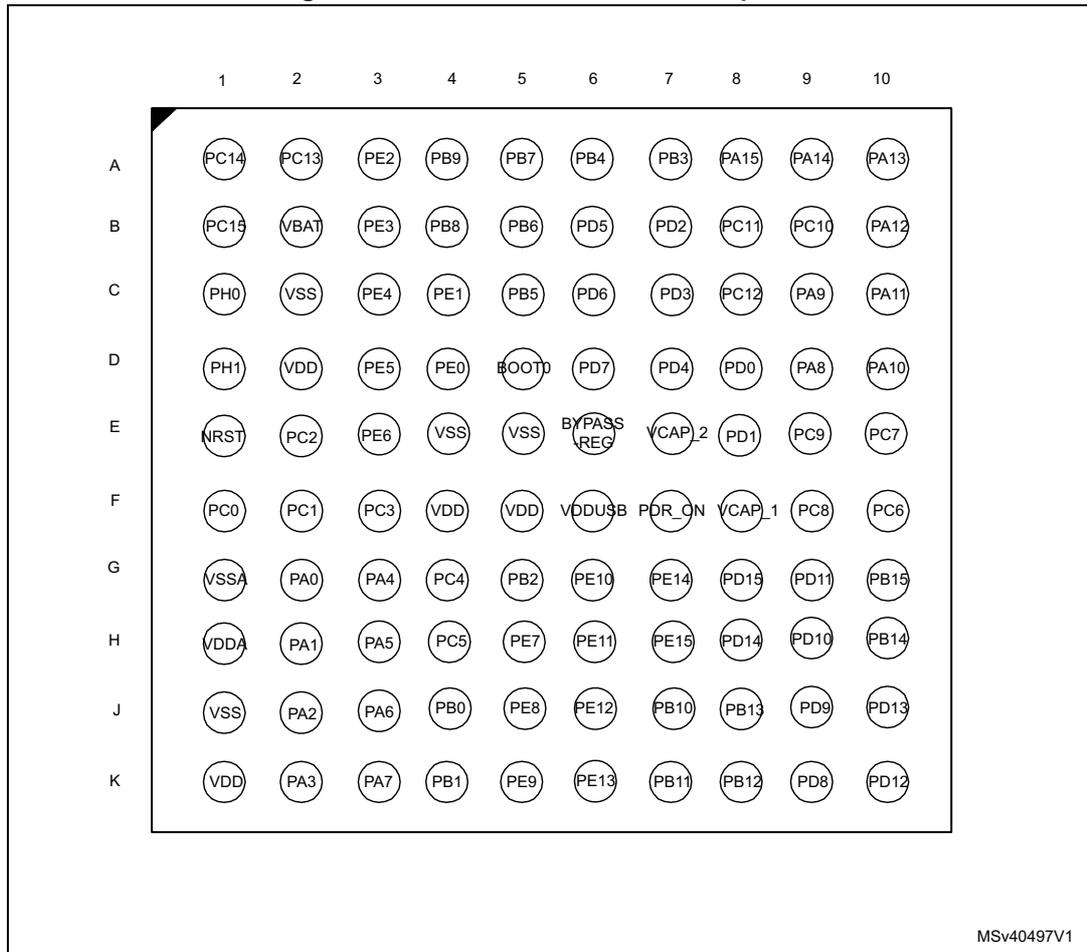
3 Pinouts and pin description

Figure 11. STM32F76xxx LQFP100 pinout



1. The above figure shows the package top view.

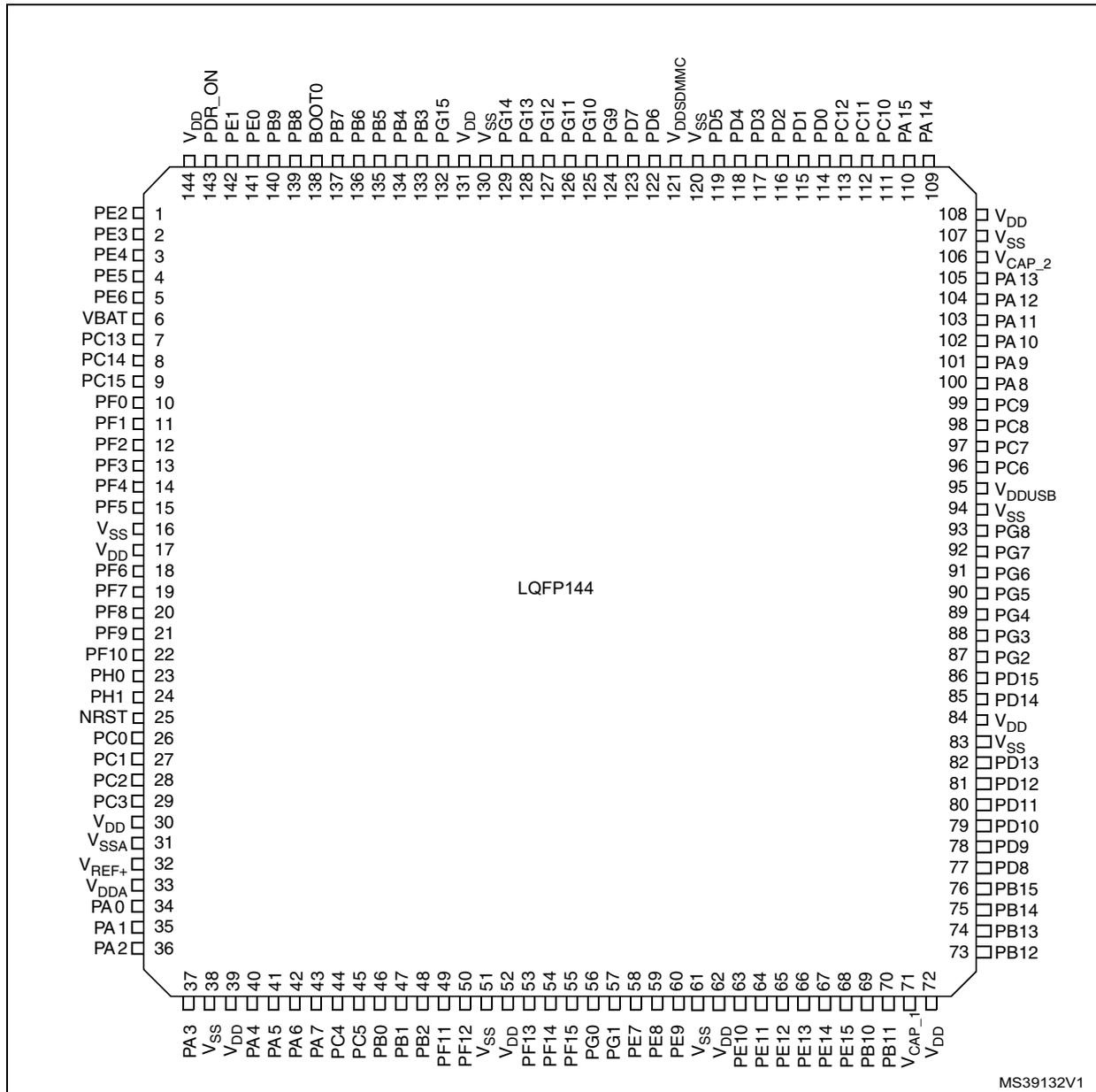
Figure 12. STM32F76xxx TFBGA100 pinout



MSv40497V1

1. The above figure shows the package top view.

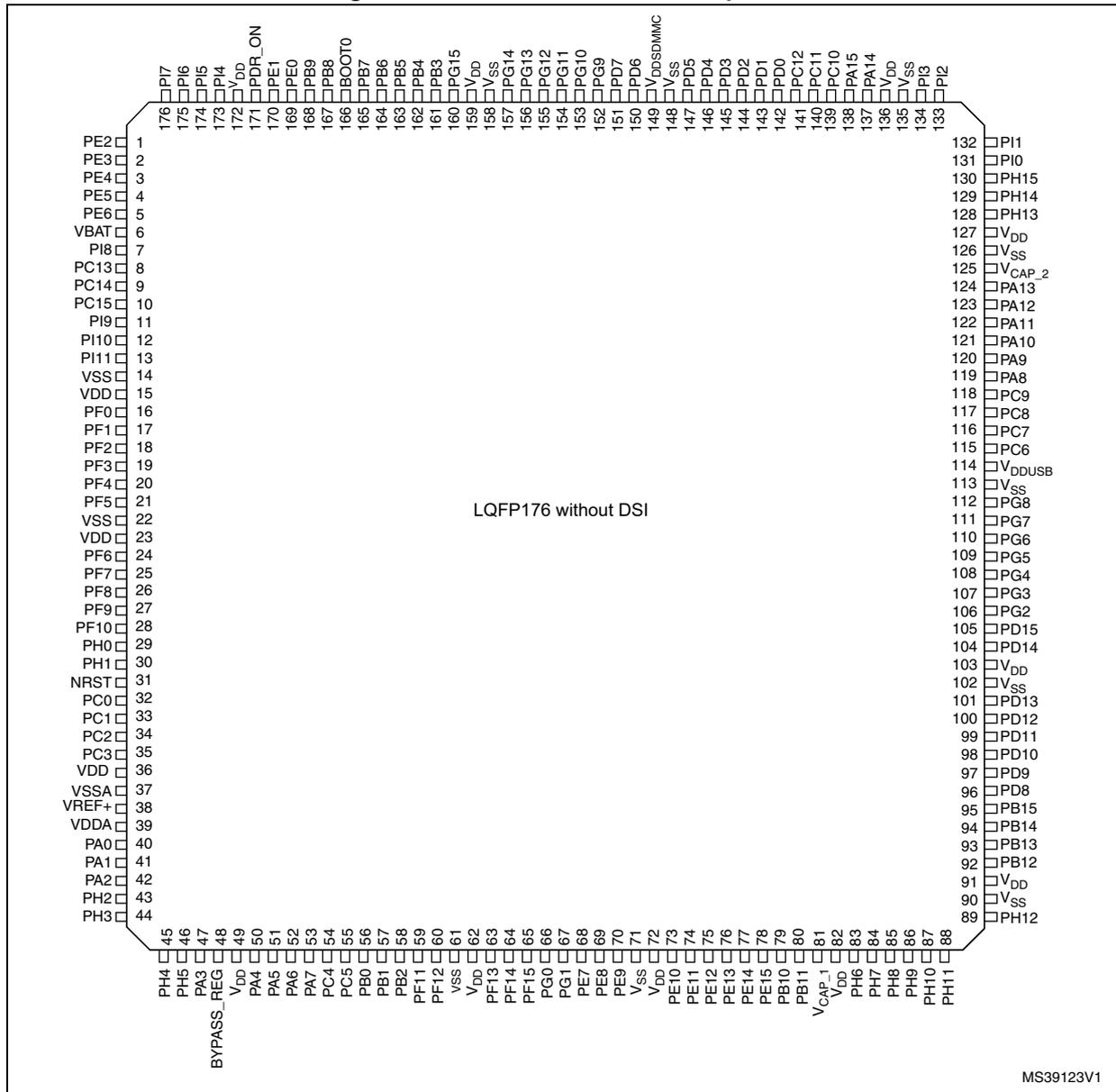
Figure 13. STM32F76xxx LQFP144 pinout



MS39132V1

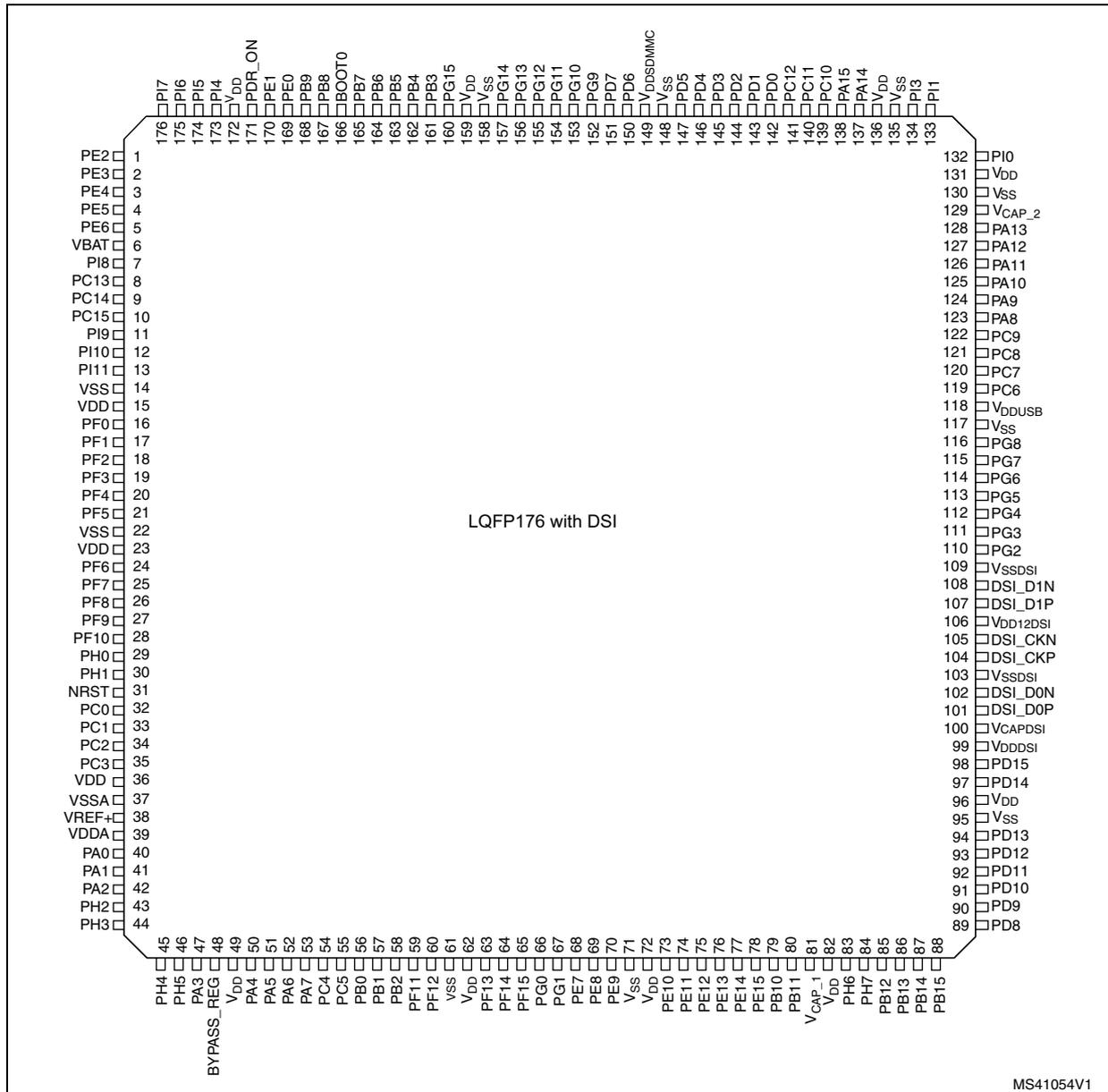
1. The above figure shows the package top view.

Figure 14. STM32F76xxx LQFP176 pinout



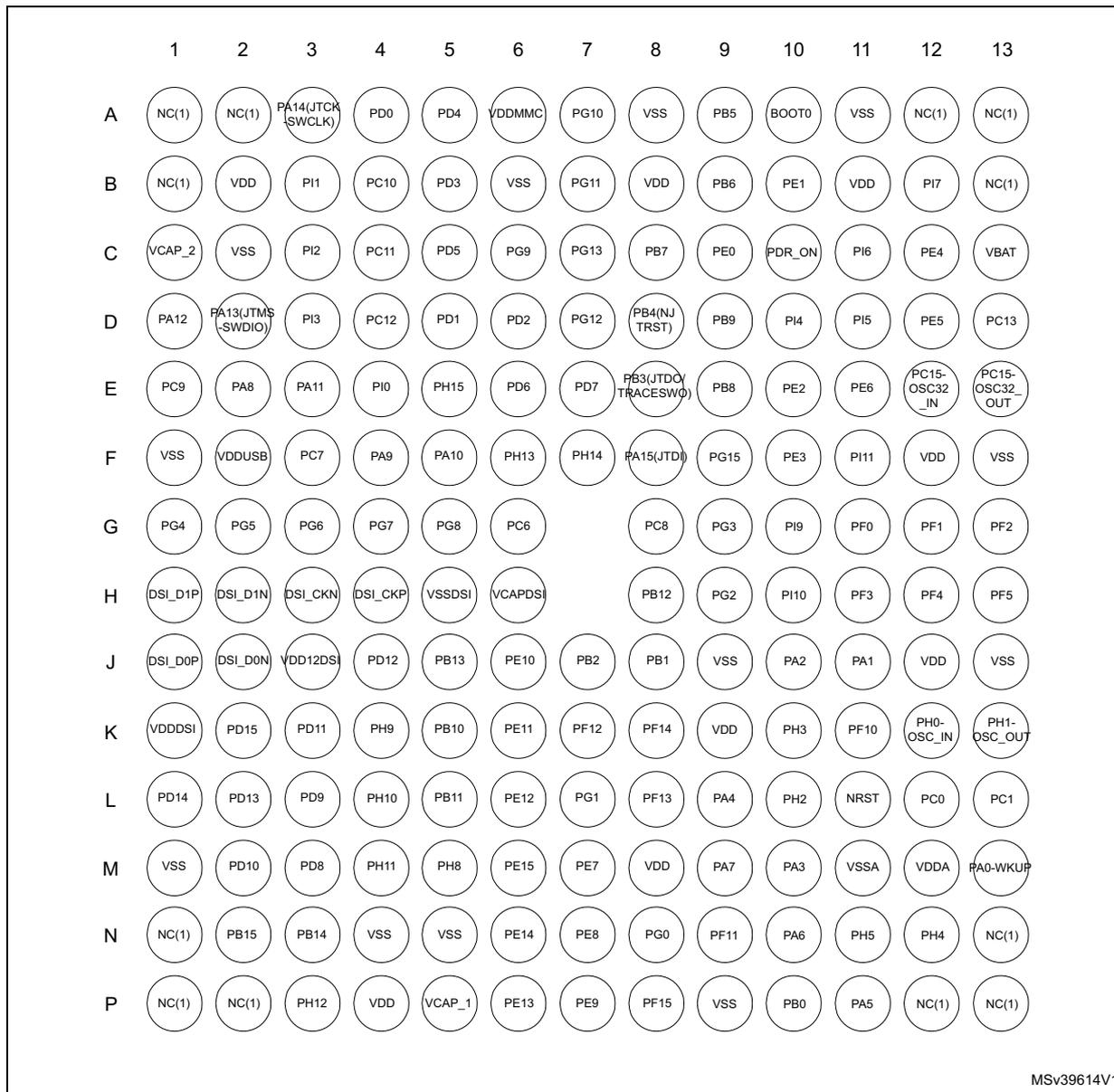
1. The above figure shows the package top view.

Figure 15. STM32F769xx LQFP176 pinout



1. The above figure shows the package top view.

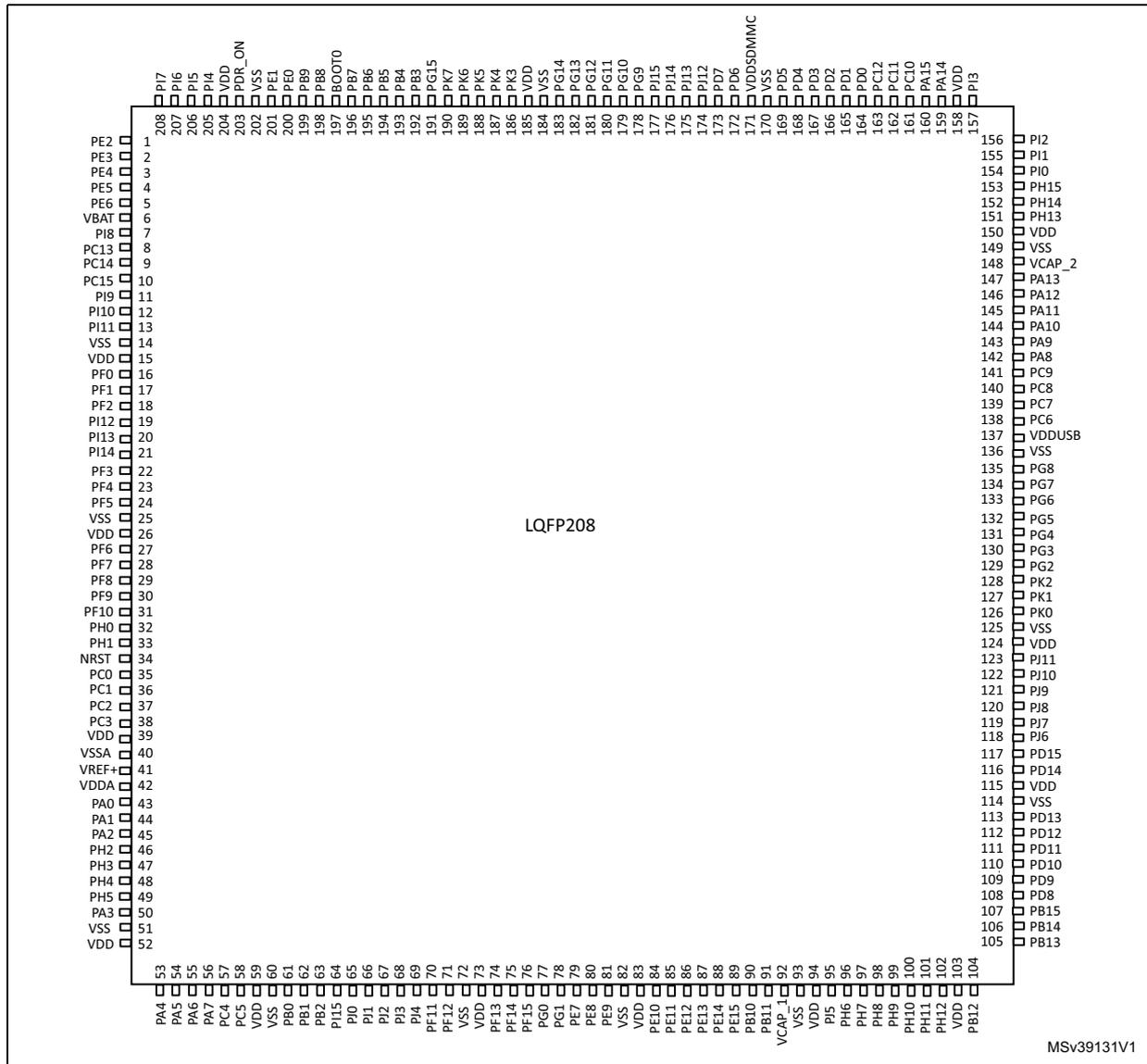
Figure 16. STM32F769Ax/STM32F768Ax WLCSP180 ballout



MSv39614V1

1. NC ball must not be connected to GND nor to VDD.
2. The above figure shows the package top view.

Figure 17. STM32F76xxx LQFP208 pinout

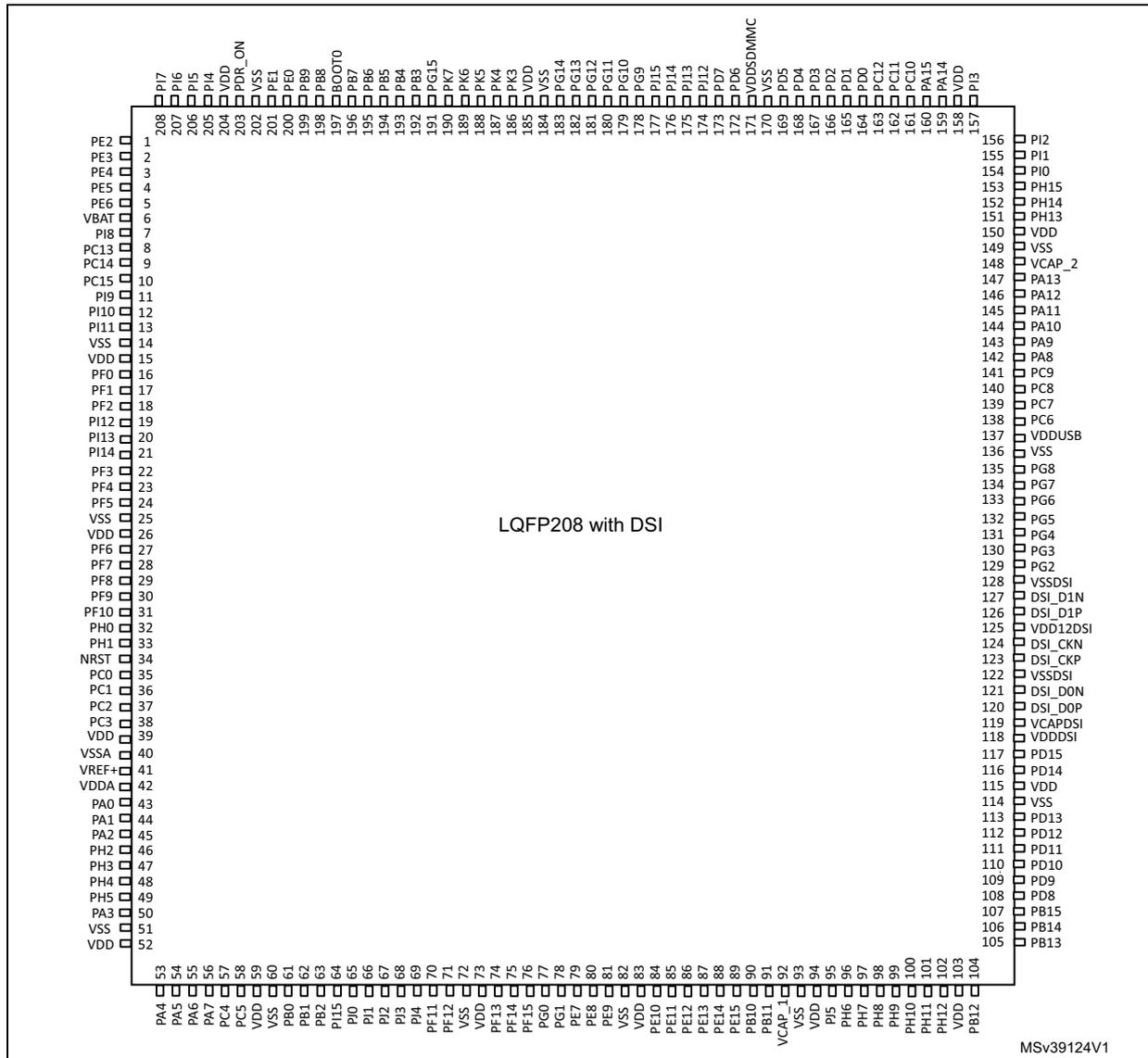


MSv39131V1

1. The above figure shows the package top view.

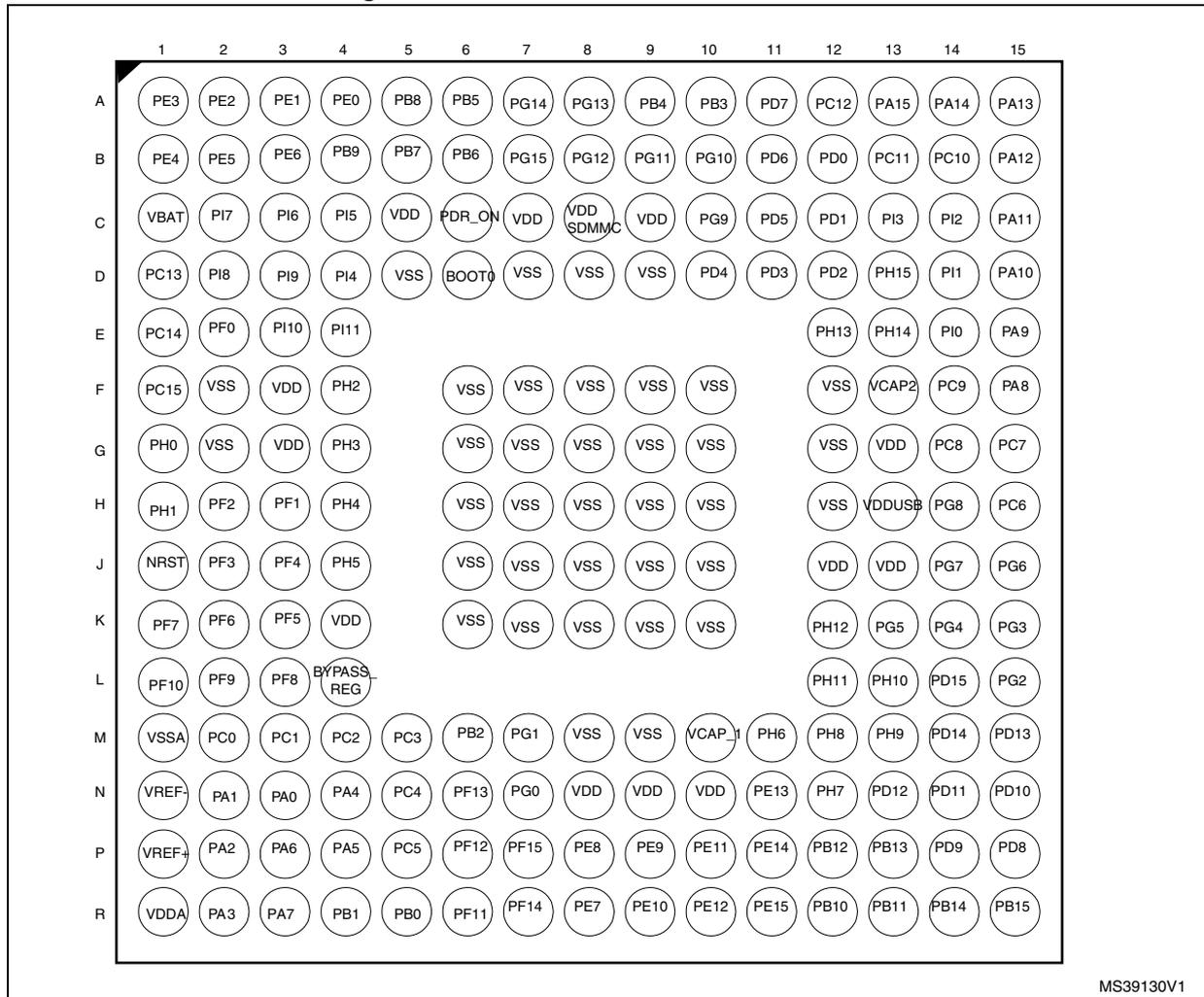


Figure 18. STM32F769xx LQFP208 pinout



1. The above figure shows the package top view.

Figure 19. STM32F76xxx UFBGA176 ballout



MS39130V1

- 1. The above figure shows the package top view.

Table 10. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions	
STM32F765xx STM32F767xx					STM32F768Ax STM32F769xx											
TFBGA100	LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 ⁽¹⁾	LQFP176	LQFP208							TFBGA216
A3	1	1	A2	1	1	A3	E10	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
B3	2	2	A1	2	2	A2	F10	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-

Table 11. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number											Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx										
TFBGA100	LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 ⁽¹⁾	LQFP176	LQFP208	TFBGA216						
H2	23	35	N2	41	44	N2	J11	41	44	N2	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_ REF_CLK, LCD_R2, EVENTOUT	ADC1_IN1, ADC2_IN1, ADC3_IN1
J2	24	36	P2	42	45	P2	J10	42	45	P2	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	-	F4	43	46	K4	L10	43	46	K4	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRIS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	-	G4	44	47	J4	K10	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	-	H4	45	48	H4	N12	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-
-	-	-	J4	46	49	J3	N11	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
K2	25	37	R2	47	50	R2	M10	47	50	R2	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
J1	26	38	-	-	51	K6	J9	-	51	K6	VSS	S	-	-	-	-
E6	-	-	L4	48	-	L5	-(⁵)	48	-	L5	BYPASS_ REG	I	FT	-	-	-
K1	27	39	K4	49	52	K5	K9	49	52	K5	VDD	S	-	-	-	-
G3	28	40	N4	50	53	N4	L9	50	53	N4	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1



Table 11. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number											Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx							STM32F768Ax STM32F769xx									
TFBGA100	LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 ⁽¹⁾	LQFP176	LQFP208	TFBGA216						
H3	29	41	P4	51	54	P4	P11	51	54	P4	PA5	I/O	Ta	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
J3	30	42	P3	52	55	P3	N10	52	55	P3	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, SPI6_MISO, TIM13_CH1, MDIOS_MDC, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC1_IN6, ADC2_IN6
K3	31	43	R3	53	56	R3	M9	53	56	R3	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
G4	32	44	N5	54	57	N5	NC	54	57	N5	PC4	I/O	FT	-	DFSDM1_CKIN2, I2S1_MCK, SPDIF_RX2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDN0, EVENTOUT	ADC1_IN14, ADC2_IN14
H4	33	45	P5	55	58	P5	NC	55	58	P5	PC5	I/O	FT	-	DFSDM1_DATIN2, SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15
-	-	-	-	-	59	L7	-	-	59	L7	VDD	S	-	-	-	-
-	-	-	-	-	60	L6	-	-	60	L6	VSS	S	-	-	-	-
J4	34	46	R5	56	61	R5	P10	56	61	R5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC1_IN8, ADC2_IN8
K4	35	47	R4	57	62	R4	J8	57	62	R4	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC1_IN9, ADC2_IN9

Table 12. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 62. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f _{HSE} /f _{CPU}]	Unit
				8/200 MHz	
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	5	dBμV
			30 to 130 MHz	10	
			130 MHz to 1 GHz	18	
			1 GHz to 2 GHz	10	
			EMI Level	3.5	
		V _{DD} = 3.6 V, T _A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering enabled.	0.1 to 30 MHz	2	dBμV
			30 to 130 MHz	9	
			130 MHz to 1 GHz	14	
			1 GHz to 2 GHz	9	
			EMI Level	3	

5.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.



Table 63. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25$ °C conforming to ANSI/ESDA/JEDEC JS-001-2012	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25$ °C conforming to ANSI/ESD S5.3.1-2009, all packages except TFBGA100	3	250	
		$T_A = +25$ °C conforming to ANSI/ESD S5.3.1-2009, TFBGA100 package	4	500	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 64. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105$ °C conforming to JESD78A	II level A

5.3.19 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5 \mu A/+0 \mu A$ range), or other functional failure (for example reset, oscillator frequency deviation).

A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in [Table 65](#).

Table 65. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I _{INJ}	Injected current on BOOT0, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N, DSI_CKP, DSI_CKN pin	- 0	0	mA
	Injected current on NRST pin	- 0	NA ⁽¹⁾	
	Injected current on PC0, PC2, PH1_OSCOUT pins	- 0	NA ⁽¹⁾	
	Injected current on any other FT pin	- 5	NA ⁽¹⁾	
	Injected current on any other pins	- 5	+5	

1. Injection is not possible.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

5.3.20 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 66: I/O static characteristics](#) are derived from tests performed under the conditions summarized in [Table 18](#). All I/Os are CMOS and TTL compliant.

Table 66. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V ≤ V _{DD} ≤ 3.6 V	-	-	0.35V _{DD} - 0.04 ⁽¹⁾	V
			-	-	0.3V _{DD} ⁽²⁾	
	BOOT I/O input low level voltage	1.75 V ≤ V _{DD} ≤ 3.6 V, -40 °C ≤ T _A ≤ 105 °C	-	-	0.1V _{DD} + 0.1 ⁽¹⁾	
V _{IH}	FT, TTa and NRST I/O input high level voltage ⁽⁵⁾	1.7 V ≤ V _{DD} ≤ 3.6 V	0.45V _{DD} + 0.3 ⁽¹⁾	-	-	V
			0.7V _{DD} ⁽²⁾	-	-	
	BOOT I/O input high level voltage	1.75 V ≤ V _{DD} ≤ 3.6 V, -40 °C ≤ T _A ≤ 105 °C	0.17V _{DD} + 0.7 ⁽¹⁾	-	-	
V _{HYS}	FT, TTa and NRST I/O input hysteresis	1.7 V ≤ V _{DD} ≤ 3.6 V	10%V _{DD} ⁽³⁾	-	-	V
			0.1	-	-	
	BOOT I/O input hysteresis	1.75 V ≤ V _{DD} ≤ 3.6 V, -40 °C ≤ T _A ≤ 105 °C	0.1	-	-	
		1.7 V ≤ V _{DD} ≤ 3.6 V, 0 °C ≤ T _A ≤ 105 °C				

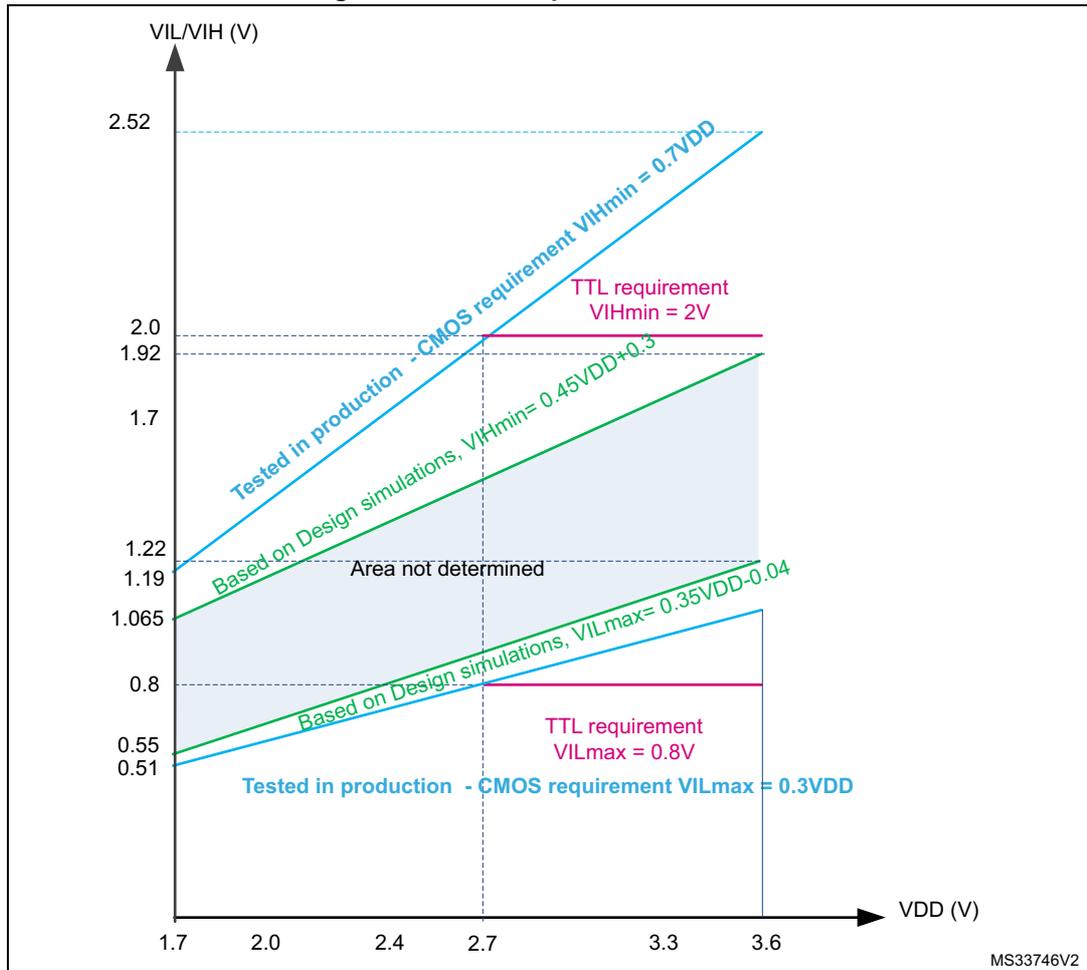
Table 66. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I _{Ikg}	I/O input leakage current ⁽⁴⁾		V _{SS} ≤ V _{IN} ≤ V _{DD}	-	-	±1	μA
	I/O FT input leakage current ⁽⁵⁾		V _{IN} = 5 V	-	-	3	
R _{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	V _{IN} = V _{SS}	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
R _{PD}	Weak pull-down equivalent resistor ⁽⁷⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	V _{IN} = V _{DD}	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
C _{IO} ⁽⁸⁾	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to [Table 65: I/O current injection susceptibility](#)
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 65: I/O current injection susceptibility](#)
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in [Figure 39](#).

Figure 39. FT I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14, PC15 and PI8 which can sink or source up to ± 3 mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#). In particular:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 16](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 16](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 67](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 18](#). All I/Os are CMOS and TTL compliant.

Table 67. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	CMOS port ⁽²⁾ $I_{IO} = -8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4$	-	
$V_{OH}^{(3)}$	Output high level voltage for PC14	CMOS port ⁽²⁾ $I_{IO} = -2 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	TTL port ⁽²⁾ $I_{IO} = -8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	1.3 ⁽⁴⁾	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	$I_{IO} = -20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 1.3^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4 ⁽⁴⁾	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	$I_{IO} = -6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4 ⁽⁵⁾	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	$I_{IO} = -4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4^{(5)}$	-	
$V_{OH}^{(3)}$	Output high level voltage for PC14	$I_{IO} = -1 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4^{(5)}$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 16](#). and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 16](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 40](#) and [Table 68](#), respectively.

Unless otherwise specified, the parameters given in [Table 68](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 18](#).

Table 68. I/O AC characteristics⁽¹⁾⁽²⁾

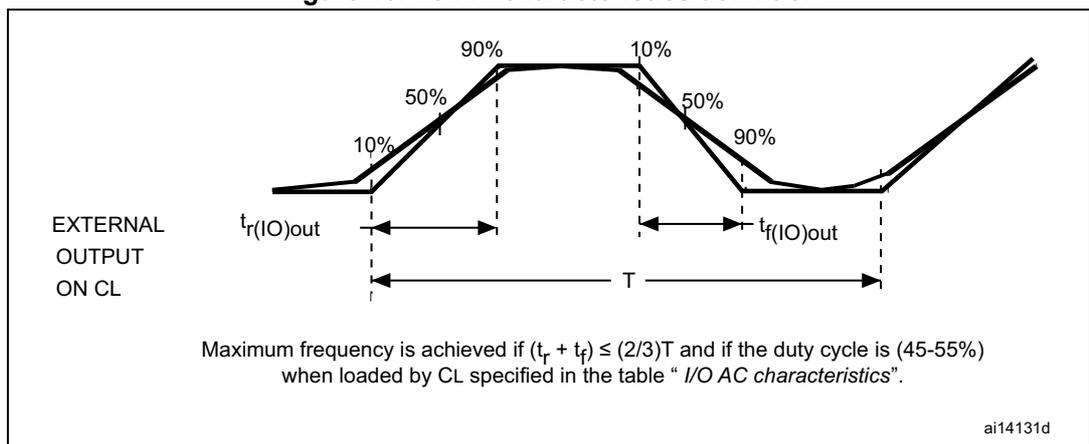
OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	MHz	
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	2		
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	8		
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	4		
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	3		
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.7 \text{ V to } 3.6 \text{ V}$	-	-	100	ns	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	25	MHz	
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	12.5		
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10		
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50		
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	20		
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	12.5		
		$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	10	ns
		$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6			
		$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	20			
		$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10			
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50 ⁽⁴⁾	MHz	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 ⁽⁴⁾		
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	25		
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50		
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5		
		$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6	ns
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4		
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10		
		$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	6			

Table 68. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 ⁽⁴⁾	MHz
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	180 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	100	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	72.5	
	$t_{f(\text{IO})\text{out}}/ t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	ns
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	6	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	7	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	2.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	3.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	4	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F76xxx and STM32F77xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in Figure 40.
4. For maximum frequencies above 50 MHz and $V_{DD} > 2.4 \text{ V}$, the compensation cell should be used.

Figure 40. I/O AC characteristics definition



5.3.21 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 66: I/O static characteristics](#)).

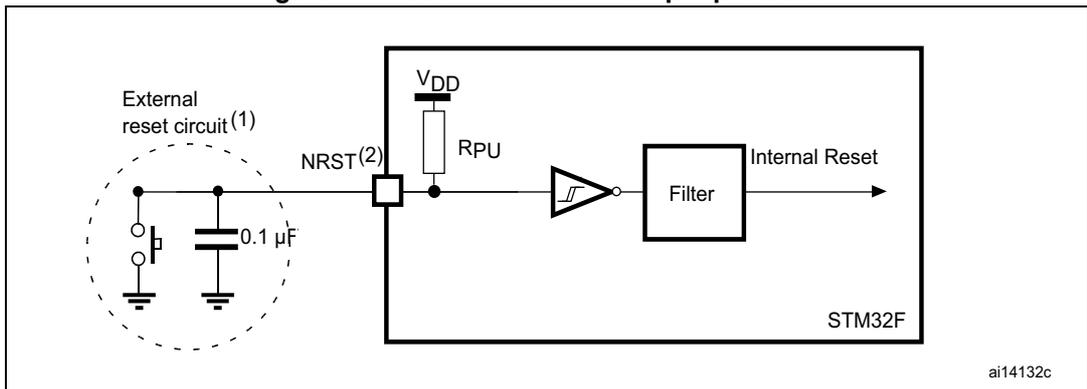
Unless otherwise specified, the parameters given in [Table 69](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 18](#).

Table 69. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}$ ⁽²⁾	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$ ⁽²⁾	NRST Input not filtered pulse	$V_{DD} > 2.7 V$	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 41. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets. 0.1 μF capacitor must be placed as close as possible to the chip.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 69](#). Otherwise the reset is not taken into account by the device.

5.3.22 TIM timer characteristics

The parameters given in [Table 70](#) are guaranteed by design.

Refer to [Section 5.3.20: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 70. TIMx characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions ⁽³⁾	Min	Max	Unit
t _{res(TIM)}	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, f _{TIMxCLK} = 216 MHz	1	-	t _{TIMxCLK}
		AHB/APBx prescaler>4, f _{TIMxCLK} = 100 MHz	1	-	t _{TIMxCLK}
f _{EXT}	Timer external clock frequency on CH1 to CH4	f _{TIMxCLK} = 216 MHz	0	f _{TIMxCLK} /2	MHz
Res _{TIM}	Timer resolution		-	16/32	bit
t _{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	t _{TIMxCLK}

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 216 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCLK, otherwise TIMxCLK = 4x PCLKx.

5.3.23 RTC characteristics

Table 71. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f _{PCLK1} /RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

5.3.24 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 72](#) are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 18](#).

Table 72. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DDA}	Power supply	V _{DDA} - V _{REF+} < 1.2 V	1.7 ⁽¹⁾	-	3.6	V
V _{REF+}	Positive reference voltage		1.7 ⁽¹⁾	-	V _{DDA}	V
f _{ADC}	ADC clock frequency	V _{DDA} = 1.7 ⁽¹⁾ to 2.4 V	0.6	15	18	MHz
		V _{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz

Table 72. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{TRIG}^{(2)}$	External trigger frequency	$f_{ADC} = 30$ MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range ⁽³⁾	-	0 (V_{SSA} or V_{REF} - tied to ground)	-	V_{REF+}	V
$R_{AIN}^{(2)}$	External input impedance	See Equation 1 for details	-	-	50	k Ω
$R_{ADC}^{(2)(4)}$	Sampling switch resistance	-	1.5	-	6	k Ω
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	4	7	pF
$t_{lat}^{(2)}$	Injection trigger conversion latency	$f_{ADC} = 30$ MHz	-	-	0.100	μ s
		-	-	-	3 ⁽⁵⁾	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	$f_{ADC} = 30$ MHz	-	-	0.067	μ s
		-	-	-	2 ⁽⁵⁾	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 30$ MHz	0.100	-	16	μ s
		-	3	-	480	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time	-	-	2	3	μ s
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	$f_{ADC} = 30$ MHz 12-bit resolution	0.50	-	16.40	μ s
		$f_{ADC} = 30$ MHz 10-bit resolution	0.43	-	16.34	μ s
		$f_{ADC} = 30$ MHz 8-bit resolution	0.37	-	16.27	μ s
		$f_{ADC} = 30$ MHz 6-bit resolution	0.30	-	16.20	μ s
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				
$f_S^{(2)}$	Sampling rate ($f_{ADC} = 36$ MHz, and $t_S = 3$ ADC cycles)	12-bit resolution Single ADC	-	-	2.4	MspS
		12-bit resolution Interleave Dual ADC mode	-	-	4.5	MspS
		12-bit resolution Interleave Triple ADC mode	-	-	7.2	MspS

Table 72. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VREF+}^{(2)}$	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	μA
$I_{VDDA}^{(2)}$	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

- V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 2.18.2: Internal reset OFF](#)).
- Guaranteed by characterization results.
- V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .
- R_{ADC} maximum value is given for $V_{DD}=1.7$ V, and minimum value for $V_{DD}=3.3$ V.
- For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 72](#).

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 73. ADC static accuracy at $f_{ADC} = 18$ MHz

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 18$ MHz $V_{DDA} = 1.7$ to 3.6 V $V_{REF} = 1.7$ to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	± 3	± 4	LSB
EO	Offset error		± 2	± 3	
EG	Gain error		± 1	± 3	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 2	± 3	

- Guaranteed by characterization results.

Table 74. ADC static accuracy at $f_{ADC} = 30$ MHz

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 30$ MHz, $R_{AIN} < 10$ k Ω , $V_{DDA} = 2.4$ to 3.6 V, $V_{REF} = 1.7$ to 3.6 V, $V_{DDA} - V_{REF} < 1.2$ V	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain error		± 1.5	± 4	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

- Guaranteed by characterization results.



Table 75. ADC static accuracy at $f_{ADC} = 36$ MHz

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 36$ MHz, $V_{DDA} = 2.4$ to 3.6 V, $V_{REF} = 1.7$ to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Guaranteed by characterization results.

Table 76. ADC dynamic accuracy at $f_{ADC} = 18$ MHz - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{ADC} = 18$ MHz $V_{DDA} = V_{REF+} = 1.7$ V Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		- 67	- 72	-	

1. Guaranteed by characterization results.

Table 77. ADC dynamic accuracy at $f_{ADC} = 36$ MHz - limited test conditions⁽¹⁾

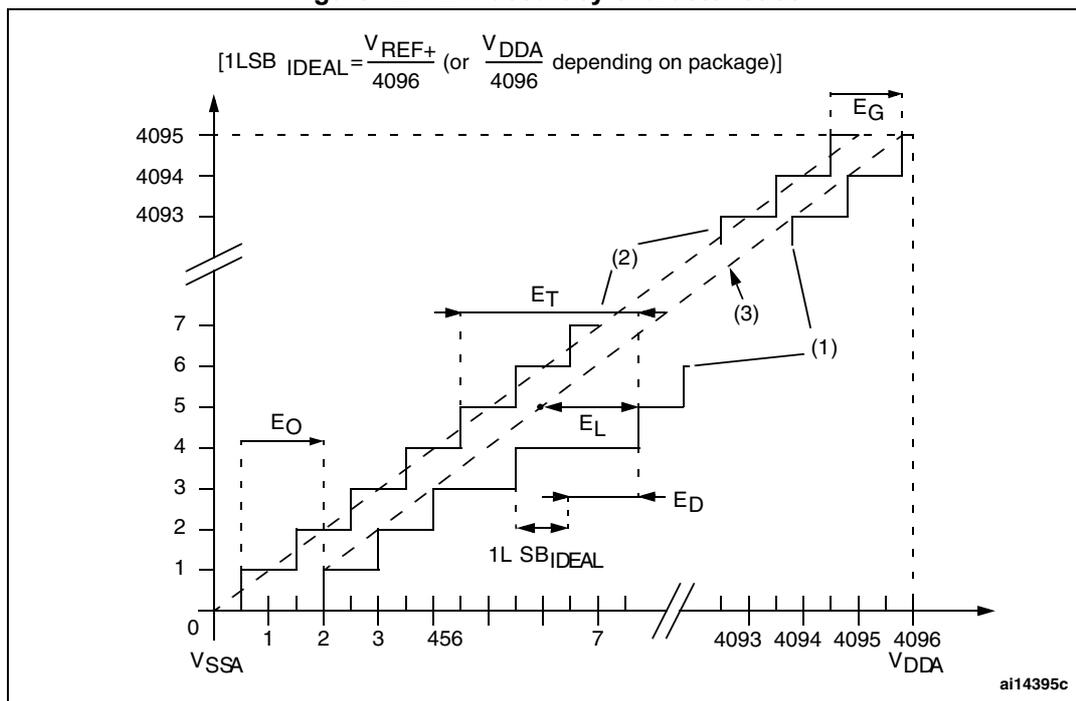
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{ADC} = 36$ MHz $V_{DDA} = V_{REF+} = 3.3$ V Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		- 70	- 72	-	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

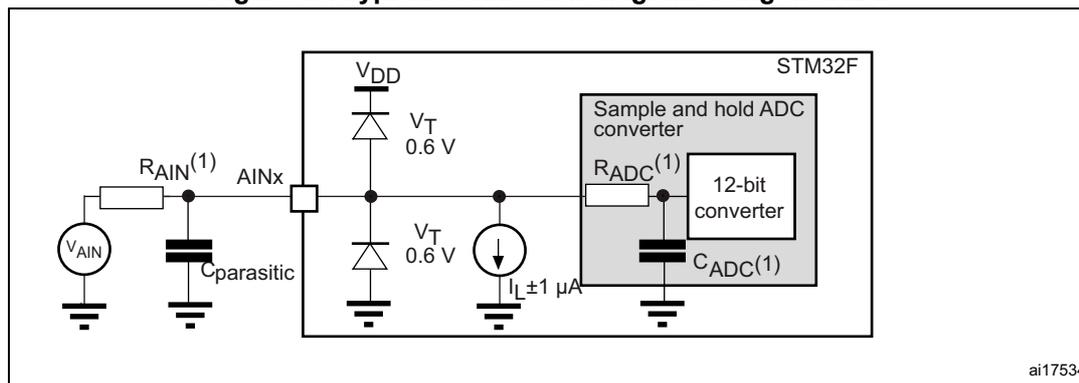
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.20](#) does not affect the ADC accuracy.

Figure 42. ADC accuracy characteristics



1. See also [Table 74](#).
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset Error: deviation between the first actual transition and the first ideal one.
 E_G = Gain Error: deviation between the last ideal transition and the last actual one.
 E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
 E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 43. Typical connection diagram using the ADC

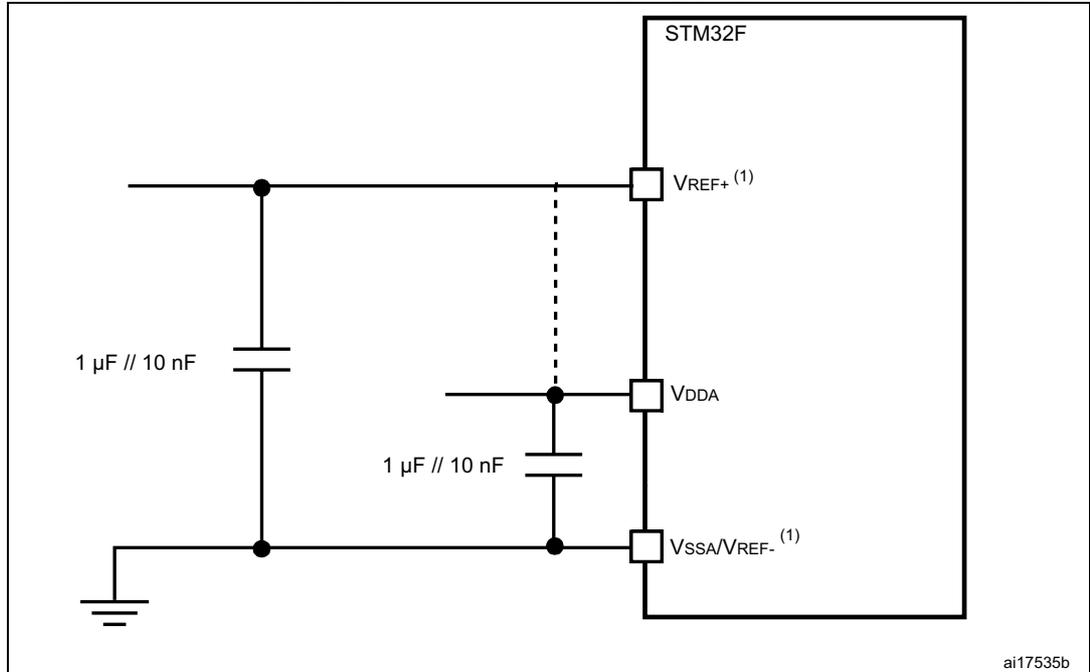


1. Refer to [Table 72](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

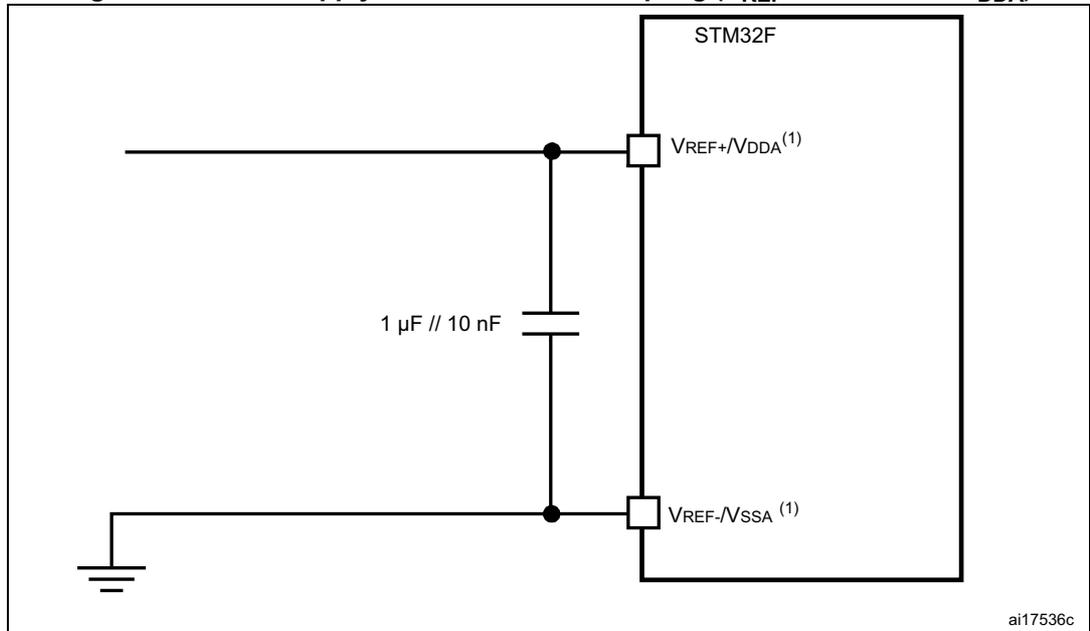
Power supply decoupling should be performed as shown in [Figure 44](#) or [Figure 45](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 44. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all packages except TFBGA100 whereas the V_{REF-} s available only on UFBGA176 and TFBGA216. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA} .

Figure 45. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all packages except TFBGA100 whereas the V_{REF-} s available only on UFBGA176 and TFBGA216. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA} .

5.3.25 Temperature sensor characteristics

Table 78. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}C$
Avg_Slope ⁽¹⁾	Average slope	-	2.5	-	mV/ $^{\circ}C$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}C$	-	0.76	-	V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S_temp}^{(2)}$	ADC sampling time when reading the temperature (1 $^{\circ}C$ accuracy)	10	-	-	μs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 79. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}C$, $V_{DDA} = 3.3 V$	0x1FF0 F44C - 0x1FF0 F44D
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}C$, $V_{DDA} = 3.3 V$	0x1FF0 F44E - 0x1FF0 F44F

5.3.26 V_{BAT} monitoring characteristics

Table 80. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	K Ω
Q	Ratio on V_{BAT} measurement	-	4	-	-
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$T_{S_vbat}^{(2)(2)}$	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	μs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.27 Reference voltage

The parameters given in [Table 81](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 18](#).

Table 81. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40^{\circ}C < T_A < +105^{\circ}C$	1.18	1.21	1.24	V
$T_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	10	-	-	μs
$V_{REFINT_s}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3V \pm 10mV$	-	3	5	mV

Table 81. internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{Coeff}}^{(2)}$	Temperature coefficient	-	-	30	50	ppm/°C
$t_{\text{START}}^{(2)}$	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 82. Internal reference voltage calibration values

Symbol	Parameter	Memory address
$V_{\text{REFIN_CAL}}$	Raw data acquired at temperature of 30 °C $V_{\text{DDA}} = 3.3 \text{ V}$	0x1FF0 F44A - 0x1FF0 F44B

5.3.28 DAC electrical characteristics

Table 83. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments	
V_{DDA}	Analog supply voltage	1.7 ⁽¹⁾	-	3.6	V	-	
$V_{\text{REF+}}$	Reference supply voltage	1.7 ⁽¹⁾	-	3.6	V	$V_{\text{REF+}} \leq V_{\text{DDA}}$	
V_{SSA}	Ground	0	-	0	V	-	
$R_{\text{LOAD}}^{(2)}$	Resistive load with buffer ON	Connected to V_{SSA}	5	-	-	kΩ	-
		Connected to V_{DDA}	25	-	-		
$R_{\text{O}}^{(2)}$	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ	
$C_{\text{LOAD}}^{(2)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).	
DAC_OUT min ⁽²⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{\text{REF+}} = 3.6 \text{ V}$ and (0x1C7) to (0xE38) at $V_{\text{REF+}} = 1.7 \text{ V}$	
DAC_OUT max ⁽²⁾	Higher DAC_OUT voltage with buffer ON	-	-	$V_{\text{DDA}} - 0.2$	V		
DAC_OUT min ⁽²⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.	
DAC_OUT max ⁽²⁾	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{\text{REF+}} - 1\text{LSB}$	V		

Table 83. DAC characteristics (continued)

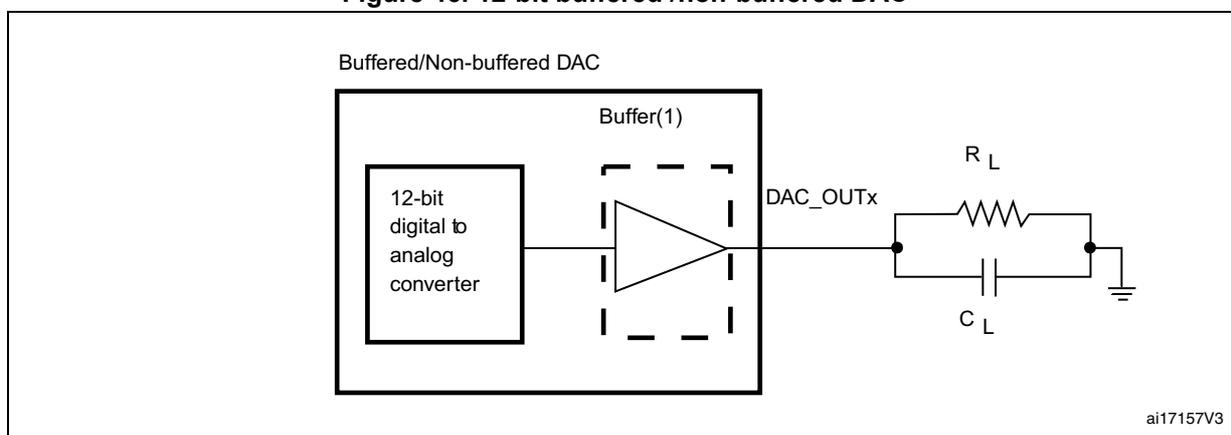
Symbol	Parameter	Min	Typ	Max	Unit	Comments
$I_{VREF+}^{(4)}$	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	μA	With no load, worst code (0x800) at $V_{REF+} = 3.6 V$ in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at $V_{REF+} = 3.6 V$ in terms of DC consumption on the inputs
$I_{DDA}^{(4)}$	DAC DC V_{DDA} current consumption in quiescent mode ⁽³⁾	-	280	380	μA	With no load, middle code (0x800) on the inputs
		-	475	625	μA	With no load, worst code (0xF1C) at $V_{REF+} = 3.6 V$ in terms of DC consumption on the inputs
DNL ⁽⁴⁾	Differential non linearity Difference between two consecutive code-1LSB)	-	-	± 0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	± 2	LSB	Given for the DAC in 12-bit configuration.
INL ⁽⁴⁾	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	± 1	LSB	Given for the DAC in 10-bit configuration.
		-	-	± 4	LSB	Given for the DAC in 12-bit configuration.
Offset ⁽⁴⁾	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	± 10	mV	Given for the DAC in 12-bit configuration
		-	-	± 3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6 V$
		-	-	± 12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6 V$
Gain error ⁽⁴⁾	Gain error	-	-	± 0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}^{(4)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 4LSB$)	-	3	6	μs	$C_{LOAD} \leq 50 pF$, $R_{LOAD} \geq 5 k\Omega$
THD ⁽⁴⁾	Total Harmonic Distortion Buffer ON	-	-	-	dB	$C_{LOAD} \leq 50 pF$, $R_{LOAD} \geq 5 k\Omega$
Update rate ⁽²⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50 pF$, $R_{LOAD} \geq 5 k\Omega$

Table 83. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$t_{WAKEUP}^{(4)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μs	$C_{LOAD} \leq 50 \text{ pF}$, $R_{LOAD} \geq 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ ⁽²⁾	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-67	-40	dB	No R_{LOAD} , $C_{LOAD} = 50 \text{ pF}$

- V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 2.18.2: Internal reset OFF).
- Guaranteed by design.
- The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
- Guaranteed by characterization results.

Figure 46. 12-bit buffered /non-buffered DAC



- The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.29 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0410 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

Table 84. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON DNF=0	8	
			Analog filter OFF DNF=1	9	
		Fast-mode Plus	Analog filter ON DNF=0	16	
			Analog filter OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.
- The 20mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

$$Tr(SDA/SCL)=0.8473 \times R_p \times C_{load}$$

$$R_p(\text{min})= (V_{DD}-V_{OL}(\text{max}))/I_{OL}(\text{max})$$

Where R_p is the I2C lines pull-up. Refer to [Section 5.3.20: I/O port characteristics](#) for the I2C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to [Table 85](#) for the analog filter characteristics:

Table 85. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t _{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	70 ⁽³⁾	ns

1. Guaranteed by characterization results.
2. Spikes with widths below t_{AF(min)} are filtered.
3. Spikes with widths above t_{AF(max)} are not filtered.

SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 86](#) for the SPI interface are derived from tests performed under the ambient temperature, f_{PLCKx} frequency and V_{DD} supply voltage conditions summarized in [Table 18](#), with the following configuration:

- Output speed is set to $\text{OSPEEDRy}[1:0] = 11$
- Capacitive load $C = 30 \text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{\text{DD}}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 86. SPI dynamic characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{\text{c(SCK)}}$	SPI clock frequency	Master mode SPI1,4,5,6 $2.7 \leq V_{\text{DD}} \leq 3.6$	-	-	54 ⁽²⁾	MHz
		Master mode SPI1,4,5,6 $1.71 \leq V_{\text{DD}} \leq 3.6$			27	
		Master transmitter mode SPI1,4,5,6 $1.71 \leq V_{\text{DD}} \leq 3.6$			54	
		Slave receiver mode SPI1,4,5,6 $1.71 \leq V_{\text{DD}} \leq 3.6$			54	
		Slave mode transmitter/full duplex SPI1,4,5,6 $2.7 \leq V_{\text{DD}} \leq 3.6$			50 ⁽³⁾	
		Slave mode transmitter/full duplex SPI1,4,5,6 $1.71 \leq V_{\text{DD}} \leq 3.6$			37 ⁽³⁾	
		Master & Slave mode SPI2,3 $1.71 \leq V_{\text{DD}} \leq 3.6$			27	
$t_{\text{su(NSS)}}$	NSS setup time	Slave mode, SPI presc = 2	$4 \cdot T_{\text{PLCK}}$	-	-	ns
$t_{\text{h(NSS)}}$	NSS hold time	Slave mode, SPI presc = 2	$2 \cdot T_{\text{PLCK}}$	-	-	
$t_{\text{w(SCKH)}}$ $t_{\text{w(SCKL)}}$	SCK high and low time	Master mode	$T_{\text{PLCK}} - 2$	T_{PLCK}	$T_{\text{PLCK}} + 2$	

Table 86. SPI dynamic characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tsu(MI)	Data input setup time	Master mode	4 g ⁽⁴⁾	-	-	ns
tsu(SI)		Slave mode	4.5	-	-	
th(MI)	Data input hold time	Master mode	3 0 ⁽⁴⁾	-	-	
th(SI)		Slave mode	2	-	-	
ta(SO)	Data output access time	Slave mode	7	-	21	
t _{dis} (SO)	Data output disable time	Slave mode	5	-	12	
tv(SO)	Data output valid time	Slave mode 2.7≤VDD≤3.6V	-	6.5	10	
		Slave mode 1.71≤VDD≤3.6V	-	6.5	13.5	
tv(MO)		Master mode	-	2	6	
th(SO)	Data output hold time	Slave mode 1.71≤VDD≤3.6V	4.5	-	-	
th(MO)		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Excepting SPI1 with SCK IO pin mapped on PA5. In this configuration, Maximum achievable frequency is 40MHz.
3. Maximum Frequency of Slave Transmitter is determined by sum of Tv(SO) and Tsu(MI) intervals which has to fit into SCK level phase preceding the SCK sampling edge. This value can be achieved when it communicates with a Master having Tsu(MI)=0 while signal Duty(SCK)=50%.
4. Only for SPI6.

Figure 47. SPI timing diagram - slave mode and CPHA = 0

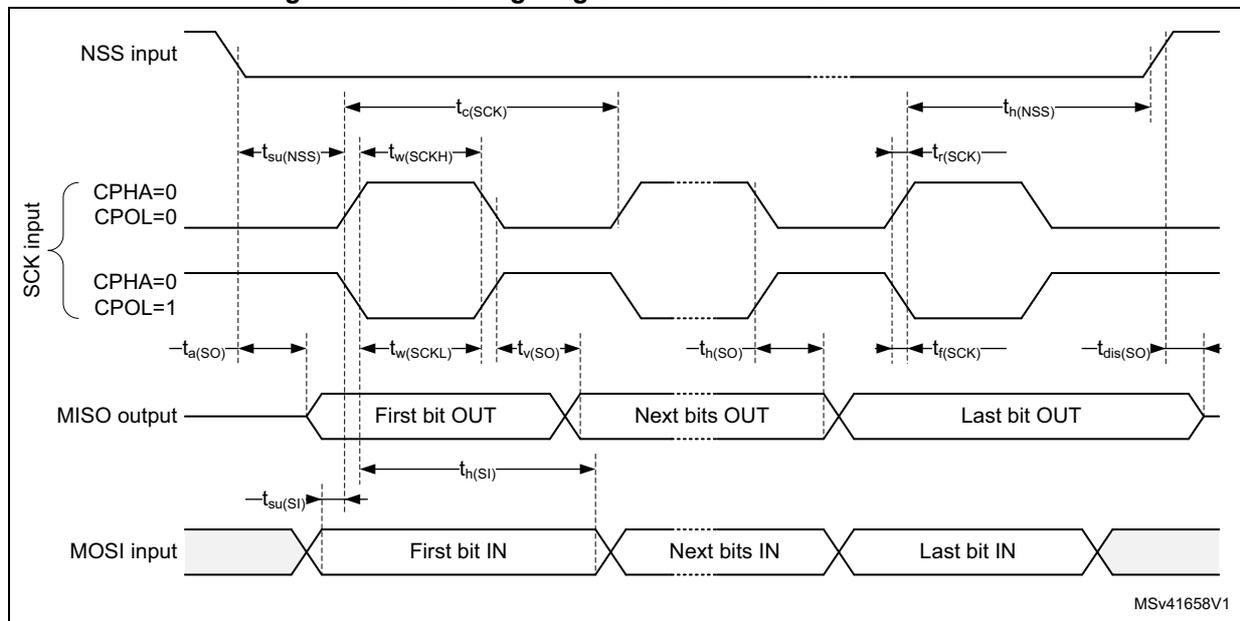
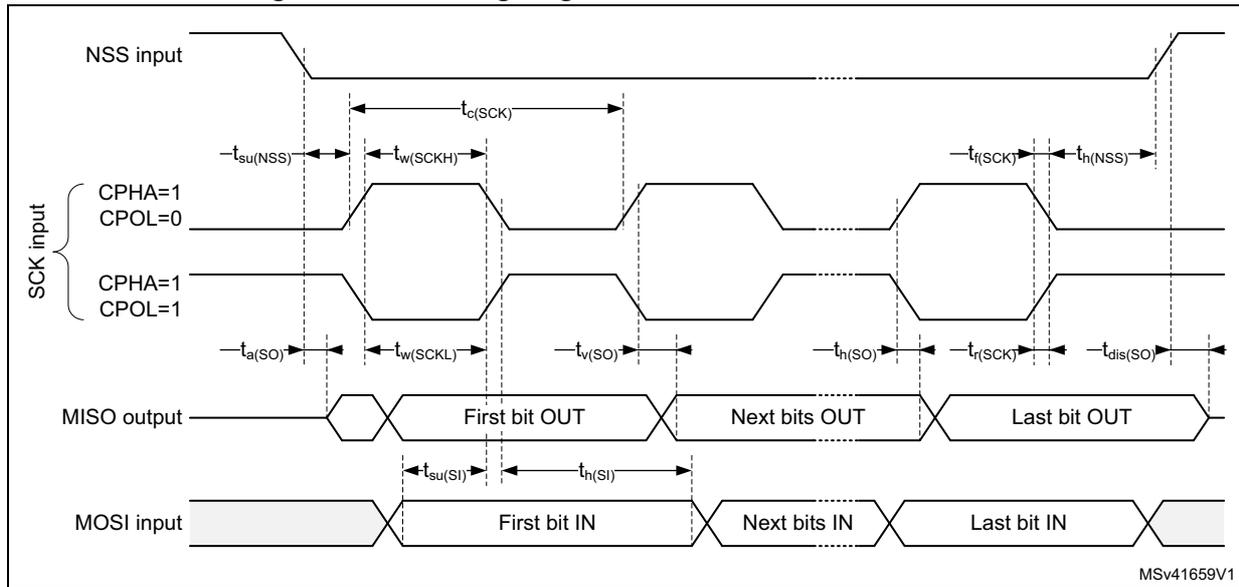
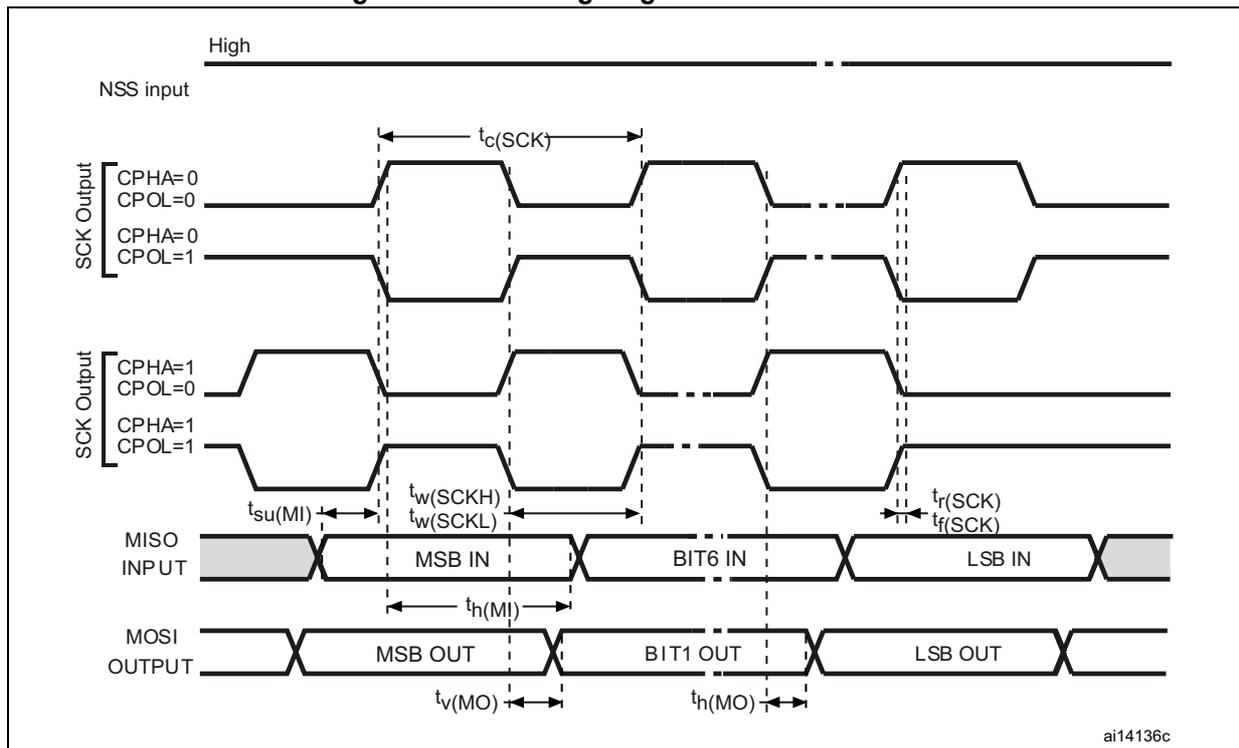


Figure 48. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾



1. Measurement points are done at 0.5V_{DD} and with external C_L = 30 pF.

Figure 49. SPI timing diagram - master mode⁽¹⁾



1. Measurement points are done at 0.5V_{DD} and with external C_L = 30 pF.

I²S interface characteristics

Unless otherwise specified, the parameters given in [Table 87](#) for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 18](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CK, SD, WS).

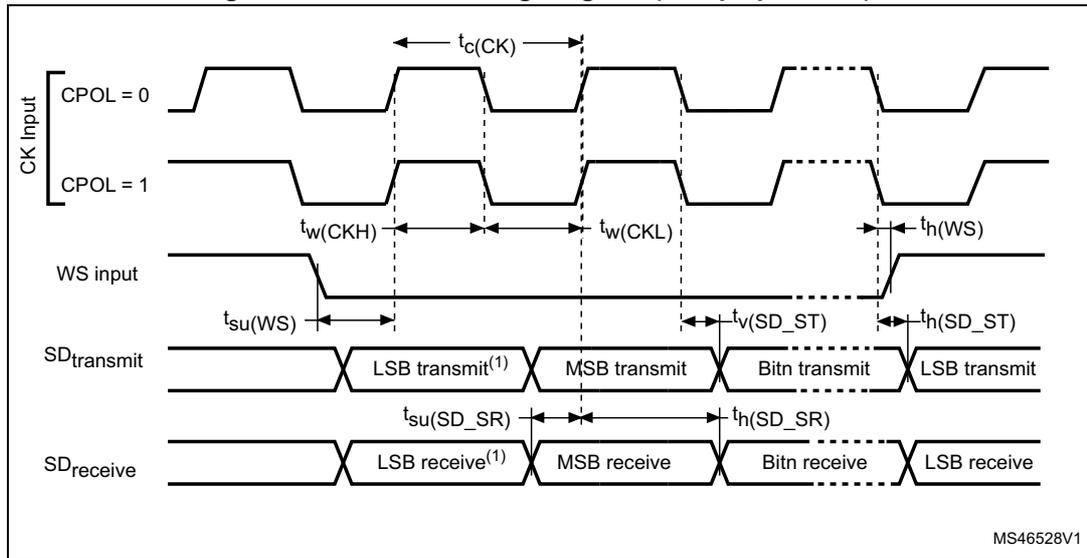
Table 87. I²S dynamic characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256x F_S ⁽²⁾	MHz
f_{CK}	I2S clock frequency	Master data	-	64x F_S	MHz
		Slave data	-	64x F_S	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD_SR)}$		Slave receiver	2.5	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD_SR)}$		Slave receiver	2	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.
2. The maximum value of 256x F_S is 49.152 MHz (APB1 maximum frequency).

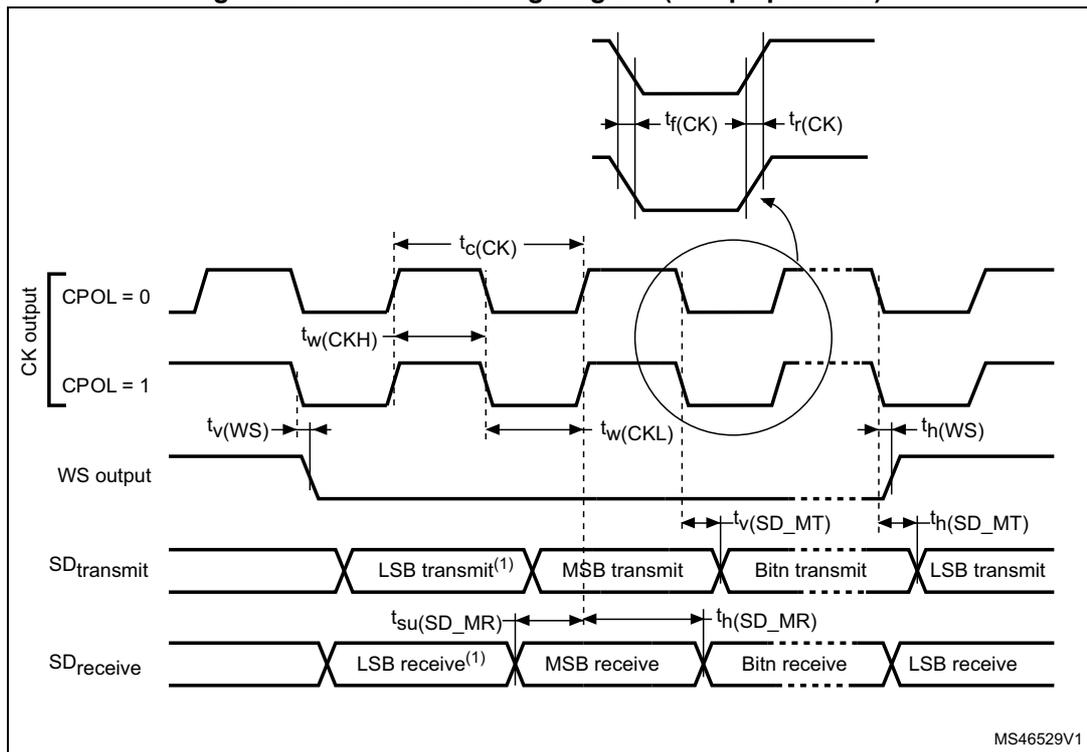
Note: Refer to RM0410 reference manual I2S section for more details about the sampling frequency (F_S). f_{MCK} , f_{CK} , and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of $(I2SDIV)/(2*I2SDIV+ODD)$ and a maximum value of $(I2SDIV+ODD)/(2*I2SDIV+ODD)$. F_S maximum value is supported for each mode/condition.

Figure 50. I²S slave timing diagram (Philips protocol)⁽¹⁾



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 51. I²S master timing diagram (Philips protocol)⁽¹⁾



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

JTAG/SWD characteristics

Unless otherwise specified, the parameters given in [Table 88](#) for JTAG/SWD are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage conditions summarized in [Table 18](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5V_{DD}

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 88. Dynamics characteristics: JTAG characteristics

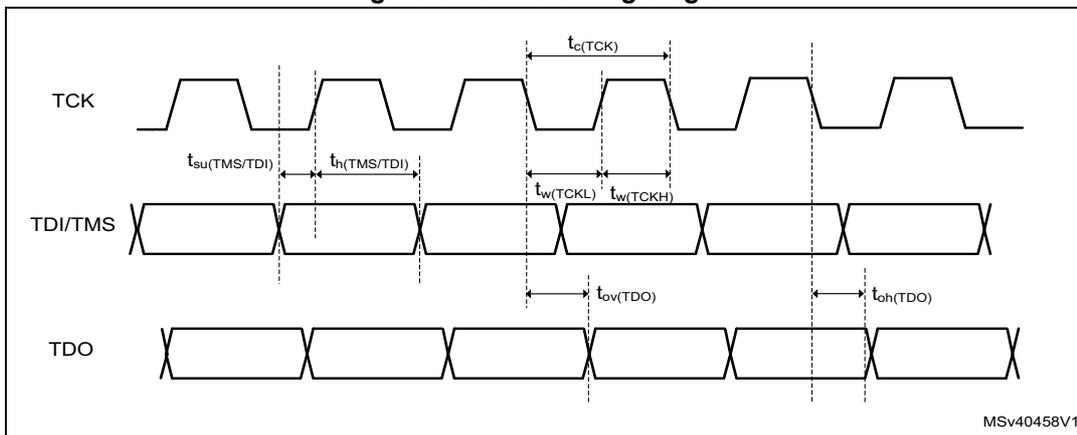
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	TCK clock frequency	2.7V <VDD< 3.6V	-	-	40	MHz
$1/t_c(TCK)$		1.71 <VDD< 3.6V	-	-	35	
$t_w(TCKH)$	SCK high and low time	-	$T_{PCLK} - 1$	T_{PCLK}	$T_{PCLK} + 1$	ns
$t_w(TCKL)$						
$t_{su}(TMS)$	TMS input setup time	-	3	-	-	
$t_h(TMS)$	TMS input hold time	-	0	-	-	
$t_{su}(TDI)$	TDI input setup time	-	0.5	-	-	
$t_h(TDI)$	TDI input hold time	-	2	-	-	
$t_{ov}(TDO)$	TDO output valid time	2.7V <VDD< 3.6V	-	9	11	
		1.71 <VDD< 3.6V	-	9	13	
$t_{oh}(TDO)$	TDO output hold time	-	7.5	-	-	

Table 89. Dynamics characteristics: SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	$2.7V < VDD < 3.6V$	-	-	80	MHz
$1/t_{c(SWCLK)}$		$1.71 < VDD < 3.6V$	-	-	50	
$t_{w(SWCLKH)}$ $t_{w(SWCLKL)}$	SCK high and low time	-	$T_{PCLK} - 1$	T_{PCLK}	$T_{PCLK} + 1$	ns
$t_{su(SWDIO)}$	SWDIO input setup time	-	3.5	-	-	
$t_{h(SWDIO)}$	SWDIO input hold time	-	0	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	$2.7V < VDD < 3.6V$	-	11	12	
		$1.71 < VDD < 3.6V$	-	11	16.5	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	9	-	-	

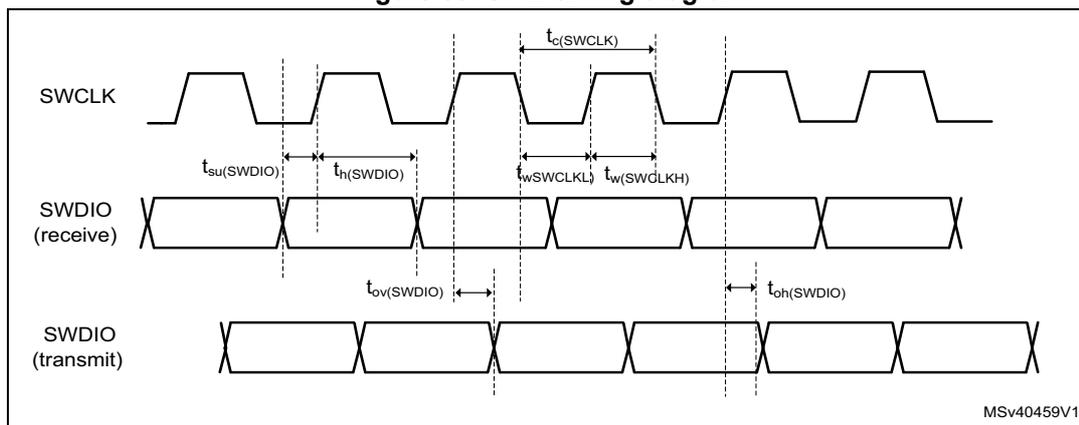
JTAG/SWD timing diagrams

Figure 52. JTAG timing diagram



MSv40458V1

Figure 53. SWD timing diagram



SAI characteristics:

Unless otherwise specified, the parameters given in [Table 90](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in [Table 18](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 90. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256 x 8K	256xFs	MHz
F_{CK}	SAI clock frequency ⁽²⁾	Master data: 32 bits	-	128xFs ⁽³⁾	MHz
		Slave data: 32 bits	-	128xFs	
$t_{v(FS)}$	FS valid time	Master mode $2.7 \leq V_{DD} \leq 3.6V$	-	15	ns
		Master mode $1.71 \leq V_{DD} \leq 3.6V$	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	7	-	
$t_h(FS)$	FS hold time	Master mode	1	-	
		Slave mode	1	-	
$t_{su}(SD_A_MR)$	Data input setup time	Master receiver	3	-	
$t_{su}(SD_B_SR)$		Slave receiver	3.5	-	
$t_h(SD_A_MR)$	Data input hold time	Master receiver	5	-	
$t_h(SD_B_SR)$		Slave receiver	1	-	

Table 90. SAI characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) $2.7 \leq VDD \leq 3.6V$	-	12	ns
		Slave transmitter (after enable edge) $1.71 \leq VDD \leq 3.6V$	-	20	
$t_{h(SD_B_MT)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{v(SD_MT_A)}$	Data output valid time	Master transmitter (after enable edge) $2.7 \leq VDD \leq 3.6V$	-	15	
		Master transmitter (after enable edge) $1.71 \leq VDD \leq 3.6V$	-	20	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With $F_S=192kHz$.

Figure 54. SAI master timing waveforms

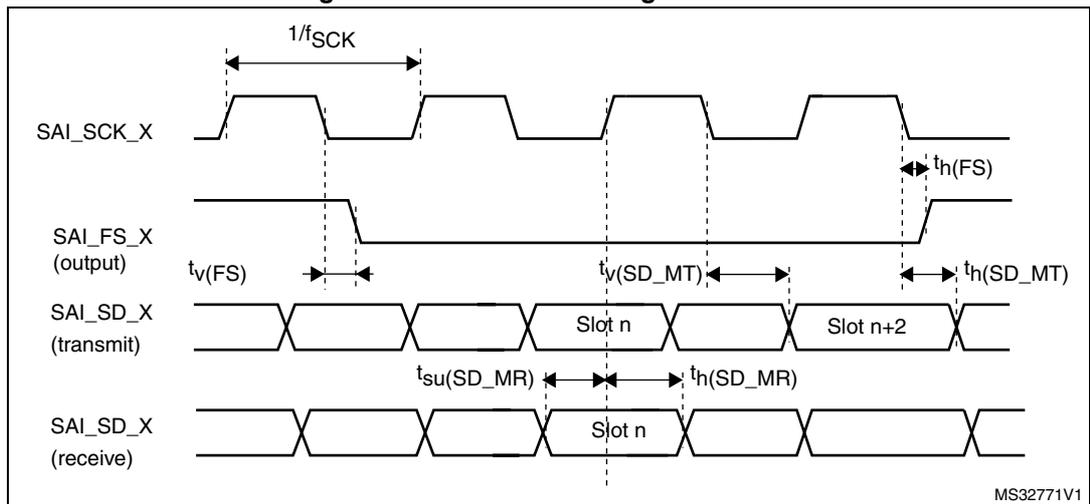
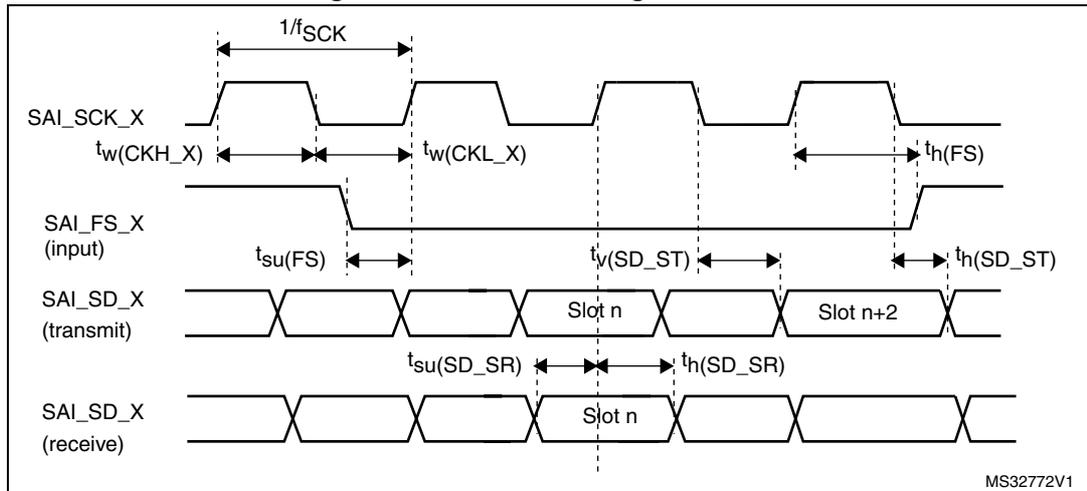


Figure 55. SAI slave timing waveforms



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 91. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}^{(1)}$	USB OTG full speed transceiver startup time	1	μs

1. Guaranteed by design.

Table 92. USB OTG full speed DC electrical characteristics

Symbol	Parameter	Conditions	Min. (1)	Typ.	Max. (1)	Unit	
Input levels	V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0 ⁽²⁾	-	3.6	V
	$V_{DI}^{(3)}$	Differential input sensitivity	$I(USB_FS_DP/DM, USB_HS_DP/DM)$	0.2	-	-	V
	$V_{CM}^{(3)}$	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	$V_{SE}^{(3)}$	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 k Ω to 3.6 V ⁽⁴⁾	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 k Ω to $V_{SS}^{(4)}$	2.8	-	3.6	

Table 92. USB OTG full speed DC electrical characteristics (continued)

Symbol	Parameter	Conditions	Min. (1)	Typ.	Max. (1)	Unit
R _{PD}	PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	V _{IN} = V _{DD}	17	21	24	kΩ
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		2.4	5.2	8	
R _{PU}	PA12, PB15 (USB_FS_DP, USB_HS_DP)	V _{IN} = V _{SS}	1.5	1.8	2.1	
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V _{IN} = V _{SS}	0.55	0.95	1.35	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DDUSB} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 μA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

Figure 56. USB OTG full speed timings: definition of data signal rise and fall time

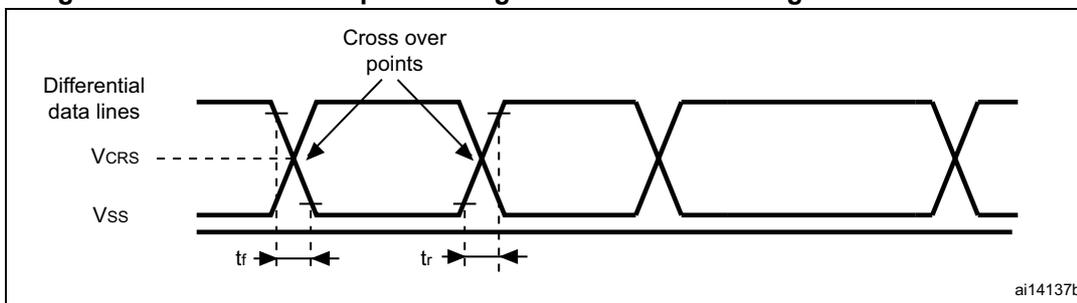


Table 93. USB OTG full speed electrical characteristics⁽¹⁾

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t _r	Rise time ⁽²⁾	C _L = 50 pF	4	20	ns
t _f	Fall time ⁽²⁾	C _L = 50 pF	4	20	ns
t _{rfm}	Rise/ fall time matching	t _r /t _f	90	110	%
V _{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z _{DRV}	Output driver impedance ⁽³⁾	Driving high or low	28	44	Ω

1. Guaranteed by design.

- Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
- No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

USB high speed (HS) characteristics

Unless otherwise specified, the parameters given in [Table 96](#) for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 95](#) and V_{DD} supply voltage conditions summarized in [Table 94](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11, unless otherwise specified
- Capacitive load C = 20 pF, unless otherwise specified
- Measurement points are done at CMOS levels: $0.5V_{\text{DD}}$.

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output characteristics.

Table 94. USB HS DC electrical characteristics

Symbol	Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level	V_{DD} USB OTG HS operating voltage	1.7	3.6	V

- All the voltages are measured from the local ground potential.

Table 95. USB HS clock timing parameters⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit	
-	f_{HCLK} value to guarantee proper operation of USB HS interface	30	-	-	MHz	
$F_{\text{START_8BIT}}$	Frequency (first transition) 8-bit $\pm 10\%$	54	60	66	MHz	
F_{STEADY}	Frequency (steady state) ± 500 ppm	59.97	60	60.03	MHz	
$D_{\text{START_8BIT}}$	Duty cycle (first transition) 8-bit $\pm 10\%$	40	50	60	%	
D_{STEADY}	Duty cycle (steady state) ± 500 ppm	49.975	50	50.025	%	
t_{STEADY}	Time to reach the steady state frequency and duty cycle after the first transition	-	-	1.4	ms	
$t_{\text{START_DEV}}$	Clock startup time after the de-assertion of SuspendM	Peripheral	-	-	5.6	ms
$t_{\text{START_HOST}}$		Host	-	-	-	
t_{PREP}	PHY preparation time after the first transition of the input clock	-	-	-	μs	

- Guaranteed by design.

Figure 57. ULPI timing diagram

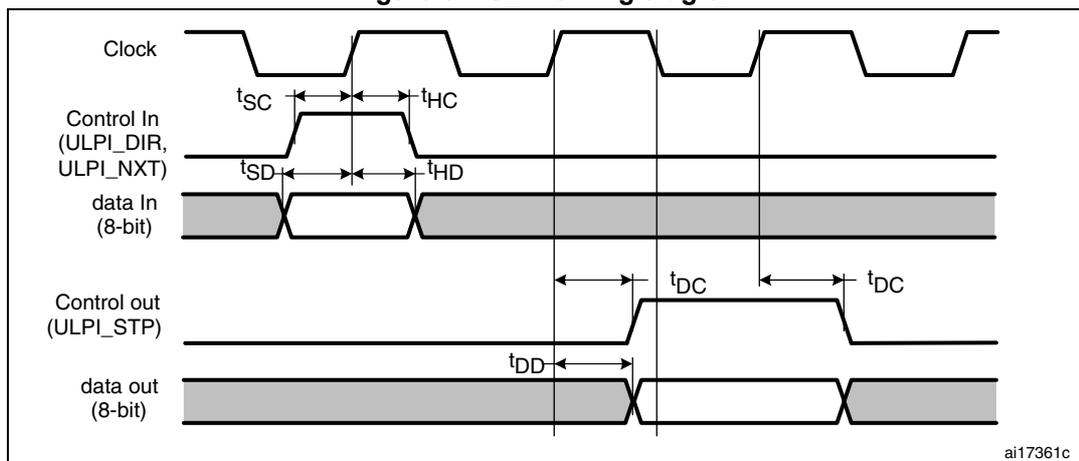


Table 96. Dynamic characteristics: USB ULPI⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	2	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	1.5	-	-	
t_{SD}	Data in setup time	-	2	-	-	
t_{HD}	Data in hold time	-	1	-	-	
t_{DC}/t_{DD}	Data/control output delay	$2.7\text{ V} < V_{DD} < 3.6\text{ V},$ $C_L = 20\text{ pF}$	-	6.5	8	ns
		$1.7\text{ V} < V_{DD} < 3.6\text{ V},$ $C_L = 15\text{ pF}$	-	6.5	11	

1. Guaranteed by characterization results.

Ethernet characteristics

Unless otherwise specified, the parameters given in [Table 97](#), [Table 98](#) and [Table 99](#) for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 18](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 20\text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output characteristics.

[Table 97](#) gives the list of Ethernet MAC signals for the SMI (station management interface) and [Figure 58](#) shows the corresponding timing diagram.

Figure 58. Ethernet SMI timing diagram

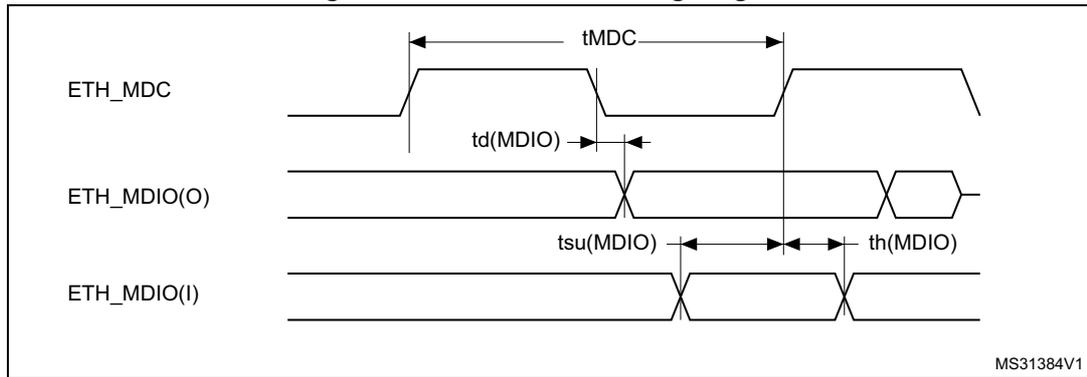


Table 97. Dynamics characteristics: Ethernet MAC signals for SMI⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	400	400	403	ns
$T_d(MDIO)$	Write data valid time	$T_{HCLK} + 1$	$T_{HCLK} + 1.5$	$T_{HCLK} + 3$	
$t_{su}(MDIO)$	Read data setup time	12.5	-	-	
$t_h(MDIO)$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Table 98 gives the list of Ethernet MAC signals for the RMII and Figure 59 shows the corresponding timing diagram.

Figure 59. Ethernet RMII timing diagram

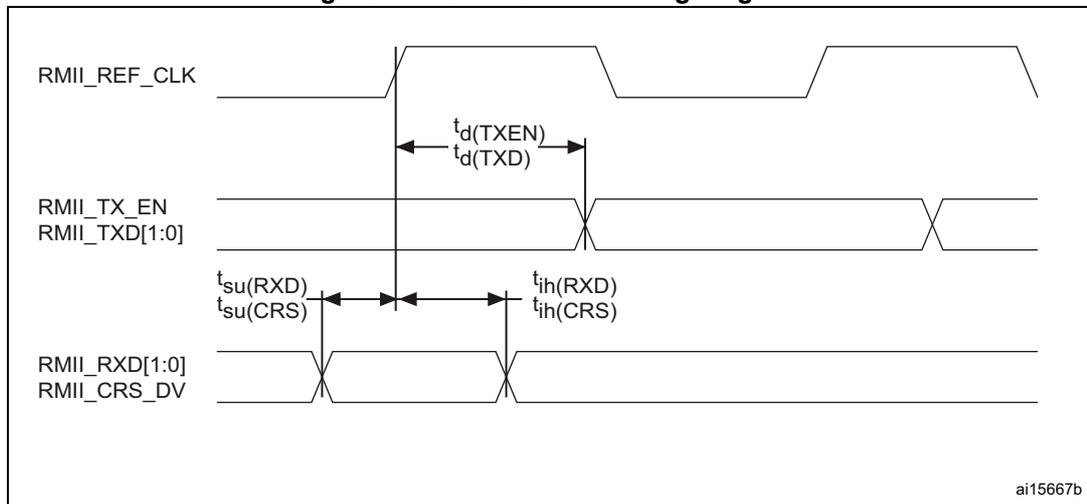


Table 98. Dynamics characteristics: Ethernet MAC signals for RMII⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su}(RXD)$	Receive data setup time	1	-	-	ns
$t_{ih}(RXD)$	Receive data hold time	2	-	-	
$t_{su}(CRS)$	Carrier sense setup time	2	-	-	
$t_{ih}(CRS)$	Carrier sense hold time	2	-	-	
$t_d(TXEN)$	Transmit enable valid delay time	7.5	8	12	
$t_d(TXD)$	Transmit data valid delay time	7	7.5	12.5	

1. Guaranteed by characterization results.

Table 99 gives the list of Ethernet MAC signals for MII and Figure 59 shows the corresponding timing diagram.

Figure 60. Ethernet MII timing diagram

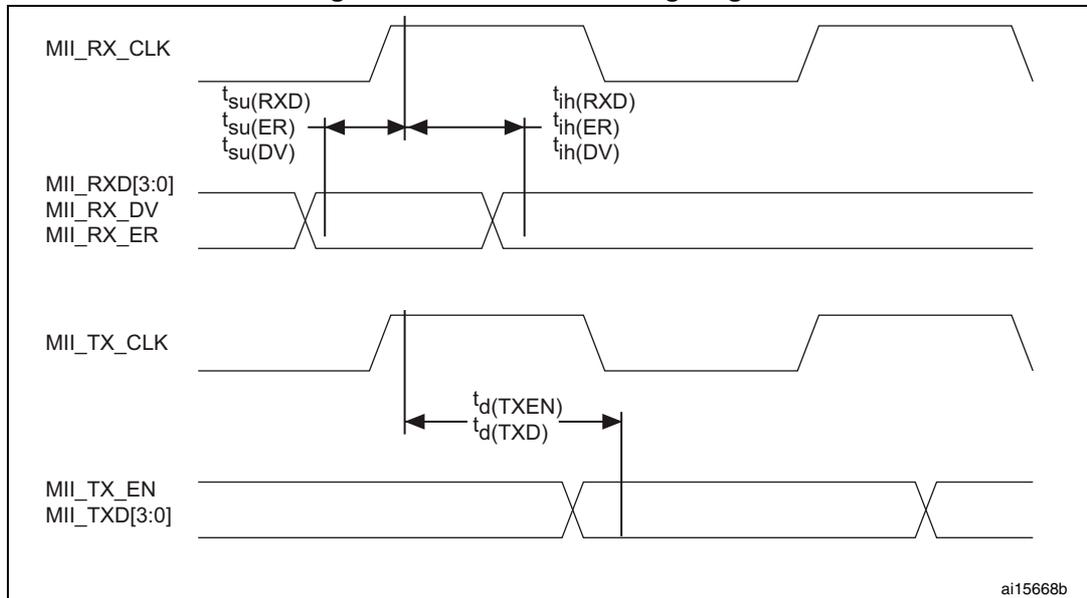


Table 99. Dynamics characteristics: Ethernet MAC signals for MII⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su}(RXD)$	Receive data setup time	1	-	-	ns
$t_{ih}(RXD)$	Receive data hold time	2.5	-	-	
$t_{su}(DV)$	Data valid setup time	1.5	-	-	
$t_{ih}(DV)$	Data valid hold time	0.5	-	-	
$t_{su}(ER)$	Error setup time	2.5	-	-	
$t_{ih}(ER)$	Error hold time	0.5	-	-	
$t_d(TXEN)$	Transmit enable valid delay time	10	8	13	
$t_d(TXD)$	Transmit data valid delay time	9	7.5	13	

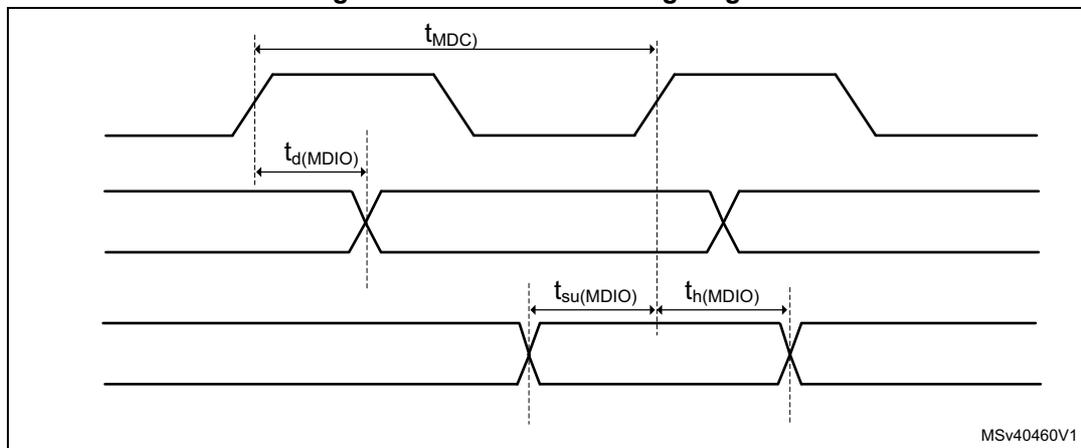
- 1. Guaranteed by characterization results.

Table 100. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management Data clock	-	-	40	MHz
$t_{d(MDIO)}$	Management Data input/output output valid time	7	8	20	ns
$t_{su(MDIO)}$	Management Data input/output setup time	4	-	-	
$t_h(MDIO)$	Management Data input/output hold time	1	-	-	

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$

Figure 61. MDIO Slave timing diagram



CAN (controller area network) interface

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.30 FMC characteristics

Unless otherwise specified, the parameters given in [Table 101](#) to [Table 114](#) for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in [Table 18](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output characteristics.

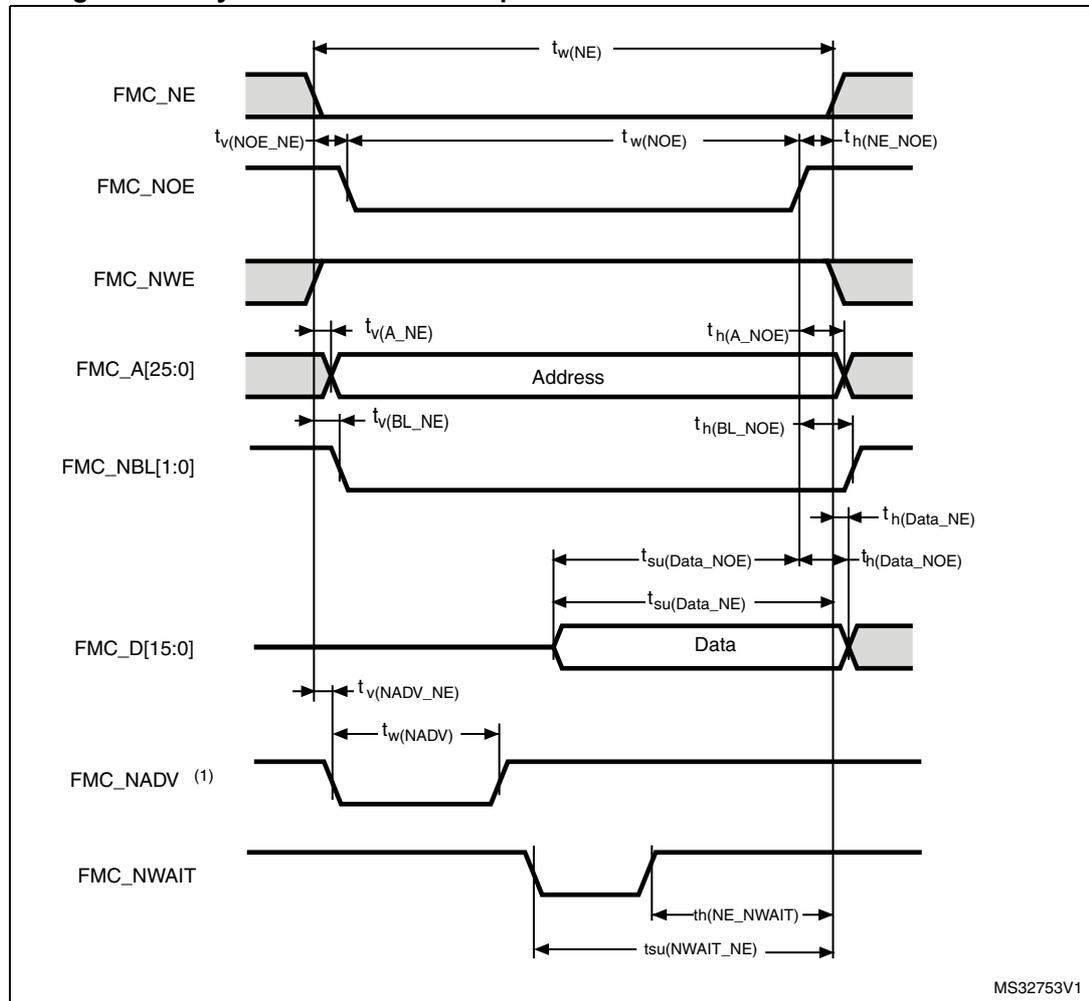
Asynchronous waveforms and timings

[Figure 62](#) through [Figure 65](#) represent asynchronous waveforms and [Table 101](#) through [Table 108](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load CL = 30 pF

In all timing tables, the T_{HCLK} is the HCLK clock period

Figure 62. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 101. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} - 1$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} - 1$	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK} + 1$	

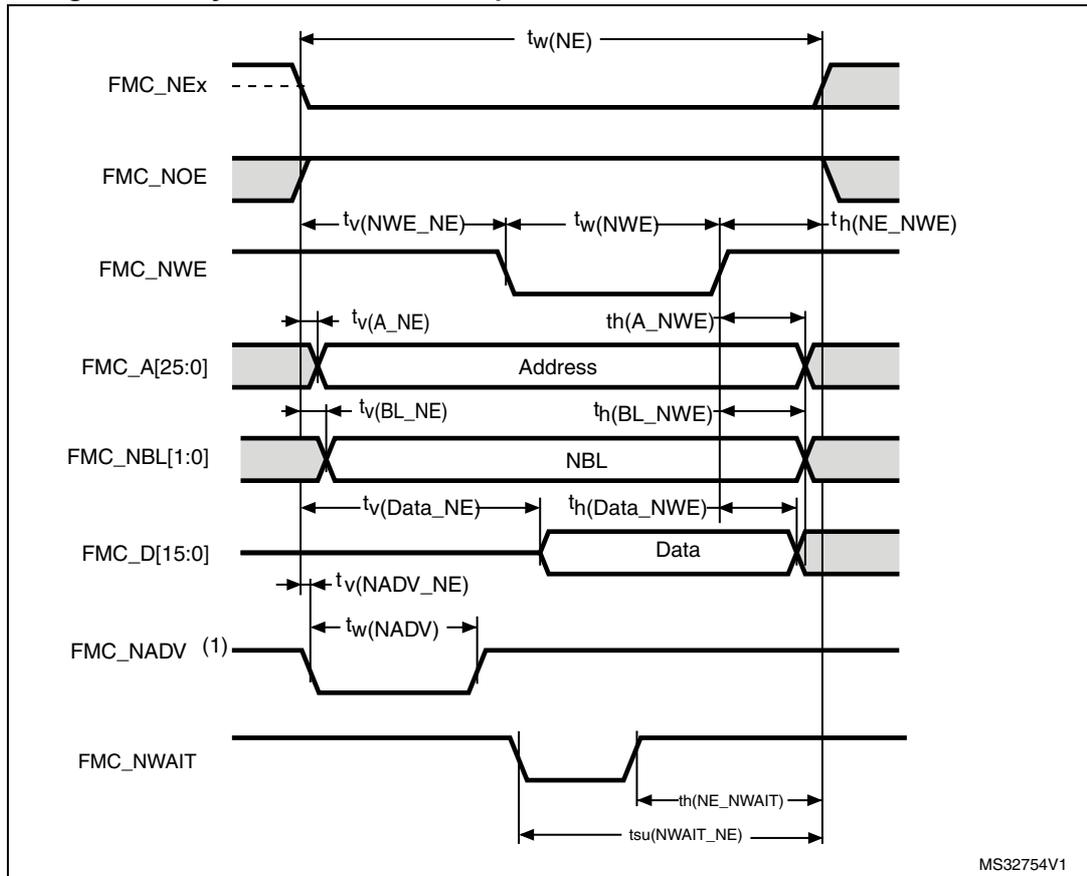
1. $C_L = 30$ pF.
2. Guaranteed by characterization results.

Table 102. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK} + 1$	$7T_{HCLK} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{HCLK} - 0.5$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 1$	-	

1. Guaranteed by characterization results.

Figure 63. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



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1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 103. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{HCLK} - 1.5$	$T_{HCLK} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK} - 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 0.5$	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK} + 2$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK} + 1$	

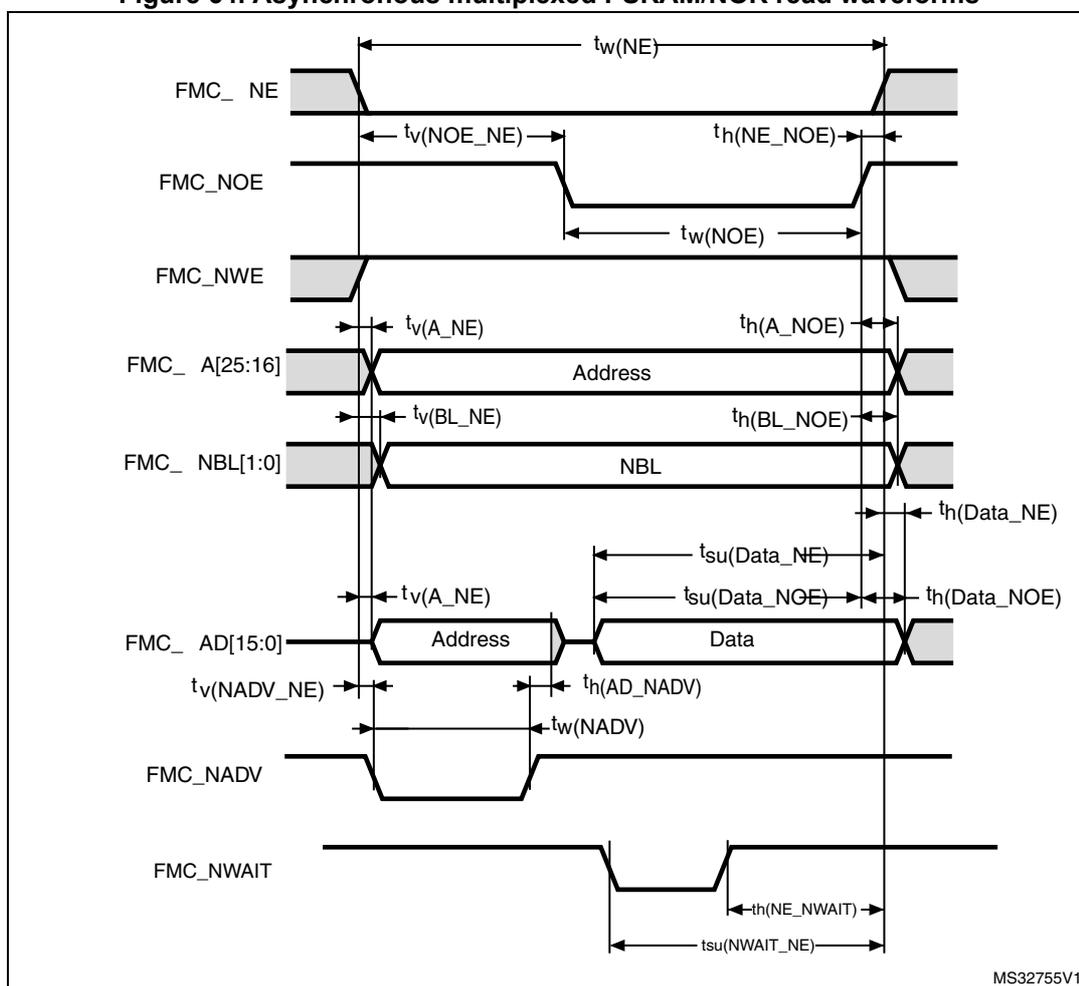
1. Guaranteed by characterization results.

Table 104. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} - 1$	$8T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK} - 1.5$	$6T_{HCLK} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} - 1$	-	
$t_h(NE_NWAIT)$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 2$	-	

1. Guaranteed by characterization results.

Figure 64. Asynchronous multiplexed PSRAM/NOR read waveforms



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Table 105. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK}$	$2T_{HCLK} + 0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} + 0.5$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} - 1$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK} - 1$	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

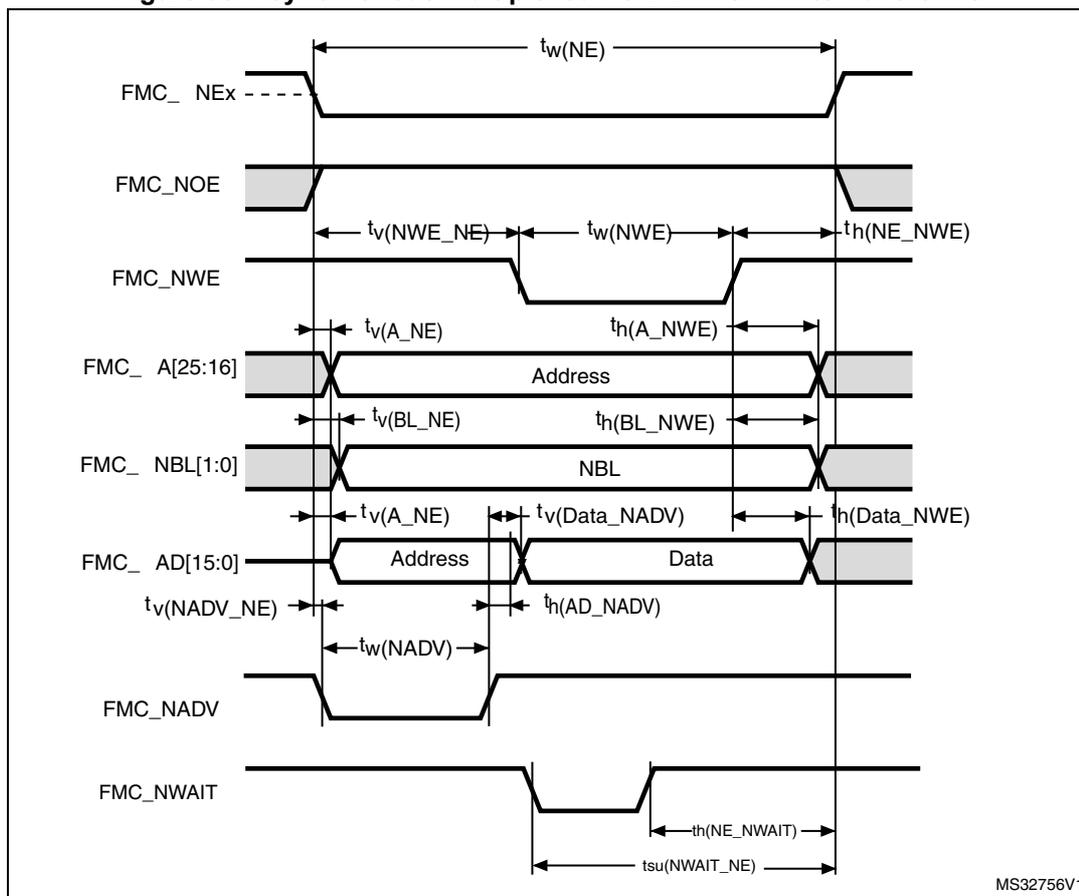
1. Guaranteed by characterization results.

Table 106. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} - 1$	$8T_{HCLK} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1.5$	$5T_{HCLK} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 1$	-	

1. Guaranteed by characterization results.

Figure 65. Asynchronous multiplexed PSRAM/NOR write waveforms



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Table 107. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK} - 1$	$4T_{HCLK} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}	$T_{HCLK} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} - 0.5$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK} + 2$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	

1. Guaranteed by characterization results.

Table 108. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK} - 1$	$9T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK} - 0.5$	$7T_{HCLK} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} + 2$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} - 1$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

[Figure 66](#) through [Figure 69](#) represent synchronous waveforms and [Table 109](#) through [Table 112](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all the timing tables, the T_{HCLK} is the HCLK clock period.

- For $2.7 V \leq V_{DD} \leq 3.6 V$, maximum FMC_CLK = 100 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
- For $1.71 V \leq V_{DD} < 2.7 V$, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Figure 66. Synchronous multiplexed NOR/PSRAM read timings

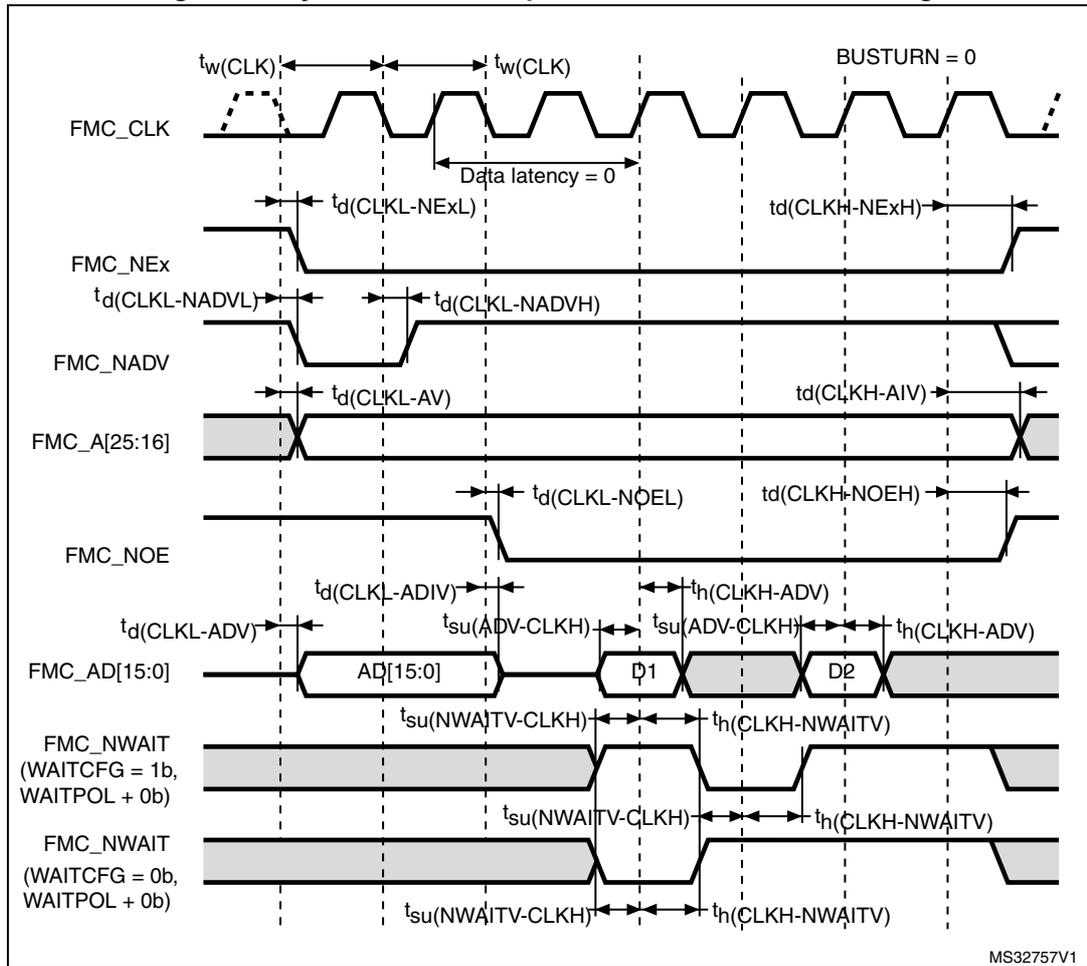


Table 109. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(\text{CLK})}$	FMC_CLK period	$2T_{\text{HCLK}} - 0.5$	-	ns
$t_{d(\text{CLKL-NExL})}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(\text{CLKH-NExH})}$	FMC_CLK high to FMC_NEx high (x= 0...2)	$T_{\text{HCLK}} + 0.5$	-	
$t_{d(\text{CLKL-NADV})}$	FMC_CLK low to FMC_NADV low	-	1.	
$t_{d(\text{CLKL-NADVH})}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(\text{CLKL-AV})}$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	2.5	
$t_{d(\text{CLKH-AIV})}$	FMC_CLK high to FMC_Ax invalid (x=16...25)	T_{HCLK}	-	
$t_{d(\text{CLKL-NOEL})}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(\text{CLKH-NOEH})}$	FMC_CLK high to FMC_NOE high	$T_{\text{HCLK}} - 0.5$	-	
$t_{d(\text{CLKL-ADV})}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(\text{CLKL-ADIV})}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(\text{ADV-CLKH})}$	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
$t_h(\text{CLKH-ADV})$	FMC_A/D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{su(\text{NWAIT-CLKH})}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_h(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

Figure 67. Synchronous multiplexed PSRAM write timings

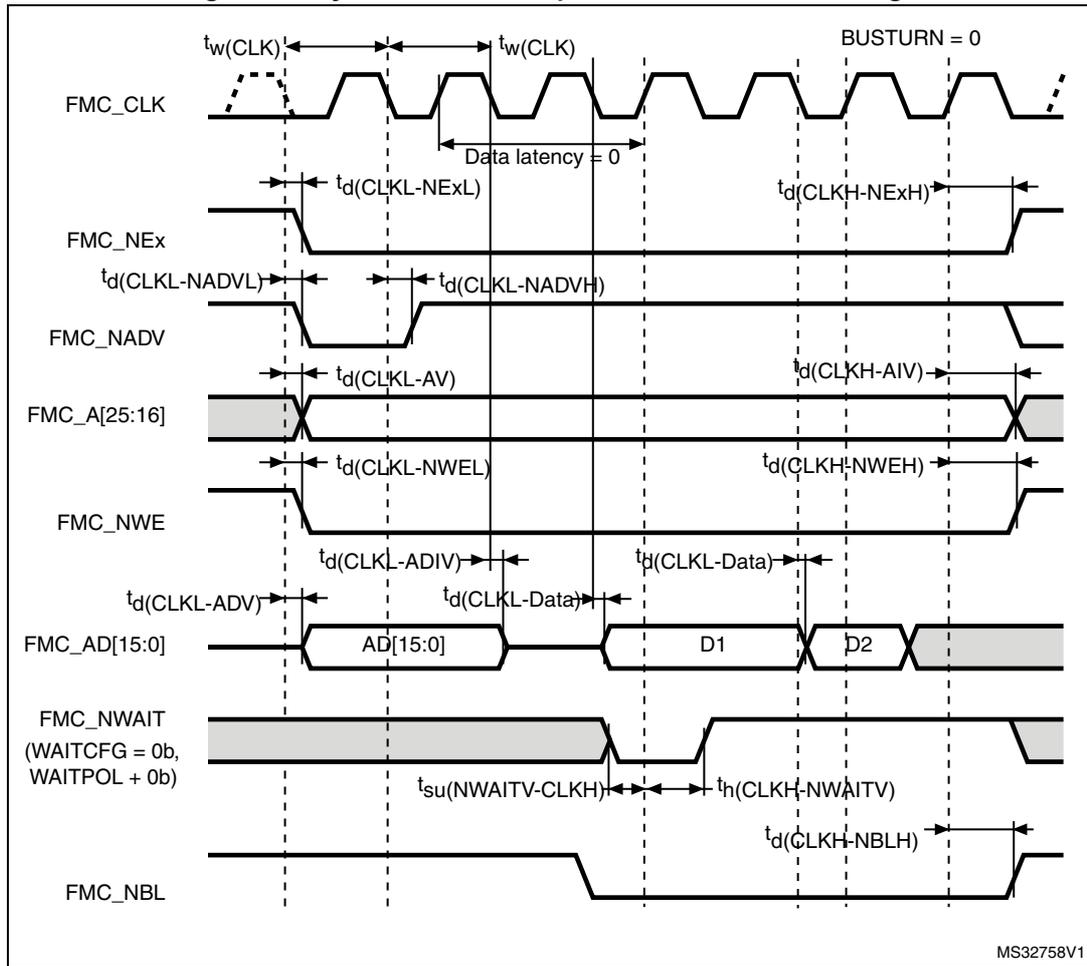


Table 110. Synchronous multiplexed PSRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(\text{CLK})}$	FMC_CLK period	$2T_{\text{HCLK}} - 0.5$	-	ns
$t_{d(\text{CLKL-NExL})}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(\text{CLKH-NExH})}$	FMC_CLK high to FMC_NEx high (x= 0...2)	$T_{\text{HCLK}} + 0.5$	-	
$t_{d(\text{CLKL-NADVl})}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(\text{CLKL-NADVh})}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(\text{CLKL-AV})}$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	2.5	
$t_{d(\text{CLKH-AIV})}$	FMC_CLK high to FMC_Ax invalid (x=16...25)	T_{HCLK}	-	
$t_{d(\text{CLKL-NWEL})}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(\text{CLKH-NWEH})}$	FMC_CLK high to FMC_NWE high	$T_{\text{HCLK}} + 0.5$	-	
$t_{d(\text{CLKL-ADV})}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(\text{CLKL-ADIV})}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(\text{CLKL-DATA})}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(\text{CLKL-NBLL})}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(\text{CLKH-NBLH})}$	FMC_CLK high to FMC_NBL high	$T_{\text{HCLK}} + 0.5$	-	
$t_{su(\text{NWAIT-CLKH})}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_h(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

Figure 68. Synchronous non-multiplexed NOR/PSRAM read timings

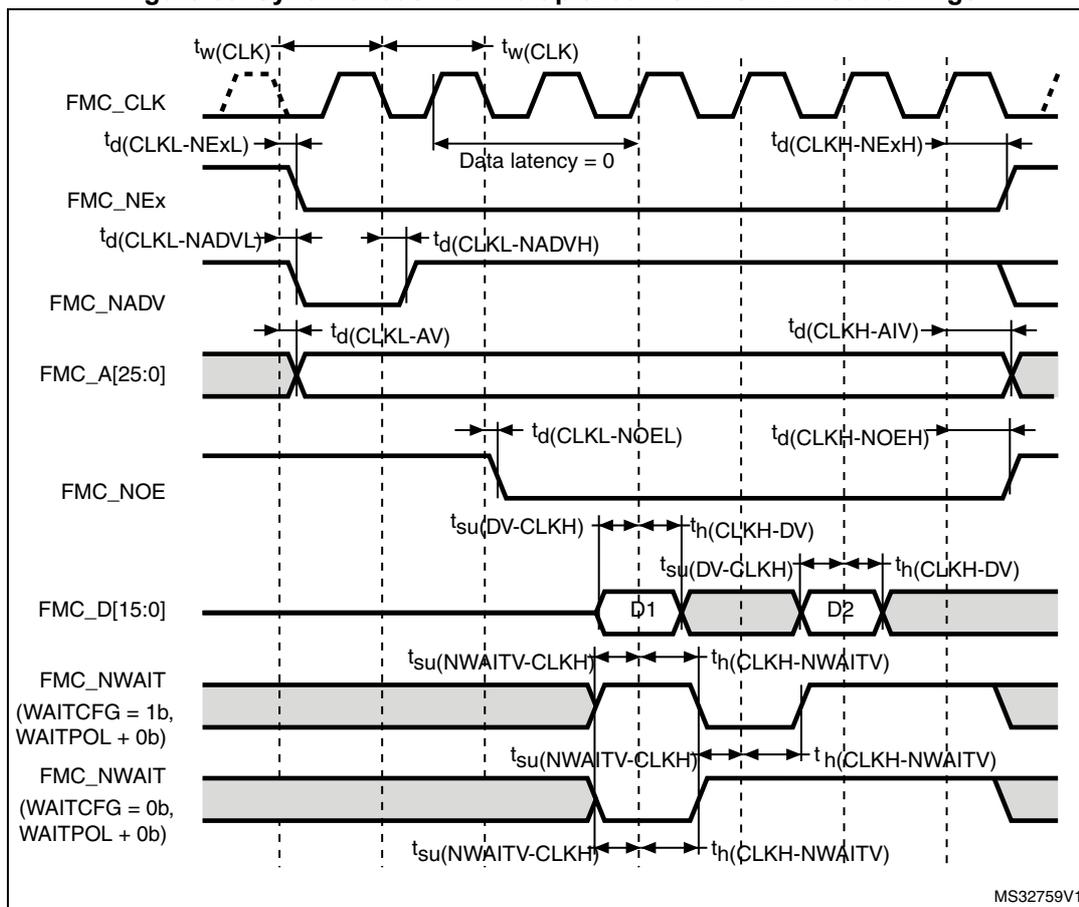


Table 111. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FMC_CLK period	$2T_{\text{HCLK}} - 0.5$	-	ns
$t_{\text{d}}(\text{CLKL-NExL})$	FMC_CLK low to FMC_NEx low ($x=0..2$)	-	2	
$t_{\text{d}}(\text{CLKH-NExH})$	FMC_CLK high to FMC_NEx high ($x=0..2$)	$T_{\text{HCLK}} + 0.5$	-	
$t_{\text{d}}(\text{CLKL-NADV})$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{\text{d}}(\text{CLKL-NADVH})$	FMC_CLK low to FMC_NADV high	0	-	
$t_{\text{d}}(\text{CLKL-ADV})$	FMC_CLK low to FMC_Ax valid ($x=16..25$)	-	2.5	
$t_{\text{d}}(\text{CLKH-AIV})$	FMC_CLK high to FMC_Ax invalid ($x=16..25$)	T_{HCLK}	-	
$t_{\text{d}}(\text{CLKL-NOEL})$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{\text{d}}(\text{CLKH-NOEH})$	FMC_CLK high to FMC_NOE high	$T_{\text{HCLK}} + 0.5$	-	
$t_{\text{su}}(\text{DV-CLKH})$	FMC_D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{\text{h}}(\text{CLKH-DV})$	FMC_D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{\text{su}}(\text{NWAITV-CLKH})$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{\text{h}}(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

Figure 69. Synchronous non-multiplexed PSRAM write timings

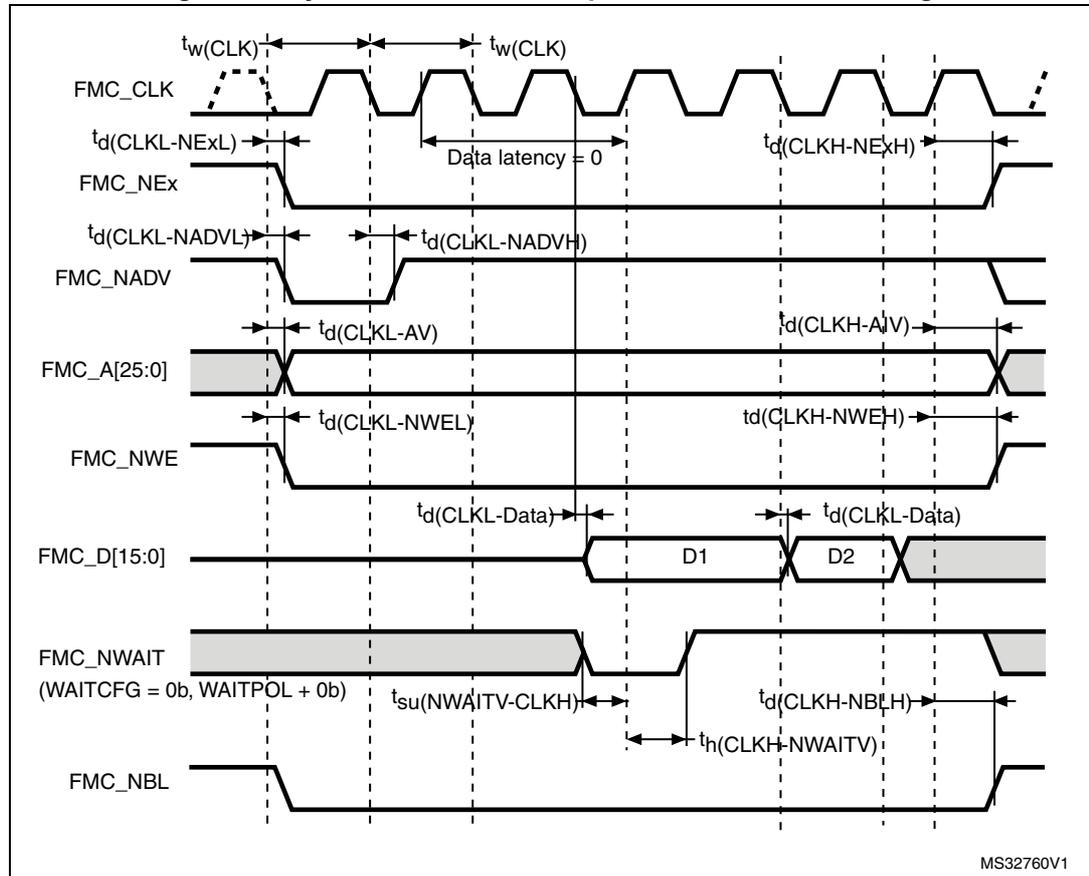


Table 112. Synchronous non-multiplexed PSRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0...2)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADVl)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVh)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16..25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16..25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{HCLK} + 1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLl)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{HCLK} + 1$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 70 through Figure 73 represent synchronous waveforms, and Table 113 and Table 114 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 70. NAND controller waveforms for read access

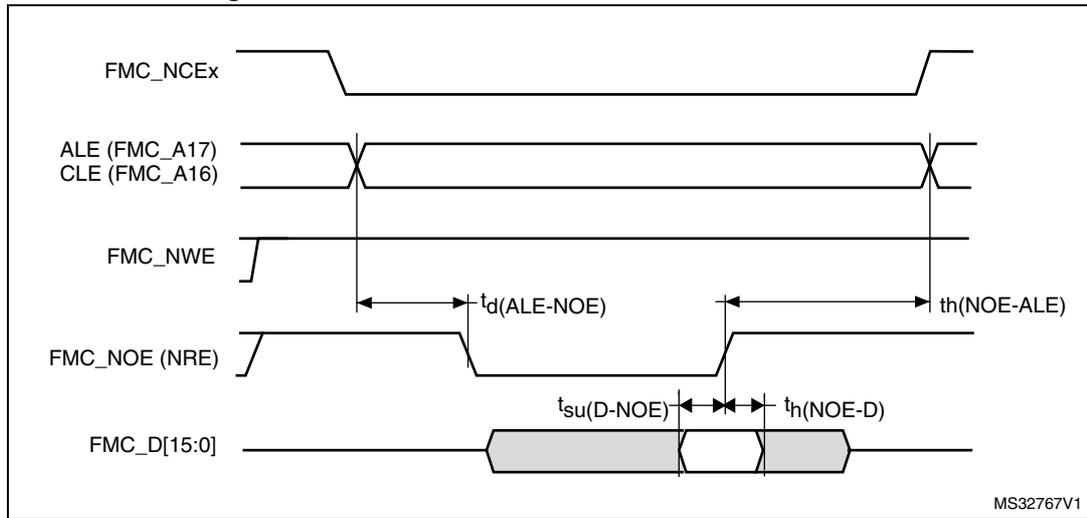


Figure 71. NAND controller waveforms for write access

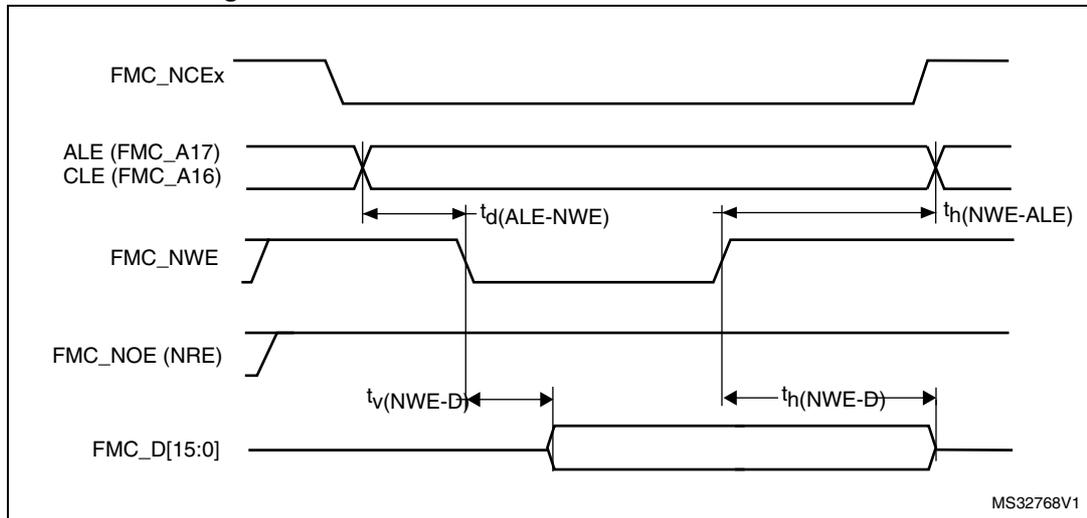
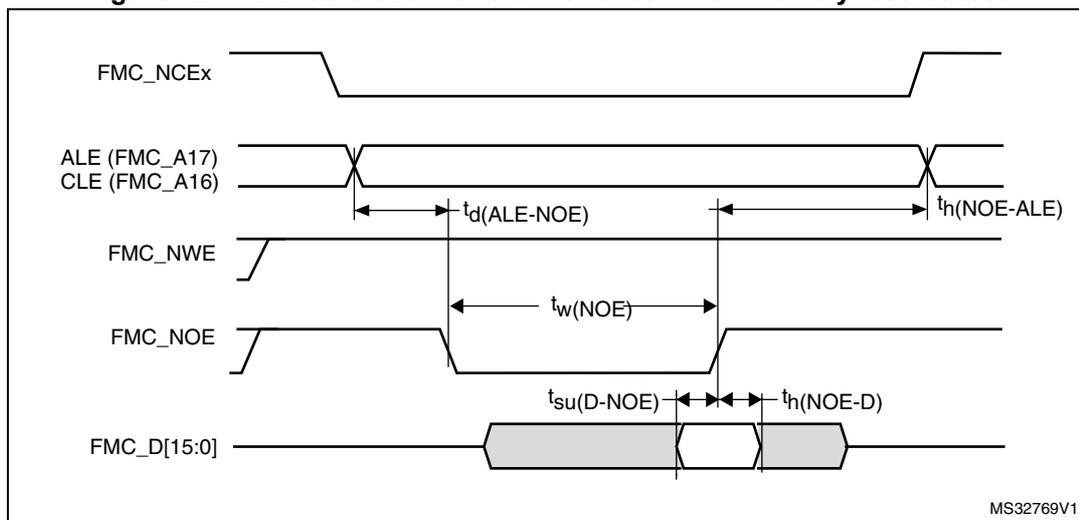
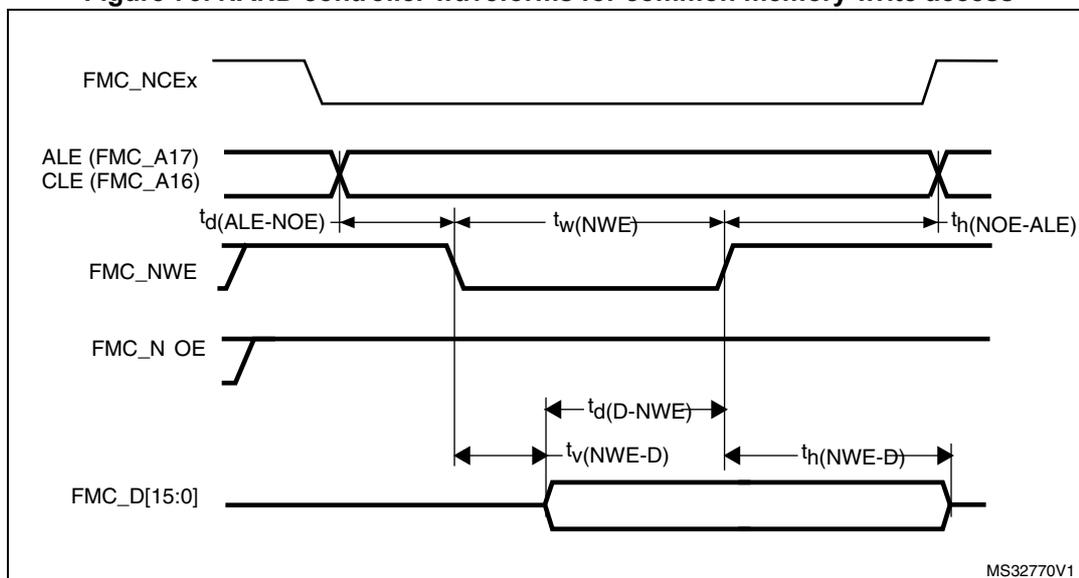


Figure 72. NAND controller waveforms for common memory read access



MS32769V1

Figure 73. NAND controller waveforms for common memory write access



MS32770V1

Table 113. Switching characteristics for NAND Flash read cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{NOE})$	FMC_NOE low width	$4T_{\text{HCLK}} - 0.5$	$4T_{\text{HCLK}} + 0.5$	ns
$t_{su}(\text{D-NOE})$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_h(\text{NOE-D})$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_d(\text{ALE-NOE})$	FMC_ALE valid before FMC_NOE low	-	$3T_{\text{HCLK}} + 1$	
$t_h(\text{NOE-ALE})$	FMC_NWE high to FMC_ALE invalid	$4T_{\text{HCLK}} - 2$	-	

1. Guaranteed by characterization results.

Table 114. Switching characteristics for NAND Flash write cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK} - 0.5$	$4T_{HCLK} + 0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK} - 1$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK} - 1$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{HCLK} + 1$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{HCLK} - 2$	-	

1. Guaranteed by characterization results.

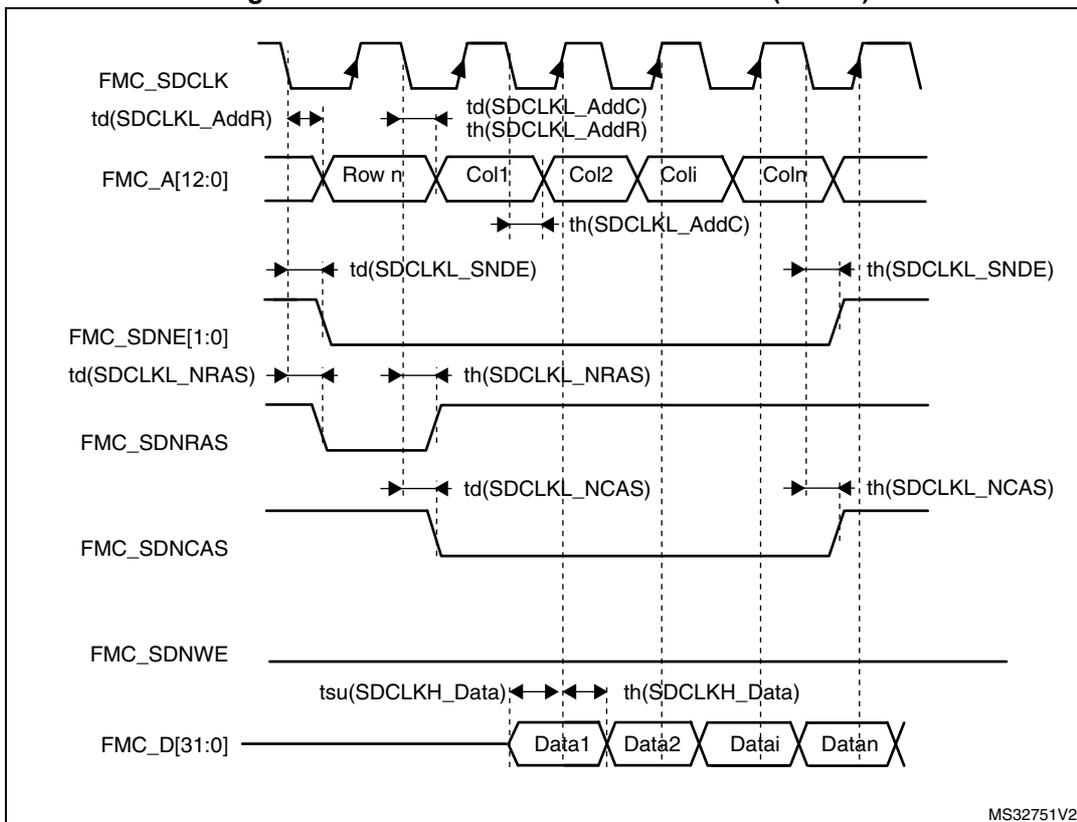
SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For $3.0 V \leq V_{DD} \leq 3.6 V$, maximum FMC_SDCLK = 100 MHz at CL=20 pF (on FMC_SDCLK).
- For $2.7 V \leq V_{DD} \leq 3.6 V$, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For $1.71 V \leq V_{DD} < 1.9 V$, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 74. SDRAM read access waveforms (CL = 1)



MS32751V2

Table 115. SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	1.5	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	3.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

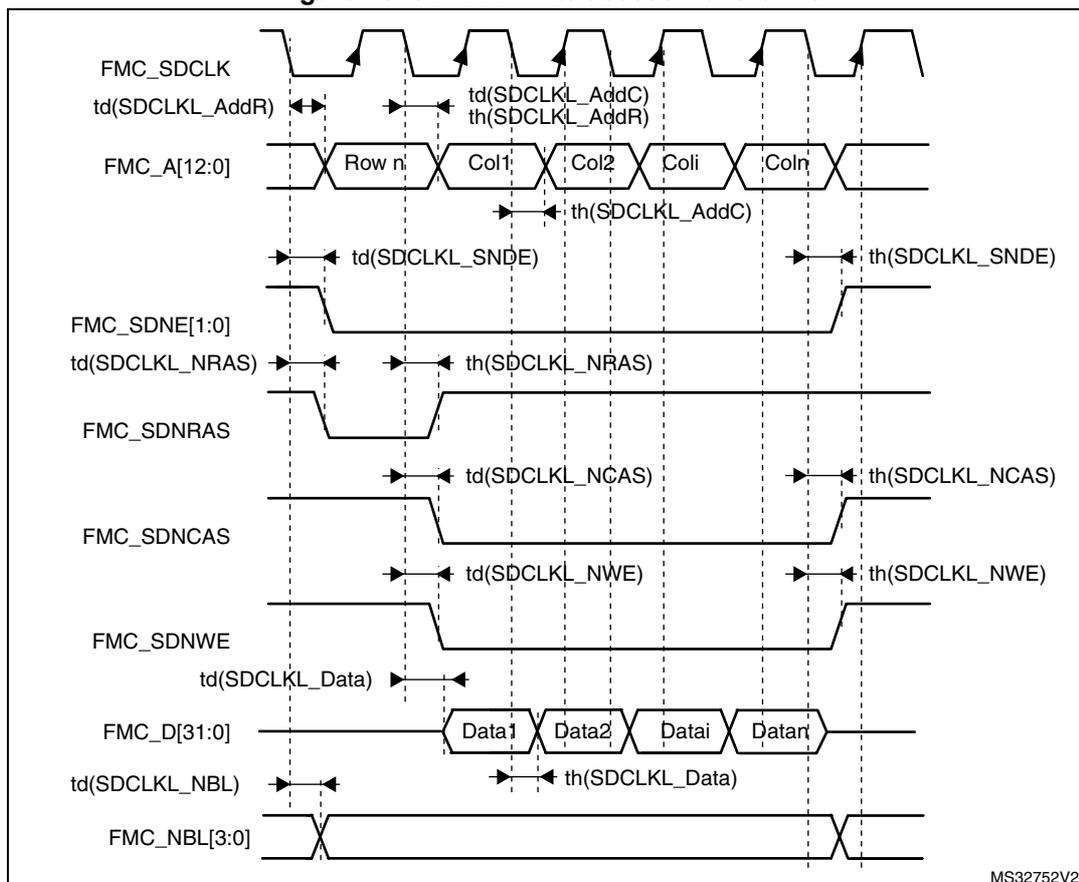
1. Guaranteed by characterization results.

Table 116. LPDDR SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	0	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	4.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Figure 75. SDRAM write access waveforms



MS32752V2

Table 117. SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}} - 0.5$	$2T_{\text{HCLK}} + 0.5$	ns
$t_d(\text{SDCLKL_Data})$	Data output valid time	-	3	
$t_h(\text{SDCLKL_Data})$	Data output hold time	0	-	
$t_d(\text{SDCLKL_Add})$	Address valid time	-	3.5	
$t_d(\text{SDCLKL_SDNWE})$	SDNWE valid time	-	1.5	
$t_h(\text{SDCLKL_SDNWE})$	SDNWE hold time	0.5	-	
$t_d(\text{SDCLKL_SDNE})$	Chip select valid time	-	1.5	
$t_h(\text{SDCLKL_SDNE})$	Chip select hold time	0.5	-	
$t_d(\text{SDCLKL_SDNRAS})$	SDNRAS valid time	-	1	
$t_h(\text{SDCLKL_SDNRAS})$	SDNRAS hold time	0.5	-	
$t_d(\text{SDCLKL_SDNCAS})$	SDNCAS valid time	-	1	
$t_h(\text{SDCLKL_SDNCAS})$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 118. LPSDR SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}} - 0.5$	$2T_{\text{HCLK}} + 0.5$	ns
$t_d(\text{SDCLKL_Data})$	Data output valid time	-	2.5	
$t_h(\text{SDCLKL_Data})$	Data output hold time	0	-	
$t_d(\text{SDCLKL_Add})$	Address valid time	-	2.5	
$t_d(\text{SDCLKL-SDNWE})$	SDNWE valid time	-	2.5	
$t_h(\text{SDCLKL-SDNWE})$	SDNWE hold time	0	-	
$t_d(\text{SDCLKL-SDNE})$	Chip select valid time	-	0.5	
$t_h(\text{SDCLKL-SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL-SDNRAS})$	SDNRAS valid time	-	1.5	
$t_h(\text{SDCLKL-SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL-SDNCAS})$	SDNCAS valid time	-	1.5	
$t_d(\text{SDCLKL-SDNCAS})$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

5.3.31 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 119](#) and [Table 120](#) for Quad-SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in [Table 18: General operating conditions](#), with the following configuration:

- Output speed is set to $\text{OSPEEDRy}[1:0] = 11$
- Capacitive load $C = 20 \text{ pF}$
- Measurement points are done at CMOS levels: $0.5 \times V_{\text{DD}}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics.

Table 119. Quad-SPI characteristics in SDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{\text{ck1}}/t(\text{CK})$	Quad-SPI clock frequency	$2.7 \text{ V} \leq V_{\text{DD}} < 3.6 \text{ V}$ $\text{CL} = 20 \text{ pF}$	-	-	108	MHz
		$1.71 \text{ V} < V_{\text{DD}} < 3.6 \text{ V}$ $\text{CL} = 15 \text{ pF}$	-	-	100	

Table 119. Quad-SPI characteristics (continued)in SDR mode⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN)	Data input setup time	-	0.5	-	-	
th(IN)	Data input hold time		3	-	-	
tv(OUT)	Data output valid time	2.7 V < V _{DD} < 3.6 V	-	1.5	3.5	
		1.71 V < V _{DD} < 3.6 V	-	1.5	2	
th(OUT)	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

Table 120. Quad SPI characteristics in DDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V < V _{DD} < 3.6 V CL=20 pF	-	-	80	MHz
		1.8 V < V _{DD} < 3.6 V CL=15 pF	-	-	80	
		1.71 V < V _{DD} < 3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2 + 1	
ts(IN), tsf(IN)	Data input setup time	2.7 V < V _{DD} < 3.6 V	0.75	-	-	
		1.71 V < V _{DD} < 2 V	0.5	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V < V _{DD} < 3.6 V	2	-	-	
		1.71 V < V _{DD} < 2 V	3	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V < V _{DD} < 3.6 V	-	8.5	10	
		1.71 V < V _{DD} < 3.6 V DHHC=0	-	8	12	
		DHHC=1 Pres=1, 2...	-	T _{HCLK} /2 + 1.5	T _{HCLK} /2 + 2.5	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	7.5	-	-	
		DHHC=1 Pres=1, 2...	T _{HCLK} /2 + 0.5	-	-	

1. Guaranteed by characterization results.

Figure 76. Quad-SPI timing diagram - SDR mode

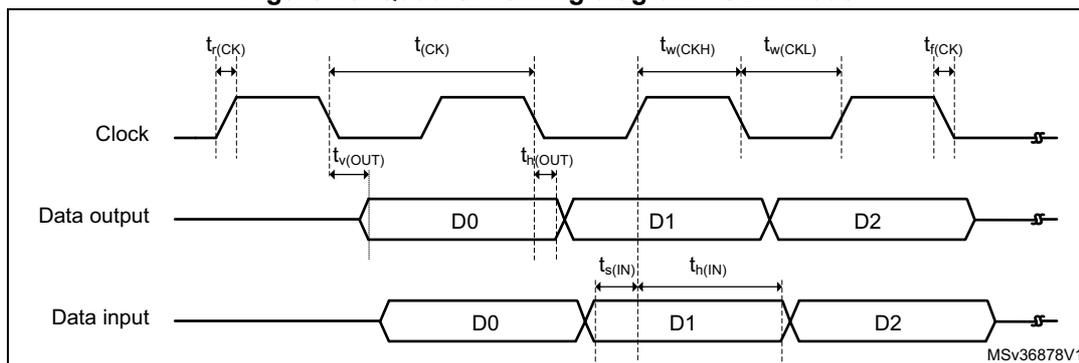
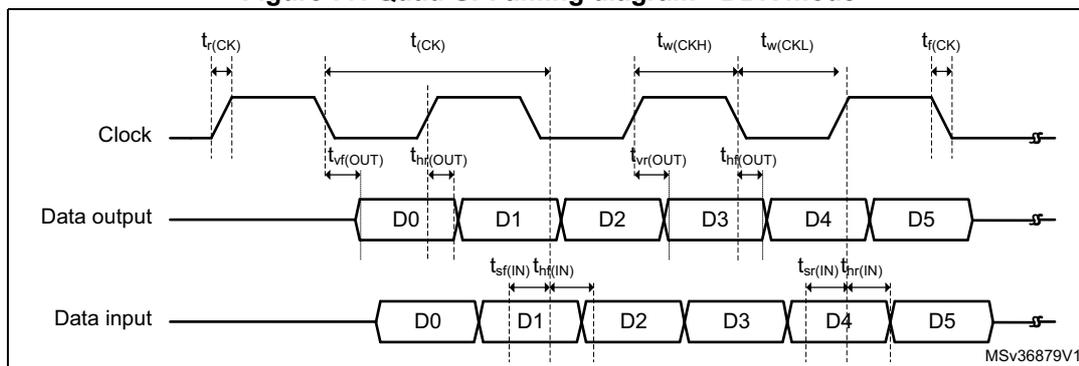


Figure 77. Quad-SPI timing diagram - DDR mode



5.3.32 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in [Table 121](#) for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 18](#), with the following configuration:

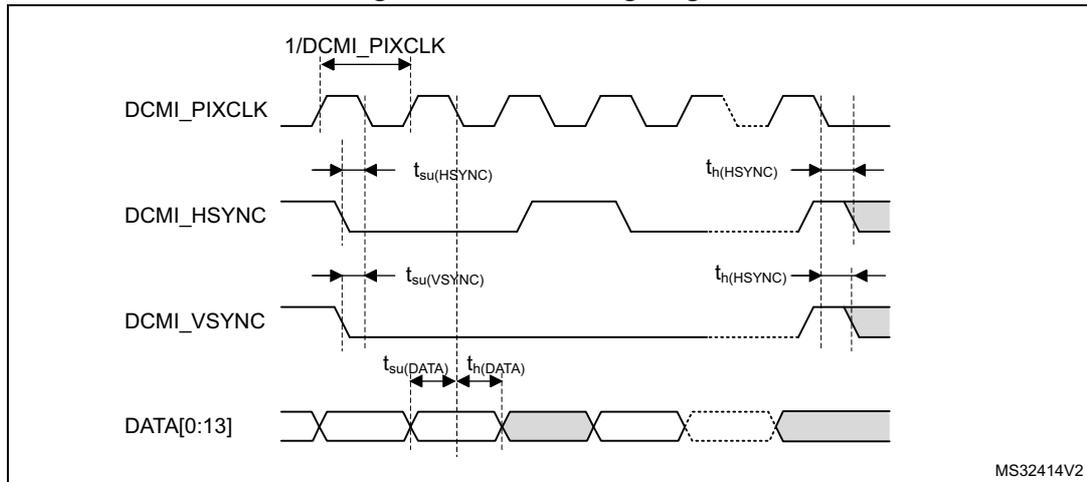
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 121. DCMI characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/ f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data input hold time	0.5	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2.5	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	3	-	

1. Guaranteed by characterization results.

Figure 78. DCMI timing diagram



MS32414V2

5.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in [Table 122](#) for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 18](#), with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

Table 122. LTDC characteristics ⁽¹⁾

Symbol	Parameter	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	-	83	MHz
D_{CLK}	LTDC clock output duty cycle	45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time	$tw(CLK)/2-0.5$	$tw(CLK)/2+0.5$	ns
$t_{v(DATA)}$	Data output valid time	-	6	
$t_{h(DATA)}$	Data output hold time	0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	-	3.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time	0.5	-	

1. Guaranteed by characterization results.

Figure 79. LCD-TFT horizontal timing diagram

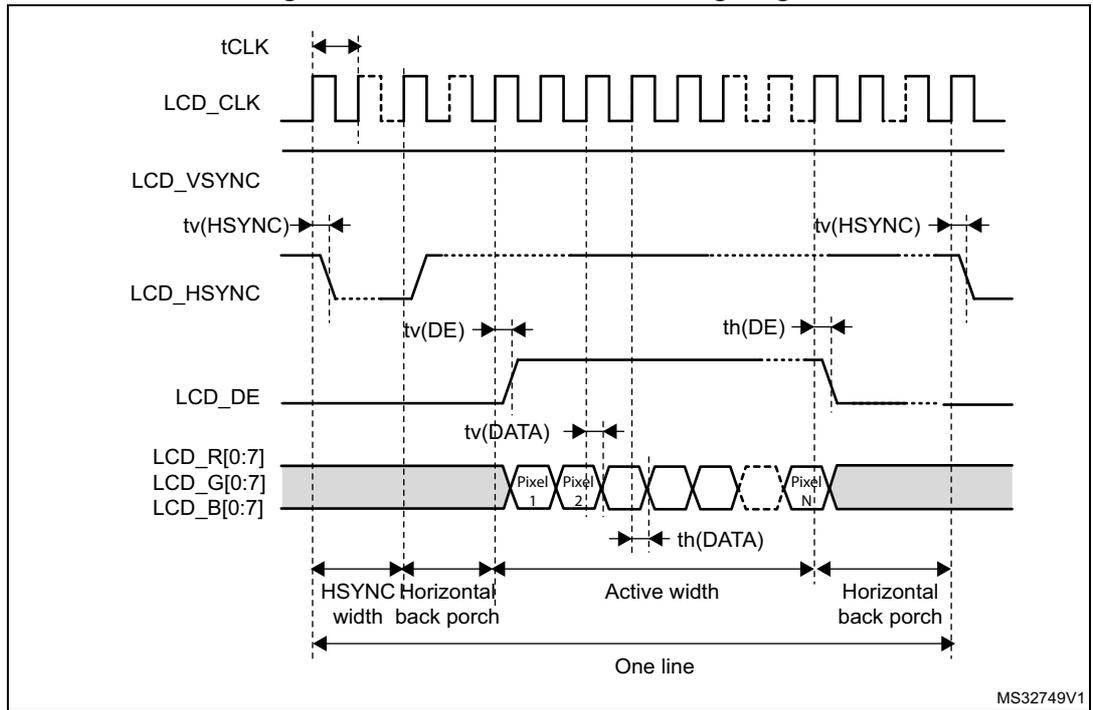
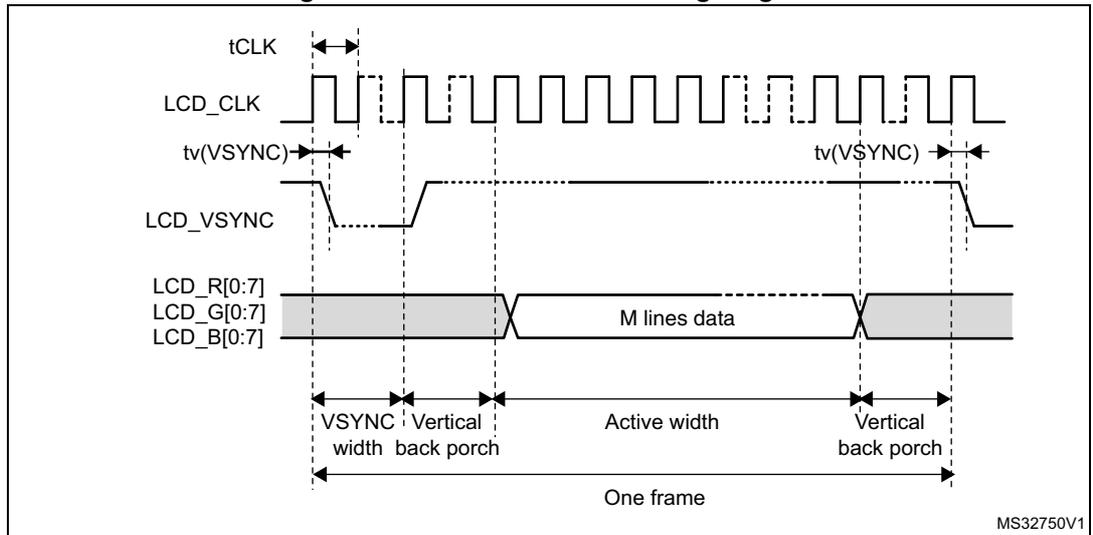


Figure 80. LCD-TFT vertical timing diagram



5.3.34 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in [Table 123](#) for DFSDM are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage summarized in [Table 18](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30\text{pF}$
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output alternate function characteristics (DFSDM1_CKINx, DFSDM1_DATINx, DFSDM1_CKOUT for DFSDM1).

Table 123. DFSDM measured timing 1.71-3.6V

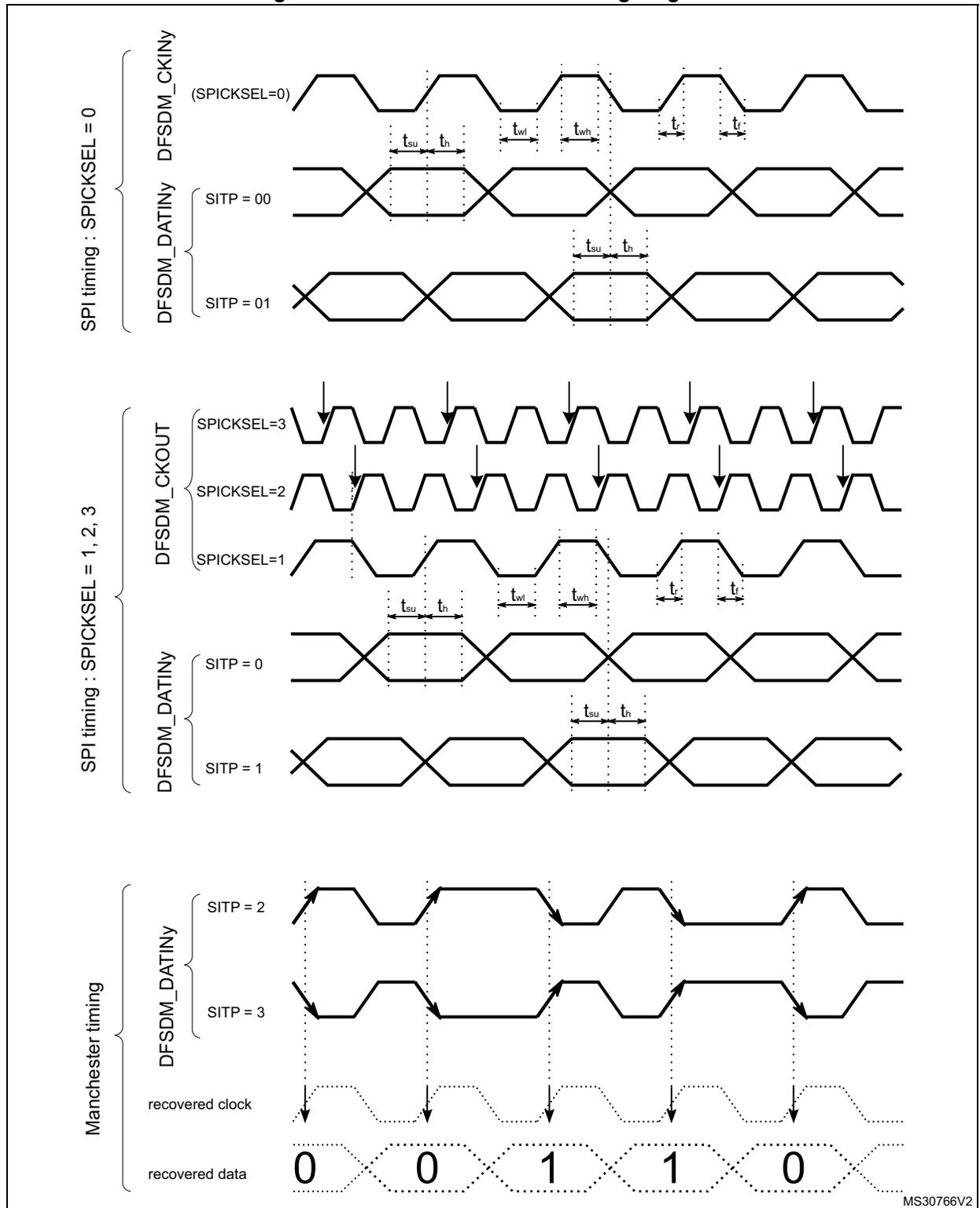
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	$1.71 < V_{DD} < 3.6 \text{ V}$	-	-	f_{SYSCLK}	
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.71 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	MHz
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $2.7 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), $1.71 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), $2.7 < V_{DD} < 3.6 \text{ V}$	-	-	20 ($f_{DFSDMCLK}/4$)	
f_{CKOUT}	Output clock frequency	$1.71 < V_{DD} < 3.6 \text{ V}$	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	$1.71 < V_{DD} < 3.6 \text{ V}$	45	50	55	%

Table 123. DFSDM measured timing 1.71-3.6V (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V _{DD} < 3.6 V	TCKIN/2 - 0.5	T _{CKIN} /2	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V _{DD} < 3.6 V	2	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V _{DD} < 3.6 V	3	-	-	
T _{Manchester}	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V _{DD} < 3.6 V	(CKOUTDIV+1) * T _{DFSDMCLK}	-	(2*CKOUTDIV) * T _{DFSDMCLK}	

5.3.35 DFSDM timing diagrams

Figure 81. Channel transceiver timing diagrams



5.3.36 SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in [Table 124](#) for the SDIO/MMC interface are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in [Table 18](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 11$
- Capacitive load $C = 30\text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output characteristics.

Figure 82. SDIO high-speed mode

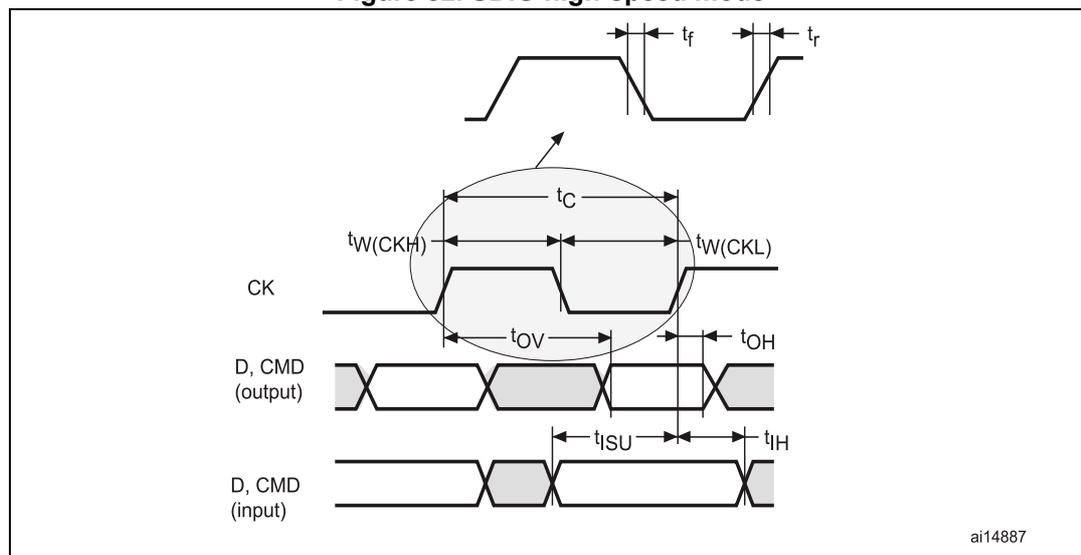


Figure 83. SD default mode

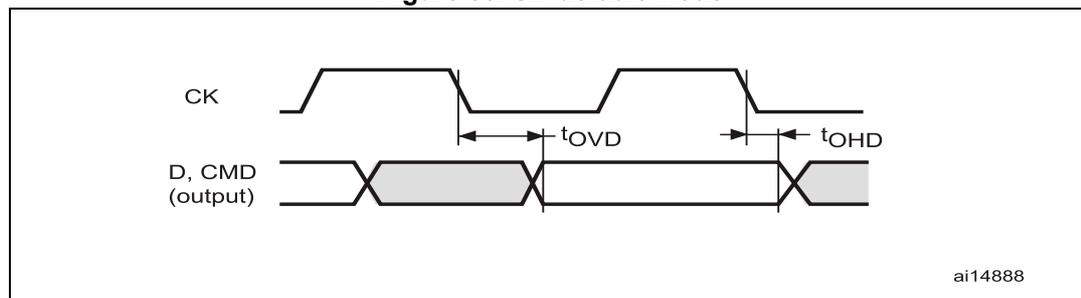


Table 124. Dynamic characteristics: SD / MMC characteristics, $V_{DD}=2.7V$ to $3.6V^{(1)}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	$f_{pp} = 50$ MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	$f_{pp} = 50$ MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	$f_{pp} = 50$ MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	$f_{pp} = 50$ MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	$f_{pp} = 50$ MHz	-	11	12	ns
t_{OH}	Output hold time HS	$f_{pp} = 50$ MHz	9	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	$f_{pp} = 25$ MHz	3.5	-	-	ns
t_{IHD}	Input hold time SD	$f_{pp} = 25$ MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	$f_{pp} = 25$ MHz	-	0.5	1.5	ns
t_{OHD}	Output hold default time SD	$f_{pp} = 25$ MHz	0	-	-	

1. Guaranteed by characterization results.

Table 125. Dynamic characteristics: eMMC characteristics, $V_{DD}=1.71V$ to $1.9V^{(1)(2)}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	$f_{pp} = 50$ MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	$f_{pp} = 50$ MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	$f_{pp} = 50$ MHz	3	-	-	ns
t_{IH}	Input hold time HS	$f_{pp} = 50$ MHz	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	$f_{pp} = 50$ MHz	-	11	15.5	ns
t_{OH}	Output hold time HS	$f_{pp} = 50$ MHz	9.5	-	-	

1. Guaranteed by characterization results.

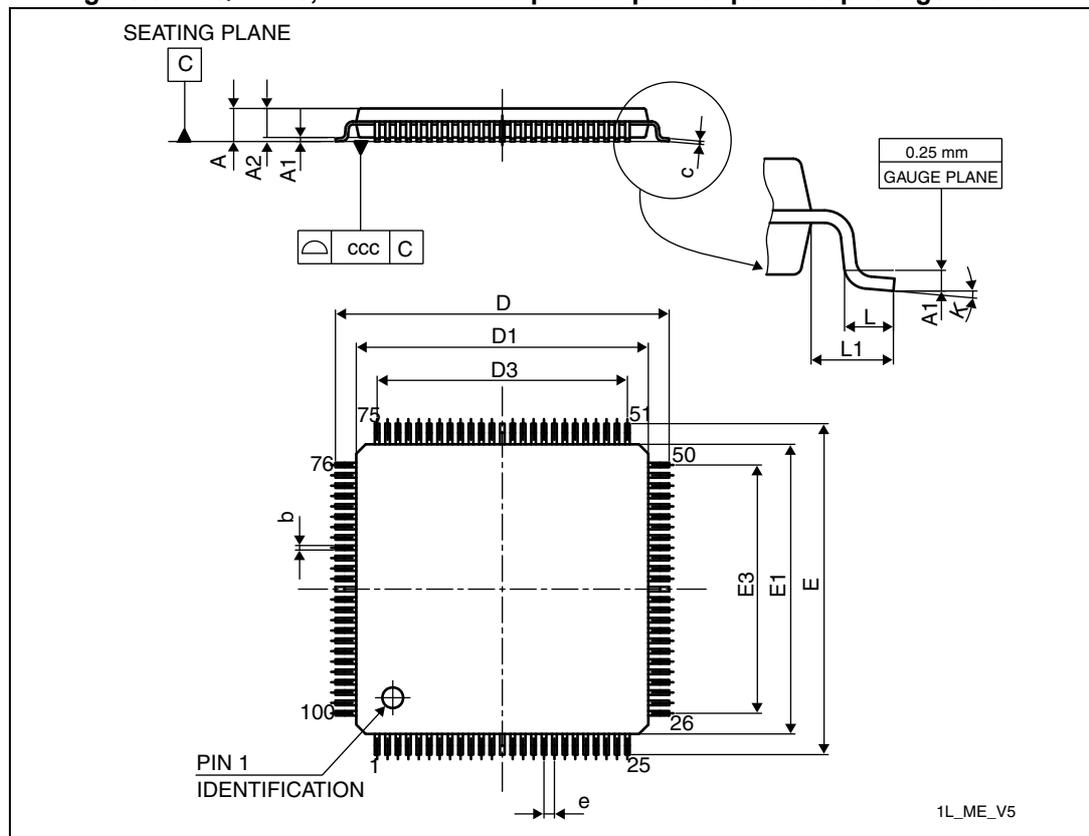
2. $C_{load} = 20$ pF.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

6.1 LQFP100 14x 14 mm, low-profile quad flat package information

Figure 84. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



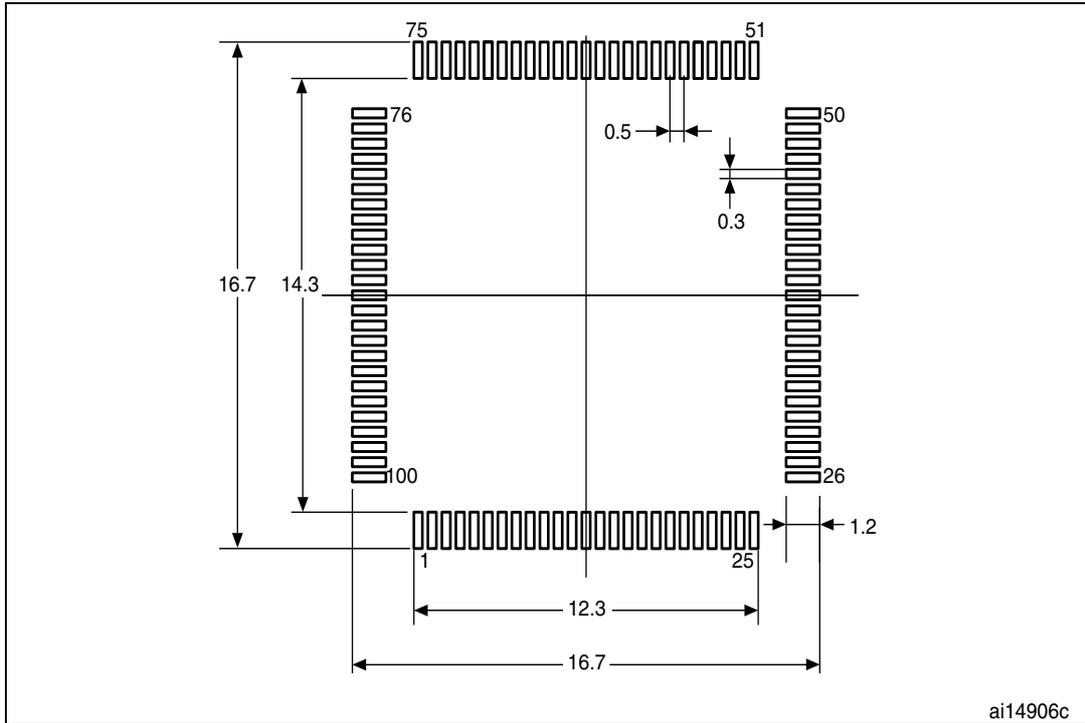
1. Drawing is not to scale.

Table 126. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 85. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint



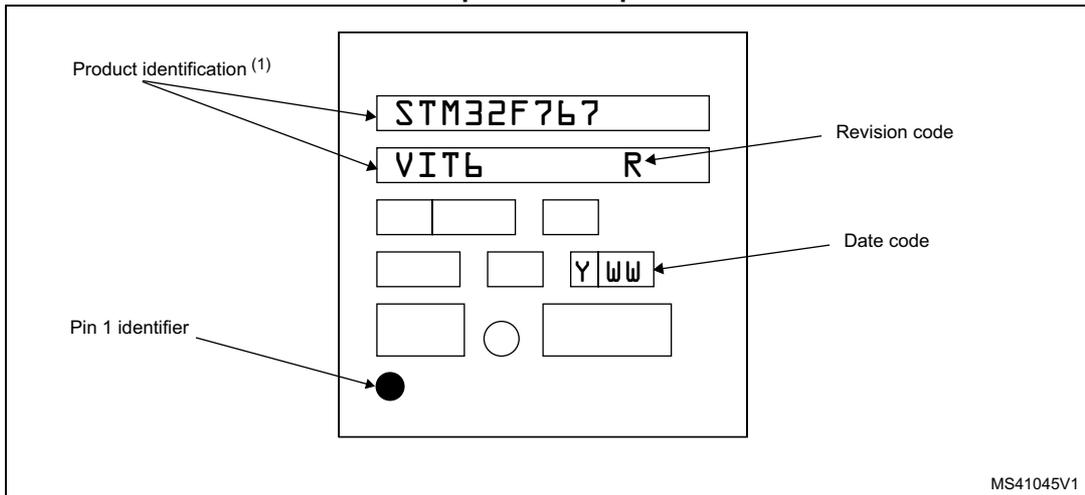
1. Dimensions are expressed in millimeters.

LQFP100 device making

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

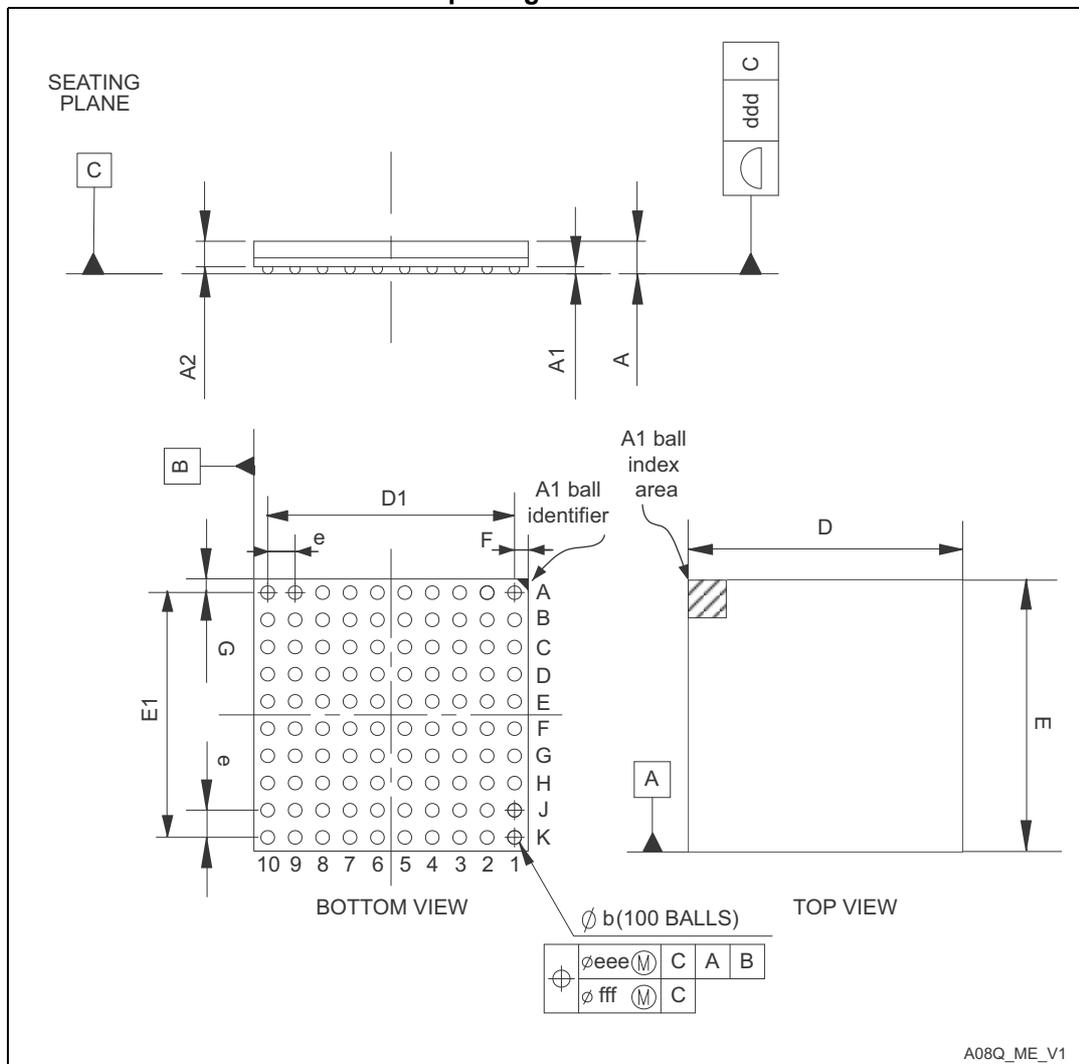
Figure 86. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.2 TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package information

Figure 87. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 127. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package mechanical data

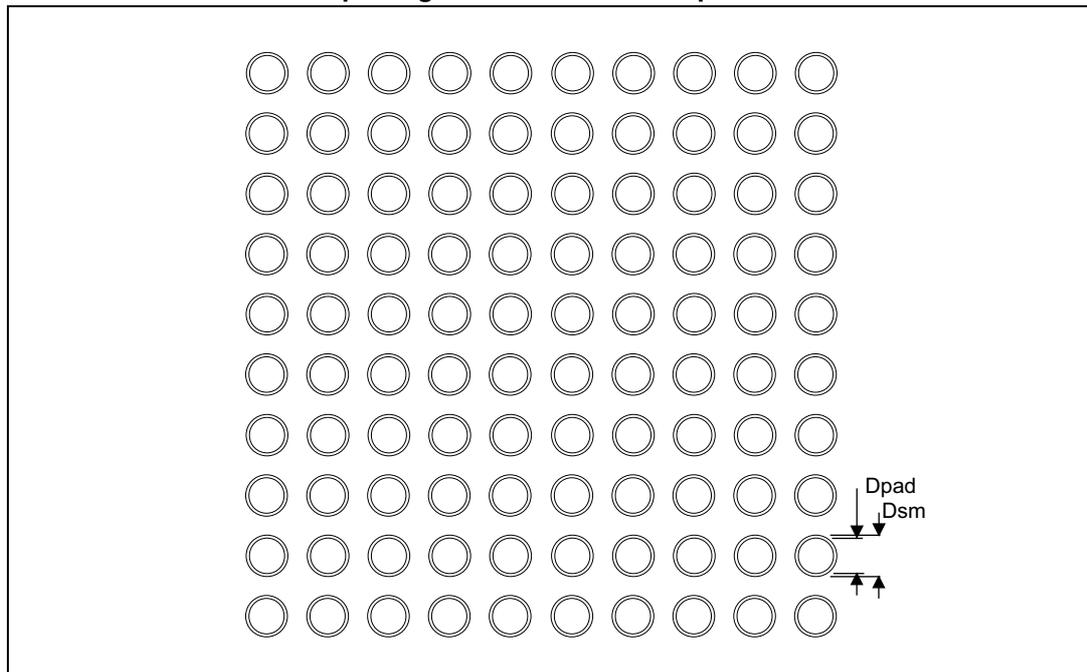
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177

Table 127. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D	7.850	8.000	8.150	0.3091	0.3150	0.3209
D1	-	7.200	-	-	0.2835	-
E	7.850	8.000	8.150	0.3091	0.3150	0.3209
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	0.400	-	-	0.0157	-
G	-	0.400	-	-	0.0157	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 88. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package recommended footprint



1. Dimensions are expressed in millimeters.

Table 128. TFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

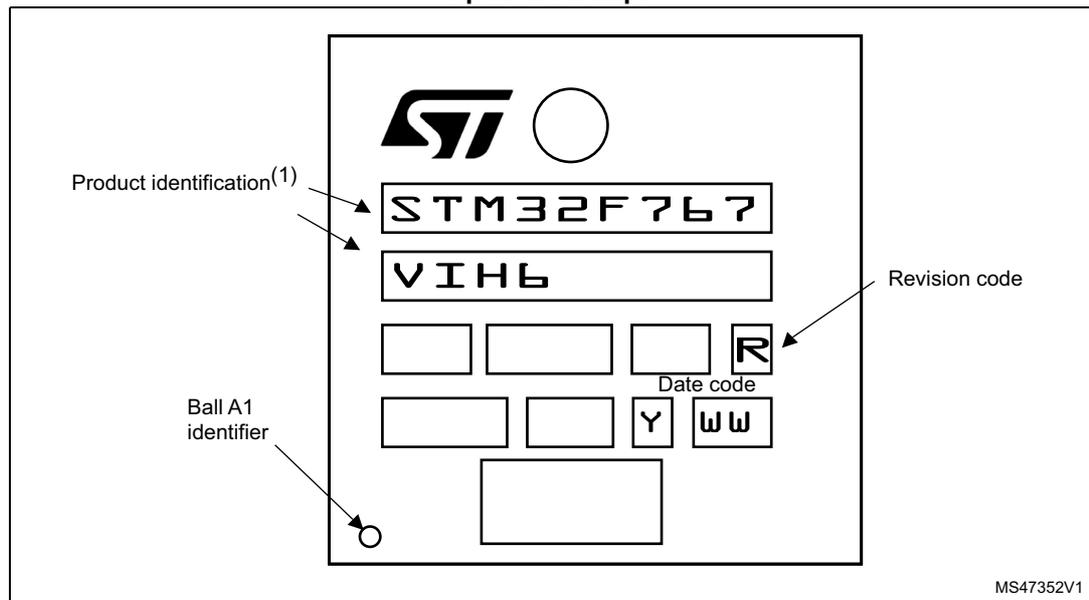
Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

TFBGA100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

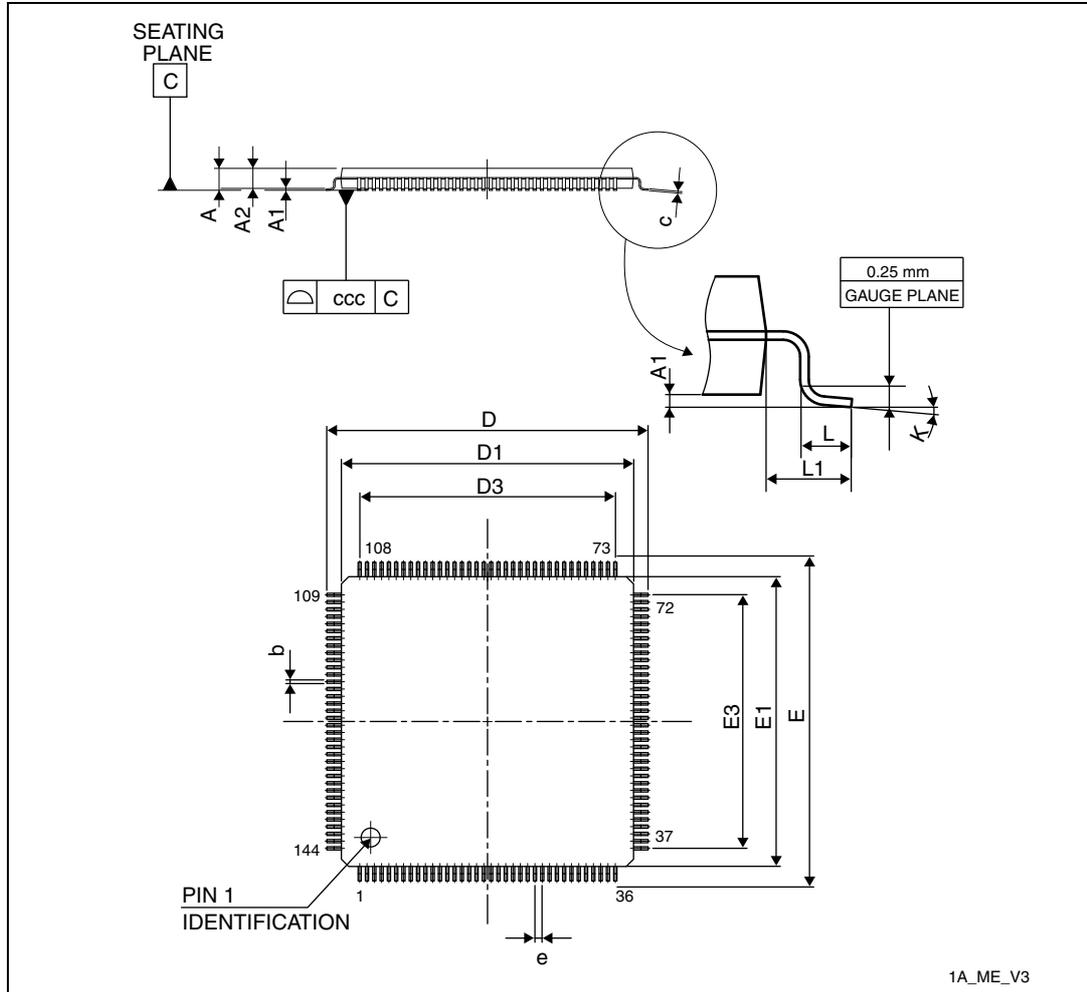
Figure 89. TFBGA100, 8 × 8 × 0.8mm thin fine-pitch ball grid array package top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.3 LQFP144 20 x 20 mm, low-profile quad flat package information

Figure 90. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



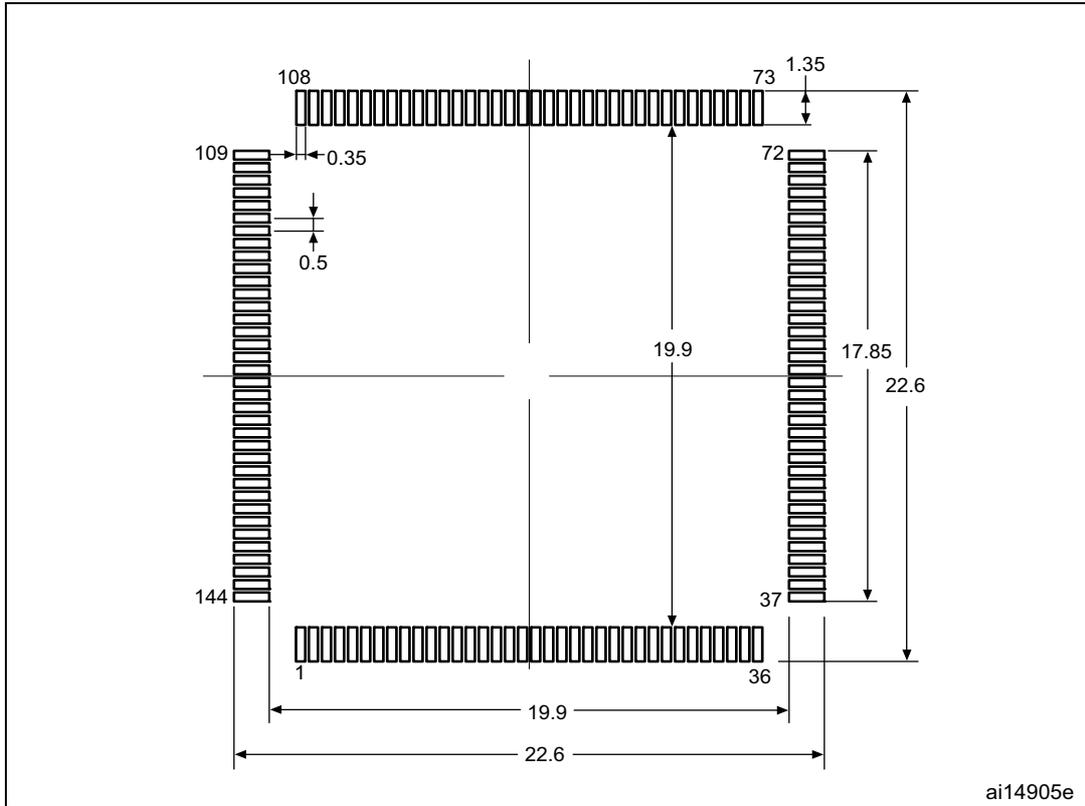
1. Drawing is not to scale.

Table 129. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 91. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint



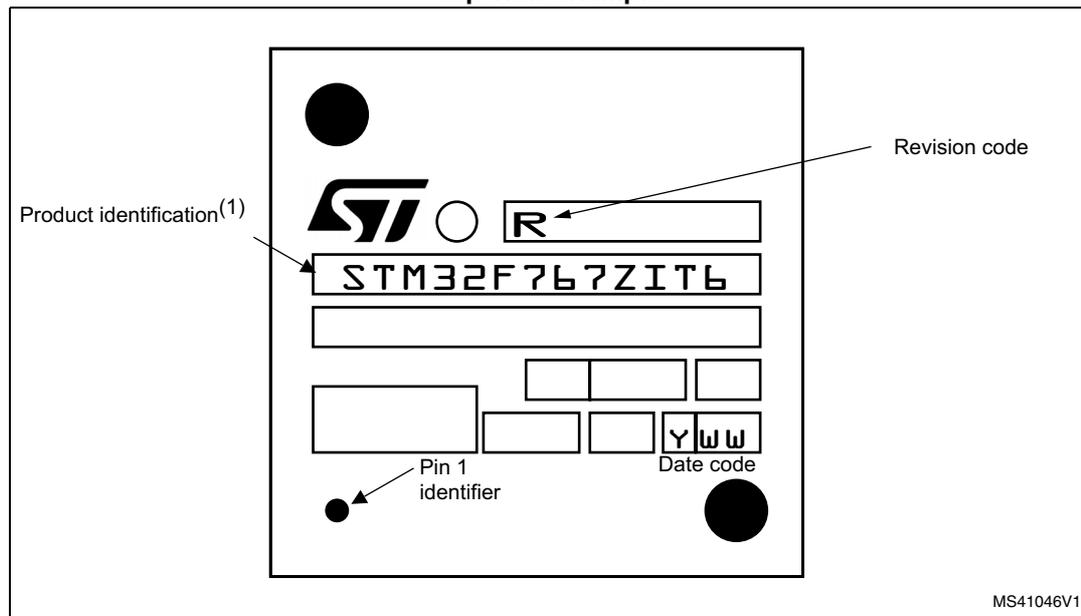
1. Dimensions are expressed in millimeters.

LQFP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

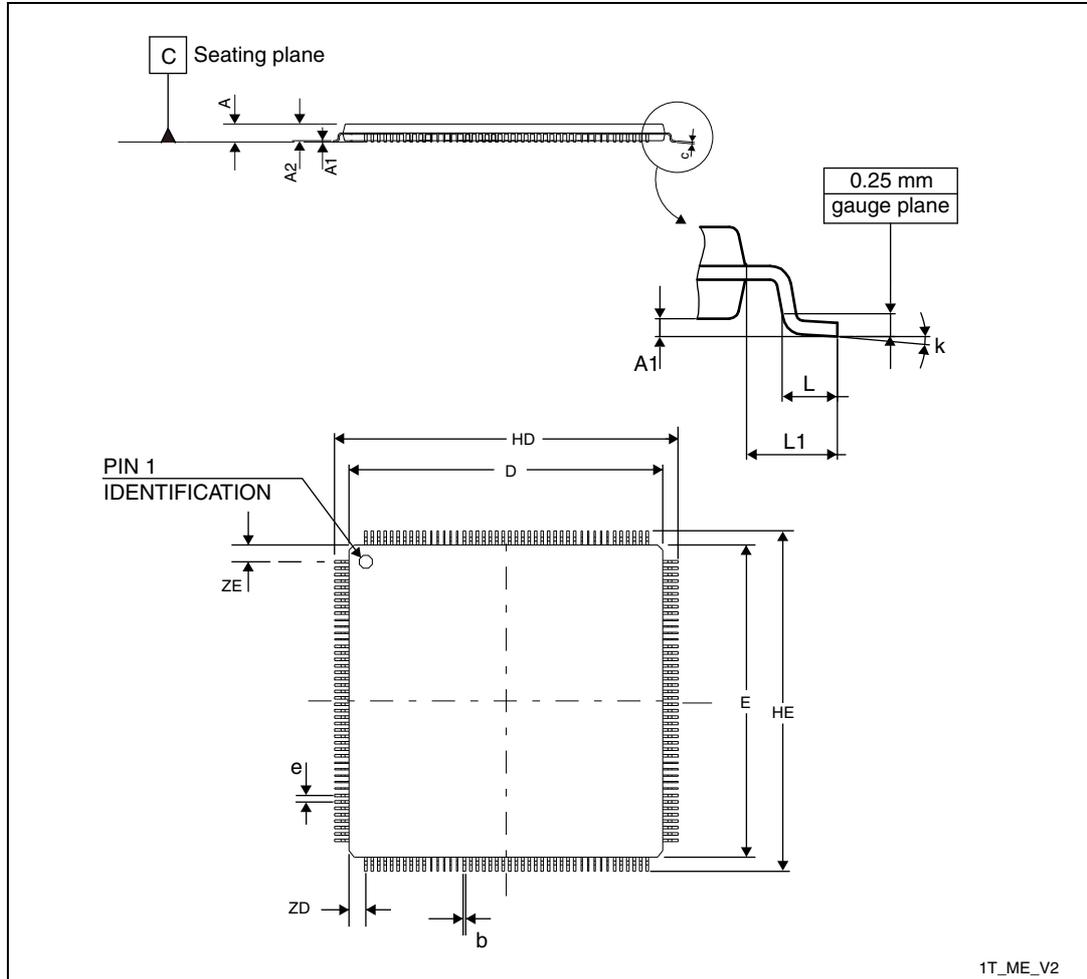
Figure 92. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.4 LQFP176 24 x 24 mm, low-profile quad flat package information

Figure 93. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline



1. Drawing is not to scale.

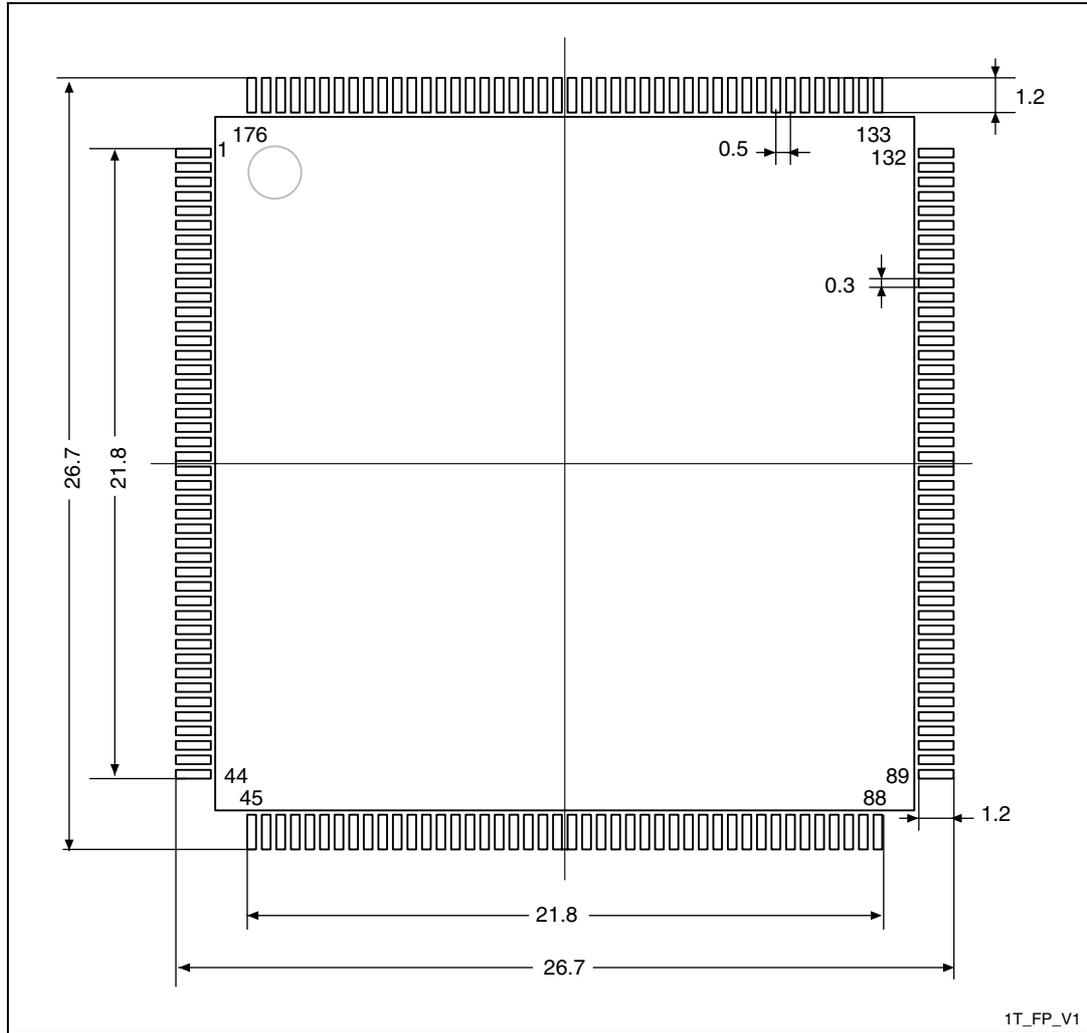
1T_ME_V2

Table 130. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
E	23.900	-	24.100	0.9409	-	0.9488
e	-	0.500	-	-	0.0197	-
HD	25.900	-	26.100	1.0200	-	1.0276
HE	25.900	-	26.100	1.0200	-	1.0276
L	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
ZD	-	1.250	-	-	0.0492	-
ZE	-	1.250	-	-	0.0492	-
ccc	-	-	0.080	-	-	0.0031
k	0°	-	7°	0°	-	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 94. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint



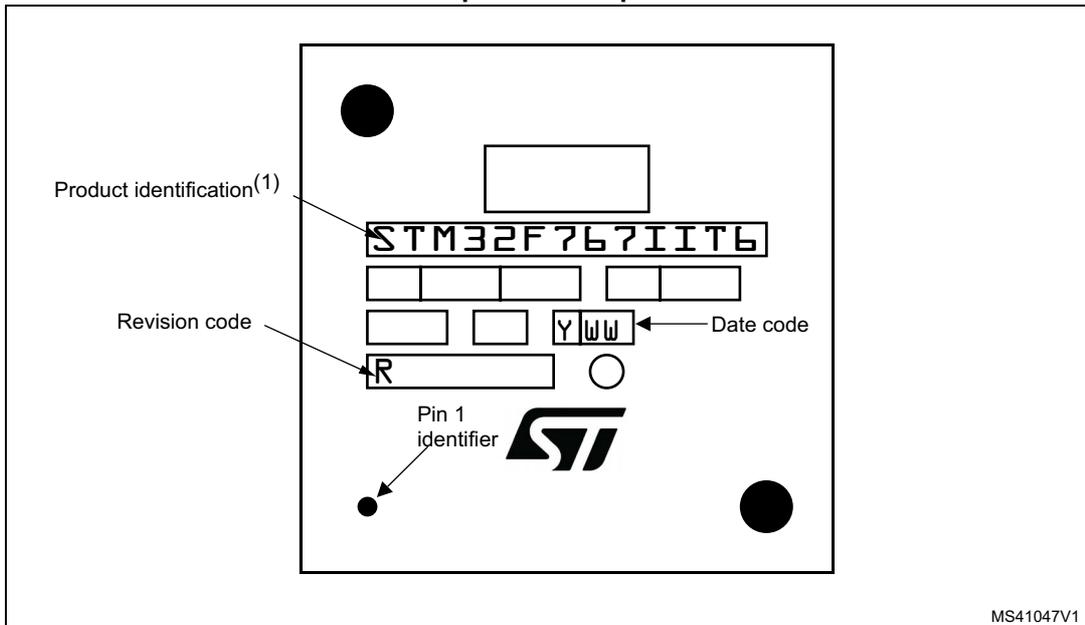
1. Dimensions are expressed in millimeters.

LQFP176 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 95. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example

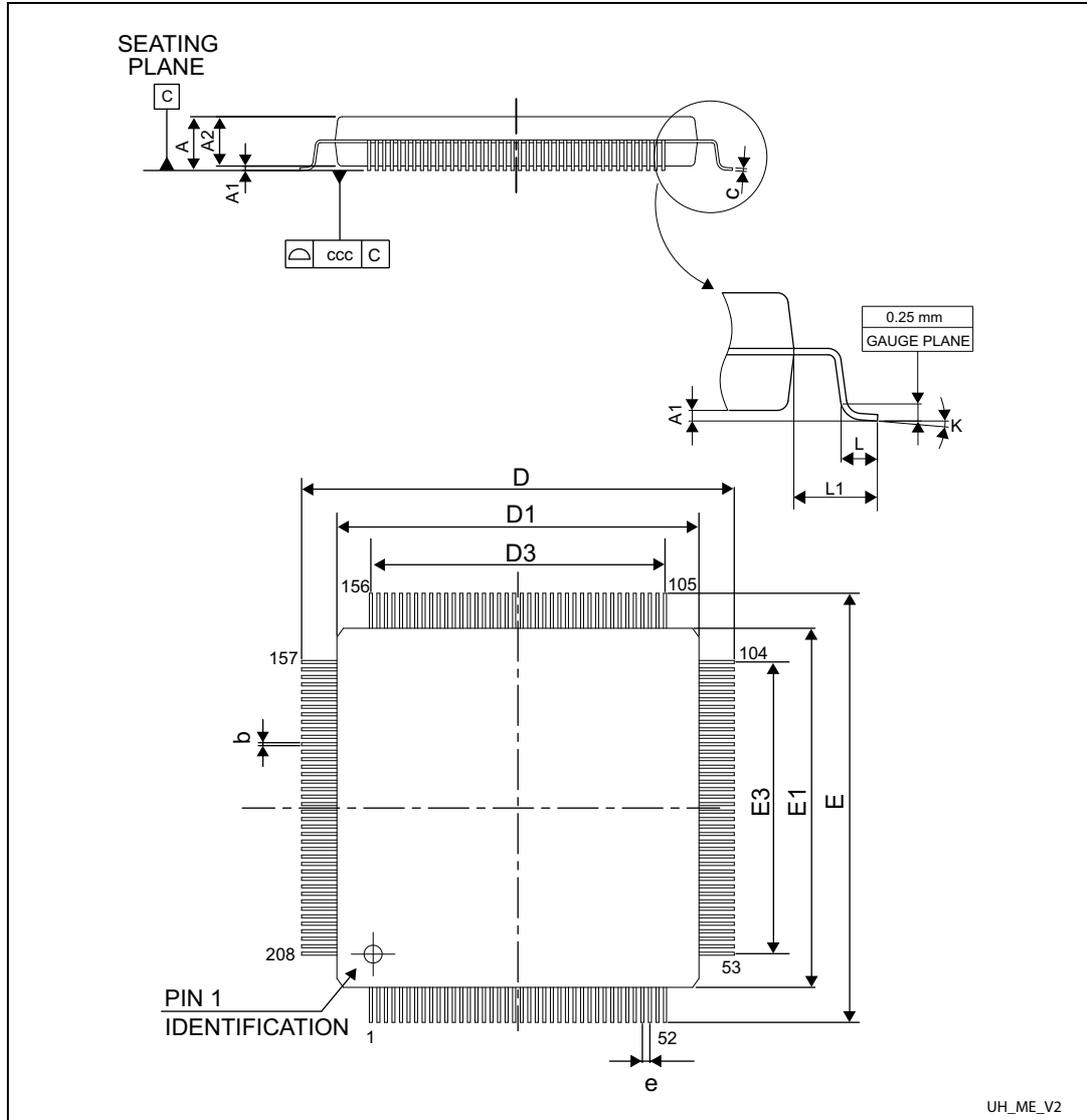


MS41047V1

1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.5 LQFP208 28 x 28 mm low-profile quad flat package information

Figure 96. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package outline



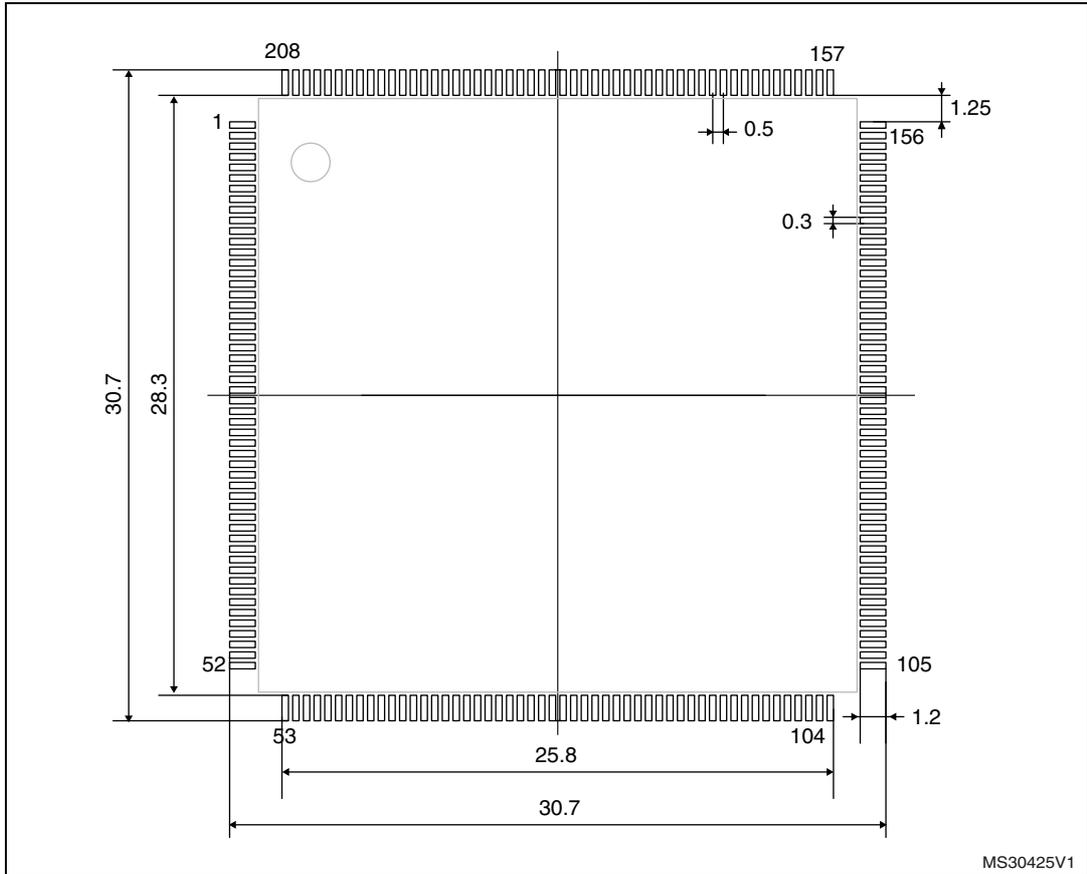
1. Drawing is not to scale.

Table 131. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	--	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1732	1.1811	1.1890
D1	27.800	28.000	28.200	1.0945	1.1024	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1732	1.1811	1.1890
E1	27.800	28.000	28.200	1.0945	1.1024	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7.0°	0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 97. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

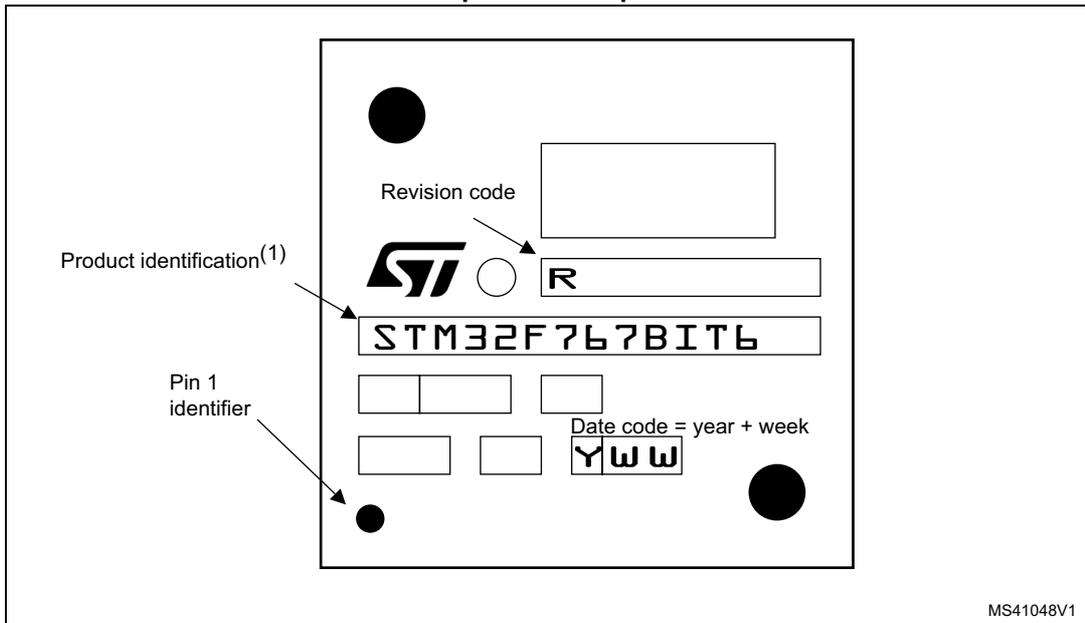
MS30425V1

LQFP208 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 98. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package top view example

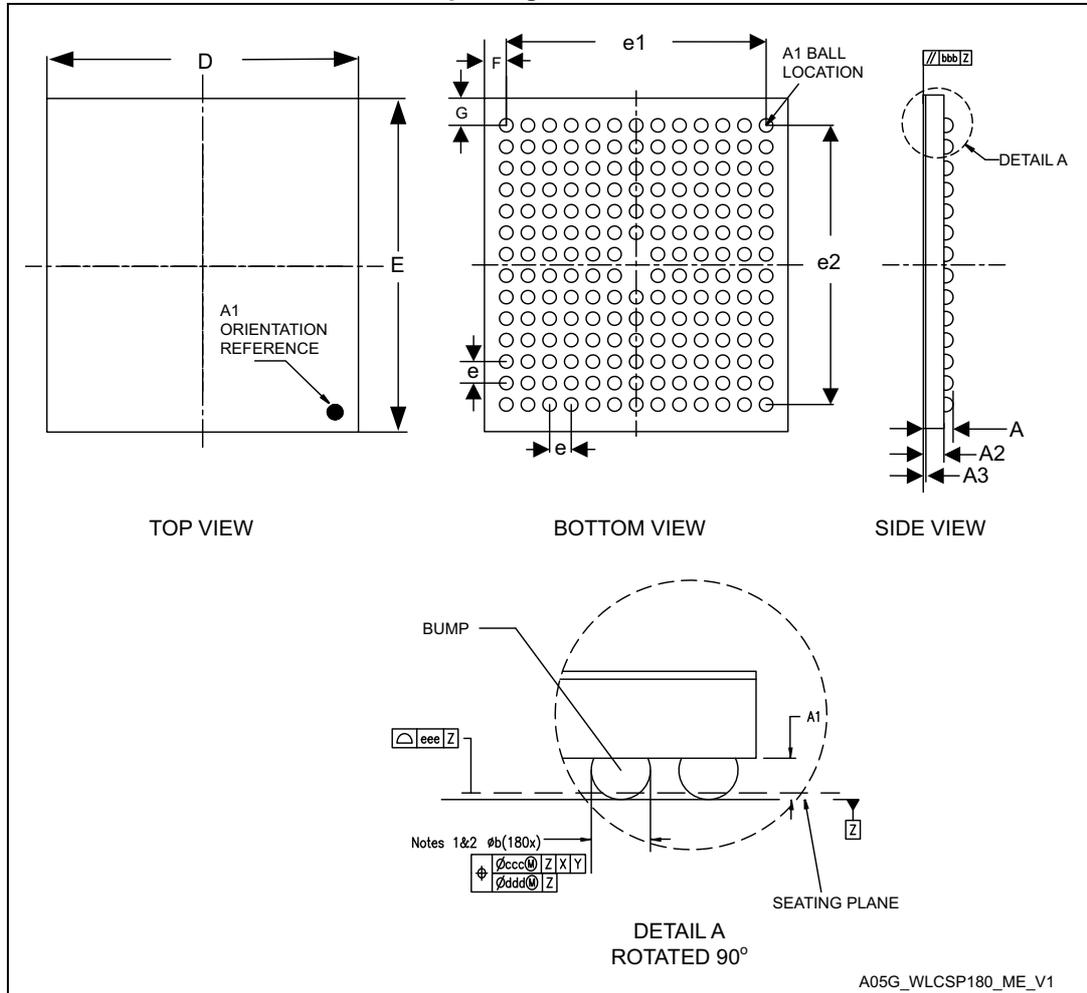


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6.6 WLCSP 180-bump, 5.5 x 6 mm, wafer level chip scale package information

Figure 99. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package outline



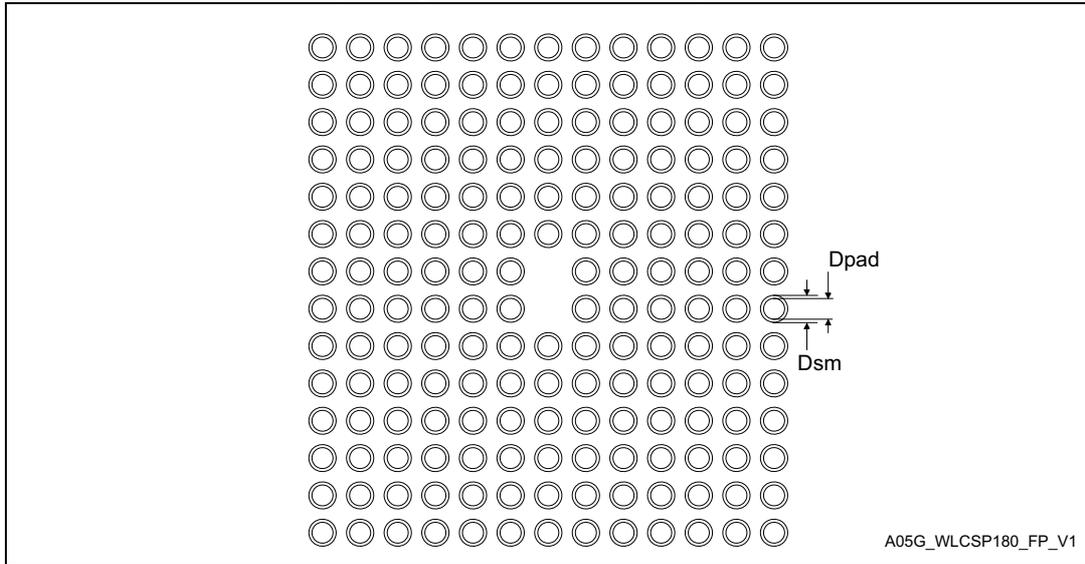
1. Drawing is not to scale.

Table 132. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b ⁽²⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	5.502	5.537	5.572	0.2166	0.2180	0.2194
E	6.060	6.095	6.130	0.2386	0.2400	0.2413
e	-	0.400	-	-	0.0157	-
e1	-	4.800	-	-	0.1890	-
e2	-	5.200	-	-	0.2047	-
F	-	0.368	-	-	0.0145	-
G	-	0.477	-	-	0.0188	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 100. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



1. Dimensions are expressed in millimeters.

Table 133. WLCSP 180-bump, 5.5 x 6 mm, recommended PCB design rules (0.4 mm pitch)

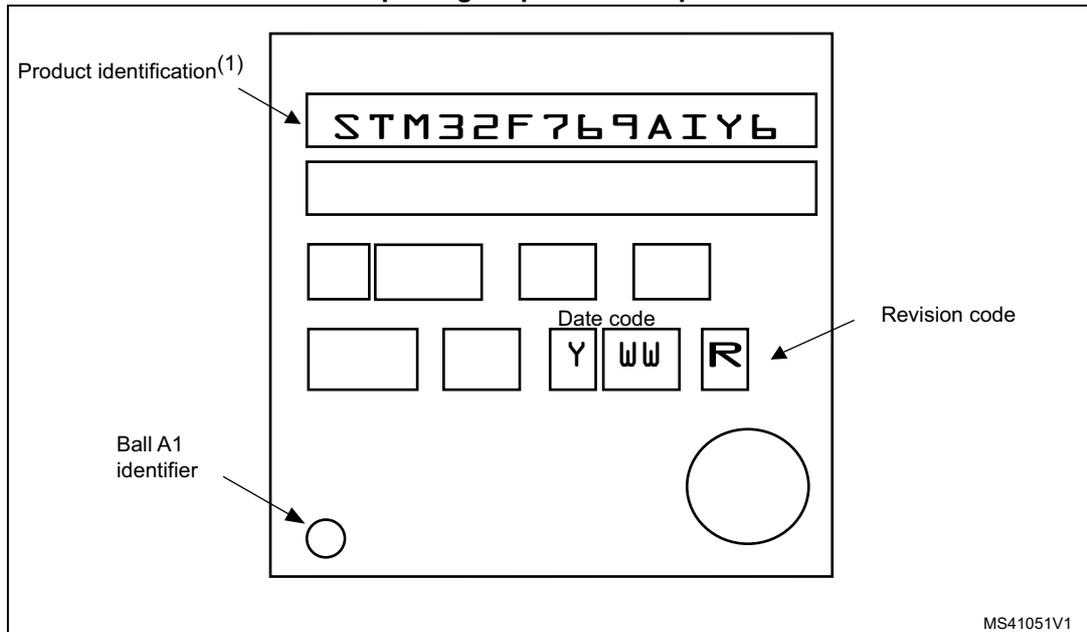
Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.1 mm

WLCSP180 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

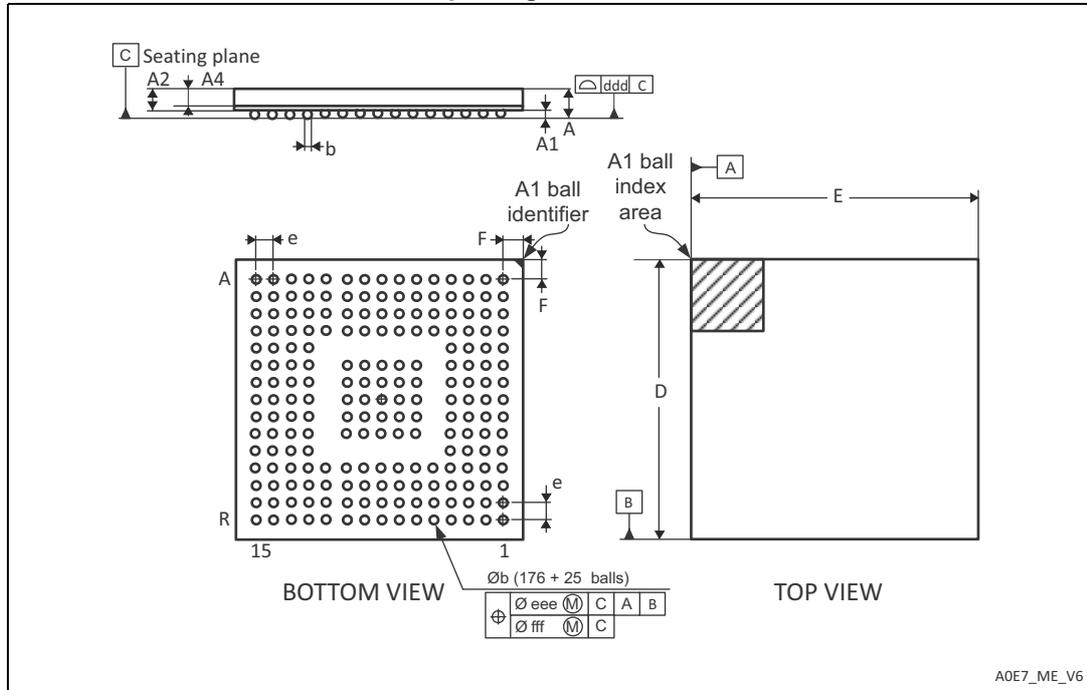
Figure 101. WLCSP180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package top view example



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6.7 UFBGA176+25, 10 x 10, 0.65 mm ultra thin fine-pitch ball grid array package information

Figure 102. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 134. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 103. UFBGA176+25, 10 x 10 mm x 0.65 mm, ultra fine-pitch ball grid array package recommended footprint

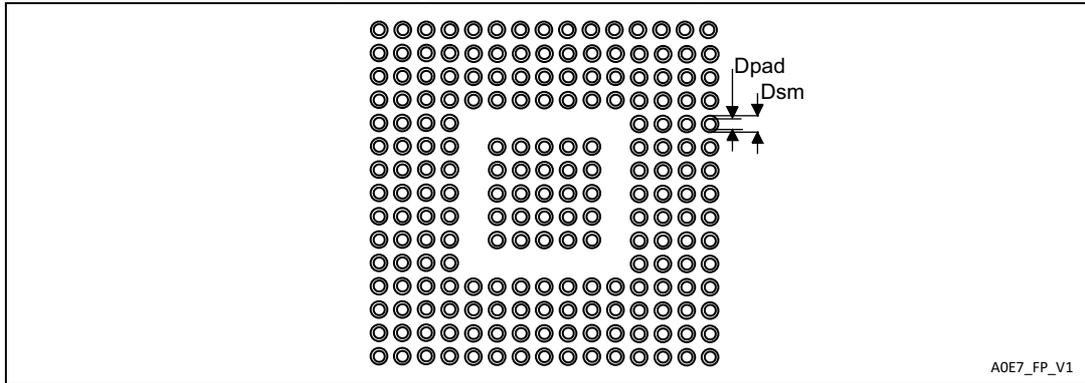


Table 135. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

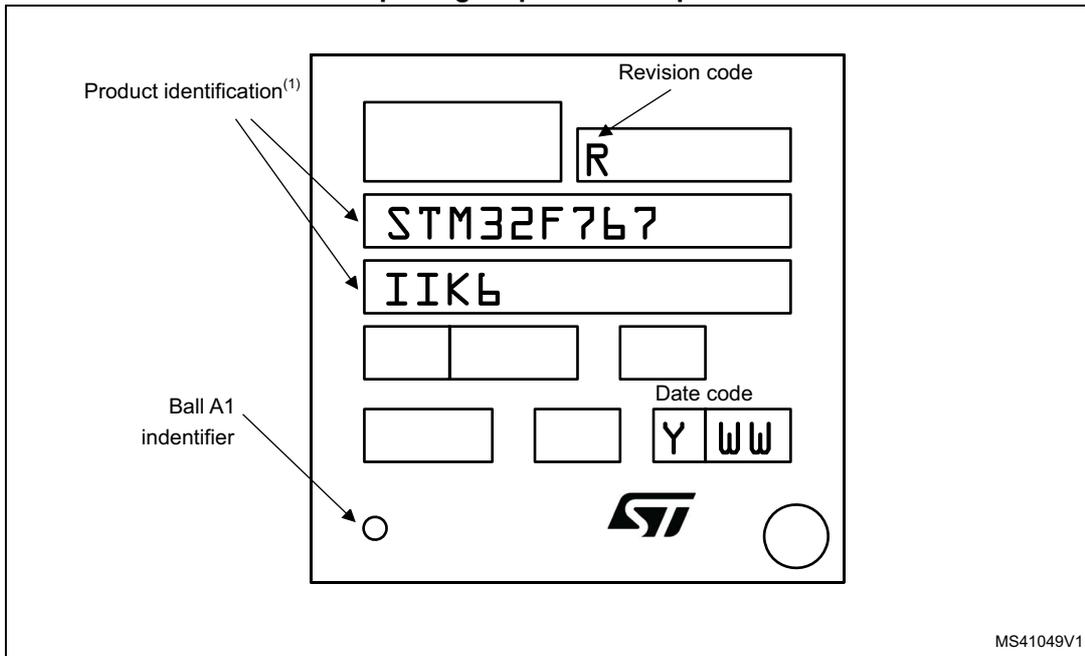
Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

UFBGA 176+25 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

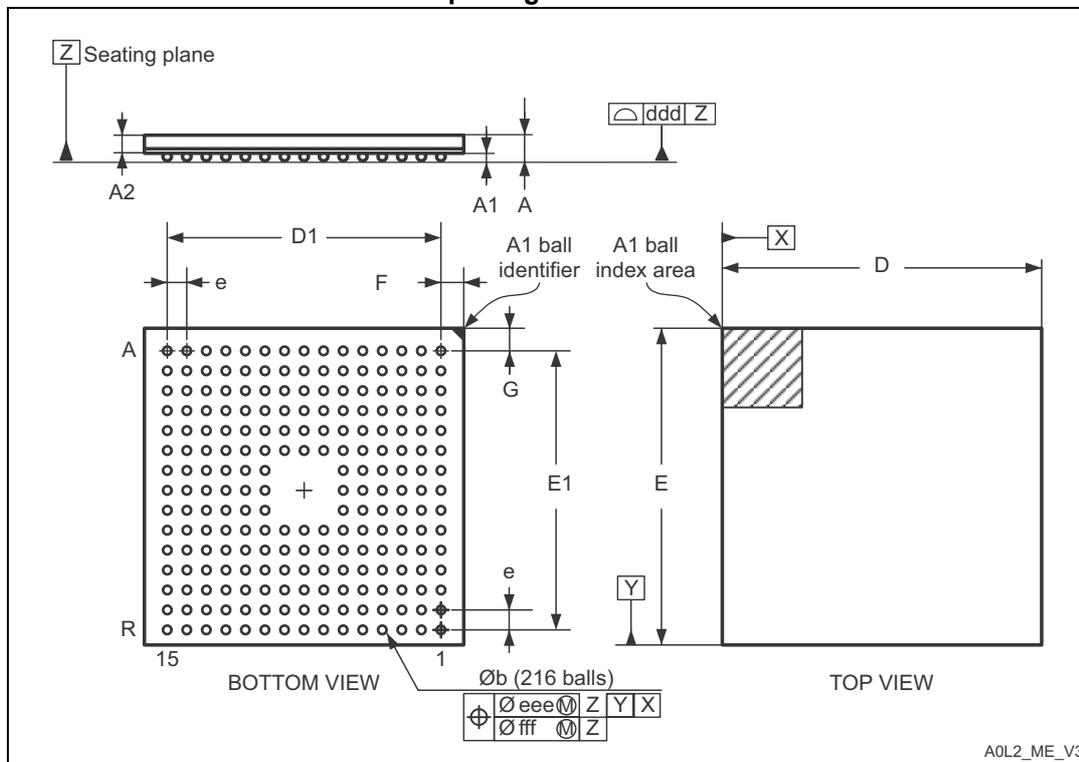
Figure 104. UFBGA 176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package top view example



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6.8 TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package information

Figure 105. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 136. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-

Table 136. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
G	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 106. TFBGA216, 13 x 13 mm, 0.8 mm pitch, thin fine-pitch ball grid array package recommended footprint

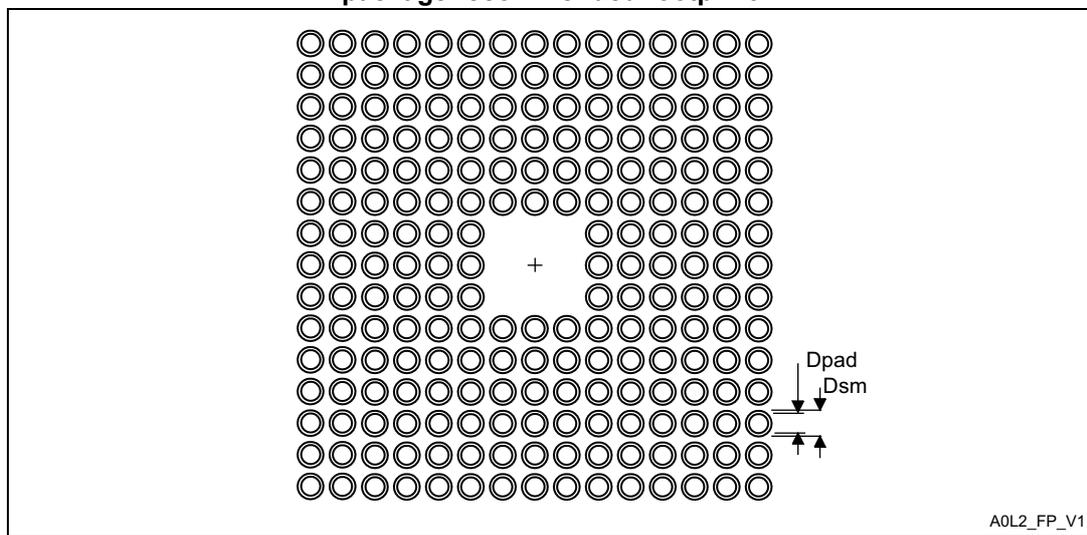


Table 137. TFBGA216 recommended PCB design rules (0.8 mm pitch BGA)

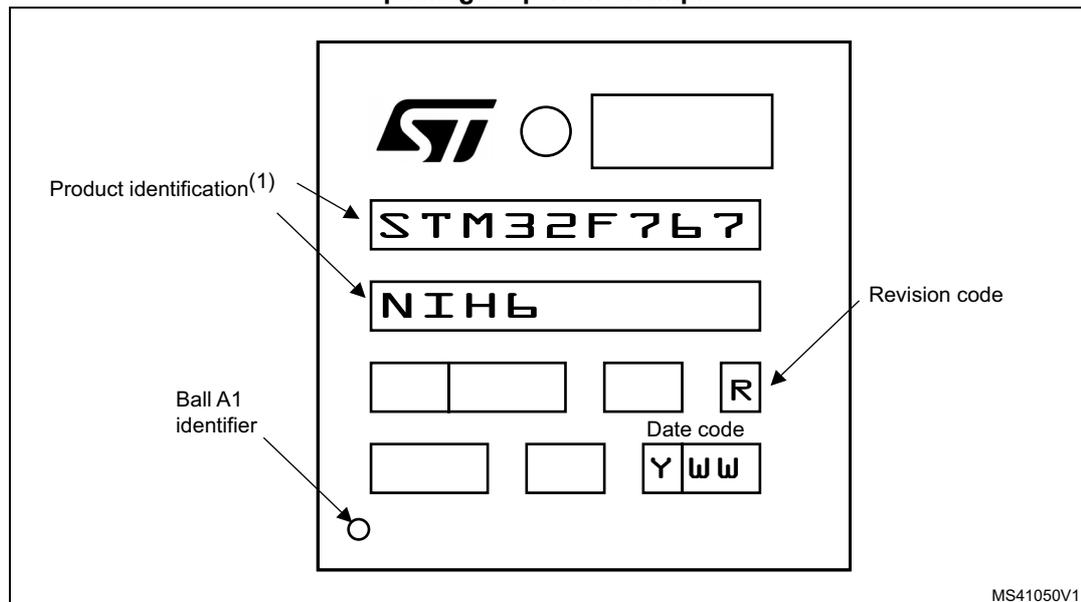
Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

TFBGA216 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 107. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package top view example



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6.9 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 138. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient TFBGA100 - 8 × 8 mm / 0.8 mm pitch	36.2	
	Thermal resistance junction-ambient WLCSP180 - 0.4 mm pitch	30	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Ordering information

Table 139. Ordering information scheme

Example:	STM32	F	76x	V	G	T	6	xxx
Device family	STM32 = Arm-based 32-bit microcontroller	F = general-purpose	765 = STM32F765xx, USB OTG FS/HS, camera interface, Ethernet 767 = STM32F767xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT 768 = STM32F768Ax, USB OTG FS/HS, camera interface, DSI host, WLCSP with internal regulator OFF 769 = STM32F769xx, USB OTG FS/HS, camera interface, Ethernet, DSI host	V = 100 pins Z = 144 pins I = 176 pins A = 180 pins B = 208 pins N = 216 pins	G = 1024 Kbytes of Flash memory I = 2048 Kbytes of Flash memory	T = LQFP K = UFBGA H = TFBGA Y = WLCSP	6 = Industrial temperature range, -40 to 85 °C. 7 = Industrial temperature range, -40 to 105 °C.	xxx = programmed parts TR = tape and reel
Product type								
Device subfamily								
Pin count								
Flash memory size								
Package								
Temperature range								
Options								

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.



Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}
- The over-drive mode is not supported

A.1 Operating conditions

Table 140. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states (f _{Flashmax})	Maximum Flash memory access frequency with wait states ⁽¹⁾⁽²⁾	I/O operation	Possible Flash memory operations
V _{DD} = 1.7 to 2.1 V ⁽³⁾	Conversion time up to 1.2 Msps	20 MHz	168 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from the Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to [Section 2.18.1: Internal reset ON](#)).

Revision history

Table 141. Document revision history

Date	Revision	Changes
21-Mar-2016	1	Initial release.
26-Apr-2016	2	<p>DFSDM replaced by DFSDM1 in:</p> <ul style="list-style-type: none"> – Table 11: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions. – Table 13: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping. – Table 14: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses. – Section 5.3.34: Digital filter for Sigma-Delta Modulators (DFSDM) characteristics. <p>Updated Table 2: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts adding DFSDM1 features.</p> <p>Updated Table 40: Peripheral current consumption adding DFSDM1 current consumption.</p> <p>Updated cover in 2 pages.</p> <p>Update cover replacing for SPI 'up to 50 Mbit/s' by 'up to 54 Mbit/s'.</p>
06-May-2016	3	<p>Updated Table 2: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts GPIO number.</p> <p>Updated Table 13: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping adding CAN3_RX alternate function on PA8/AF11.</p>
22-Dec-2016	4	<p>Updated Table 98: Dynamics characteristics: Ethernet MAC signals for RMII.</p> <p>Updated Table 72: ADC characteristics sampling rate.</p> <p>Updated all the notes removing 'not tested in production'.</p> <p>Updated Figure 47: SPI timing diagram - slave mode and CPHA = 0 and Figure 48: SPI timing diagram - slave mode and CPHA = 1(1) with modified NSS timing waveforms (among other changes).</p> <p>Updated Table 122: LTDC characteristics clock output frequency at 65 MHz.</p> <p>Updated Section 5.2: Absolute maximum ratings.</p> <p>Updated Section 6: Package information adding information about other optional marking or inset/upset marks.</p>

Table 141. Document revision history (continued)

Date	Revision	Changes
09-Aug-2017	5	<p>Updated note 1 below all the package device marking figures. Updated cover title. Updated Section 1: Description. Updated Section 2.47: DSI Host (DSIHOST) video mode interface features. Added Table 9: DFSDM implementation. Updated Figure 11: STM32F76xxx LQFP100 pinout pin 43 and pin 44. Updated Table 65: I/O current injection susceptibility note by 'injection is not possible'. Updated Table 122: LTDC characteristics LTDC clock frequency at 83 MHz. Updated Table 72: ADC characteristics R_{ADC} min at 1.5 Kohm. Updated Figure 41: Recommended NRST pin protection note about the 0.1uF capacitor. Updated Table 83: DAC characteristics R_{LOAD} feature.</p>
11-Sep-2017	6	<p>Added TFBGA100 package: – Updated cover page. – Updated Table 2: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts. – Updated Table 4: Regulator ON/OFF and internal reset ON/OFF availability. – Added Figure 12: STM32F76xxx TFBGA100 pinout. – Updated Table 11: STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions. – Updated Table 18: General operating conditions. – Updated Table 63: ESD absolute maximum ratings. – Updated note below Figure 44: Power supply and reference decoupling (VREF+ not connected to VDDA). – Updated note below Figure 45: Power supply and reference decoupling (VREF+ connected to VDDA). – Added Section 6.2: TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package information. – Updated Table 138: Package thermal characteristics.</p>

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