XR-T6166

Codirectional Digital Data Processor

...the analog plus company™

Dec 2010

FEATURES

- Low Power CMOS Technology
- All Receiver and Transmitter Inputs and Outputs are TTL Compatible
- Transmitter Inhibits Bipolar Violation Insertion for Transmission of Alarm Conditions
- Alarm Output Indicates Loss of Received Bipolar Violations
- Tolerance of 125µs Variance of Data Transfer Timing in Both Transmit and Receive Paths Allows Operation in Plesiochronous Networks
- Both Receiver and Transmitter Perform Byte Insertion or Deletion in Response to Local Clock Slips and Provide Outputs Indicating Slip Logic Activity

APPLICATIONS

- CCITT G.703 Compliant 64kbps Codirectional Interface
- Performs the Digital and Analog Functions for a Complete 64kbps Data Adaption Unit (DAU) When Used With the XR-T6164

GENERAL DESCRIPTION

The XR-T6166 is a CMOS device which contains the digital circuitry necessary to interface both directions of a 64kbps data stream to 2.048Mbps transmit and receive PCM time-slots. The XR-T6166 and the companion XR-T6164 line interface chip together form a CCITT G.703 compliant 64kbps codirectional interface.

The XR-T6166 contains separate transmit and receive sections. The transmitter transforms 8 bit serial data from a 2.048Mbps time-slot into an encoded 64kbps data stream. The receiver , which performs the reverse operation, decodes the 64kbps data, extracts a clock signal, and then outputs the data to a 2.048Mbps time-slot. The XR-T6166 provides features which allow the repetitions and deletions of both received and transmitted data as clock skews and transients occur . These slip occurrences are indicated by byte insertion and deletion flags. Outputs are also provided for extracted receive clock and clock recovery circuit loss of lock.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-T6166CD	28 Lead 300 Mil JEDEC SOIC	0°C to +70°C
XR-T6166ID	28 Lead 300 Mil JEDEC SOIC	–40°C to 85°C

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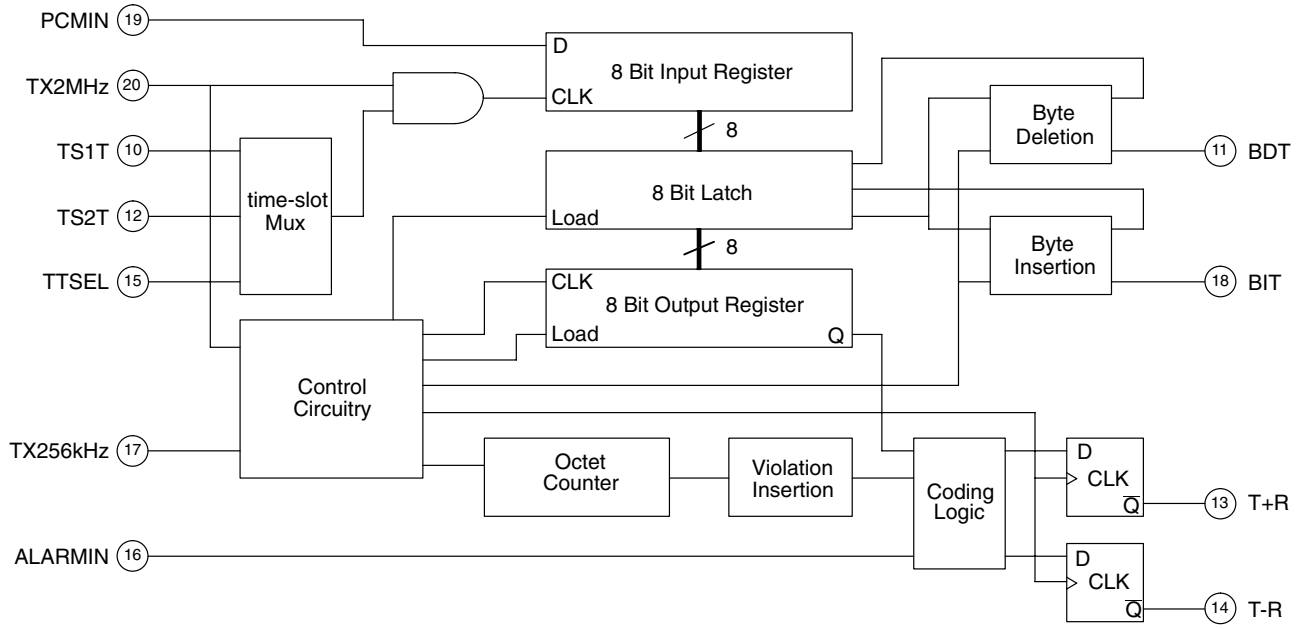


Figure 1. XR-T6166 Transmitter Section Block Diagram

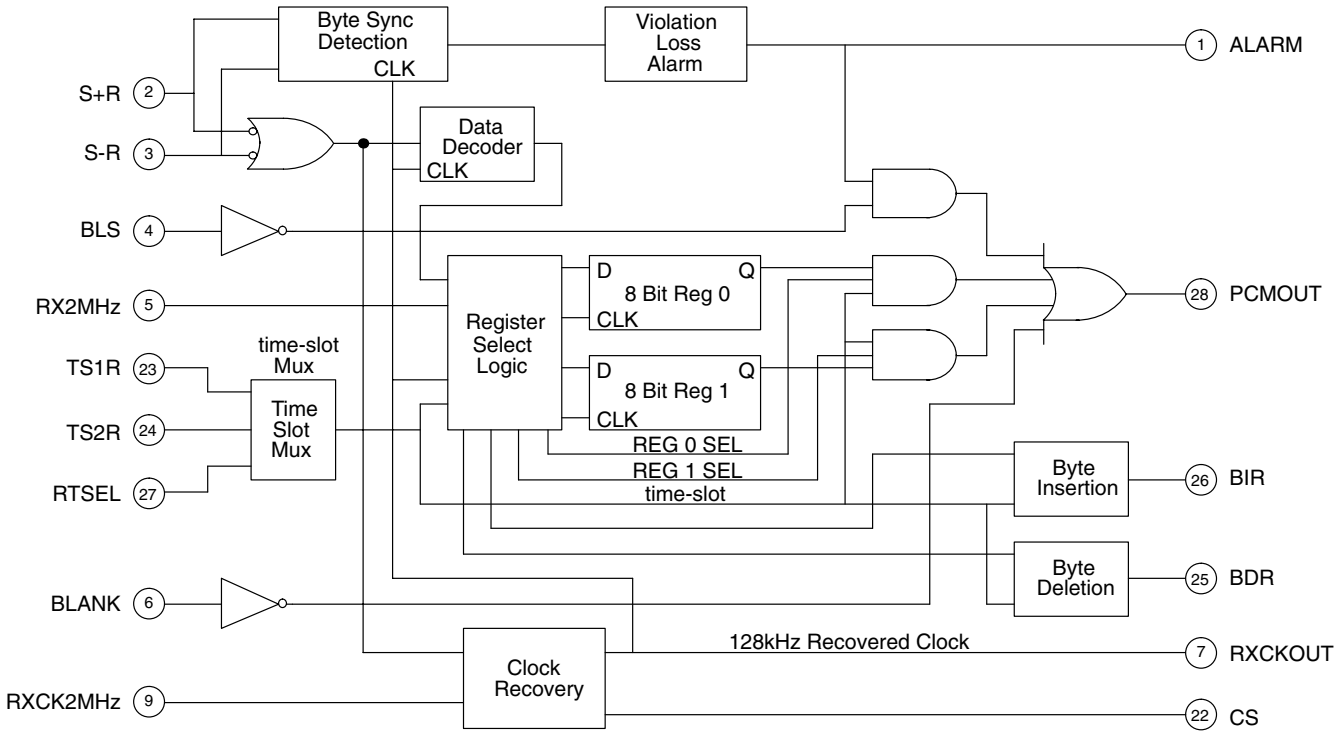
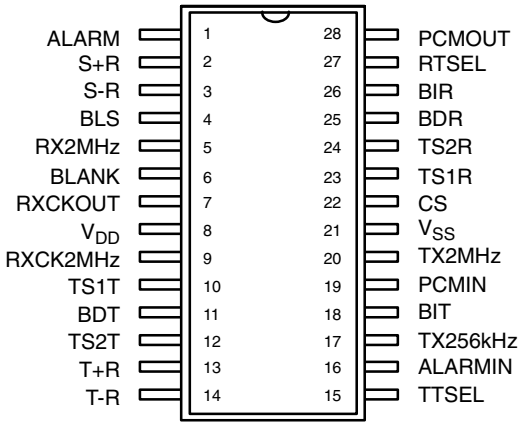


Figure 2. XR-T6166 Receiver Section Block Diagram

PIN CONFIGURATION



28 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	ALARM	O	**Octet Timing Alarm**. When active, indicates loss of received bipolar violations that are used for octet timing. Active high.
2	S+R	I	**Positive AMI Data to Receiver.** Positive data from the XR-T6164 receive-side. Active low.
3	S-R	I	**Negative AMI Data to Receiver.** Negative data from the XR-T6164 receive-side. Active low.
4	BLS	I	**Byte Locking Supervision.** When active, causes blanking of PCMOUT under received alarm conditions. Active low.
5	RX2MHz	I	**Receiver 2.048MHz Clock**. Used to clock out PCM data.
6	BLANK	I	**PCMOUT Data Blanking**. When active, forces PCMOUT data to all ones (AIS). Active high.
7	RXCKOUT	O	**128kHz Extracted Clock.** Clock recovered from received data.
8	V_{DD}		**+5V ±10% Power Source.**
9	RXCK2MHz	I	**2.048MHz Clock.** Used by receiver clock recovery circuit.
10	TS1T	I	**Transmitter Time-slot 1 Input**.
11	BDT	O	**Transmitter Byte Deletion Flag**. Active when a transmit byte is deleted. Active high.
12	TS2T	I	**Transmitter Time-slot 2 Input.**
13	T+R	O	**Transmit Positive AMI Data Output**. Data to XR-T6164 positive transmitter input. Active low.
14	T-R	O	**Transmit Negative AMI Data Output.** Data to XR-T6164 negative transmitter input. Active low.
15	TTSEL	I	**Transmit Time-slot Select.** When high, pin 10 is selected; when low, pin 12 is selected.
16	ALARMIN	I	**Alarm Input.** When active, inhibits insertion of violations used for octet timing in transmitter output. Active high.

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Type	Description
17	TX256kHz	I	**Transmitter 256kHz Clock**. Used to output 64kbps encoded data.
18	BIT	O	**Transmitter Byte Insertion Flag.** Active when a transmit byte is repeated. Active high.
19	PCMIN	I	**Transmitter PCM Input.** Data read from the system PCM bus.
20	TX2MHz	I	**Transmitter 2.048MHz Clock.** Clocks PCM data in PCMIN.
21	V_{SS}		**Ground.**
22	CS	O	**Clock Seek.** Indicates that clock recovery circuit has loss of lock with received data. Active high.
23	TS1R	I	**Receiver Time-slot 1 Input.**
24	TS2R	I	**Receiver Time-slot 2 Input.**
25	BDR	O	**Receiver Byte Deletion Flag.** Active when received data byte is deleted. Active high.
26	BIR	O	**Receiver Byte Insertion Flag**. Active when a received data byte is repeated. Active high.
27	RTSEL	I	**Receive Time-slot Select**. When high, pin 23 is selected; when low, pin 24 is selected.
28	PCMOUT	O	**Received PCM Output Data**. Data sent to the system PCM bus.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5V ±10%, T_A = 25°C, Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC Electrical Characteristics						
V_{IH}	Logic 1	2.4			V	
V_{IL}	Logic 0			0.4	V	
V_{DD}	Supply	4.5		5.5	V	
I_{DD}	Supply Current		500		µA	Dynamic Supply Current
I_{IL}	Input Leakage			1	µA	
V_{OL}				0.4	V	At 1.6mA
V_{OH}		2.4			mA	At 0.4mA
AC Electrical Characteristics						
General						
tr, tf	Output Rise/Fall Time			20	ns	All Outputs
Receiver						
tRS	RX2MHz Rising Edge to TS Rising Edge Set Up Time	0		tRXL-100	ns	*Figure 3*
tRH	RX2MHz Rising Edge to TS Falling Edge Hold Time	0		tRXL-100	ns	*Figure 3*
tDRS	TS Rising Edge to Leading Edge of PCMOUT D0 Bit Delay			10	ns	*Figure 3*
tDRH	TS Falling Edge to Trailing Edge of PCMOUT D7 Bit Hold Time	0		10	ns	*Figure 3*
tRXD	RX2MHz Rising Egde to PCMOUT Bits D1 Through D6 Rising Edge Delay			10	ns	*Figure 3*
tPW	PCMOUT Pulse Width		488		ns	*Figure 3*
tRXH	RX2MHz High Time		244		ns	*Figure 3*
tRXL	RX2MHz Low Time		244		ns	*Figure 3*
tRXCLK	RX2MHz Period		488		ns	±100ppm
Transmitter						
tTS	TS Rising Edge to TX2MHz Set Up Time	20		tTXL-100	ns	*Figure 5*
tTH	TS Falling Edge to TX2MHz Hold Time	0		tTXL-100	ns	*Figure 5*
tDS	PCMIN Edge to TX2MHz Set Up Time	100			ns	*Figure 5*
tDH	PCMIN Edge to TX2MHz Hold Time	100			ns	*Figure 5*
tTXH	TX2MHz High Time		244		ns	*Figure 5*
tTXL	TX2MHz Low Time		244		ns	*Figure 5*
tTXCLK	TX2MHz Period		488		ns	±100ppm

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
AC Electrical Characteristics (Cont'd)						
Transmitter (Cont'd)						
tKXH	TX256kHz High Time		1.95		µs	
tKXL	TX256kHz Low Time		1.95		µs	
tKXCLK	TX256kHz Period		3.9063		µs	
tBDTH	BDT High Time	488			ns	
tBITH	BIT High Time	12.5			µs	
tALH	ALARMIN High Time	15.6			µs	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 20V
Operating Temperature . . . . . .0°C to +70°C
Storage Temperature . . . . . .-65°C to +150°C

Magnetic Supplier Information:

Pulse
Telecom Product Group
P.O. Box 12235
San Diego, CA 92112
Tel. (619) 674-8100
Fax. (619) 674-8262

Transpower Technologies, Inc.
24 Highway 28, Suite 202
Crystal Bay, NV 89402-0187
Tel. (702) 831-0140
Fax. (702) 831-3521

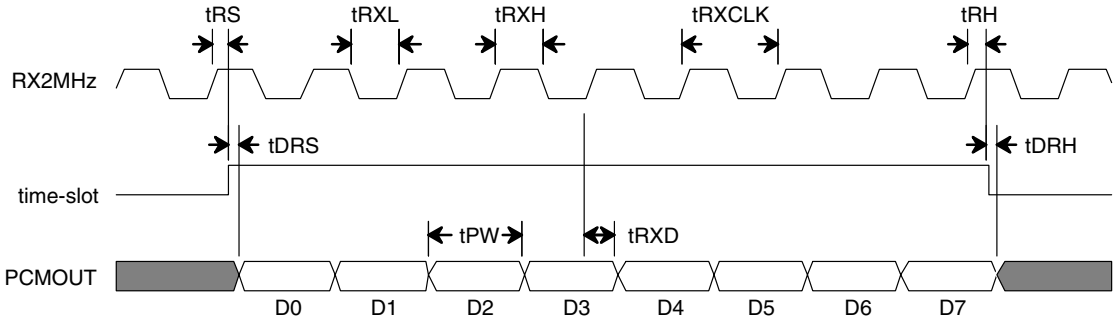


Figure 3. Receive Time-slot Timing

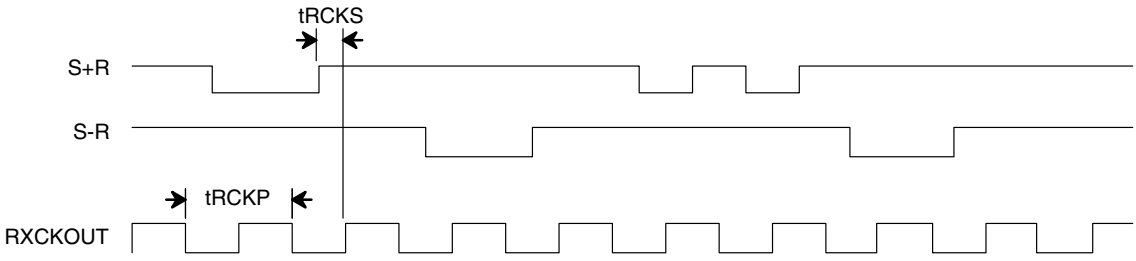


Figure 4. Extracted Clock Timing

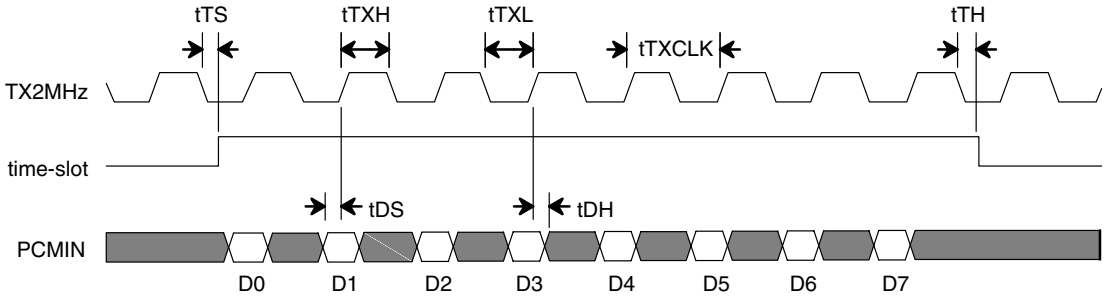


Figure 5. Transmit Time-slot Timing

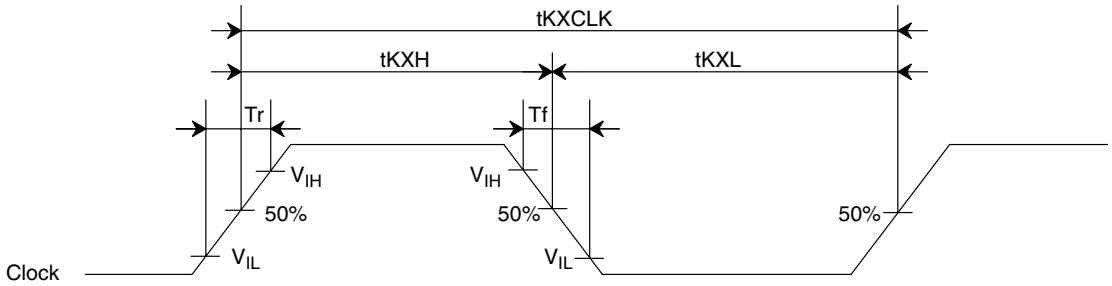


Figure 6. Clock Timing

SYSTEM DESCRIPTION

Transmitter

Figure 1 shows the XR-T6166 transmitter section block diagram. The transmitter converts eight bit bursts or octets of 2.048Mbps serial data present in a PCM time-slot to a coded continuous 64kbps data stream. During operation, data input is controlled by external clock and time-slot signals, and the 64kbps data output is timed by an external 256kHz clock. Since the input and output rates may not be exactly equal because of slight clock rate dif ferences, periodic slips can occur . Therefore, circuitry is included to delete or repeat octets, if necessary. Transmitter operation is as follows.

PCM data is applied to PCMIN (pin 19), a 2.048MHz local clock is applied to TX2MHz (pin 20), and a time-slot signal is applied through the time-slot multiplexer . This multiplexer allows the transmitter to be hard wired totwo time-slot positions. A time-slot signal is applied to multiplexer inputs TS1T (pin 10) or TS2T (pin 12), and a time-slot select logic level is applied to TTSEL (pin 15). A high level at TTSEL selects TS1T while a low level enables TS2T. The time-slot is an envelope derived externally from TX2MHz that covers eight clock pulses. The rising edge of the time-slot signal should be made to coincide with the falling edge of TX2MHz. Eight bits of PCM data are clocked into the transmitter input register on the rising edge of TX2MHz while the selected time-slot signal is high. The input register data is then transferred to a storage latch.

Transmission of 64kbps data is controlled by the 256kHz local clock that is applied to TX256kHz (pin 17). It is not necessary for this clock to be synchronized with any other signals that are applied to the transmitter . The output process begins by transferring data from the storage latch to the output shift register after transmission of the previous eight bits of data is complete. Four periods of TX256kHz are required to encode each data bit. A “logic 0” applied to PCMIN is coded as 0101 while a “logic 1” is coded as 0011. This data is output on either T+R (pin 13) or T-R (pin 14) according to the AMI (alternate mark inversion) coding rule. Note that the T+R and T-R outputs as well as the corresponding XR-T6164 transmitter inputs (TX+I/P, TX-I/P) are all active-low. Therefore, a “logic 0” is coded as a 1010 and a “logic 1” as a 1100 at the bipolar transmitter output as specified by CCITT G.703. Transmission of octet timing is performed by feeding the seventh and eighth data bits in each word to the same transmitter output. This function may be inhibited by setting ALARMIN (pin 16) high to transmit an alarm condition.

Should skew occur between the TX2MHz and TX256kHz clocks signals, or during an adjustment of the timing of the time-slot signal, circuitry is included to delete or repeat complete words of data. This could happen, for example, when changing from one time-slot position to another . Outputs are provided to indicate when a data byte is inserted or deleted. A byte repetition or insertion occurs once if no new PCM data is received. The BIT flag (pin 18) is active during the transmission of inserted data. A byte repetition just occurs once. If no new PCM data is received, the T+R and T -R outputs stay high. A byte deletion occurs when the transmitter receives a new byte of data before the previous byte is transferred from the storage latch to the output register. Under this condition, the stored data is overwritten and the BDT flag (pin 1) is active.

Receiver

Figure 2 shows the block diagram of the XR-T6166 receiver section. The receiver converts coded continuous 64kbps data to eight bit bursts of 2.048Mbps serial data suitable for insertion in a PCM time-slot. During operation, data input is timed by a clock that is extracted from the input signal, while output is controlled by external locally supplied clock and time-slot signals. Since the data input and output rates may not be exactly equal, circuitry is included to delete or repeat eight bit data blocks, if necessary. Receiver operation is as follows.

A line interface chip such as the receive section of the XR-T6164 converts the encoded bipolar 64kbps signal to dual-rail active-low logic levels. These signals are applied to the XR-T6166 receiver S+R (pin 2) and S-R (pin 3) inputs. A 128kHz clock, which is derived from the received signal, is used to decode this data, and then to clock it into one of two storage registers. T wo registers are used so that one may be receiving continuous data at 64kbps while the other is sending eight bit bursts at a 2.048Mbps rate to PCMOUT (pin 28) while the receiver time-slot signal is high. The time-slot is an envelope derived externally from RX2MHz (pin 5) that covers eight clock pulses. The rising edge of the time-slot signal should be made to coincide with the rising edge of RX2MHz. Eight bits of PCM data are clocked out of the receiver register on the rising edge of RX2MHz while the

time-slot signal is high. A two input multiplexer at the time-slot input allows the receiver to be hard wired to two time-slot positions. time-slot signals are applied to TS1R (pin 23) and TS2R (pin 24) and the active time-slot is selected by R TSEL (pin 27). A high level applied to RTSEL selects TS1R and a low level selects TS2R. Data appearing at PCMOUT is framed by the read time-slot signal and is guaranteed glitch free.

Recovery of the 128kHz timing signal is performed by a variable length counter which is clocked by the 2.048MHz signal applied to RXCK2MHz (pin 9). This clock is not required to be synchronized with any other signals that are applied to the XR-T6166. However , the RX2MHz clock may also be used for this function. Positive input data transitions are used to synchronize this counter with the data. If synchronization is lost, the counter length is shortened, and the clock recovery circuit enters a seek mode until a transition is found. This mode is identified by a high level at the CS output (pin 22). The extracted 128kHz signal is available at RXCKOUT (pin 7).

Octet timing ensures that bit grouping is maintained when the data is converted from a 64kbps continuous stream to eight bit 2.048Mbps bursts. Bipolar violations are used to identify the last bit in each eight bit octet. In the absence of these violations, for example when receiving a transmitted alarm condition (transmitter ALARMIN is high), the circuit will continue to operate in synchronization with respect to the last received violation. During this time, the data present at PCMOUT is still correct as long as synchronization based on the last received violation is still valid, and the BLS input (pin 4) is held high. However , if BLS is low and an octet timing violation is not received, receiver output data is blanked by forcing PCMOUT to a high level. Also, if eight successive octet timing violations are not received, the ALARM output (pin 1) goes to a high level. A high level applied to the BLANK input (pin 6) will also force PCMOUT to an all-ones state.

Slip control logic is included in the receiver to accommodate rate differences between input and output data. The 64kbps input rate is determined by the remote transmitter, while the PCMOUT rate is set by RX2MHz which is a local clock. If this clock is slow, an octet will be deleted periodically, while the last octet will be repeated under fast conditions. Octet timing is maintained during these operations. Outputs are provided to indicate when an octet is inserted or deleted. The BIR flag (pin 26) is high when PCMOUT data is repeated, and the BDR flag (pin 25) is high when the receiver deletes an octet.

APPLICATION INFORMATION

64kbps Codirectional Interface

Figure 7 shows a codirectional interface circuit using the XR-T6166 with the XR-T6164 line interface. The XR-T6164 first converts the bipolar 64kbps transmit and receive signals to active-low TTL compatible data required by the XR-T6166. The XR-T6166 then performs the digital functions that are necessary to interface this 64kbps continuous data to a 2.048Mbps PCM time-slot. The 64kbps signals that have been attenuated and distorted by the twisted pair cable are transformer-coupled to the line side of the XR-T6164 as shown on the left side of *Figure 7.* A suggested transformer for both the input and output applications is the pulse type PE-65535.

The right side of *Figure 7* shows the XR-T6164 LOS (Loss of Signal) output and the XR-T6166 digital inputs and outputs. All of these pins are TTL compatible. Please refer to the Pin Description section of this data sheet for detailed information about each signal.

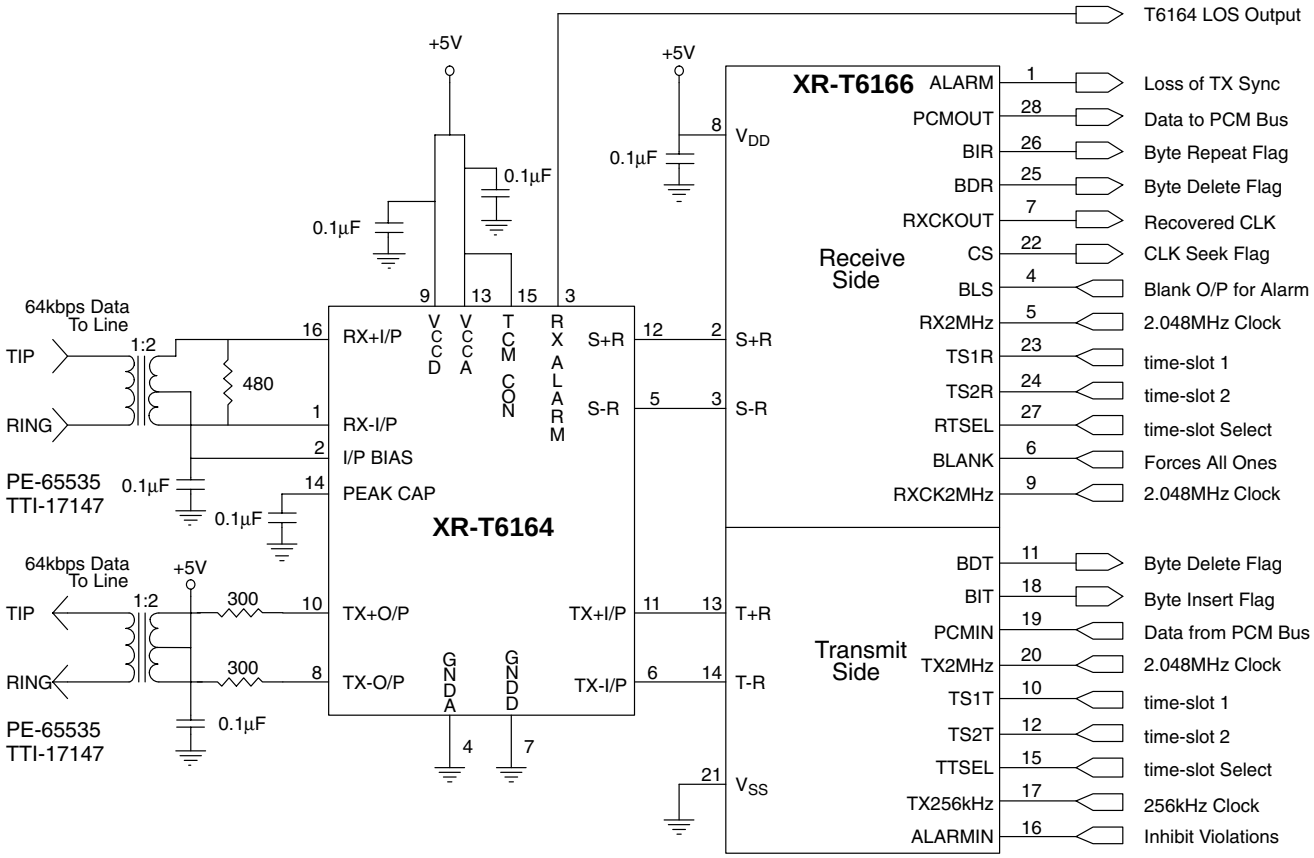


Figure 7. Typical Codirectional Application Circuit

Transmitter Code Conversion

Figure 8 shows the transmitter code conversion process that CCITT G.703 specifies for a 64kbps codirectional interface.

Step 1 - A 64kbps bit period is divided into four unit intervals.

Step 2 - A binary 1 is coded as a 1100.

Step 3 - A binary 0 is coded as a 1010.

Step 4 - The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 - The alternation in polarity of the blocks is violated every eighth block. The violation block marks the last bit in an octet.

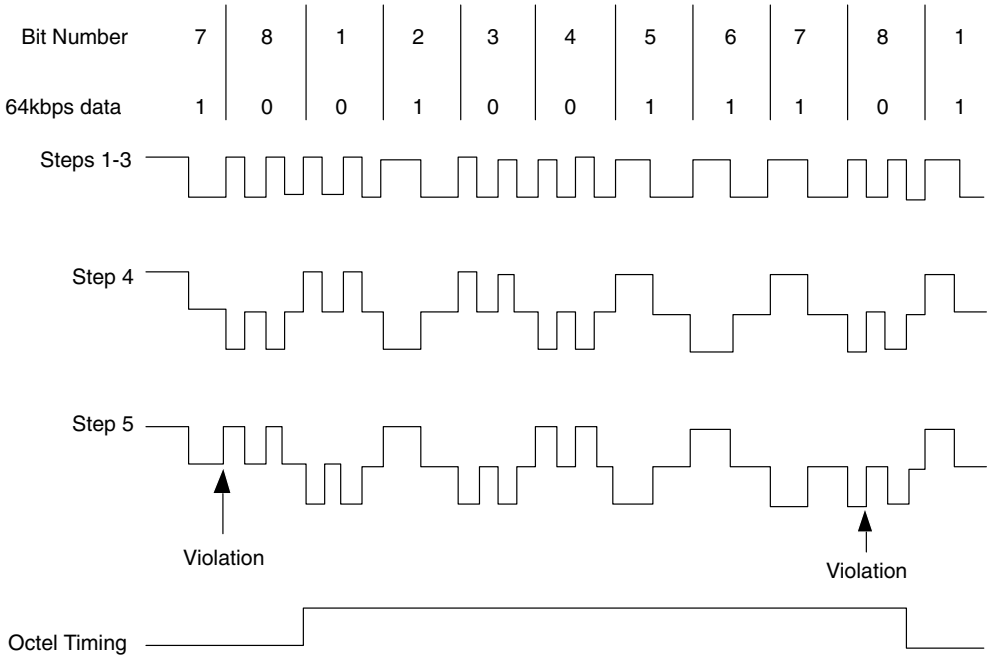


Figure 8. Transmitter Code Conversion for a 64kbps Bipolar Line Signal

Codirectional Interface Pulse Masks

Figure 9 and *Figure 10* show the CCITT G.703 64kbps codirectional interface pulse masks for single and double pulses respectively of either polarity. Note that this mask is for the pulse measured at the XR-T6164 transmitter output (application circuit shown in *Figure 5*) when terminated with a 120Ω resistor.

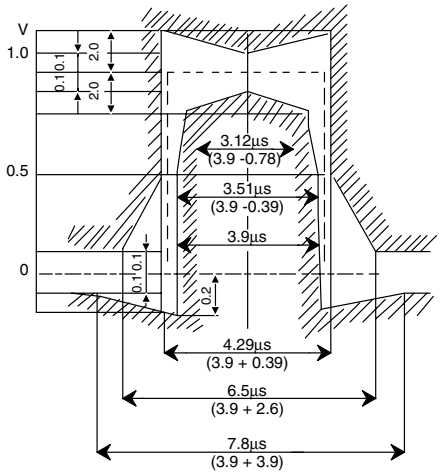


Figure 9. Mask for a Single Pulse

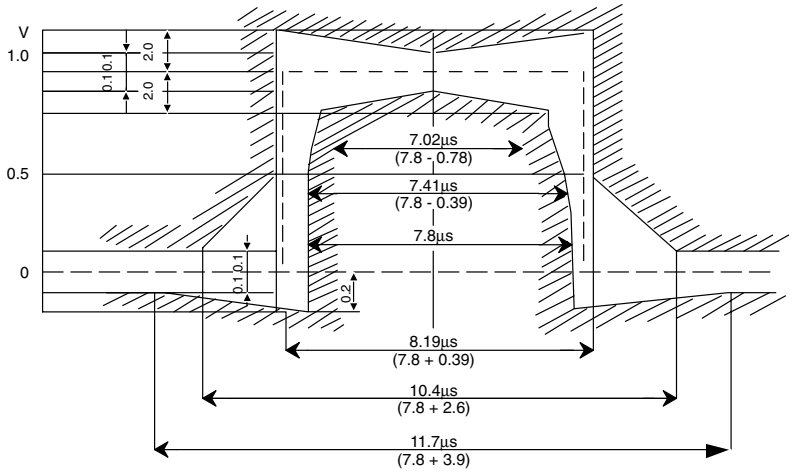
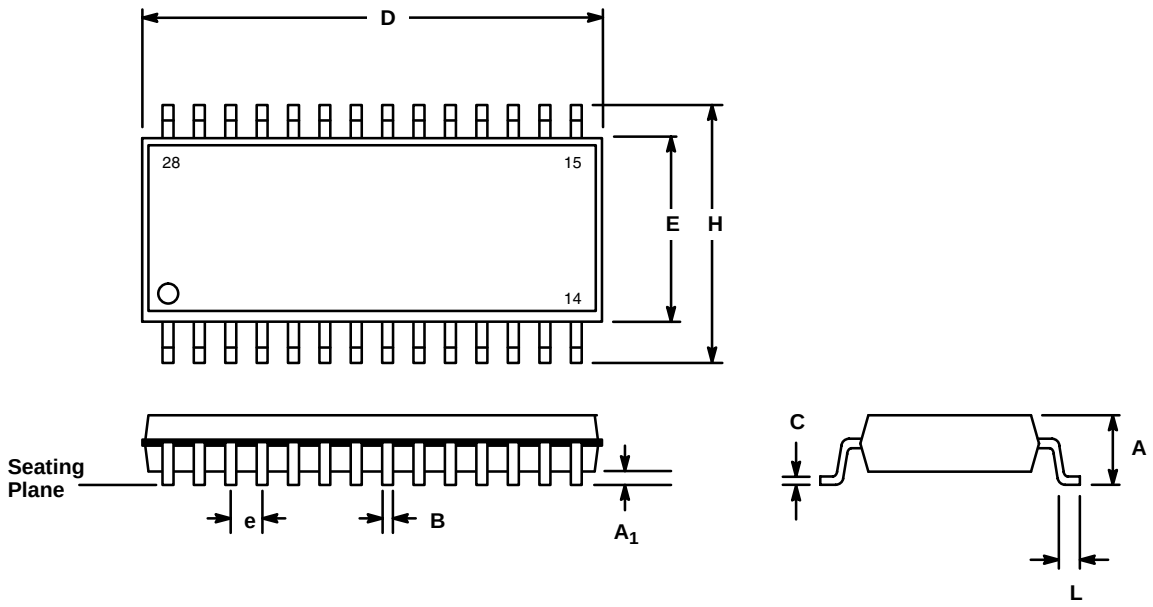


Figure 10. Mask for a Double Pulse

28 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

Notes

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Телефон: 8 (812) 309-75-97 (многоканальный)
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Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А