

Description

The F2270 is a 75Ω, low insertion loss voltage variable RF attenuator (VVA) designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 5MHz to 3000MHz. In addition to providing low insertion loss, the F2270 provides excellent linearity performance over its entire attenuation range.

The F2270 uses a positive supply voltage of 3.3V or 5V. Other features include a V_{MODE} pin allowing either a positive or negative voltage control slope versus attenuation and multi-directional operation where the RF input can be applied to either the RF1 or RF2 pins. The attenuation control voltage range is from 0V to 5V using either a 3.3V or 5V power supply.

Competitive Advantage

The F2270 provides extremely low insertion loss and superb IP3, IP2, return loss performance, and slope linearity across the control range. Compared to the previous state-of-the-art for silicon VVAs, this device provides superior performance:

- Operation down to 5MHz
- Insertion loss at 300MHz of 1.1dB
- Typical attenuation slope: 10dB/Volt
- Minimum OIP3 (maximum attenuation): +35dBm
- Minimum IIP2 (maximum attenuation, > 35MHz): +85dBm

Typical Applications

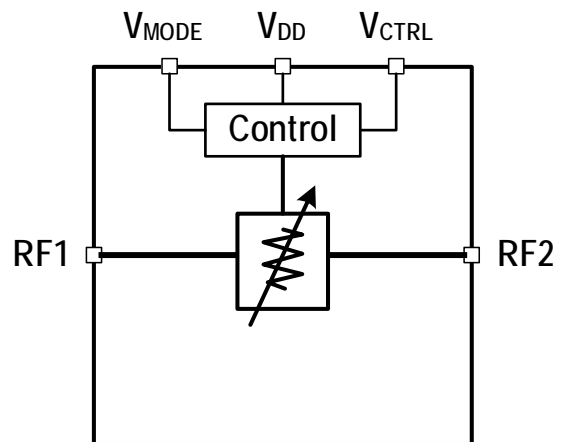
- CATV/Broadband Applications
 - Headend
 - Fiber/HFC Distribution Nodes
- CATV Test Equipment

Features

- Frequency range: 5MHz to 3000MHz
- Low insertion loss: 1.1dB at 300MHz
- Typical/Minimum IIP3 \geq 50MHz: 62dBm / 46dBm
- Typical/Minimum IIP2 \geq 50MHz: 98dBm / 77dBm
- Up to 35dB attenuation range
- Attenuation slope versus V_{CTRL} : 10dB/Volt
- Bi-directional RF ports
- +36dBm input P1dB
- V_{MODE} pin allows either positive or negative attenuation control response
- Linear-in-dB attenuation characteristic
- Nominal supply voltage: 3.3V or 5V
- V_{CTRL} range: 0V to 5V using 3.3V or 5V supply
- -40°C to +105°C operating temperature range
- 3mm x 3mm, 16-pin QFN package

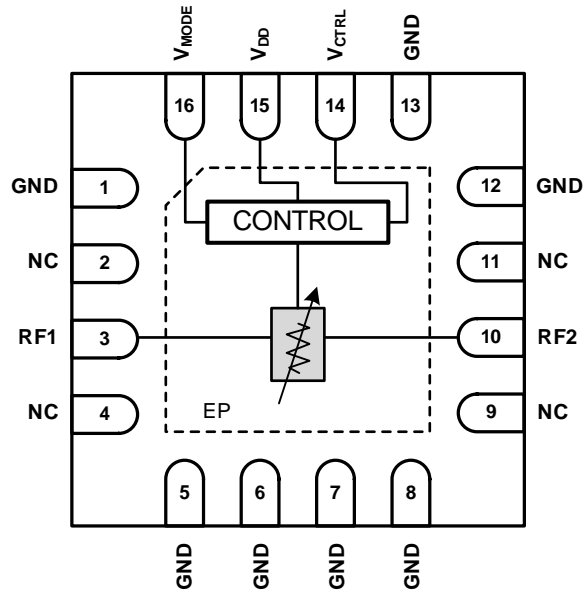
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 3mm x 3mm x 0.9mm 16-QFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Description |
|------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 5 – 8, 12, 13 | GND | Internally grounded. This pin must be grounded as close to the device as possible. |
| 2, 4, 9, 11 | NC | No internal connection. These pins can be left unconnected, have a voltage applied, or be connected to ground (recommended). |
| 3 | RF1 | RF Port 1. Matched to 75Ω. Since the RF pin internally has DC present, an external AC coupling capacitor must be used. For low-frequency operation, increase the capacitor value to result in a low reactance at the frequency of interest. An external series inductor of 2.4nH can also be used to improve the high frequency match. This inductor, if used, should be placed as close to the device as possible. |
| 10 | RF2 | RF Port 2. Matched to 75Ω. Since the RF pin internally has DC present, an external AC coupling capacitor must be used. For low-frequency operation, increase the capacitor value to result in a low reactance at the frequency of interest. An external series inductor of 2.8nH can also be used to improve the high frequency match. This inductor, if used, should be placed as close to the device as possible. |
| 14 | V _{CTRL} | Attenuator control voltage. Apply a voltage in the range specified in under “Recommended Operating Conditions.” See the “Application Information” section for details about V _{CTRL} . This pin is connected to an internal 100kΩ series resistor that drives a biased voltage divider network. |
| 15 | V _{DD} | Power supply input. Bypass to ground (GND) with capacitors as close as possible to the pin. |
| 16 | V _{MODE} | Attenuator slope control. Set to logic LOW to enable negative attenuation slope (maximum attenuation at maximum V _{CTRL}). Set to logic HIGH to enable positive attenuation slope (maximum attenuation at minimum V _{CTRL}). This pin is internally connected to a 170kΩ pull-down resistor to ground. |
| | – EPAD | Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |

Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

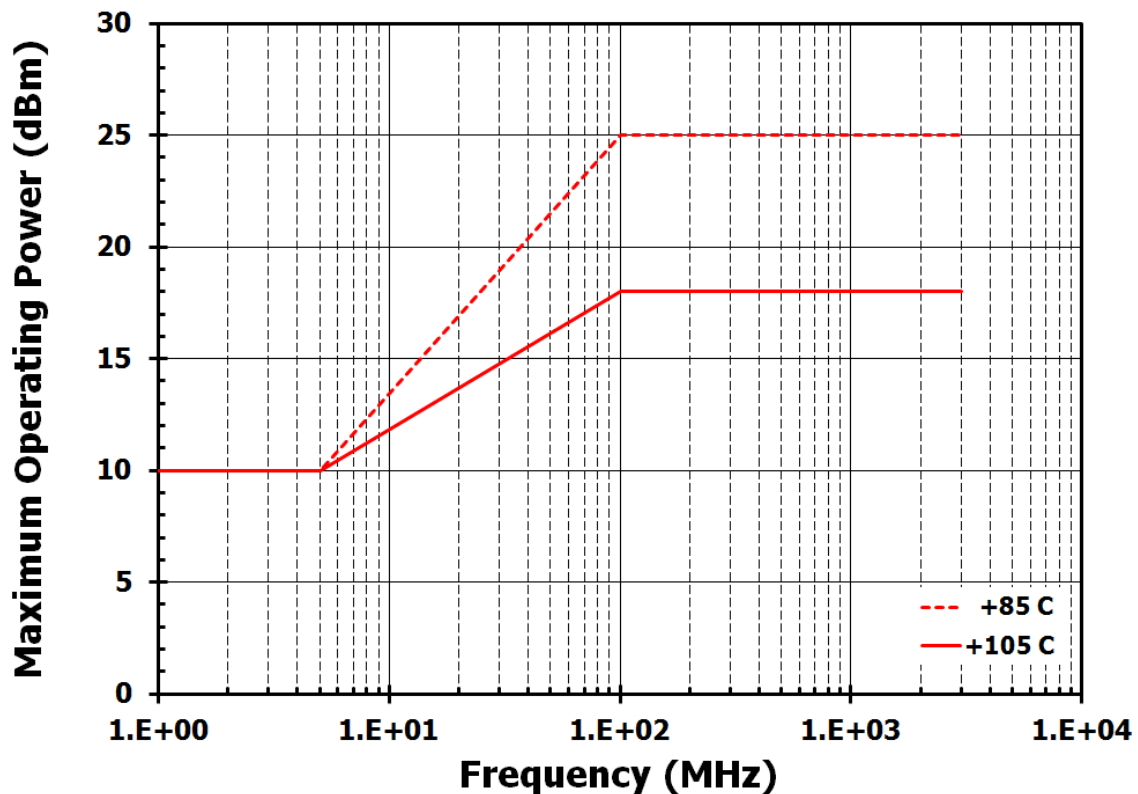
| Parameter | Symbol | Minimum | Maximum | Units |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|------------------------------------------|-------|
| V _{DD} to GND | V _{DD} | -0.3 | 6.0 | V |
| V _{MODE} to GND | V _{MODE} | -0.3 | Lower of (V _{DD} , 3.9) | V |
| V _{CTRL} to GND | V _{CTRL} | -0.3 | Lower of (V _{DD} + 3.0, 5.3) | V |
| RF1, RF2 to GND | V _{RF} | -0.3 | 0.3 | V |
| RF1 or RF2 Input Power Applied for 24 Hours Maximum (V _{DD} applied at 1GHz and T _{EP} [Exposed Paddle] = +85°C, Z _S = Z _L = 75Ω) | P _{MAX24} | | +28 | dBm |
| Junction Temperature | T _{JMAX} | | +150 | °C |
| Storage Temperature Range | T _{STOR} | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | T _{LEAD} | | +260 | °C |
| Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012) | V _{ESDHMB} | | 2000 (Class 2) | V |
| Electrostatic Discharge – CDM (JEDEC 22-C101F) | V _{ESDHCDM} | | 500 (Class C2) | V |

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|-----------------------------|------------|------------------------------------|---------|---------|----------------------------------|----------|
| Power Supply Voltage | V_{DD} | | 3.15 | | 5.5 | V |
| Mode Voltage [a] | V_{MODE} | | 0 | | Lower of (V_{DD} , 3.6) | V |
| Control Voltage [a] | V_{CTRL} | | 0 | | Lower of ($V_{DD} + 3.0$, 5.0) | V |
| Operating Temperature Range | T_{EP} | Exposed Paddle | -40 | | +105 | °C |
| RF Frequency Range | f_{RF} | | 5 | | 3000 | MHz |
| Maximum Input RF Power | P_{MAX} | Power can be applied to RF1 or RF2 | | | See Figure 3 | dBm |
| RF1 Port Impedance | Z_{RF1} | | | 75 | | Ω |
| RF2 Port Impedance | Z_{RF2} | | | 75 | | Ω |

[a] The power supply voltage must be applied before all other voltages.

 Figure 3. Maximum Operating CW RF Input Power vs. Frequency ($Z_s = Z_L = 75\Omega$)


Electrical Characteristics

Table 4. Electrical Characteristics (General)

Refer to the application circuit in Figure 60 for the required circuit and use $L1 = L2 = 0\Omega$. The specifications in this table apply at $V_{DD} = +5.0V$, $T_{EP} = +25^{\circ}C$, $f_{RF} = 500MHz$, $Z_S = Z_L = 75\Omega$, signal applied to RF1, minimum attenuation, $P_{IN} = 0dBm$ for small signal parameters, $P_{IN} = +20dBm$ per tone for two tone tests, V_{MODE} is LOW or HIGH, and Evaluation Board (EVKit) trace and connector losses are de-embedded, unless otherwise noted.

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|-----------------------------------------------------------------------|---------------|-------------------------------------------------------------------------------------------------------------|-----------------|---------|----------------|---------|
| V_{MODE} Logic Input HIGH | V_{IH} | $3.9V \leq V_{DD} \leq 5.5V$ | 1.07 [a] | | 3.6 | V |
| | | $V_{DD} < 3.9V$ | 1.07 | | $V_{DD} - 0.3$ | |
| V_{MODE} Logic Input LOW | V_{IL} | | 0 | | 0.63 | V |
| V_{DD} Current | I_{DD} | | | 1.4 | 2.5 | mA |
| V_{MODE} Current | I_{MODE} | | -40 | | 40 | μA |
| V_{CTRL} Current | I_{CTRL} | | -50 | | 50 | μA |
| Attenuation Slope | ATT_{SLOPE} | $V_{MODE} = LOW$ | | 10 | | dB/V |
| | | $V_{MODE} = HIGH$ | | -10 | | |
| Attenuation Variation over Temperature (reference to $+25^{\circ}C$) | ATT_{VAR} | $f_{RF} = 50MHz$ ($-40^{\circ}C$ to $105^{\circ}C$, over full signal range of V_{CTRL}) | | ± 1 | | dB |
| Settling Time | t_{SETTLE} | Any 1dB step in the 0dB to 33dB control range, 50% of V_{CTRL} signal to RF settled to within $\pm 0.1dB$ | | 25 | | μs |

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Electrical Characteristics (continued)

Table 5. Electrical Characteristics (No External RF Tuning)

Refer to the application circuit in Figure 60 for the required circuit and use $L1 = L2 = 0\Omega$. The specifications in this table apply at $V_{DD} = +5.0V$, $T_{EP} = +25^\circ C$, $f_{RF} = 500MHz$, $Z_S = Z_L = 75\Omega$, signal applied to RF1, minimum attenuation, $P_{IN} = 0dBm$ for small signal parameters, $P_{IN} = +20dBm$ per tone for two tone tests, V_{MODE} is LOW or HIGH, and Evaluation Board (EVKit) trace and connector losses are de-embedded, unless otherwise noted.

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|-------------------------------------------------|-----------------------|--------------------------------------------------------|-----------|-----------|----------------|-------|
| Insertion Loss, IL | A_{MIN} | Minimum attenuation | | 1.1 | 1.8 [a] | dB |
| Maximum Attenuation | A_{MAX} | $f_{RF} = 5MHz$ | | 23 | | dB |
| | | $f_{RF} = 10MHz$ | | 28 | | |
| | | $f_{RF} = 500MHz$ | 33 | 35 | | |
| | | $300MHz < f_{RF} \leq 1800MHz$ | | 35 | | |
| Attenuation Variation [c] | A_{VAR} | $V_{CTRL} = 1.0V$, $V_{MODE} = LOW$ | | ± 1.5 | | dB |
| | | $V_{CTRL} = 2.1V$, $V_{MODE} = LOW$ | | ± 2.8 | | |
| Relative Insertion Phase | $\Phi_{\Delta MAX}$ | At maximum attenuation relative to minimum attenuation | | 9 | | deg |
| RF1 Return Loss (over control voltage range) | S_{11} | $5MHz \leq f_{RF} \leq 300MHz$ | | 23 | | dB |
| | | $300MHz < f_{RF} \leq 1220MHz$ | | 15 | | |
| | | $1220MHz < f_{RF} \leq 1800MHz$ | | 12 | | |
| RF2 Return Loss (over control voltage range) | S_{22} | $5MHz \leq f_{RF} \leq 300MHz$ | | 23 | | dB |
| | | $300MHz < f_{RF} \leq 1220MHz$ | | 15 | | |
| | | $1220MHz < f_{RF} \leq 1800MHz$ | | 12 | | |
| Input Power Compression [b] | IP1dB | | | 36 | | dBm |
| Input IP3 | IIP3 | $f_{RF} = 5MHz$, 1MHz spacing | | 45 | | dBm |
| | | $f_{RF} = 50MHz$, 5MHz spacing | | 57 | | |
| | | $300MHz < f_{RF} < 2GHz$, 50MHz spacing | | 60 | | |
| Input IP3 over Attenuation | IIP3 _{ATTEN} | All attenuation settings | | 46 | | dBm |
| Minimum Output IP3 | OIP3 _{MIN} | Maximum attenuation | | 35 | | dBm |
| Input IP2 | IIP2 | IM2 term is $f_1 + f_2$ | | 98 | | dBm |
| Minimum Input IP2 | IIP2 _{MIN} | All attenuation settings | | 77 | | dBm |
| Input 2 nd Harmonic Intercept Point | IIP _{H2} | $P_{IN} + H2_{dBc}$ | | 82 | | dBm |
| Input 3 rd Harmonic Intercept Point | IIP _{H3} | $P_{IN} + (H3_{dBc} / 2)$ | | 50 | | dBm |

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] The input 1dB compression point is a linearity figure of merit. Refer to the "Absolute Maximum Ratings" section for the maximum RF input power.

[c] This value is for part to part variation at the given voltage.

Electrical Characteristics (continued)

Table 6. Electrical Characteristics – Extended Bandwidth Tuning (EBT) using external components
 Refer to the application circuit in Figure 60 for the required circuit and use $L1 = 2.4\text{nH}$ and $L2 = 2.8\text{nH}$. The specifications in this table apply at $V_{DD} = +5.0\text{V}$, $T_{EP} = +25^\circ\text{C}$, $f_{RF} = 500\text{MHz}$, $Z_S = Z_L = 75\Omega$, signal applied to RF1, minimum attenuation, $P_{IN} = 0\text{dBm}$ for small signal parameters, $P_{IN} = +20\text{dBm}$ per tone for two tone tests, V_{MODE} is LOW or HIGH, and Evaluation Board (EVKit) trace and connector losses are embedded, unless otherwise noted.

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|-------------------------------------------------|-----------------------|-----------------------------------------------------------|---------|-----------|---------|-------|
| Insertion Loss, IL | A_{MIN} | Minimum attenuation | | 1.1 | | dB |
| Maximum Attenuation | A_{MAX} | $f_{RF} = 5\text{MHz}$ | | 23 | | dB |
| | | $f_{RF} = 10\text{MHz}$ | | 28 | | |
| | | $50\text{MHz} < f_{RF} \leq 300\text{MHz}$ | | 35 | | |
| | | $300\text{MHz} < f_{RF} \leq 1800\text{MHz}$ | | 35 | | |
| Attenuation Variation [c] | A_{VAR} | $V_{CTRL} = 1.0\text{V}$, $V_{MODE} = \text{LOW}$ | | ± 1.5 | | dB |
| | | $V_{CTRL} = 2.1\text{V}$, $V_{MODE} = \text{LOW}$ | | ± 2.8 | | |
| Relative Insertion Phase | $\Phi_{\Delta MAX}$ | At maximum attenuation relative to minimum attenuation | | 9 | | deg |
| RF1 Return Loss (over control voltage range) | S_{11} | $5\text{MHz} \leq f_{RF} \leq 300\text{MHz}$ | | 23 | | dB |
| | | $300\text{MHz} < f_{RF} \leq 1220\text{MHz}$ | | 18 | | |
| | | $1220\text{MHz} < f_{RF} \leq 1800\text{MHz}$ | | 12 | | |
| RF2 Return Loss (over control voltage range) | S_{22} | $5\text{MHz} \leq f_{RF} \leq 300\text{MHz}$ | | 23 | | dB |
| | | $300\text{MHz} < f_{RF} \leq 1220\text{MHz}$ | | 18 | | |
| | | $1220\text{MHz} < f_{RF} \leq 1800\text{MHz}$ | | 12 | | |
| Input Power Compression [b] | IP1dB | | | 36 | | dBm |
| Input IP3 (Minimum Attenuation) | IIP3 | $f_{RF} = 5\text{MHz}$, 1MHz spacing | | 45 | | dBm |
| | | $f_{RF} = 50\text{MHz}$, 5MHz spacing | | 57 | | |
| | | $300\text{MHz} < f_{RF} < 2\text{GHz}$, 50MHz spacing | | 60 | | |
| Input IP3 over attenuation | IIP3 _{ATTEN} | All attenuation settings | | 46 | | dBm |
| Minimum Output IP3 | OIP3 _{MIN} | Maximum attenuation | | 35 | | dBm |
| Input IP2 | IIP2 | IM2 term is $f_1 + f_2$ | | 98 | | dBm |
| Minimum Input IP2 | IIP2 _{MIN} | All attenuation settings | | 77 | | dBm |
| Input 2 nd Harmonic Intercept Point | IIP _{H2} | $P_{IN} + H2_{dBc}$ | | 82 | | dBm |
| Input 3 rd Harmonic Intercept Point | IIP _{H3} | $P_{IN} + (H3_{dBc} / 2)$ | | 50 | | dBm |

- [a] Specifications in the minimum/maximum columns that are shown in **bold italics** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.
- [b] The input 1dB compression point is a linearity figure of merit. Refer to the “Absolute Maximum Ratings” section for the maximum RF input power.
- [c] This value is for part to part variation at the given voltage.

Thermal Characteristics

Table 7. Package Thermal Characteristics

| Parameter | Symbol | Value | Units |
|--------------------------------------------------------------------------------|-------------------|-------|-------|
| Junction to Ambient Thermal Resistance | θ_{JA} | 80.6 | °C/W |
| Junction to Case Thermal Resistance (case is defined as the exposed paddle) | θ_{JC-BOT} | 5.1 | °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | | MSL 1 | |

Typical Operating Conditions (TOCs)

Unless otherwise noted:

- $V_{DD} = +5.0V$
- $Z_S = Z_L = 75\Omega$
- $T_{EP} = +25^\circ C$
- RF trace and connector losses removed for insertion loss and attenuation results. All other results include the PCB trace and connector losses and mismatched effects.
- $P_{IN} = 0dBm$ for all small signal tests
 - $P_{IN} = +20dBm/$ tone for two tone linearity tests (RF1 port driven)
- Two tone frequency spacing
 - 1MHz for $5MHz \leq f_{RF} < 50MHz$
 - 5MHz for $50MHz \leq f_{RF} < 500MHz$
 - 50MHz for $500MHz \leq f_{RF} < 3500MHz$
- All temperatures are referenced to the exposed paddle.
- Extended band tuning uses $L1 = 2.4nH$ and $L2 = 2.8nH$ to improve RF1 and RF2 port match.

Typical Performance Characteristics (No External RF Tuning)

Figure 4. Insertion Loss vs. Frequency
[V_{MODE} = LOW]

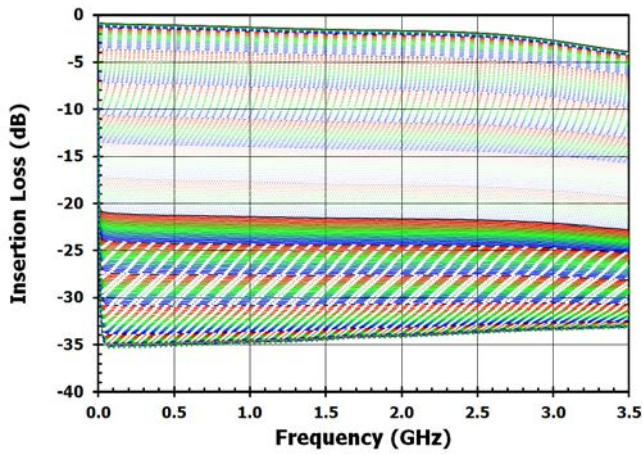


Figure 5. Relative Insertion Loss vs. V_{CTRL}
[V_{MODE} = LOW]

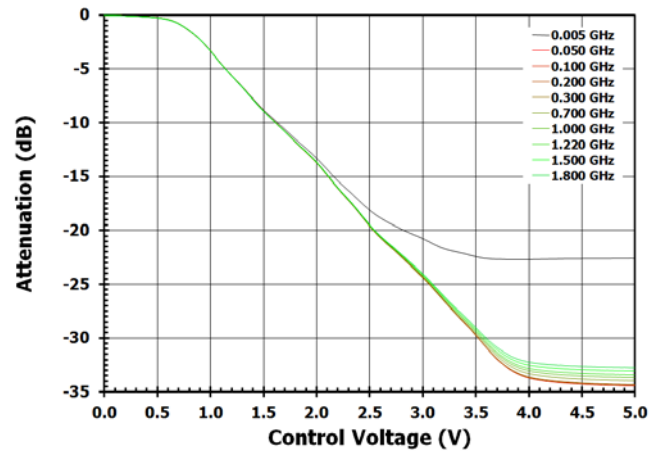


Figure 6. RF1 Return Loss vs. Frequency
[V_{MODE} = LOW]

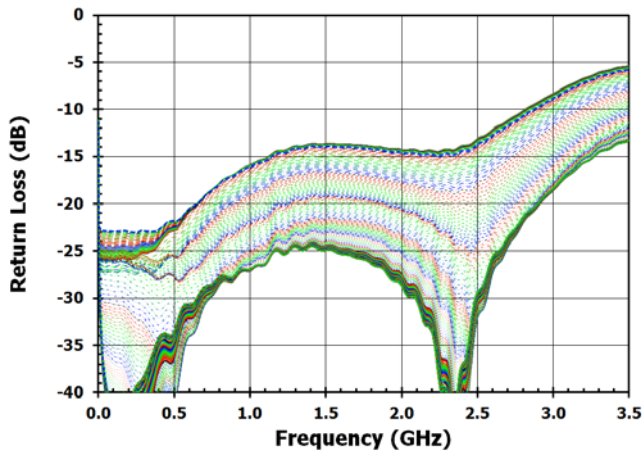


Figure 7. RF1 Return Loss vs. V_{CTRL}
[V_{MODE} = LOW]

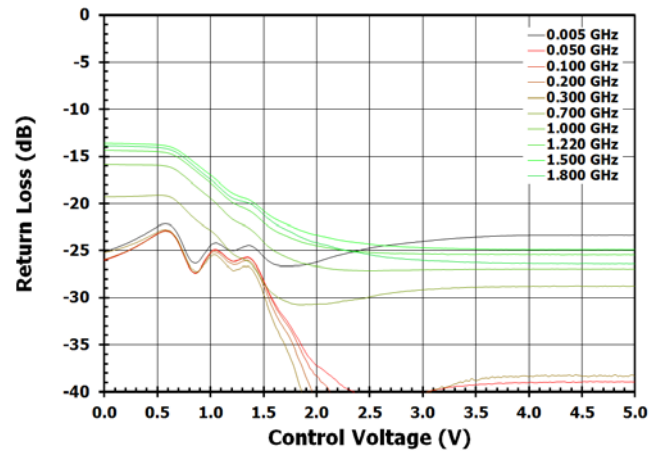


Figure 8. RF2 Return Loss vs. Frequency
[V_{MODE} = LOW]

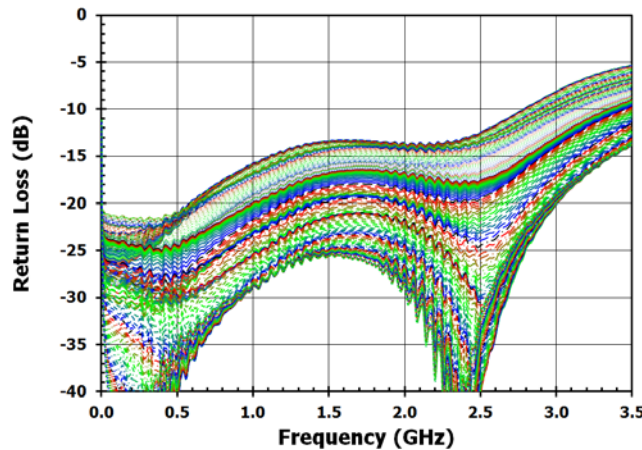
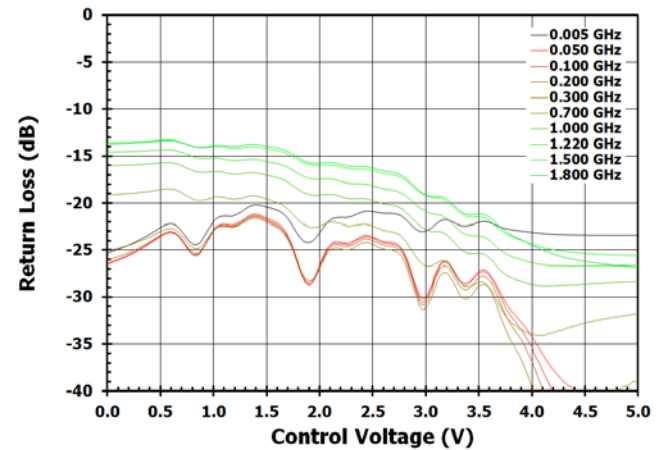


Figure 9. RF2 Return Loss vs. V_{CTRL}
[V_{MODE} = LOW]



Typical Performance Characteristics (No External RF Tuning)

Figure 10. Relative Insertion Phase vs. Frequency [$V_{MODE} = LOW$]

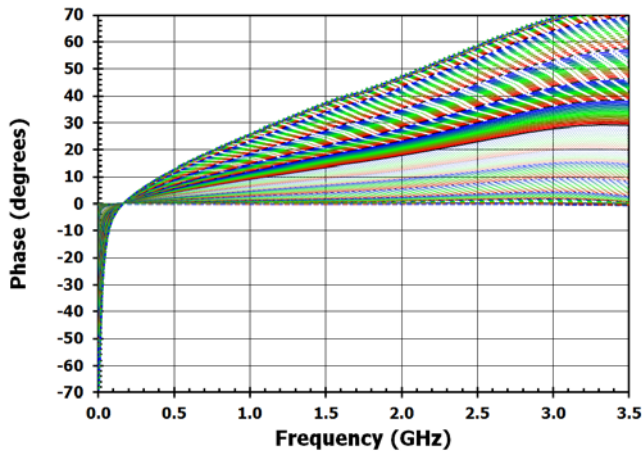


Figure 11. Relative Insertion Phase vs. V_{CTRL} [$V_{MODE} = LOW$]

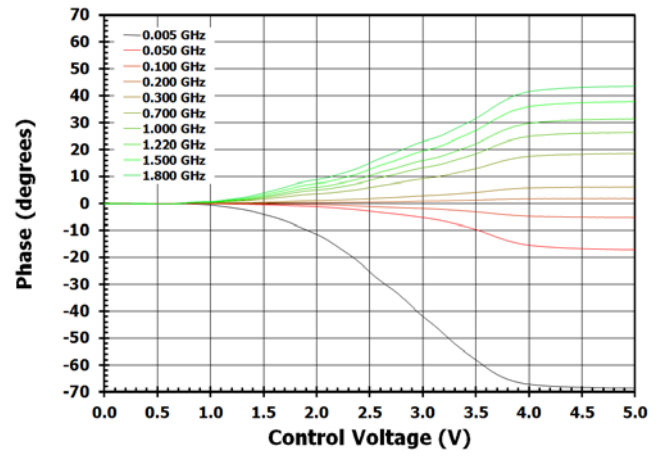


Figure 12. Insertion Loss vs. Frequency

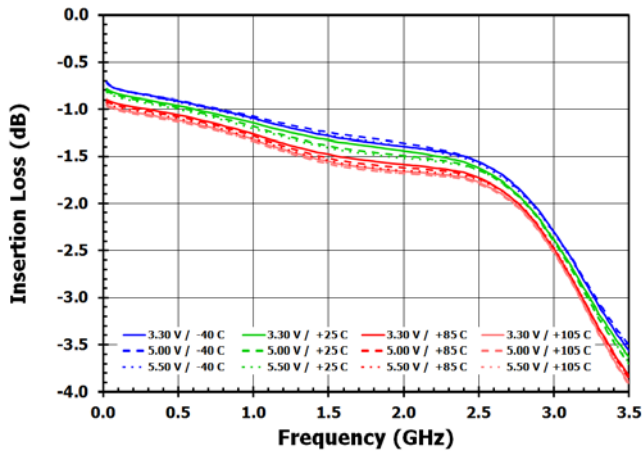
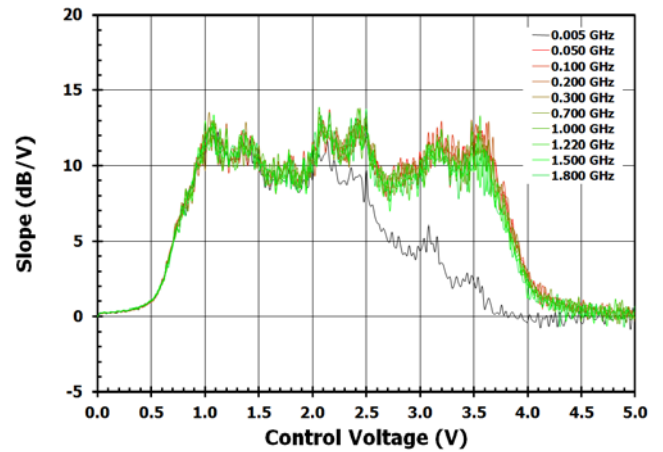


Figure 13. Attenuation Slope vs. V_{CTRL} [$V_{MODE} = LOW$]



Typical Performance Characteristics (No External RF Tuning)

Figure 14. Insertion Loss vs. Frequency
[V_{MODE} = HIGH]

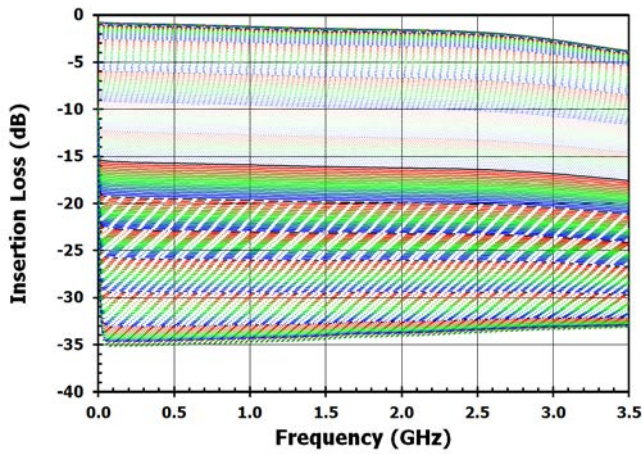


Figure 15. Relative Insertion Loss vs. V_{CTRL}
[V_{MODE} = HIGH]

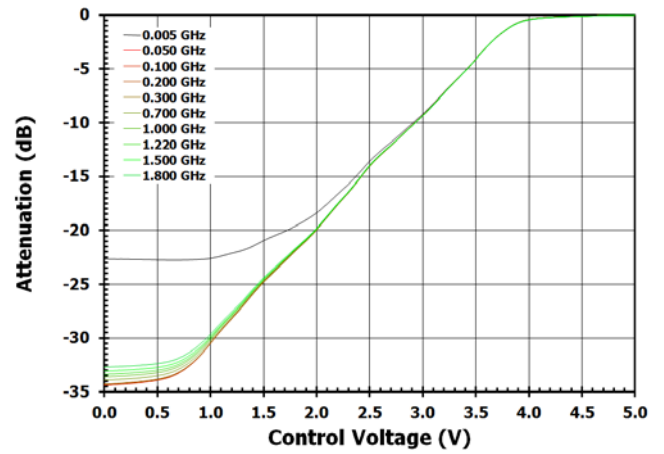


Figure 16. RF1 Return Loss vs. Frequency
[V_{MODE} = HIGH]

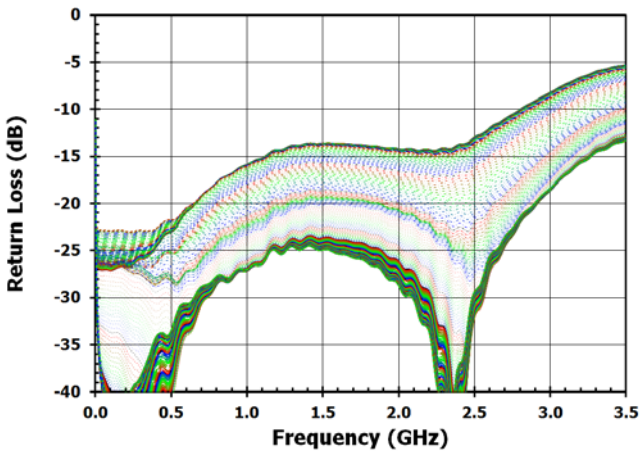


Figure 17. RF1 Return Loss vs. V_{CTRL}
[V_{MODE} = HIGH]

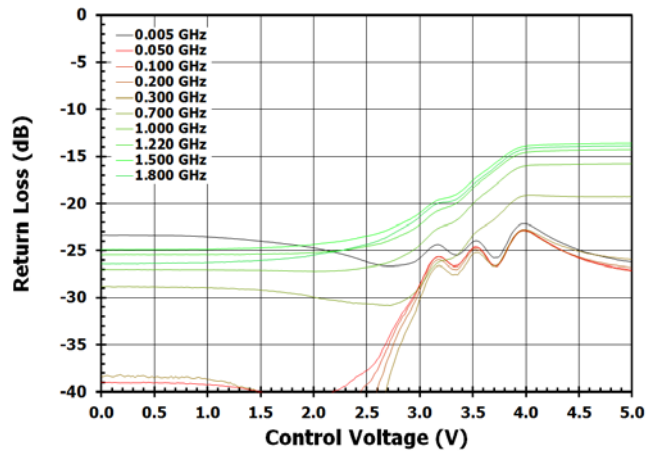


Figure 18. RF2 Return Loss vs. Frequency
[V_{MODE} = HIGH]

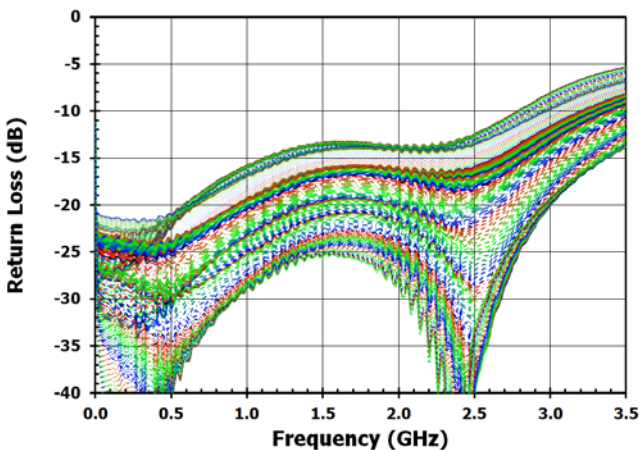
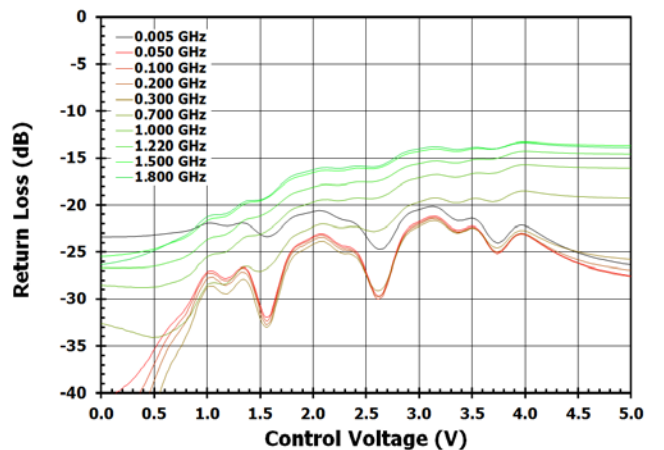


Figure 19. RF2 Return Loss vs. V_{CTRL}
[V_{MODE} = HIGH]



Typical Performance Characteristics (No External RF Tuning)

Figure 20. Relative Insertion Phase vs. Frequency [$V_{MODE} = HIGH$]

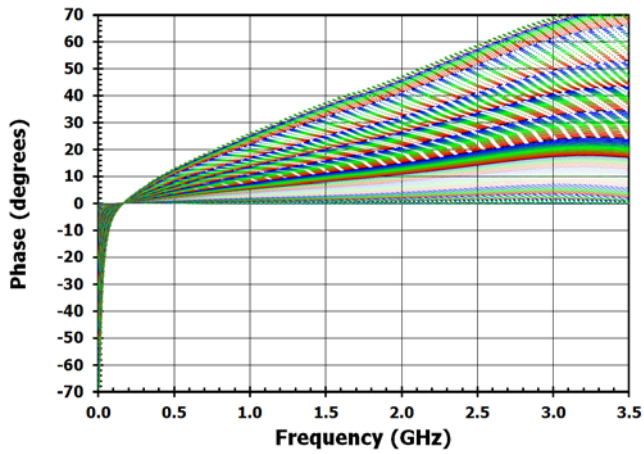


Figure 21. Relative Insertion Phase vs. V_{CTRL} [$V_{MODE} = HIGH$]

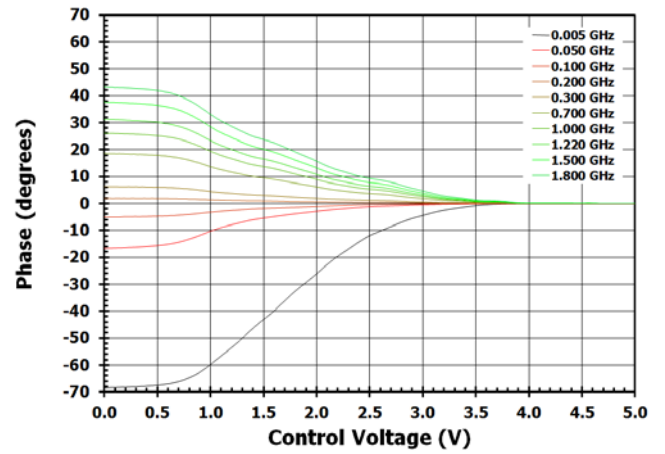
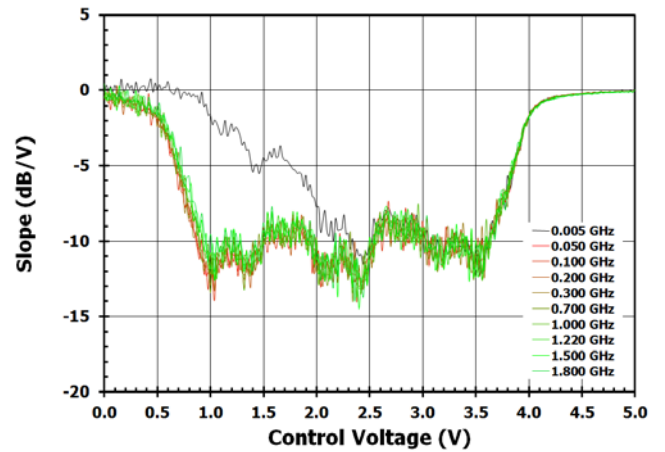


Figure 22. Attenuation Slope vs. V_{CTRL} [$V_{MODE} = HIGH$]



Typical Performance Characteristics (No External RF Tuning)

Figure 23. Input IP3 vs. V_{CTRL}
[5MHz, $V_{MODE} = LOW$]

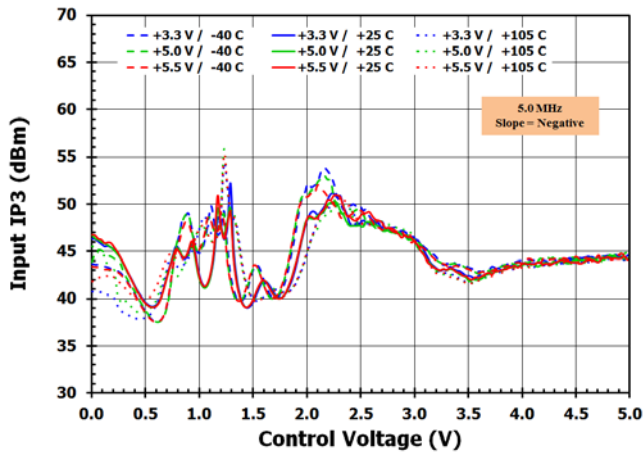


Figure 24. Input IP3 vs. V_{CTRL}
[5MHz, $V_{MODE} = HIGH$]

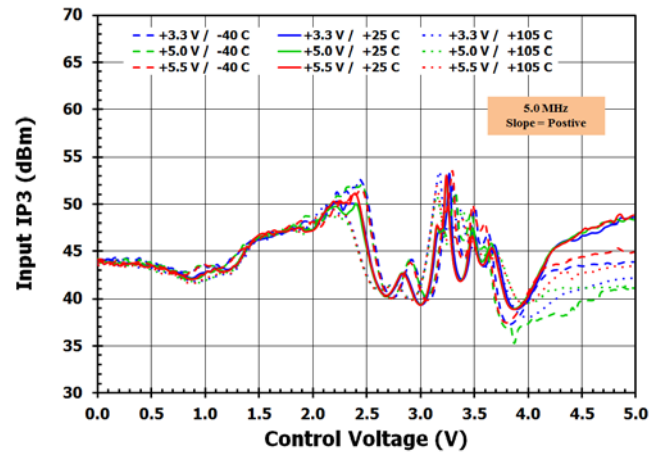


Figure 25. Input IP3 vs. V_{CTRL}
[50MHz, $V_{MODE} = LOW$]

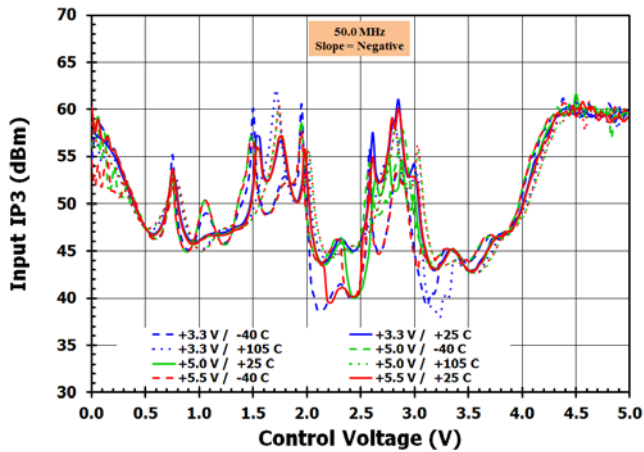


Figure 26. Input IP3 vs. V_{CTRL}
[50MHz, $V_{MODE} = HIGH$]

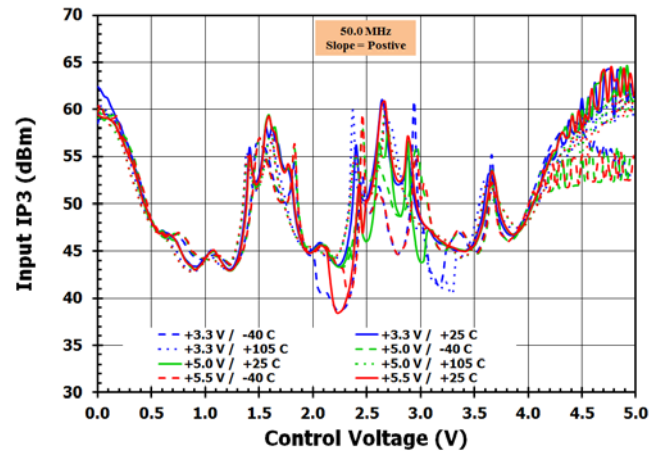


Figure 27. Input IP3 vs. V_{CTRL}
[1.2GHz, $V_{MODE} = LOW$]

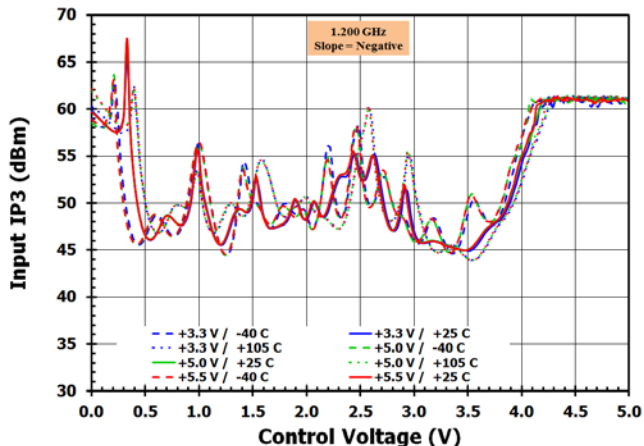
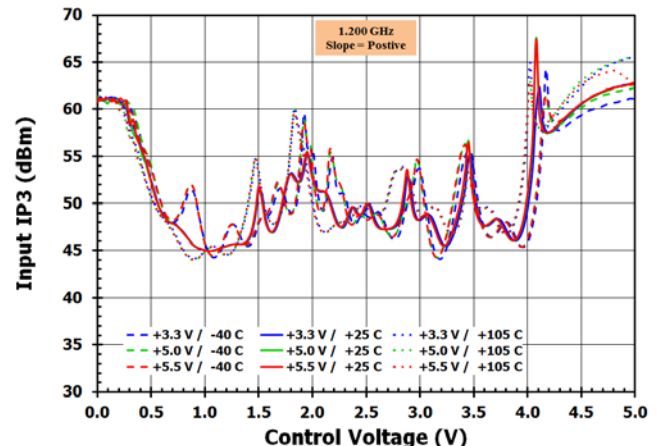


Figure 28. Input IP3 vs. V_{CTRL}
[1.2GHz, $V_{MODE} = HIGH$]



Typical Performance Characteristics (No External RF Tuning)

Figure 29. Compression vs. Input Power
[5MHz, $V_{MODE} = LOW, V_{CTRL} = 0V$]

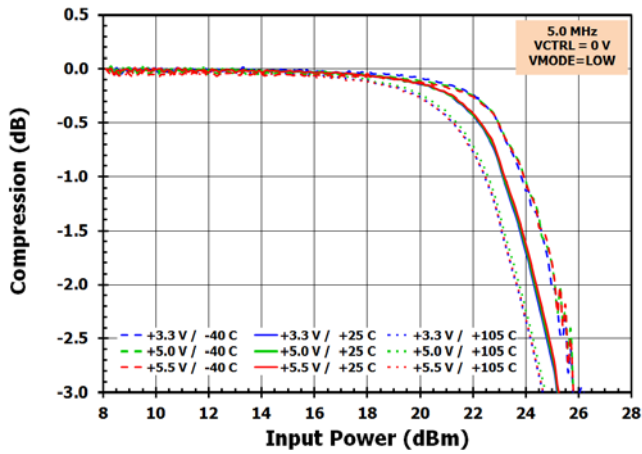


Figure 30. Compression vs. Input Power
[5MHz, $V_{MODE} = HIGH, V_{CTRL} = 5V$]

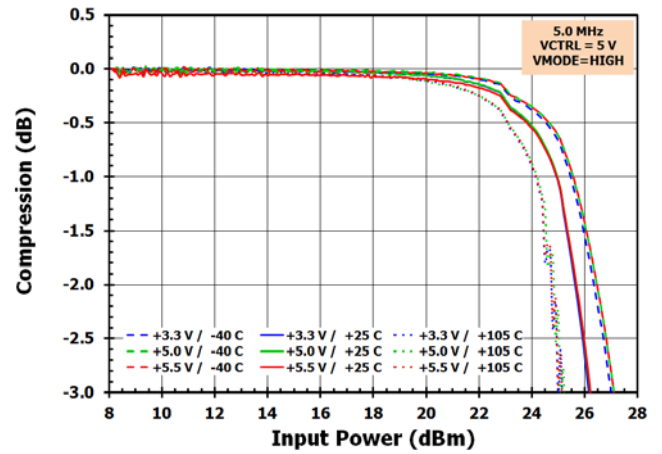


Figure 31. Compression vs. Input Power
[100MHz, $V_{MODE} = LOW, V_{CTRL} = 0V$]

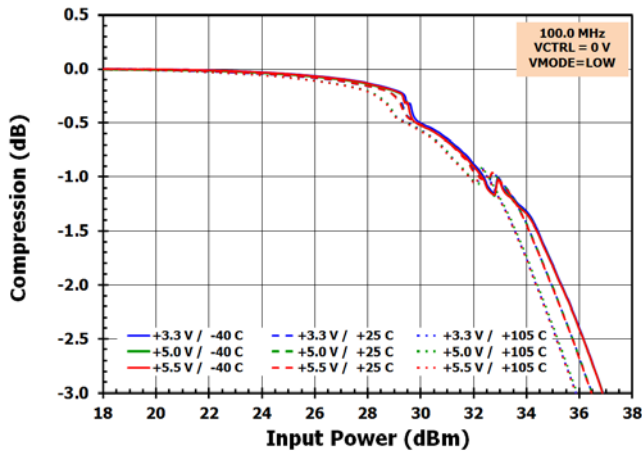


Figure 32. Compression vs. Input Power
[100MHz, $V_{MODE} = HIGH, V_{CTRL} = 5V$]

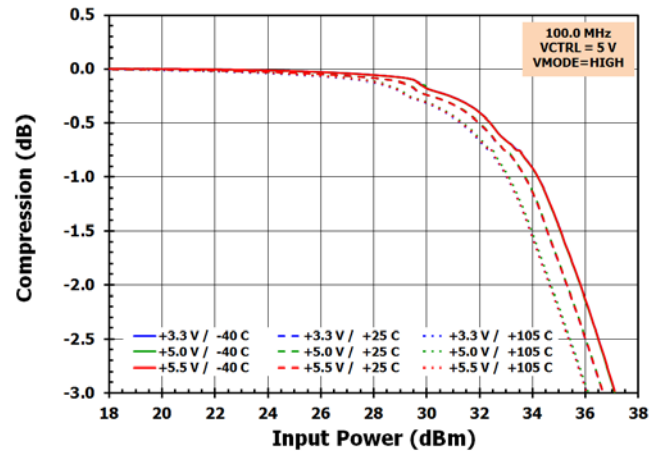


Figure 33. Compression vs. Input Power
[1.2GHz, $V_{MODE} = LOW, V_{CTRL} = 0V$]

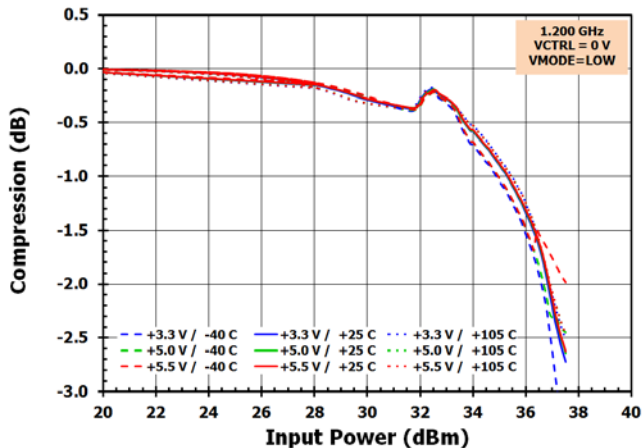
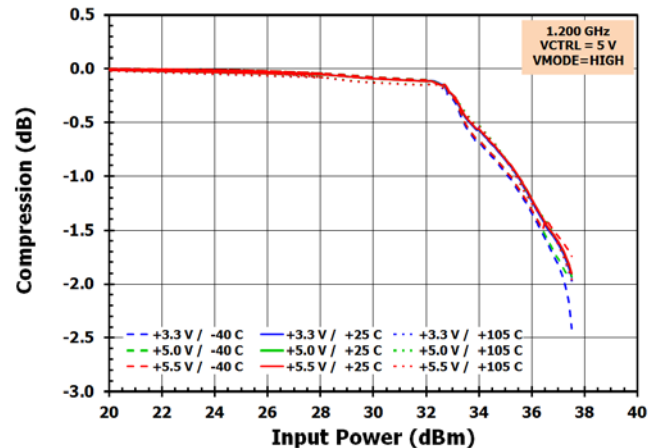


Figure 34. Compression vs. Input Power
[1.2GHz, $V_{MODE} = HIGH, V_{CTRL} = 5V$]



Typical Performance Characteristics (Extended Bandwidth Tuning)

Figure 35. Insertion Loss vs. Frequency
[V_{MODE} = LOW]

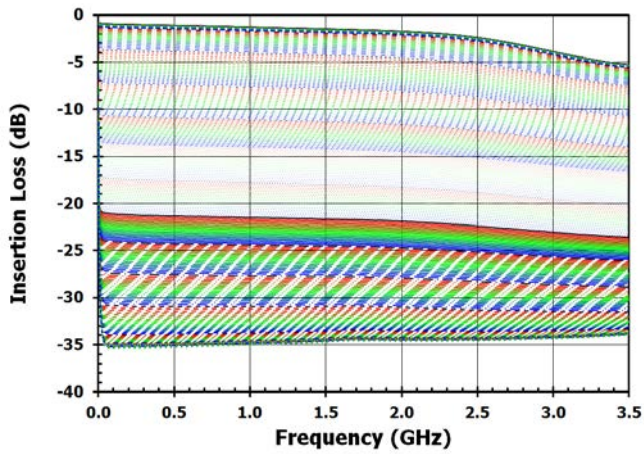


Figure 36. Relative Insertion Loss vs. V_{CTRL}
[V_{MODE} = LOW]

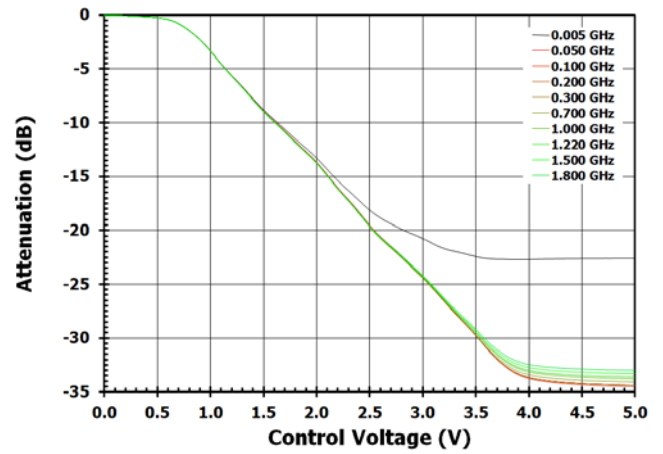


Figure 37. RF1 Return Loss vs. Frequency
[V_{MODE} = LOW]

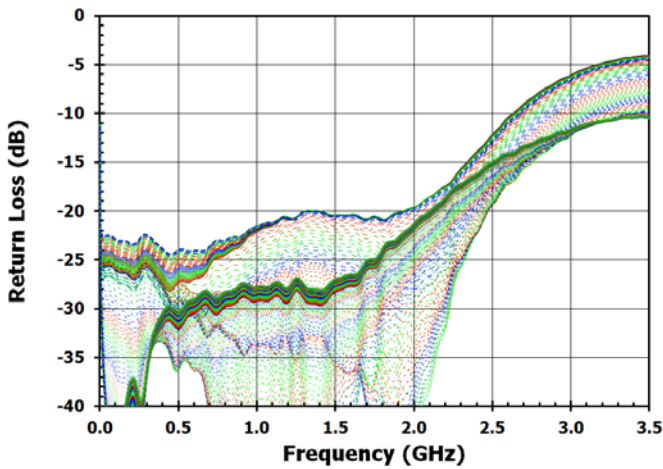


Figure 38. RF1 Return Loss vs. V_{CTRL}
[V_{MODE} = LOW]

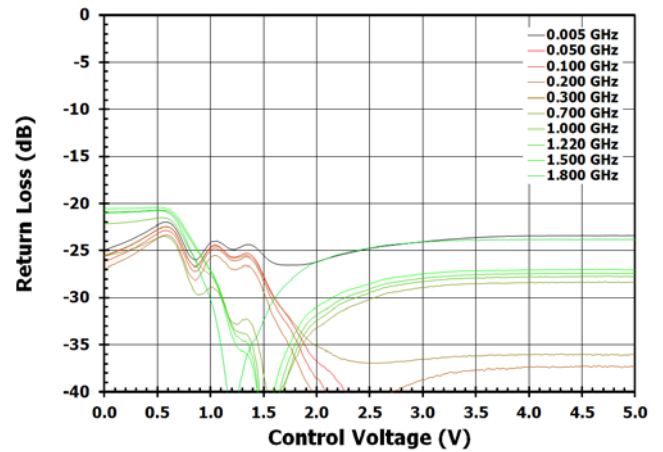


Figure 39. RF2 Return Loss vs. Frequency
[V_{MODE} = LOW]

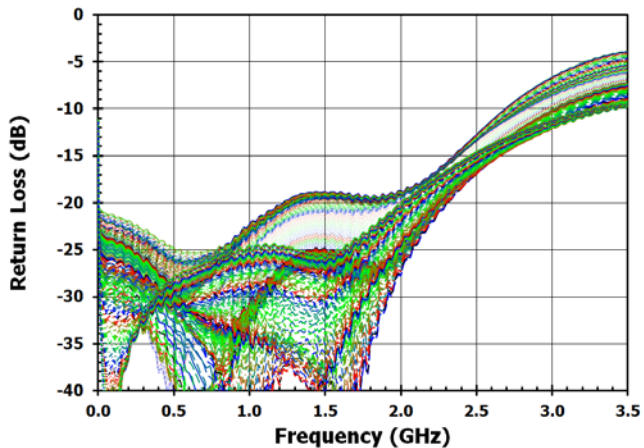
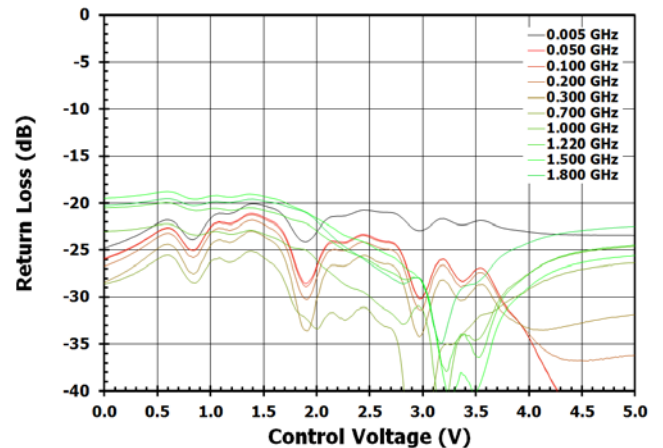


Figure 40. RF2 Return Loss vs. V_{CTRL}
[V_{MODE} = LOW]



Typical Performance Characteristics (Extended Bandwidth Tuning)

Figure 41. Relative Insertion Phase vs. Frequency [$V_{MODE} = LOW$]

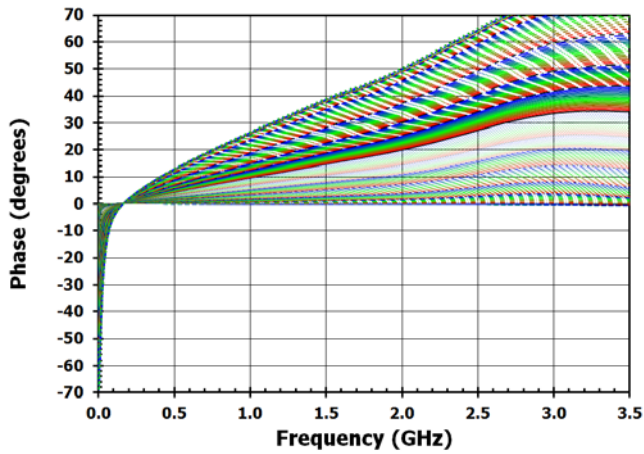


Figure 42. Relative Insertion Phase vs. V_{CTRL} [$V_{MODE} = LOW$]

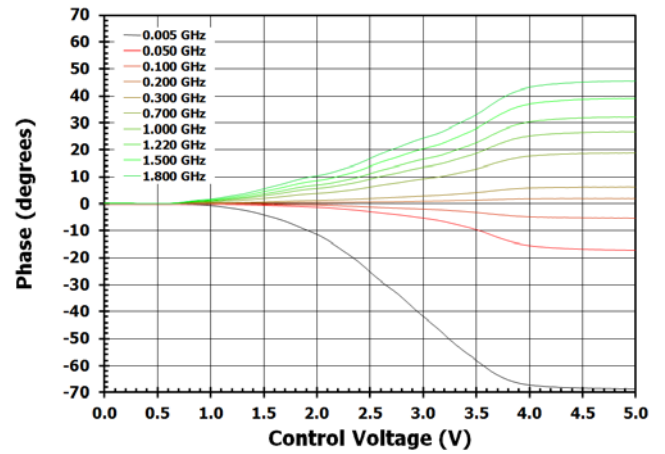


Figure 43. RF1 Return Loss vs. Frequency [$V_{MODE} = LOW$]

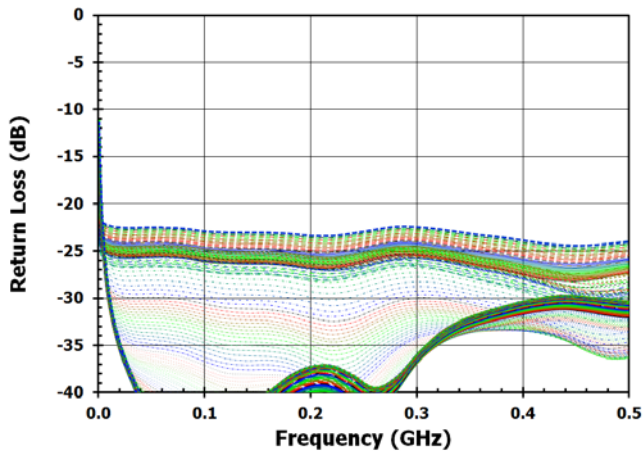


Figure 44. Attenuation Slope vs. V_{CTRL} [$V_{MODE} = LOW$]

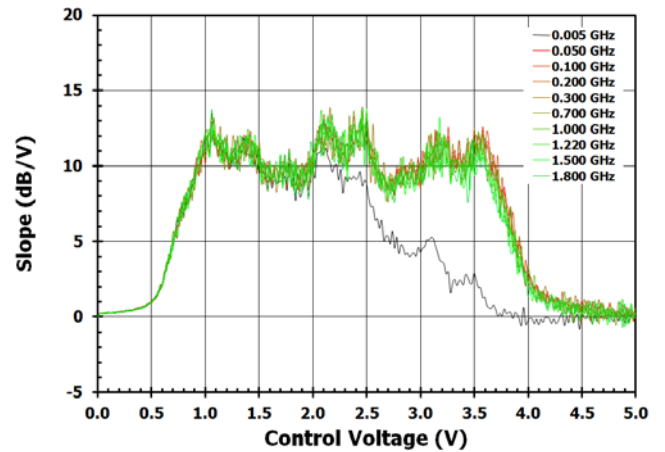
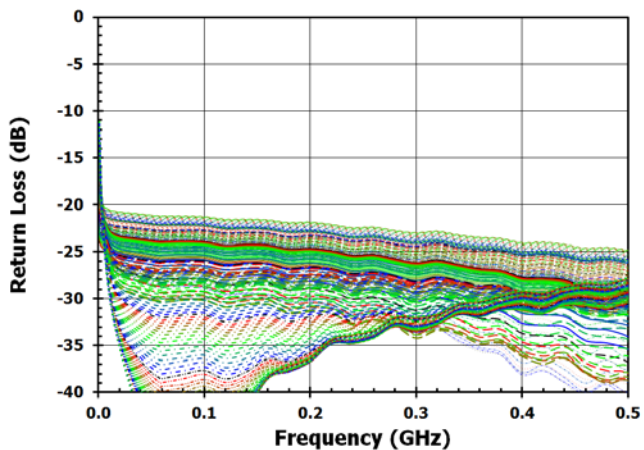


Figure 45. RF2 Return Loss vs. Frequency [$V_{MODE} = LOW$]



Typical Performance Characteristics (Extended Bandwidth Tuning)

Figure 46. Insertion Loss vs. Frequency
[V_{MODE} = HIGH]

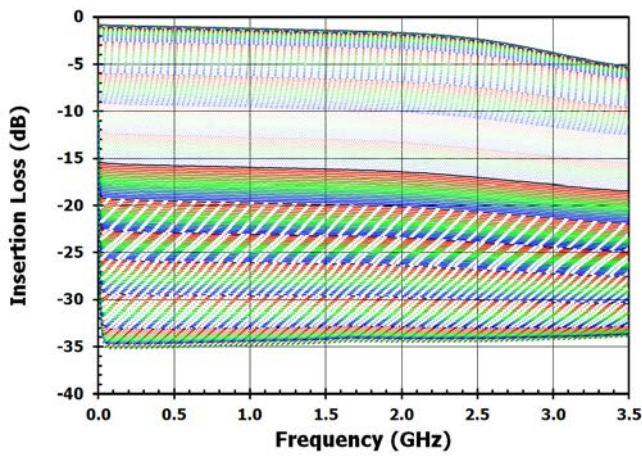


Figure 47. Relative Insertion Loss vs. V_{CTRL}
[V_{MODE} = HIGH]

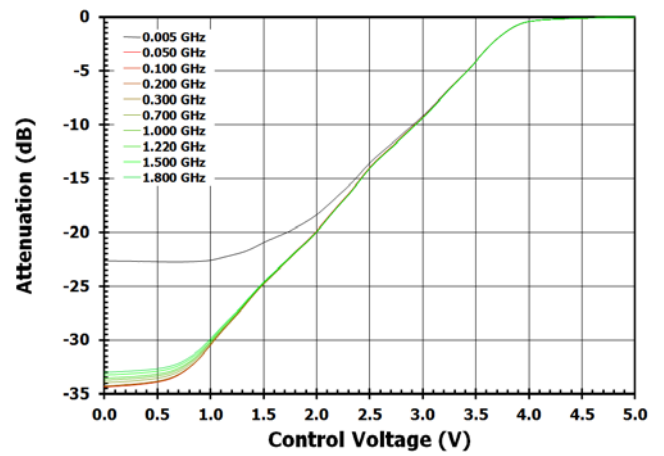


Figure 48. RF1 Return Loss vs. Frequency
[V_{MODE} = HIGH]

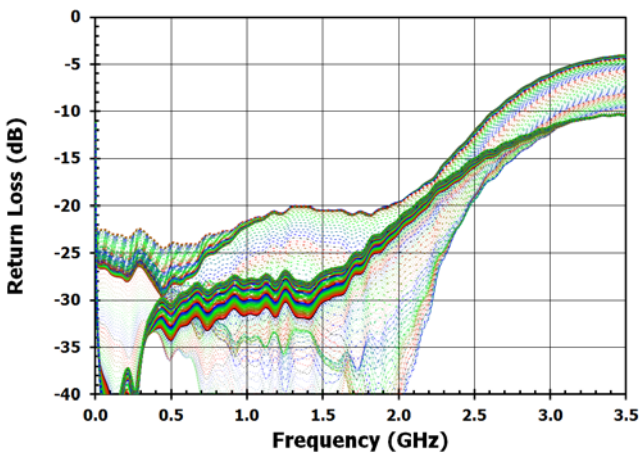


Figure 49. RF1 Return Loss vs. V_{CTRL}
[V_{MODE} = HIGH]

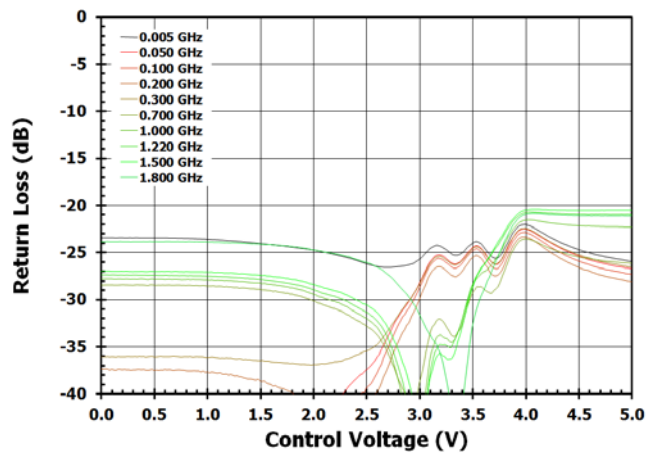


Figure 50. RF2 Return Loss vs. Frequency
[V_{MODE} = HIGH]

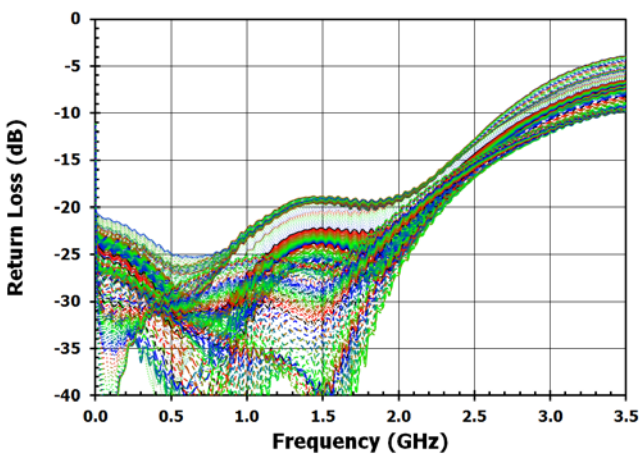
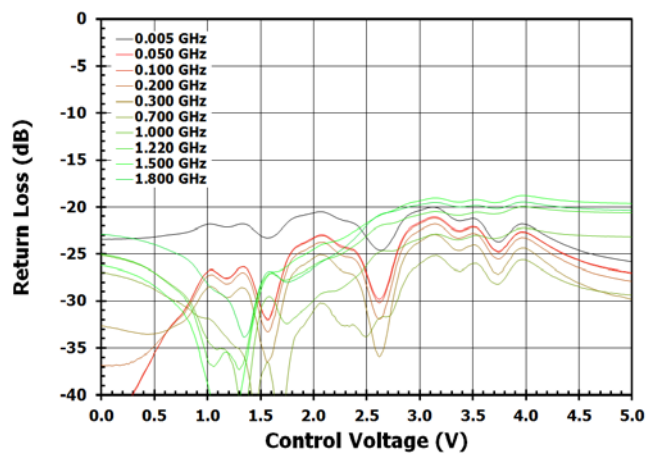


Figure 51. RF2 Return Loss vs. V_{CTRL}
[V_{MODE} = HIGH]



Typical Performance Characteristics (Extended Bandwidth Tuning)

Figure 52. Relative Insertion Phase vs. Frequency [$V_{MODE} = HIGH$]

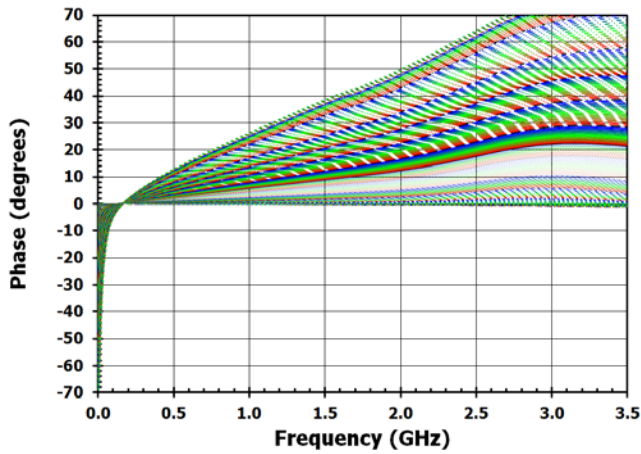


Figure 53. Relative Insertion Phase vs. V_{CTRL} [$V_{MODE} = HIGH$]

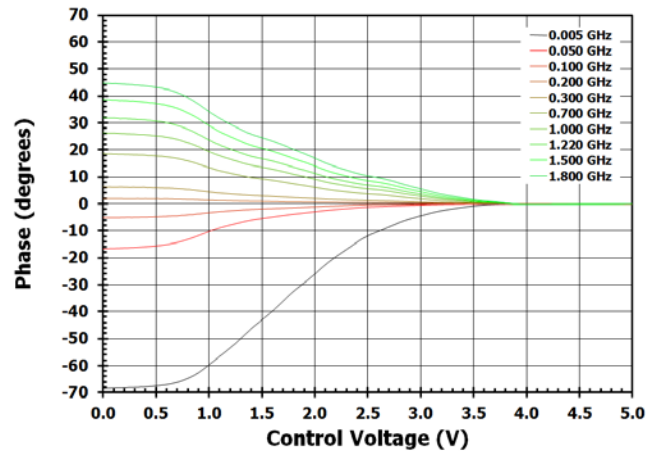


Figure 54. RF1 Return Loss vs. Frequency [$V_{MODE} = HIGH$]

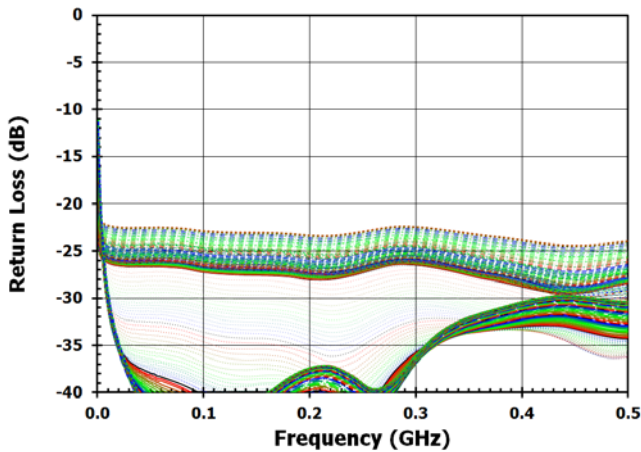


Figure 55. Attenuation Slope vs. V_{CTRL} [$V_{MODE} = HIGH$]

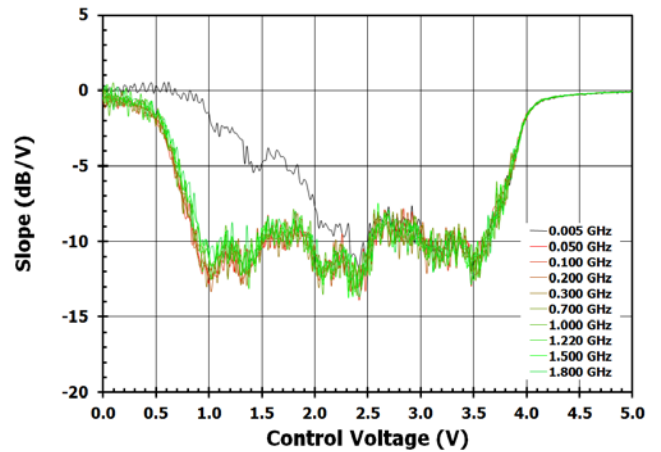
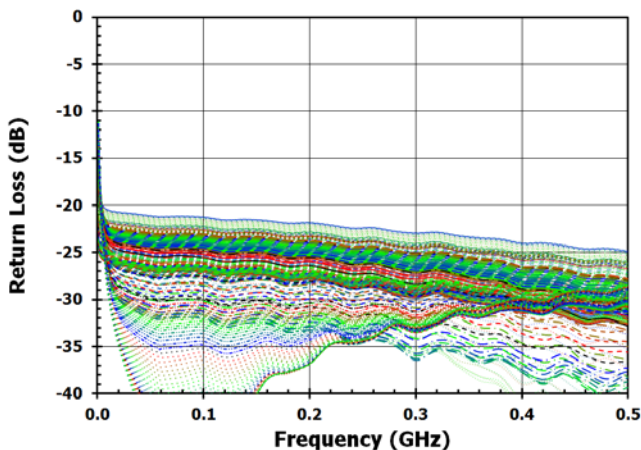


Figure 56. RF2 Return Loss vs. Frequency [$V_{MODE} = HIGH$]



Application Information

The F2270 has been optimized for use in high performance RF applications from 5MHz to 1800MHz and has a full operating range of 5MHz to 3000MHz.

Default Start-up

V_{MODE} should be tied to either logic LOW (ground) or logic HIGH. If the V_{CTRL} pin is left floating, the part will power up in the minimum attenuation state when $V_{MODE} = LOW$ or in the maximum attenuation state when $V_{MODE} = HIGH$.

V_{MODE}

The V_{MODE} pin is used to set the slope of the attenuation. The attenuation is varied by V_{CTRL} as described in the next section. Setting V_{MODE} to a logic LOW (HIGH) will set the attenuation slope to negative (positive). A negative (positive) slope is defined as an increased (decreased) attenuation with increasing V_{CTRL} voltage. The Evaluation Kit provides has an on-board jumper to manually set V_{MODE} . Install a jumper on header J7 from V_{MODE} to the pin marked Lo (Hi) to set the device for a negative (positive) slope (see Figure 58).

V_{CTRL}

The voltage level on the V_{CTRL} pin is used to control the attenuation of the F2270. At $V_{CTRL} = 0V$, the attenuation is a minimum (maximum) in the negative (positive) slope mode. An increasing voltage on V_{CTRL} produces an increasing (decreasing) attenuation respectively. The V_{CTRL} pin has an on-chip pull-up ESD diode so V_{DD} should be applied before V_{CTRL} is applied (see "Recommended Operating Conditions" for details). If this sequencing is not possible, then resistor R5 in the application circuit (see Figure 60) should be set to $1k\Omega$ to limit the current into the V_{CTRL} pin.

RF1 and RF2 Ports

The F2270 is a bi-directional device, allowing RF1 or RF2 to be used as the RF input. RF1 has some enhanced linearity performance, and therefore should be used as the RF input, when possible, for best results. The F2270 has been designed to accept high RF input power levels; therefore, V_{DD} must be applied prior to the application of RF power to ensure reliability. DC blocking capacitors are required on the RF pins and should be set to a value that results in a low reactance over the frequency range of interest. External series inductors can be added on the RF1 and RF2 lines close to the device to improve the higher frequency match.

Power Supplies

The V_{DD} supply pin should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade performance, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage changes or transients should have a slew rate smaller than $1V/20\mu s$. In addition, all control pins should remain at $0V$ ($\pm 0.3V$) while the supply voltage ramps or while it returns to zero.

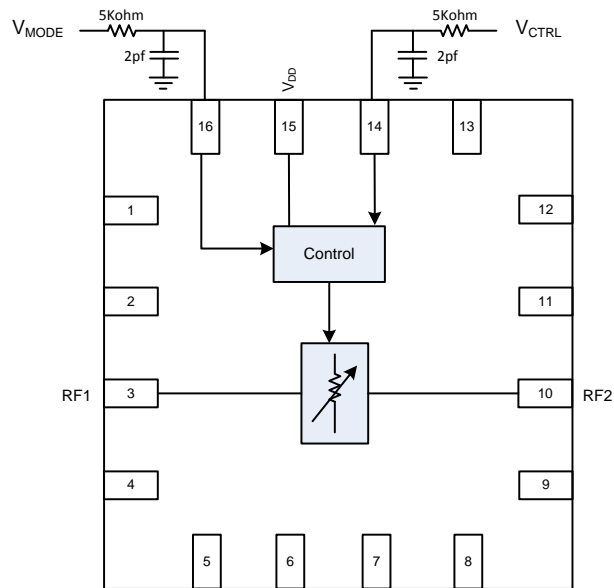
Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, or ringing, etc., then implementing the circuit shown in Figure 57 at the input of each control pin is recommended. This applies to control pins 14 (V_{CTRL}) and 16 (V_{MODE}) as shown in Figure 57. Note the recommended resistor and capacitor values do not necessarily match the Evaluation Kit BOM for the case of poor control signal integrity.

Extended Bandwidth Tuning (EBT)

There are cases where the return loss for the RF ports needs to be better than 18 dB across the frequency range. For this case, adding series inductors just next to the package on the RF ports will accomplish this. The addition of these inductors, $2.4nH$ on RF1 and $2.8nH$ on RF2, will degrade the insertion loss and return loss at frequencies above 2GHz.

Figure 57. Control Pin Interface for Signal Integrity



Evaluation Kit Pictures

Figure 58. Evaluation Kit Top View

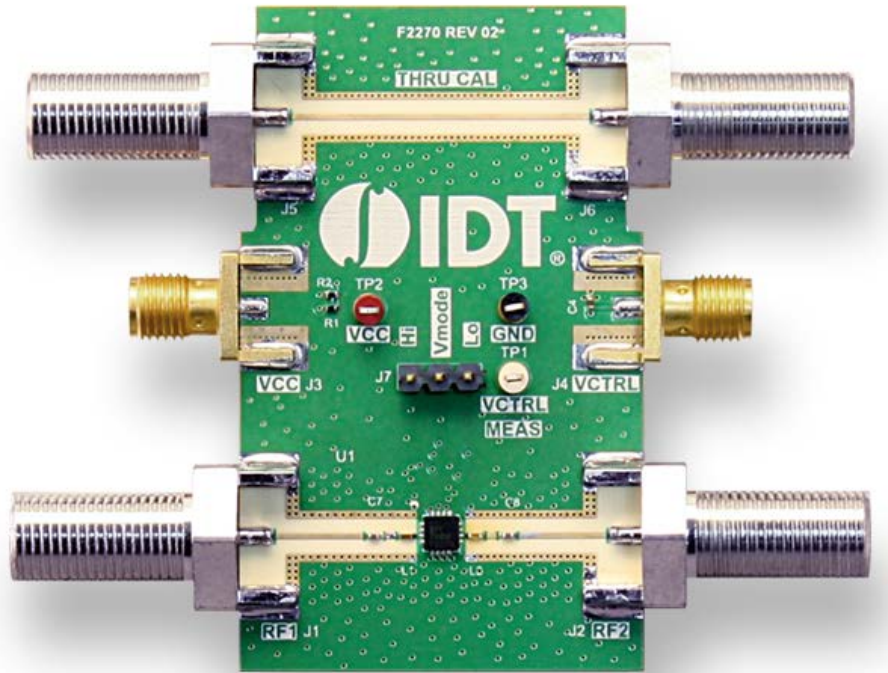
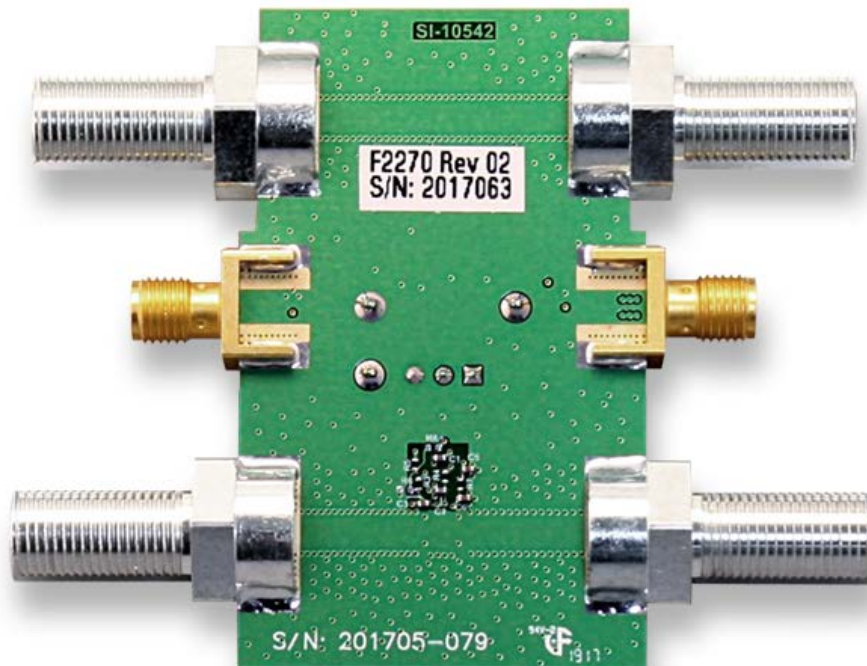


Figure 59. Evaluation Kit Bottom View



Evaluation Kit / Applications Circuit

Figure 60. Electrical Schematic

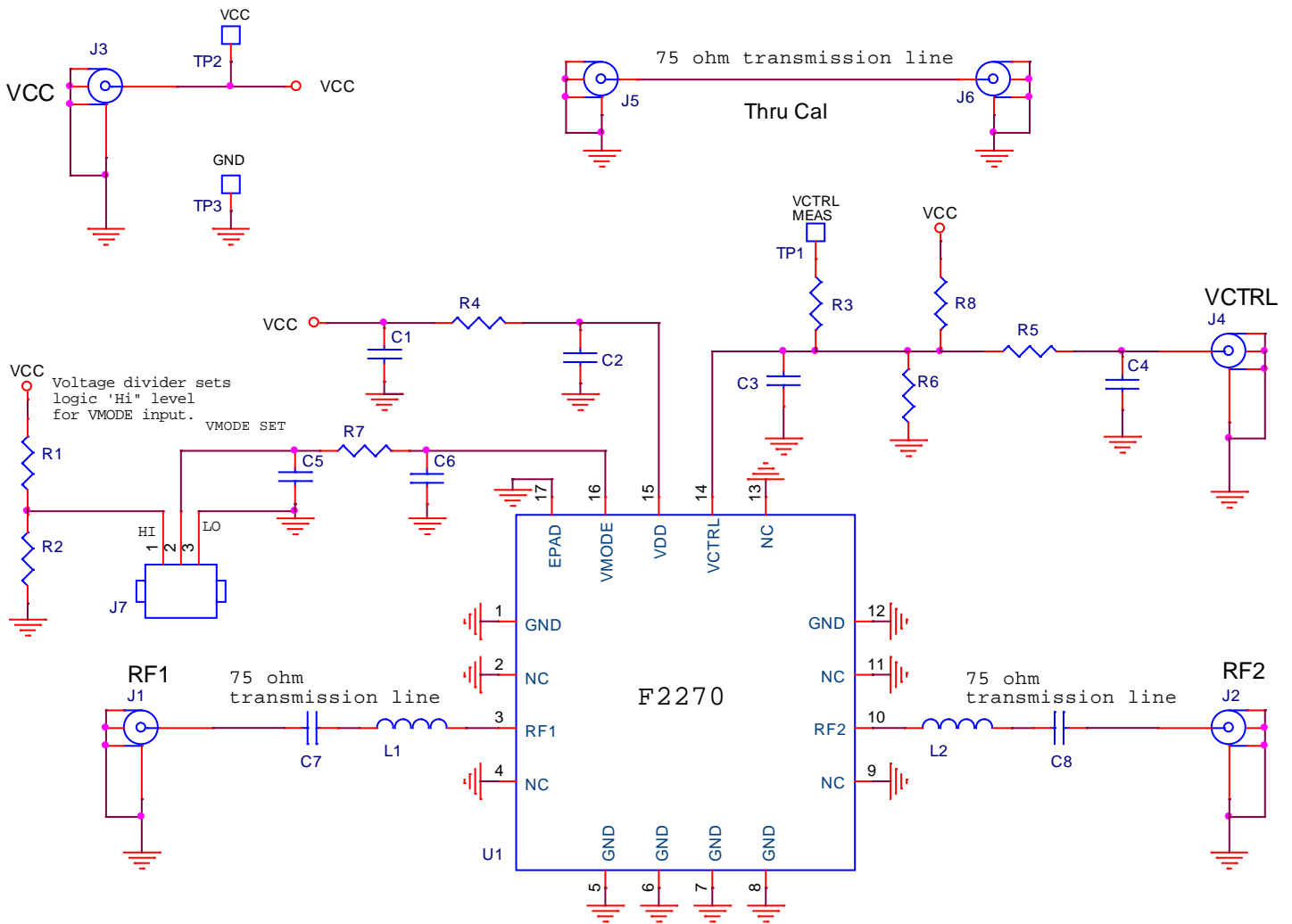


Table 8. Bill of Material (BOM)

| Part Reference | QTY | Description | Manufacturer Part # | Manufacturer |
|----------------|-----|----------------------------------------------------------|---------------------|----------------------|
| C1 – C8 | 8 | 0.1 μ F \pm 10%, 16V, X7R Ceramic Capacitor (0402) | GRM155R71C104K | Murata |
| R1, R2, R3 | 3 | 100k Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2RKF1003X | Panasonic |
| R4 | 1 | 10 Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2RKF10R0X | Panasonic |
| R5 | 1 | 1k Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2RKF1001X | Panasonic |
| R7 | 1 | 100 Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2RKF1000X | Panasonic |
| L1 [a] | 0 | 0 Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2GE0R00X | Panasonic |
| | 1 | 2.4nH \pm 0.1nH, Inductor (0402) | LQP15MN2N4B02D | Murata |
| L2 [a] | 0 | 0 Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2GE0R00X | Panasonic |
| | 1 | 2.8nH \pm 0.1nH, Inductor (0402) | LQP15MN2N8B02D | Murata |
| J1, J2, J5, J6 | 4 | Edge Launch F TYPE 75 Ω | 222181 | Amphenol |
| J3, J4 | 2 | Edge Launch SMA (0.375 inch pitch ground, tab) | 142-0701-851 | Emerson Johnson |
| J7 | 1 | Conn Header Vertical SGL 3 X 1 Pos Gold | 961103-6404-AR | 3M |
| TP1 | 1 | Test Point White | 5002 | Keystone Electronics |
| TP2 | 1 | Test Point Red | 5000 | Keystone Electronics |
| TP3 | 1 | Test Point Black | 5001 | Keystone Electronics |
| U1 | 1 | 75 Ω Voltage Variable Attenuator | F2270NLGK | IDT |
| | 1 | Printed Circuit Board | F2270 Rev 02 | IDT |
| R6, R8 | 0 | DNP | | |

[a] Series inductors are added on the RF port to improve the high-frequency port match (extended band). If not required then the 0 Ω resistor can be used.

Evaluation Kit Operation

Below is a basic setup procedure for configuring and testing the F2270 Evaluation Kit (EVKit).

Pre-Configure EVKit

This section is a guide to setting up the EVKit for testing. To configure the board for a negative attenuation slope (increasing attenuation with increasing V_{CTRL} voltage), install a header-shunt shorting pin 2 (center pin) and pin 3 (labeled Lo) on header J7 (see Figure 58). For a positive slope (decreasing attenuation with increasing V_{CTRL} voltage), this header-shunt should short pin 1 (labeled Hi) to pin 2 (center pin) on J7.

Power Supply Setup

Without making any connections to the EVKit, set up one fixed power supply (V_{CC}) for 5V with a current limit of 10mA and one variable power supply (V_{CTRL}) set to 0V with a current limit of 5mA. Disable both power supplies.

RF Test Setup

Set the RF test setup to the desired frequency and power ranges within the specified operating limits noted in this datasheet.

Disable the output power of all the RF sources.

Connect EVKit to the test setup.

With the RF sources and power supplies disabled, connect the fixed 5V power supply to connector J3, the variable supply to J4, and the RF connections to the desired RF ports.

Powering Up the EVKit

Enable the V_{CC} power supply and observe a DC current of approximately 1.4mA.

Enable the V_{CTRL} power supply.

Enable the RF sources. Verify that the DC current remains at about 1.4mA.

If the J7 connection is set for a negative (positive) attenuation slope, then increasing the variable supply will produce increased (decreased) attenuation for the attenuator path (J1 to J2).

Powering Down the EVKit

Disable the RF power applied to the device.

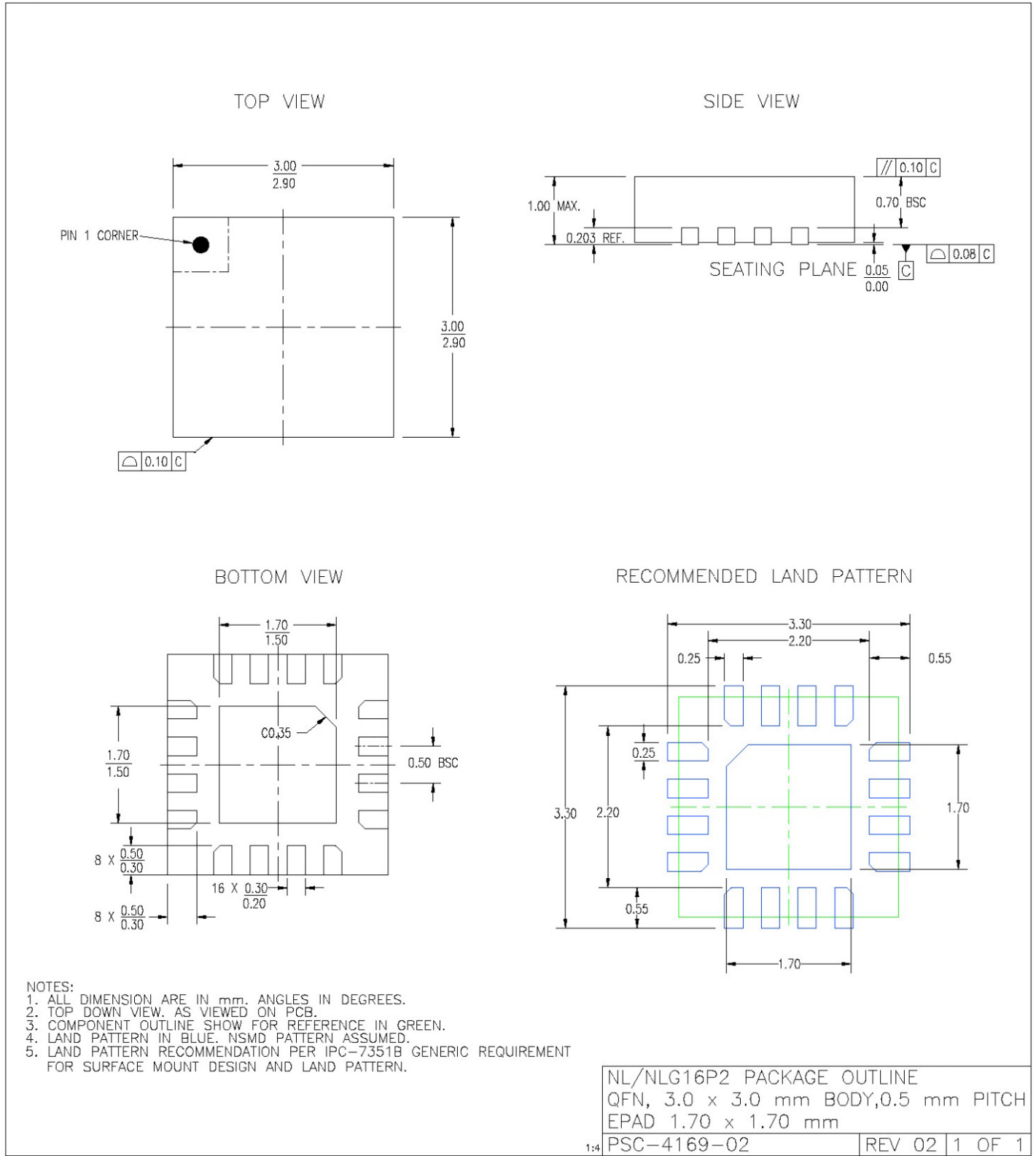
Adjust the V_{CTRL} power supply down to 0V and disable it.

Disable the V_{CC} power supply.

Disconnect the EVKit from the RF test setup.

Package Drawing and Land Pattern

Figure 61. Package Outline Drawing NLG16P2 PSC-4169-02



Marking Diagram



Line 1 "A01" is for lot code.

Line 2 "637" = has one digit for the year and week that the part was assembled.

Line 2 "W" is the assembler code.

Line 3 is the abbreviated part number.

Ordering Information

| Orderable Part Number | Package | MSL Rating | Shipping Packaging | Operating Temperature |
|-----------------------|------------------------------|------------|--------------------|-----------------------|
| F2270NLGK | 3.0mm x 3.0mm x 0.9mm 16-QFN | 1 | Tray | -40°C to +105°C |
| F2270NLGK8 | 3.0mm x 3.0mm x 0.9mm 16-QFN | 1 | Reel | -40°C to +105°C |
| F2270EVBI | Evaluation Board | | | |

Revision History

| Revision | Revision Date | Description of Change |
|----------|---------------|-----------------------|
| 0 | July 25, 2017 | Initial release |



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