



BUK6C2R1-55C

N-channel TrenchMOS intermediate level FET

Rev. 3 — 18 January 2012

Product data sheet

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high-performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- High current handling capability, up to 320 A
- Low conduction losses due to very low on-state resistance
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoids
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

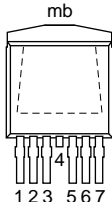
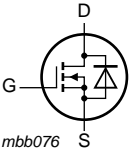
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see Figure 1	-	-	228	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	300	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 90\text{ A};$ $T_j = 25\text{ °C};$ see Figure 11	-	1.9	2.3	mΩ

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 180\text{ A}$; $V_{DS} = 44\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 13 ; see Figure 14	-	79	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped	-	-	770	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	S	source		
4	D	drain ^[1]		
5	S	source		
6	S	source		
7	S	source		
mb	D	mounting base; connected to drain	SOT427 (D2PAK)	mbb076

[1] It is not possible to connect to pin 4 of the SOT427 package.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK6C2R1-55C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)	SOT427

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	55	V
V_{GS}	gate-source voltage	Pulsed	[1] -20	20	V
		DC	[2] -16	16	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	228	A
		$T_{amb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	162	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	914	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	300	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	228	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	914	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	770	mJ

[1] Accumulated pulse duration not to exceed 5mins.

[2] -16V accumulated duration not to exceed 168 hrs.

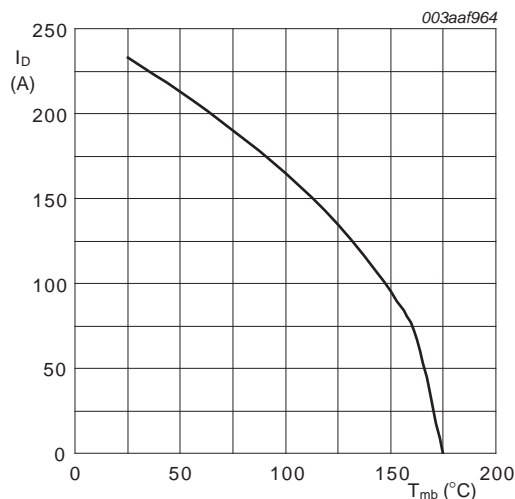
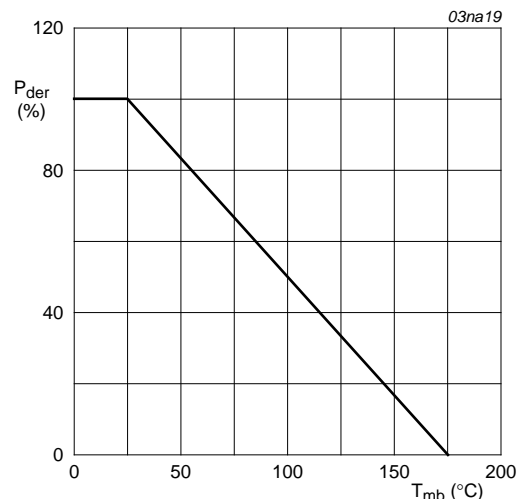


Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

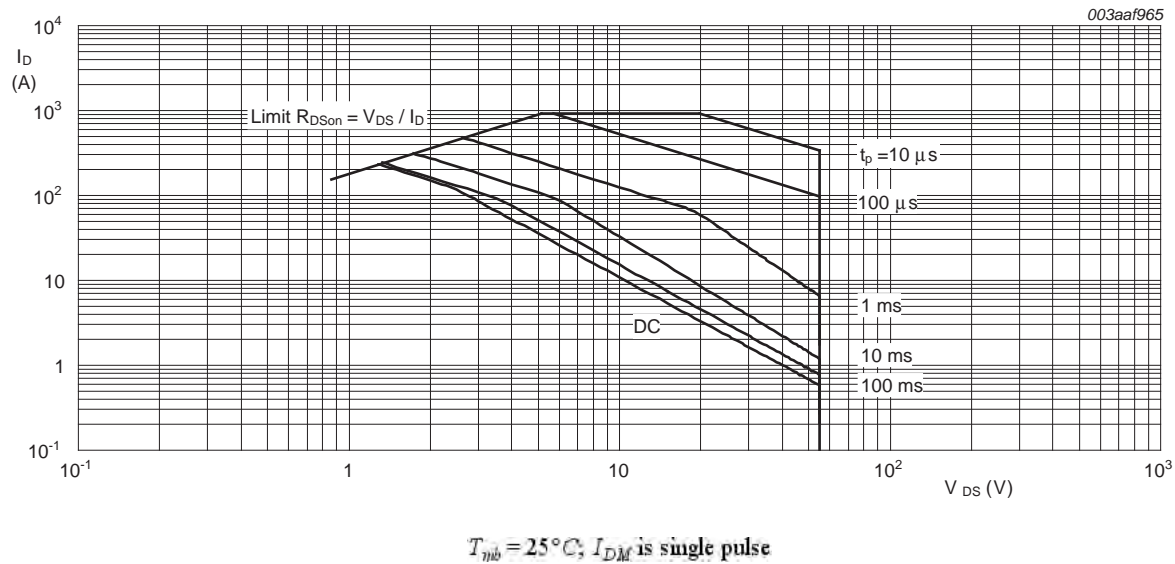


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.5	K/W

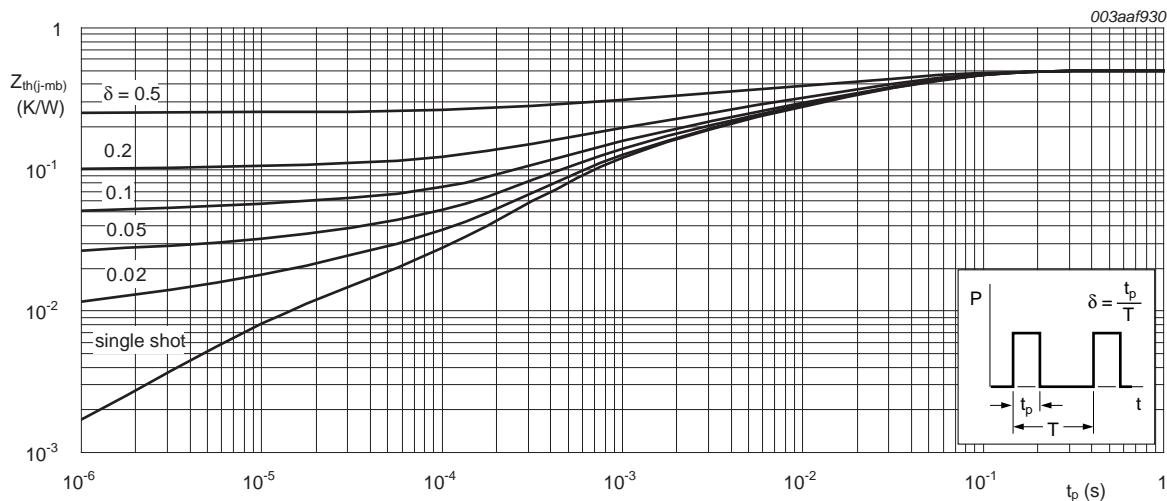


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	55	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	50	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 9 ; see Figure 10	1.8	2.3	2.8	V
V _{GSth}	gate-source threshold voltage	I _D = 2.5 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	0.8	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10	-	-	3.3	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 25 °C	-	0.04	1	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 90 A; T _j = 25 °C; see Figure 11	-	1.9	2.3	mΩ
		V _{GS} = 5 V; I _D = 90 A; T _j = 25 °C; see Figure 11	-	2.4	3.1	mΩ
		V _{GS} = 4.5 V; I _D = 90 A; T _j = 25 °C; see Figure 11	-	2.6	3.7	mΩ
		V _{GS} = 10 V; I _D = 90 A; T _j = 175 °C; see Figure 11 ; see Figure 12	-	-	5.7	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 180 A; V _{DS} = 44 V; V _{GS} = 10 V; see Figure 13 ; see Figure 14	-	253	-	nC
		I _D = 180 A; V _{DS} = 44 V; V _{GS} = 5 V; see Figure 13 ; see Figure 14	-	140	-	nC
Q _{GS}	gate-source charge	I _D = 180 A; V _{DS} = 44 V; V _{GS} = 10 V; see Figure 13 ; see Figure 14	-	40	-	nC
Q _{GD}	gate-drain charge		-	79	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 15	-	12000	16000	pF
C _{oss}	output capacitance		-	1075	1290	pF
C _{rss}	reverse transfer capacitance		-	730	1000	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 0.3 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω	-	43	-	ns
t _r	rise time		-	206	-	ns
t _{d(off)}	turn-off delay time		-	412	-	ns
t _f	fall time		-	190	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 80 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 16	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 50 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _j = 25 °C	-	56	-	ns
Q _r	recovered charge		-	115	-	nC

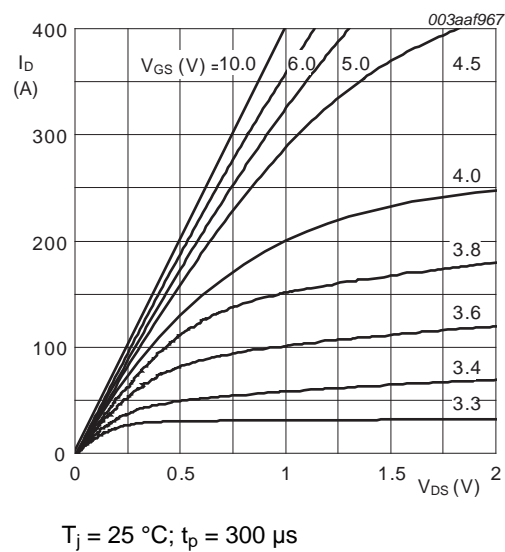


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

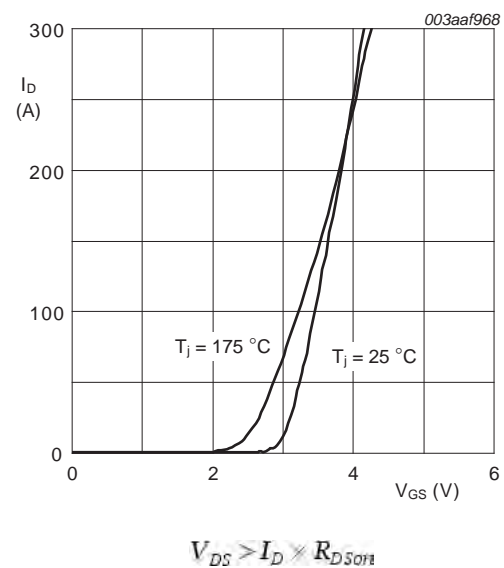


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

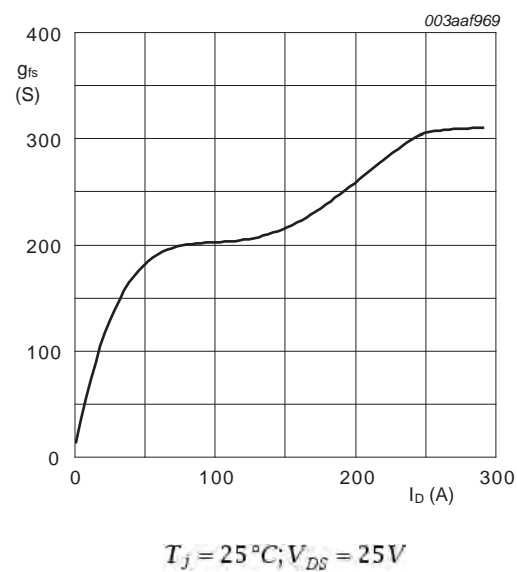


Fig 7. Forward transconductance as a function of drain current; typical values

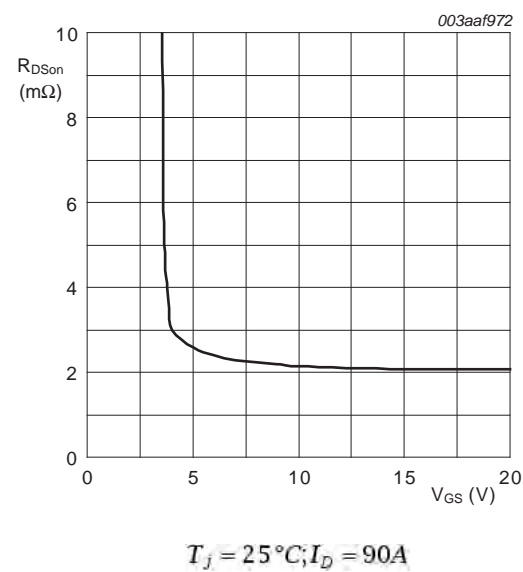
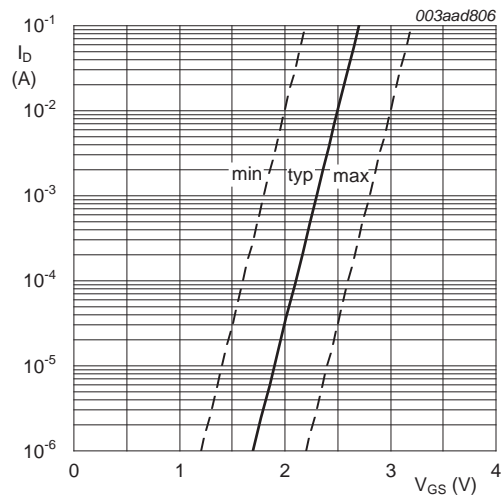
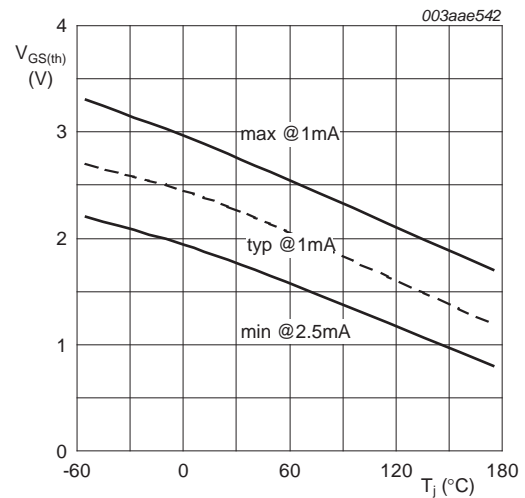


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



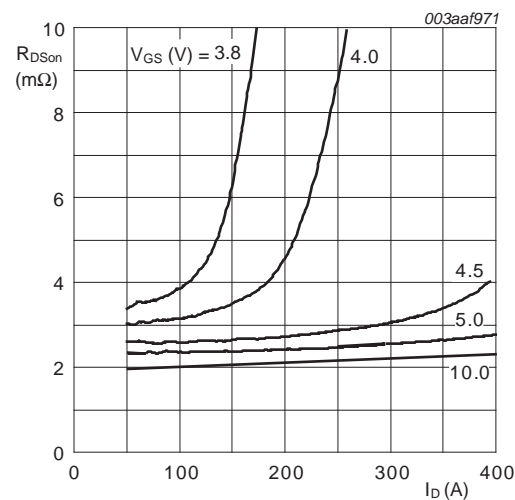
$$T_j = 25^\circ\text{C}; V_{DS} = 5V$$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



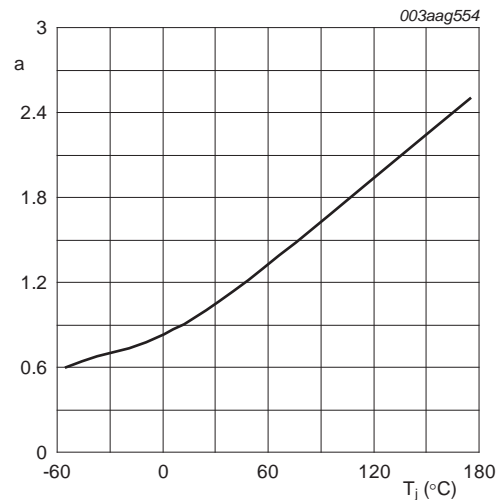
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$$T_j = 25^\circ\text{C}; t_p = 300\ \mu\text{s}$$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

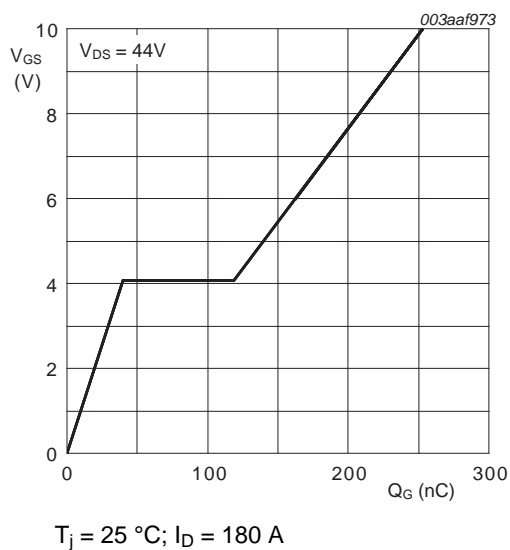


Fig 13. Gate-source voltage as a function of gate charge; typical values

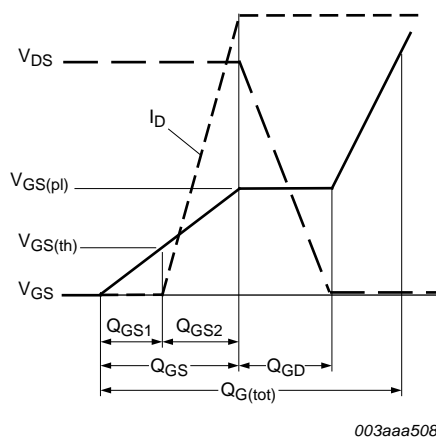


Fig 14. Gate charge waveform definitions

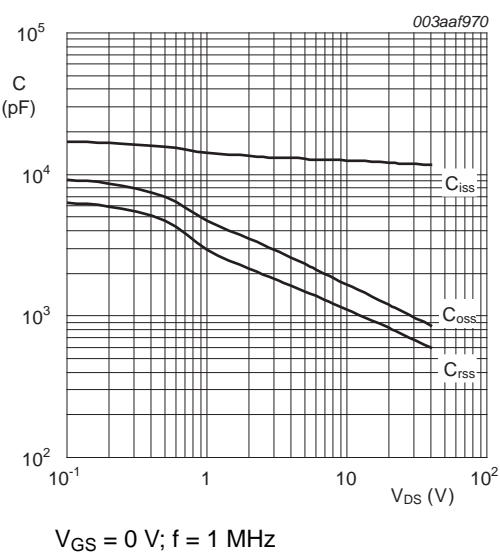


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

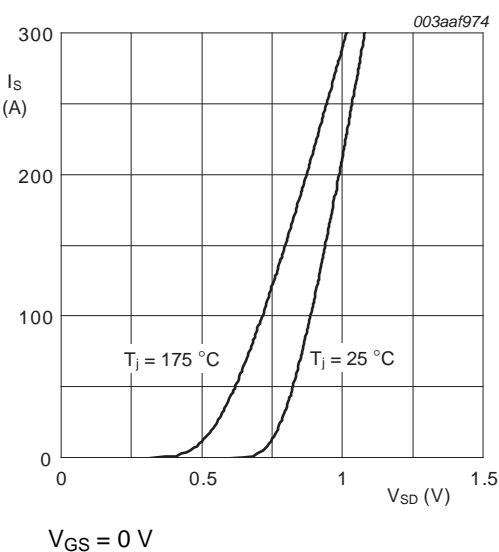
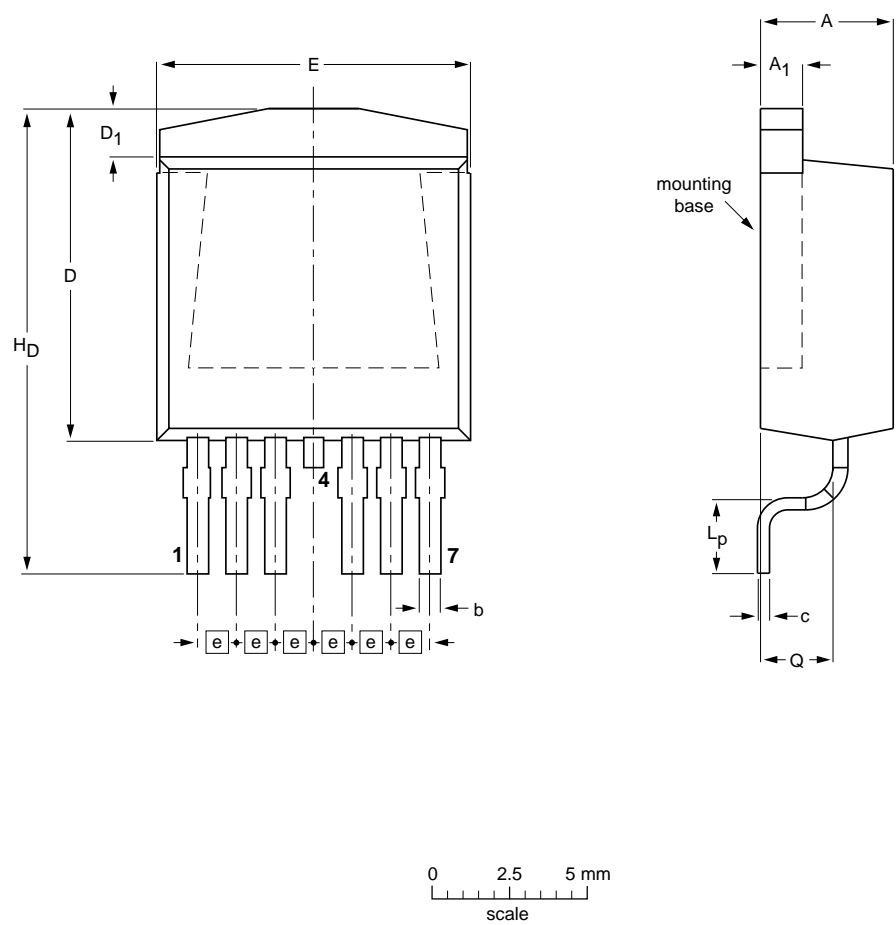


Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)

SOT427



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	1.27	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT427						05-03-09 06-03-16

Fig 17. Package outline SOT427 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6C2R1-55C v.3	20120118	Product data sheet	-	BUK6C2R1-55C v.2
Modifications:	• Status changed from preliminary to product.			
BUK6C2R1-55C v.2	20111221	Preliminary data sheet	-	BUK6C2R1-55C v.1

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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JONHON

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