M74HC259

8-bit addressable latch

Datasheet - production data


SO16


TSSOP16

Features

- High speed: t_{PD} = 20 ns (typ.) at V_{CC} = 6 V
- Low power dissipation:
  I_{CC} = 4 µA (max.) at T_A = 25 °C
- High noise immunity:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (min.)
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{PLH} \sim= t_{PHL}$
- Wide operating voltage range:
  V_{CC} (OPR) = 2 V to 6 V
- Pin and function compatible with
  74 series 259
- ESD performance
  - CDM: 1 kV
  - HBM: 1.5 kV
  - MM: 200 V

Description

The M74HC259 is a high-speed CMOS 8-bit addressable latch manufactured with silicon gate C^2MOS technology.

The M74HC259 has single data input (D) 8 latch outputs (Q0-Q7), 3 address inputs (A, B, and C), common enable input (E), and a common $\overline{\text{CLEAR}}$ input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When $\overline{\text{ENABLE}}$ is taken low, the data flows through to the address outputs. The data is stored on the positive-going edge of the $\overline{\text{ENABLE}}$ pulse. All unaddressed latches will remain unaffected. With $\overline{\text{ENABLE}}$ in the high state, the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the $\overline{\text{ENABLE}}$ should be held high (inactive) while the address lines are changing. If $\overline{\text{ENABLE}}$ is held high and $\overline{\text{CLEAR}}$ is taken low, all eight latches are cleared to the low state. If $\overline{\text{ENABLE}}$ is low, all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

All inputs are equipped with protection circuits to guard against static discharge and transient excess voltage.

Table 1: Device summary

Order code	Temperature range	Package	Packaging	Marking
M74HC259YRM13TR(1)	-40 °C to +125 °C	SO16 (automotive grade)[1]	Tape and reel	74HC259Y
M74HC259RM13TR	-55 °C to +125 °C	SO16	Tape and reel	74HC259
M74HC259TTR	-55 °C to +125 °C	TSSOP16	Tape and reel	HC259
M74HC259YTTR[1]	-40 °C to +125 °C	TSSOP16 (automotive grade)[1]	Tape and reel	HC259Y

Notes:

(1)Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

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1 Pin information

Figure 1: Pin connections and IEC logic symbols

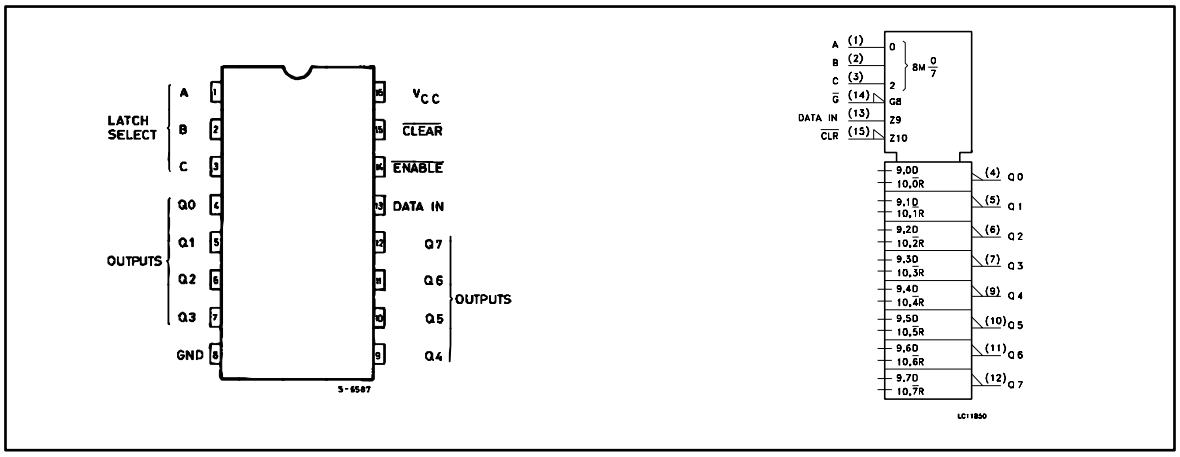


Table 2: Pin description

Pin number	Symbol	Name and function
1, 2, 3	A, B, C	Address inputs
4, 5, 6, 7, 9, 10, 11, 12	Q0 to Q7	Latch outputs
13	D	Data input
14	$\overline{\text{ENABLE}}$	Latch enable input (active low)
15	$\overline{\text{CLEAR}}$	Conditional reset input (low)
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

2 Functional description

Table 3: Truth table

Inputs		Outputs of addressed latch	Other output	Function
$\overline{\text{CLEAR}}$	$\overline{\text{ENABLE}}$			
H	L	D	Qi0	Addressable latch
H	H	Qi0	Qi0	Memory
L	L	D	L	8-line demulitplexer
L	H	L	L	Clear all bits to "L"

D: the level at the data input

Qi0: the level before the indicated steady state input conditions where established (i = 0, 1, ……, 7)

Inputs selected			Latch addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

Figure 2: Input and output equivalent circuit

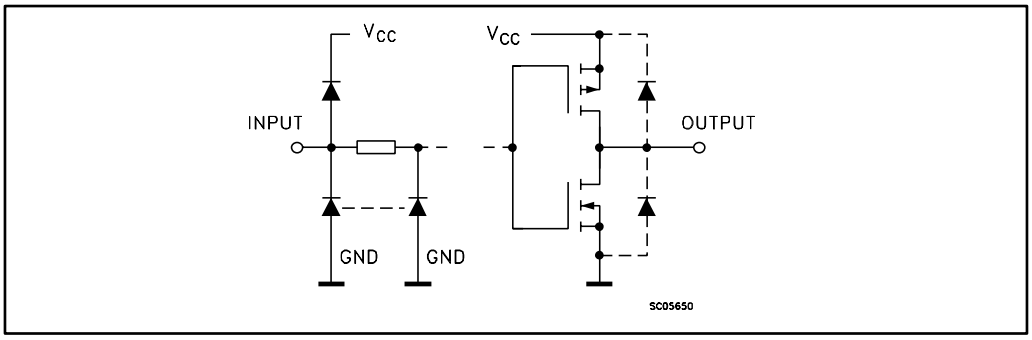
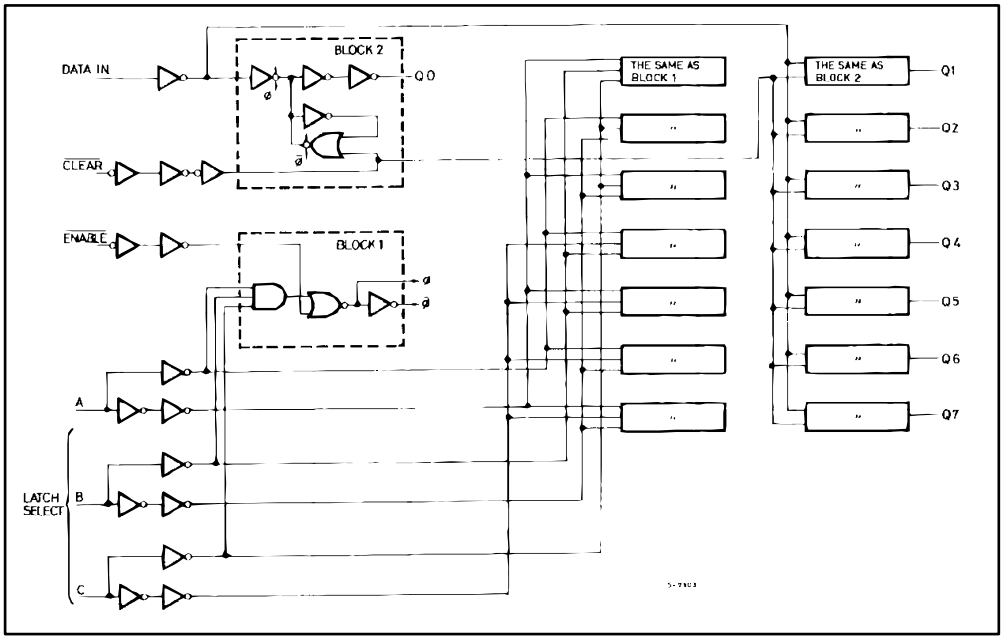


Figure 3: Logic diagram



This logic diagram has not been used to estimate propagation delays.

3 Electrical characteristics

Stressing the device above the ratings listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to V_{CC} to +0.5	V
V_O	DC output voltage	-0.5 to V_{CC} to +0.5	V
I_{IK}	DC input diode current	±20	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±25	mA
I_{CC} or I_{GND}	DC VCC or ground current	±50	mA
P_D	Power dissipation	500(1)	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	300	°C

Notes:

(1)500 mW at 65 °C; derate to 300 mW by 10 mW/°C from 65 °C to 85 °C

Table 5: Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		2 to 6	V
V_I	Input voltage		0 to V_{CC}	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
t_r, t_f	Input rise and fall time	V_{CC} = 2.0 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	ns
		V_{CC} = 6.0 V	0 to 400	ns

Table 6: DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High-level input voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low-level input voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High-level output voltage	2.0	I_O = -20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O = -20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O = -20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O = -5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low-level output voltage	2.0	I_O = 20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O = 20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O = 20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O = 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input leakage current	6.0	V_I = V_{CC} or GND			±0.1		±1		±1	µA
I_{CC}	Quiescent supply current	6.0	V_I = V_{CC} or GND			4		40		80	µA

Table 7: AC electrical characteristics (C_L = 50 pF, input t_r = t_f = 6 ns)

Symbol	Parameter	Test condition	Value							Unit
			T_A = 25°C			-40 to 85°C		-55 to 125°C		
		V_{CC} (V)	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output transition time	2.0		30	75		95		110	ns
		4.5		8	15		19		22	
		6.0		7	13		16		19	
t_{PLH} t_{PHL}	Propagation delay time (DATA – Q)	2.0		56	140		175		210	ns
		4.5		18	28		35		42	
		6.0		15	24		30		36	
t_{PLH} t_{PHL}	Propagation delay time (A, B, C – Q)	2.0		76	190		240		285	ns
		4.5		24	38		48		57	
		6.0		20	32		41		48	
t_{PLH} t_{PHL}	Propagation delay time (G – Q)	2.0		57	150		190		225	ns
		4.5		19	30		38		45	
		6.0		16	26		32		38	
t_{PLH} t_{PHL}	Propagation delay time ($\overline{\text{CLEAR}}$ – Q)	2.0		45	115		145		175	ns
		4.5		15	23		29		35	
		6.0		13	20		25		30	
$t_{W(L)}$	Minimum pulse width ($\overline{\text{ENABLE}}$)	2.0		28	75		90		115	ns
		4.5		7	15		19		23	
		6.0		6	13		16		20	
$t_{W(L)}$	Minimum pulse width ($\overline{\text{CLEAR}}$)	2.0		24	75		90		115	ns
		4.5		6	15		19		23	
		6.0		5	13		16		20	
t_S	Minimum setup time (DATA)	2.0		12	50		60		75	ns
		4.5		3	10		12		15	
		6.0		3	9		11		13	
t_S	Minimum setup time (A, B, C)	2.0			25		30		40	ns
		4.5			5		6		8	
		6.0			5		5		7	
t_h	Minimum hold time (DATA)	2.0			5		5		5	ns
		4.5			5		5		5	
		6.0			5		5		5	
t_h	Minimum hold time (A, B, C)	2.0			0		0		0	ns
		4.5			0		0		0	
		6.0			0		0		0	

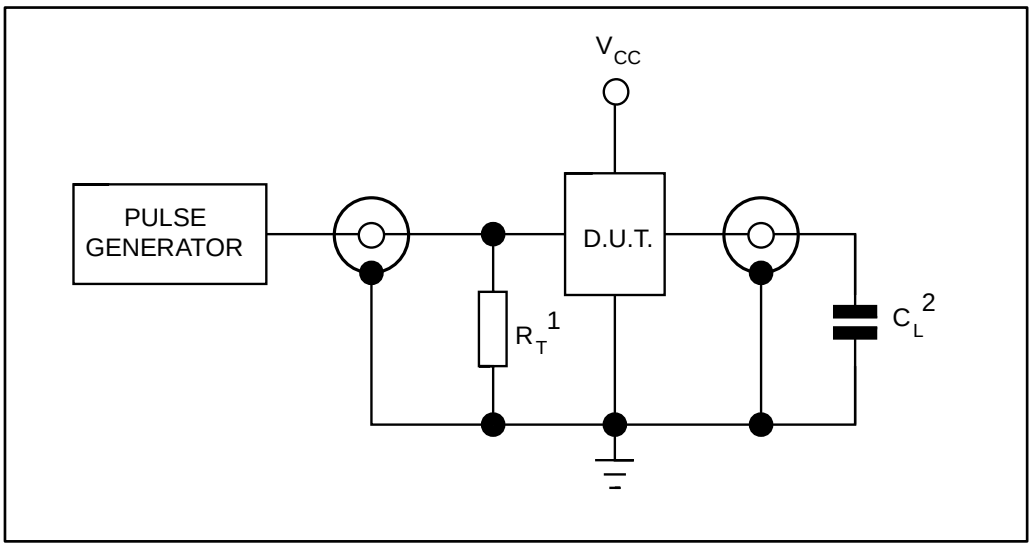
Table 8: Capacitive characteristics

Symbol	Parameter	Test condition	Value							Unit
			T_A = 25°C			-40 to 85°C		-55 to 125°C		
		V_{CC} (V)	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input capacitance	5.0		5	10		10		10	pF
C_{PD}	Power dissipation capacitance(1)	5.0		66						pF

Notes:

(1)C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to the test circuit). The average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Figure 4: Test circuit



1. $R_T = Z_{OUT}$ of pulse generator (typically 50 ohm)
2. C_L = 50 pF or equivalent (includes jig and probe capacitance)

Figure 5: Waveform 1: propagation delay time (f = 1 MHz; 50% duty cycle)

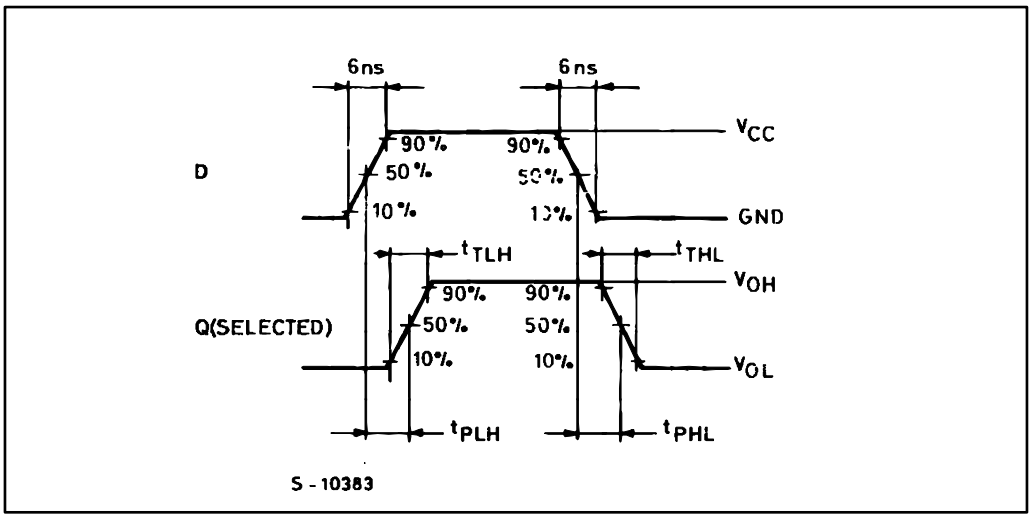


Figure 6: Waveform 2: propagation delay time (f = 1 MHz; 50% duty cycle)

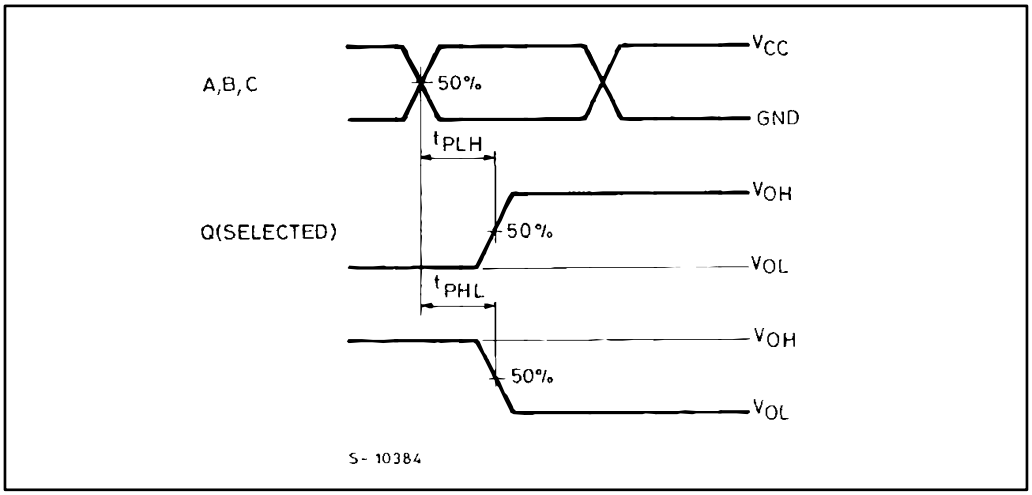


Figure 7: Waveform 3: minimum pulse width (G), setup and hold time (D to G) (f = 1 MHz; 50% duty cycle)

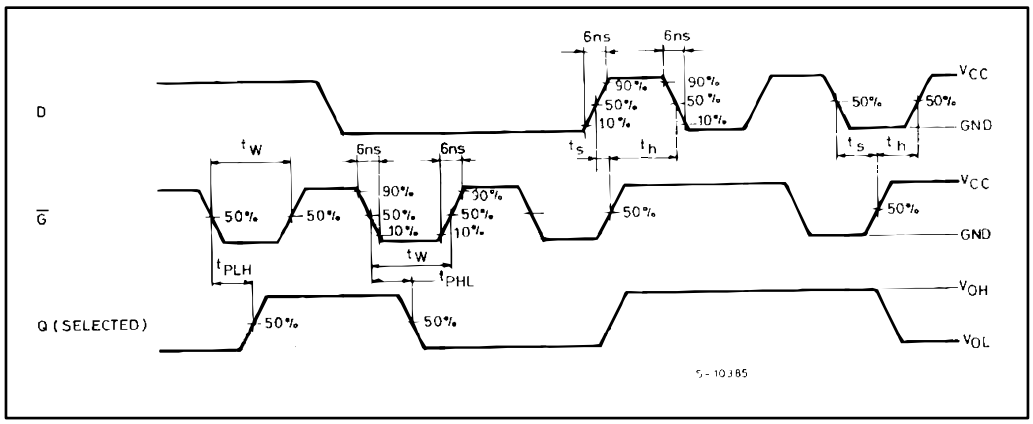


Figure 8: Waveform 4: minimum pulse width (CLR) (f = 1 MHz; 50% duty cycle)

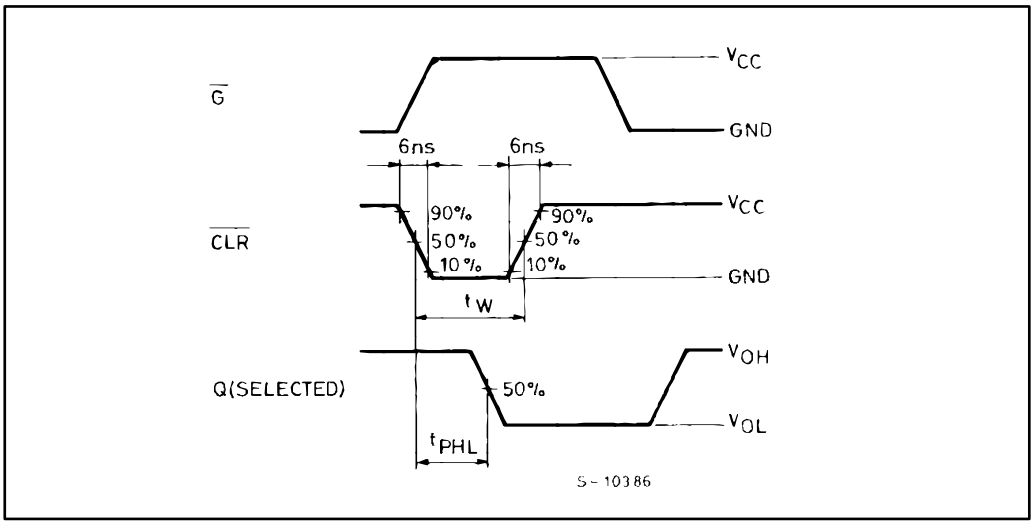


Figure 9: Waveform 5: setup and hold time (f = 1 MHz; 50% duty cycle)

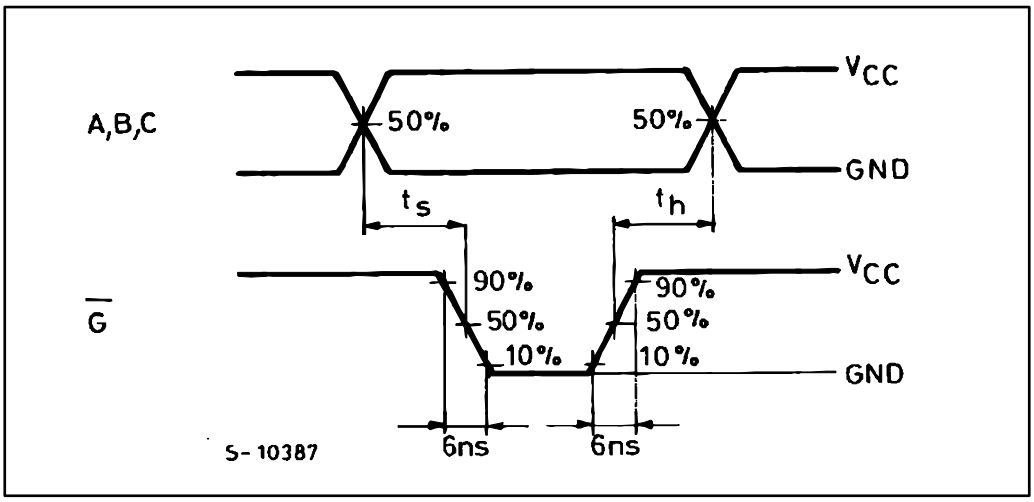
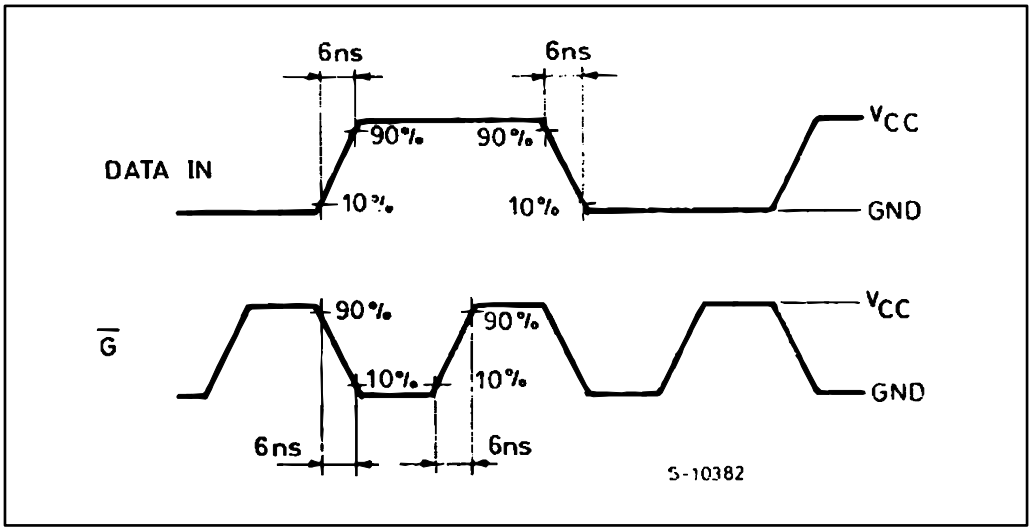


Figure 10: Waveform 6: input waveforms (f = 1 MHz; 50% duty cycle)



4 Package information

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4.1 SO16 package information

Figure 11: Plastic SO16 package mechanical outline

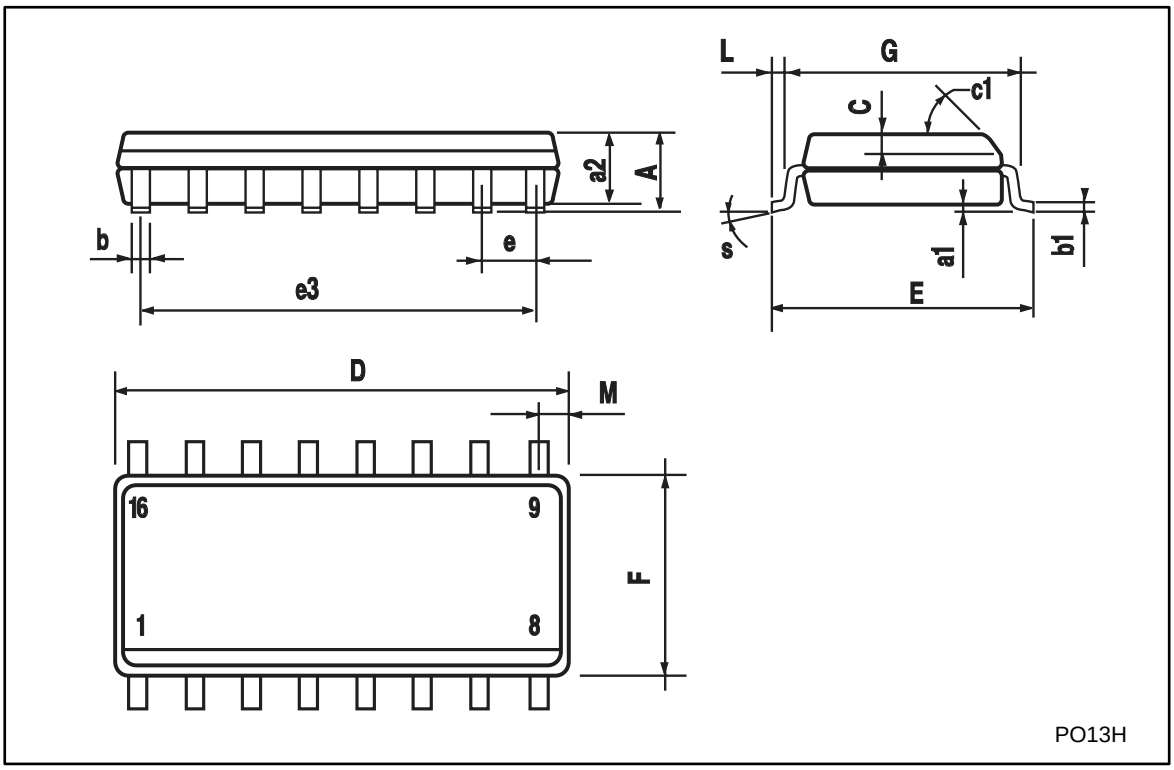

Table 9: Plastic SO16 package mechanical data

Dimensions	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 ° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 ° (max.)					

4.3 TSSOP16 package information

Figure 12: TSSOP16 package mechanical outline

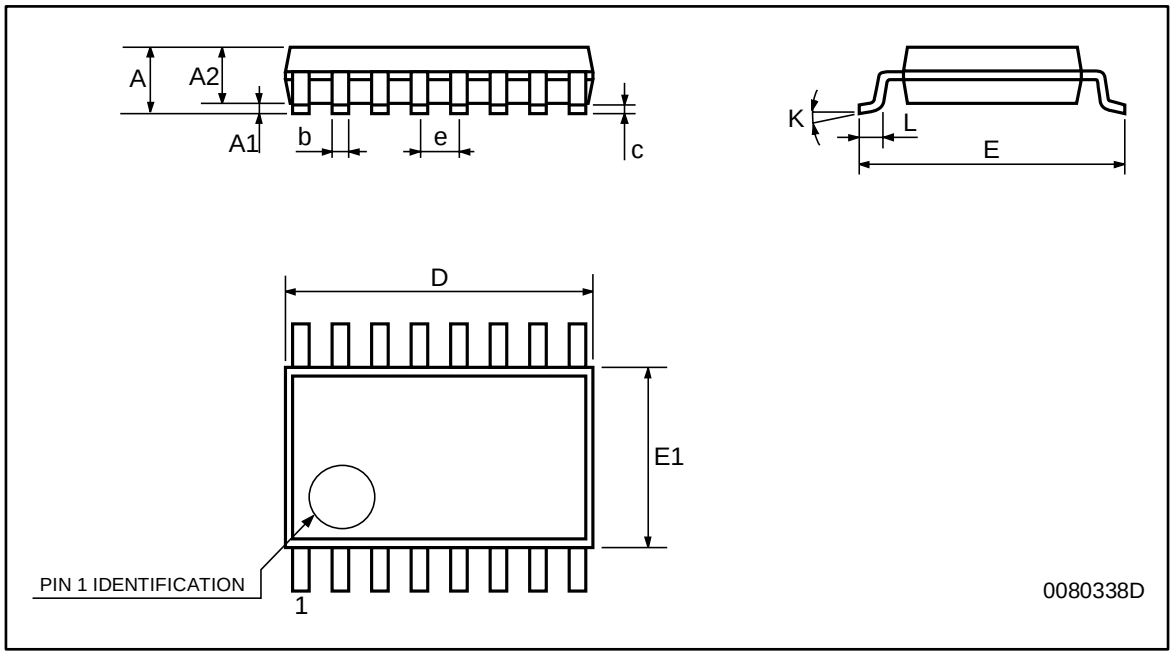

Table 10: TSSOP16 package mechanical data

Dimensions	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

5 Revision history

Table 11: Document revision history

Date	Version	Change
Jul-2001	1	Initial release
01-Nov-2013	2	Added ESD performance to *Section "Features"* Added automotive grade order codes, temperature ranges and marking information to *Table 1: "Device summary"* Removed DIP16 package option Revised document presentation, minor textual updates

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