



24AA00/24LC00/24C00

128-Bit I²C™ Bus Serial EEPROM

Device Selection Table

| Device | Vcc Range | Temp Range |
|--------|-----------|------------|
| 24AA00 | 1.7-5.5 | I |
| 24LC00 | 2.5-5.5 | I |
| 24C00 | 4.5-5.5 | I,E |

Features:

- Single supply with operation down to 1.7V for 24AA00 devices, 2.5V for 24LC00 devices
- Low-power CMOS technology:
 - Read current 500 μ A, typical
 - Standby current 100 nA, typical
- 2-wire serial interface, I²C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz and 400 kHz clock compatibility
- Page write time 3 ms, typical
- Self-timed erase/write cycle
- ESD protection >4000V
- More than 1 million erase/write cycles
- Data retention >200 years
- Factory programming available
- Packages include 8-lead PDIP, SOIC, TSSOP, DFN and 5-lead SOT-23
- Pb-free and RoHS compliant
- Temperature ranges available:
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

Description:

The Microchip Technology Inc. 24AA00/24LC00/24C00 (24XX00*) is a 128-bit Electrically Erasable PROM memory organized as 16 x 8 with a 2-wire serial interface. Low-voltage design permits operation down to 1.7 volts for the 24AA00 version, and every version maintains a maximum standby current of only 1 μ A and typical active current of only 500 μ A. This device was designed for where a small amount of EEPROM is needed for the storage of calibration values, ID numbers or manufacturing information, etc. The 24XX00 is available in 8-pin PDIP, 8-pin SOIC (3.90 mm), 8-pin TSSOP, 8-pin 2x3 DFN and the 5-pin SOT-23 packages.

*24XX00 is used in this document as a generic part number for the 24AA00/24LC00/24C00 devices.

Package Types



Block Diagram



Pin Function Table

| Name | Function |
|------|------------------------|
| Vss | Ground |
| SDA | Serial Data |
| SCL | Serial Clock |
| Vcc | +1.7V to 5.5V (24AA00) |
| | +2.5V to 5.5V (24LC00) |
| | +4.5V to 5.5V (24C00) |
| NC | No Internal Connection |

I²C is a trademark of Philips Corporation.

TABLE 1-2: AC CHARACTERISTICS

| All Parameters apply across all recommended operating ranges unless otherwise noted | | Industrial (I): TA = -40°C to +85°C, VCC = 1.8V to 5.5V Automotive (E): TA = -40°C to +125°C, VCC = 4.5V to 5.5V | | | |
|---|---------|---|---------------------|--------|--|
| Parameter | Symbol | Min | Max | Units | Conditions |
| Clock frequency | FCLK | — — — | 100 100 400 | kHz | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Clock high time | THIGH | 4000 4000 600 | — — — | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Clock low time | TLOW | 4700 4700 1300 | — — — | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| SDA and SCL rise time (Note 1) | TR | — — — | 1000 1000 300 | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| SDA and SCL fall time | TF | — | 300 | ns | (Note 1) |
| Start condition hold time | THD:STA | 4000 4000 600 | — — — | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Start condition setup time | TSU:STA | 4700 4700 600 | — — — | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Data input hold time | THD:DAT | 0 | — | ns | (Note 2) |
| Data input setup time | TSU:DAT | 250 250 100 | — — — | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Stop condition setup time | TSU:STO | 4000 4000 600 | — — — | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Output valid from clock (Note 2) | TAA | — — — | 3500 3500 900 | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Bus free time: Time the bus must be free before a new transmission can start | TBUF | 4700 4700 1300 | — — — | ns | 4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.7V ≤ VCC ≤ 4.5V 4.5V ≤ VCC ≤ 5.5V |
| Output fall time from VIH minimum to VIL maximum | TOF | 20+0.1 CB | 250 | ns | (Note 1), CB ≤ 100 pF |
| Input filter spike suppression (SDA and SCL pins) | TSP | — | 50 | ns | (Notes 1, 3) |
| Write cycle time | TWC | — | 4 | ms | |
| Endurance | | 1M | — | cycles | (Note 4) |

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained at www.microchip.com.

2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10 k Ω for 100 kHz, 2 k Ω for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 Noise Protection

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24XX00 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions, while the 24XX00 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is theoretically unlimited.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note: The 24XX00 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

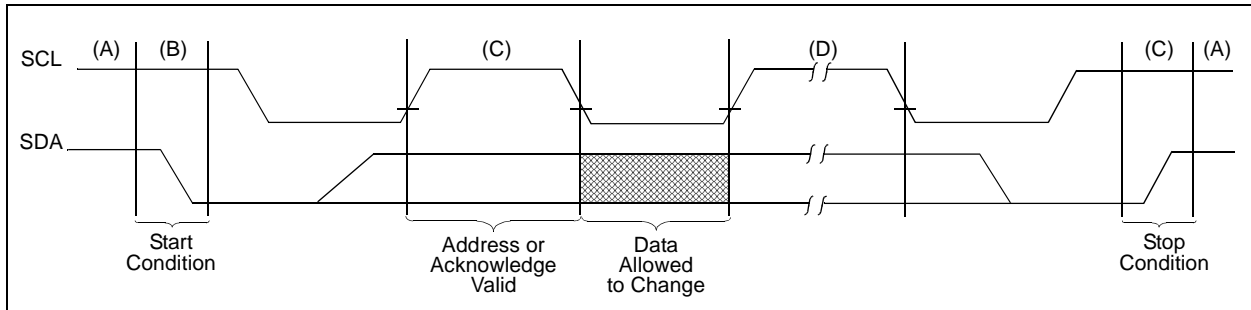
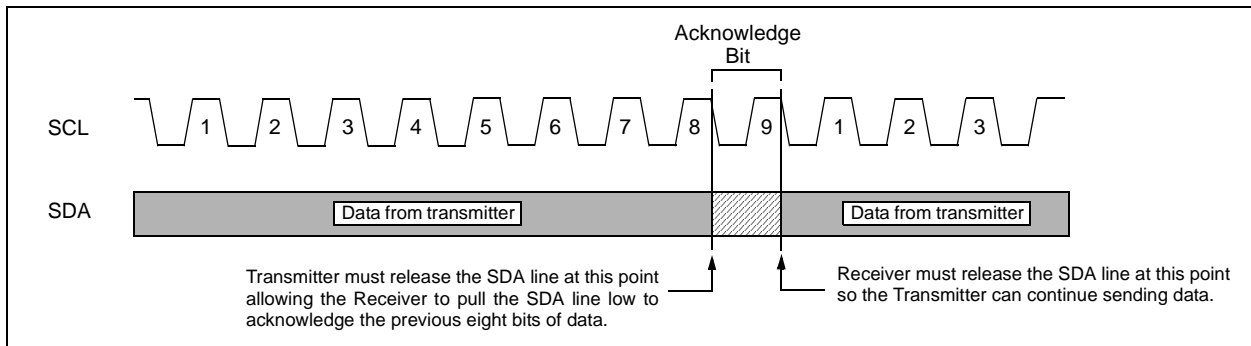


FIGURE 4-2: ACKNOWLEDGE TIMING



24AA00/24LC00/24C00

5.0 DEVICE ADDRESSING

After generating a Start condition, the bus master transmits a control byte consisting of a slave address and a Read/Write bit that indicates what type of operation is to be performed. The slave address for the 24XX00 consists of a 4-bit device code '1010' followed by three "don't care" bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected (Figure 5-1). The 24XX00 monitors the bus for its corresponding slave address all the time. It generates an Acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 5-1: CONTROL BYTE FORMAT



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start signal from the master, the device code (4 bits), the "don't care" bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24XX00. Only the lower four address bits are used by the device, and the upper four bits are "don't cares." The 24XX00 will acknowledge the address byte and the master device will then transmit the data word to be written into the addressed memory location. The 24XX00 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and during this time the 24XX00 will not generate Acknowledge signals (Figure 7-2). After a byte Write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a Stop bit is transmitted to the device at any point in the Write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the Stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a Stop bit is sent before a full eight data bits have been transmitted, then the Write command will abort and no data will be written. The 24XX00 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5V (24AA00 and 24LC00) or 3.8V (24C00) at nominal conditions.

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command ($R/\bar{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



FIGURE 7-2: BYTE WRITE



FIGURE 8-2: RANDOM READ



FIGURE 8-3: SEQUENTIAL READ



24AA00/24LC00/24C00

9.0 PACKAGING INFORMATION

9.1 Package Marking Information

8-Lead PDIP (300 mil)



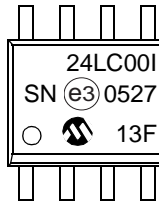
Example:



8-Lead SOIC (3.90 mm)



Example:



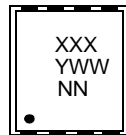
8-Lead TSSOP



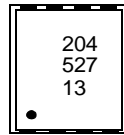
Example:



8-Lead 2x3 DFN



Example:



5-Lead SOT-23



Example:



24AA00/24LC00/24C00

| Part Number | 1st Line Marking Codes | | | | |
|-------------|------------------------|---------|---------|---------|---------|
| | TSSOP | SOT-23 | | DFN | |
| | | I Temp. | E Temp. | I Temp. | E Temp. |
| 24AA00 | 4A00 | B0NN | — | 201 | — |
| 24LC00 | 4L00 | M0NN | — | 204 | — |
| 24C00 | 4C00 | D0NN | E0NN | 207 | 208 |

Note: NN = Alphanumeric traceability code

| | | |
|----------------|--------|--|
| Legend: | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

24A00/24LC00/24C00

8-Lead Plastic Dual In-Line (P or PA) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | INCHES | | |
|----------------------------|----|-------|----------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | | |
| Pitch | e | | .100 BSC | | |
| Top to Seating Plane | A | | – | – | .210 |
| Molded Package Thickness | A2 | | .115 | .130 | .195 |
| Base to Seating Plane | A1 | | .015 | – | – |
| Shoulder to Shoulder Width | E | | .290 | .310 | .325 |
| Molded Package Width | E1 | | .240 | .250 | .280 |
| Overall Length | D | | .348 | .365 | .400 |
| Tip to Seating Plane | L | | .115 | .130 | .150 |
| Lead Thickness | c | | .008 | .010 | .015 |
| Upper Lead Width | b1 | | .040 | .060 | .070 |
| Lower Lead Width | b | | .014 | .018 | .022 |
| Overall Row Spacing § | eB | | – | – | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

24AA00/24LC00/24C00

8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

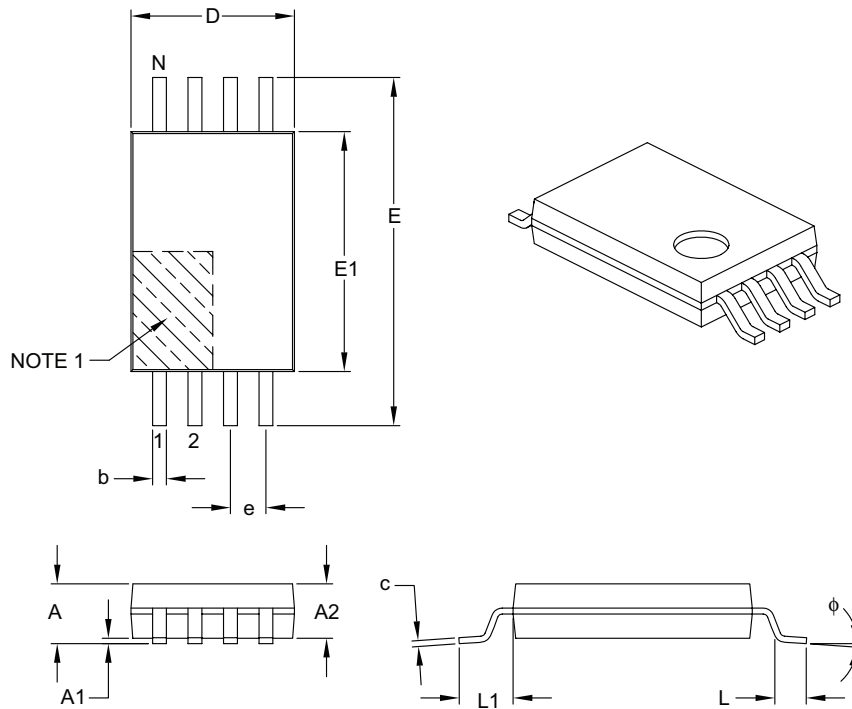
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

24A00/24LC00/24C00

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | 6.40 BSC | | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

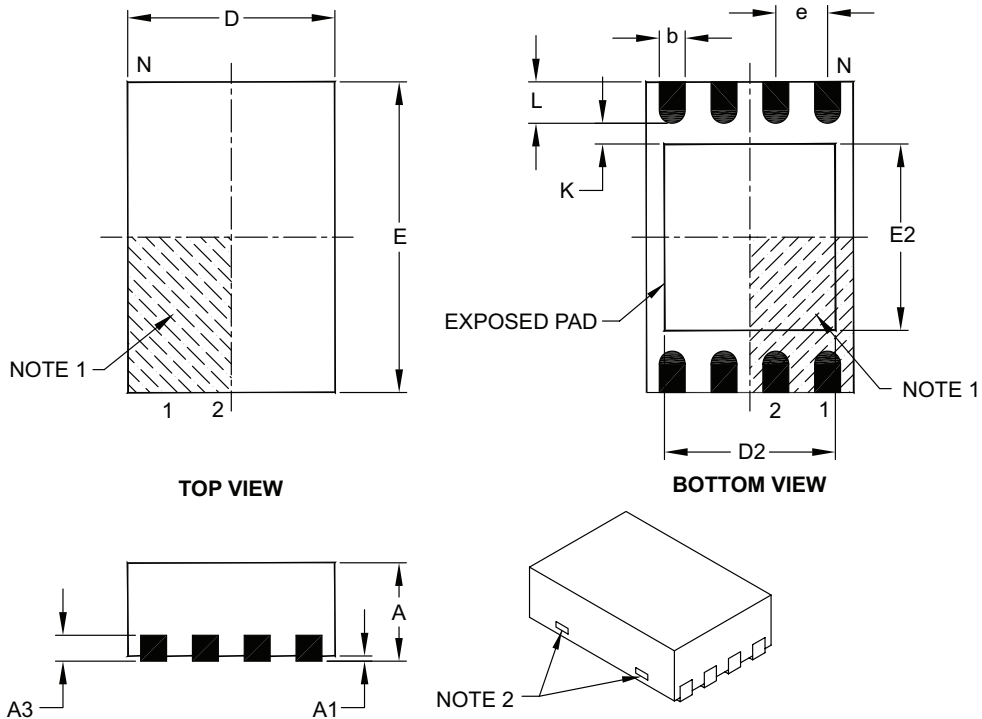
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

24AA00/24LC00/24C00

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 2.00 BSC | | |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Length | D2 | 1.30 | – | 1.75 |
| Exposed Pad Width | E2 | 1.50 | – | 1.90 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B

24A00/24LC00/24C00

5-Lead Plastic Small Outline Transistor (OT or CT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | MILLIMETERS | | |
|--------------------------|--------|-------|-------------|-----|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 5 | | |
| Lead Pitch | e | | 0.95 BSC | | |
| Outside Lead Pitch | e1 | | 1.90 BSC | | |
| Overall Height | A | 0.90 | – | | 1.45 |
| Molded Package Thickness | A2 | 0.89 | – | | 1.30 |
| Standoff | A1 | 0.00 | – | | 0.15 |
| Overall Width | E | 2.20 | – | | 3.20 |
| Molded Package Width | E1 | 1.30 | – | | 1.80 |
| Overall Length | D | 2.70 | – | | 3.10 |
| Foot Length | L | 0.10 | – | | 0.60 |
| Footprint | L1 | 0.35 | – | | 0.80 |
| Foot Angle | ϕ | 0° | – | | 30° |
| Lead Thickness | c | 0.08 | – | | 0.26 |
| Lead Width | b | 0.20 | – | | 0.51 |

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

APPENDIX A: REVISION HISTORY

Revision E

Added DFN package.

Revision F (02/2007)

Revised Device Selection Table; Features Section;
Changed 1.8V to 1.7V; Revised Tables 1-1, 1-2;
Revised Product ID System; Replaced Package
Drawings; Replaced On-line Support page.

Revision G (03/2007)

Replaced Package Drawings (Rev. AM).

24AA00/24LC00/24C00

NOTES:

THE MICROCHIP WEB SITE

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Technical support is available through the web site at: <http://support.microchip.com>

24AA00/24LC00/24C00

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Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>X</u> | <u>XX</u> |
|---|-------------------|---|
| Device | Temperature Range | Package |
| <p>Device:</p> <p>24AA00: = 1.7V, 128 bit I²C™ Serial EEPROM</p> <p>24AA00T: = 1.7V, 128 bit I²C Serial EEPROM (Tape and Reel)</p> <p>24LC00: = 2.5V, 128 bit I²C Serial EEPROM</p> <p>24LC00T: = 2.5V, 128 bit I²C Serial EEPROM (Tape and Reel)</p> <p>24C00: = 5V, 128 bit I²C™ Serial EEPROM</p> <p>24C00T: = 5V, 128 bit I²C™ Serial EEPROM (Tape and Reel)</p> | | |
| <p>Temperature Range:</p> <p>I = -40°C to +85°C</p> <p>E = -40°C to +125°C</p> | | |
| <p>Package:</p> <p>P = Plastic DIP (300 mil body), 8-lead</p> <p>SN = Plastic SOIC (3.90 mm body), 8-lead</p> <p>ST = Plastic TSSOP (4.4 mm), 8-lead</p> <p>OT = SOT-23, 5-lead (Tape and Reel only)</p> <p>MC = 2x3 DFN, 8-lead</p> | | |
| | | <p>Examples:</p> <p>a) 24AA00-I/P: Industrial Temperature, 1.8V PDIP package</p> <p>b) 24AA00-I/SN: Industrial Temperature, 1.8V, SOIC package</p> <p>c) 24AA00T-I/OT: Industrial Temperature, 1.8V, SOT-23 package, tape and reel</p> <p>d) 24LC00-I/P: Industrial Temperature, 2.5V, PDIP package</p> <p>e) 24C00-E/SN: Extended Temperature, 5V, SOIC package</p> <p>f) 24LC00T-I/OT: Industrial Temperature, 2.5V, SOT-23 package, tape and reel</p> |

24AA00/24LC00/24C00

NOTES:

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