

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> T <sub>C</sub> = +25°C (Note 9)
40V	1.8mΩ @ V <sub>GS</sub> = 10V	100A

## Description and Applications

This MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Engine Management Systems
- Body Control Electronics
- DC-DC Converters

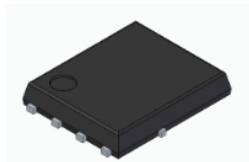
## Features

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R<sub>DS(ON)</sub> – Minimizes On State Losses
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **An Automotive-Compliant Part is Available Under Separate Datasheet (DMTH41M8SPSQ)**

## Mechanical Data

- Case: PowerDI<sup>®</sup> 5060-8
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.097 grams (Approximate)

PowerDI5060-8 (Type K)

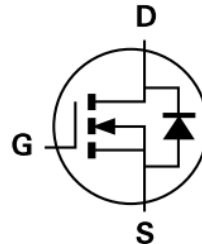


Top View

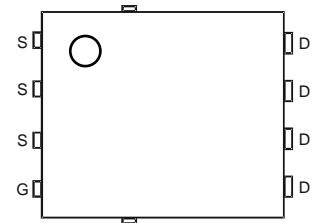


Pin1

Bottom View



Internal Schematic



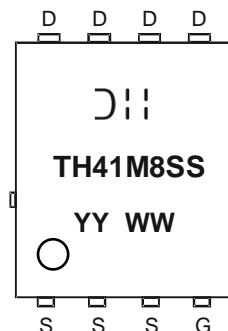
Top View  
Pin Configuration

## Ordering Information (Note 4)

Part Number	Case	Packaging
DMTH41M8SPS-13	PowerDI5060-8 (Type K)	2,500 / Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



- = Manufacturer's Marking  
 TH41M8SS = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Last Two Digits of Year (ex: 19 = 2019)  
 WW = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	40	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current, V <sub>GS</sub> = 10V (Notes 6 & 9)	I <sub>D</sub>	100 100	A
		T <sub>C</sub> = +25°C T <sub>C</sub> = +100°C	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	400	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)	I <sub>SM</sub>	400	A
Continuous Body Diode Forward Current (Note 7)	I <sub>S</sub>	100	A
		T <sub>C</sub> = +25°C	
Avalanche Current, L = 0.1mH	I <sub>AS</sub>	72.8	A
Avalanche Energy, L = 0.1mH	E <sub>AS</sub>	265	mJ

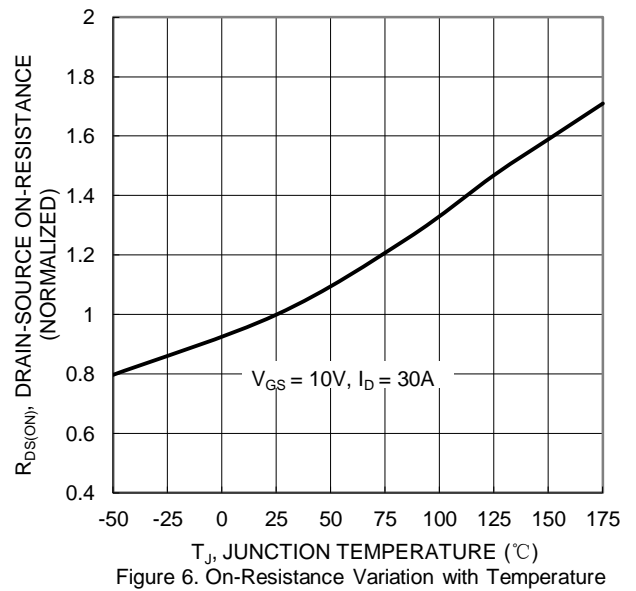
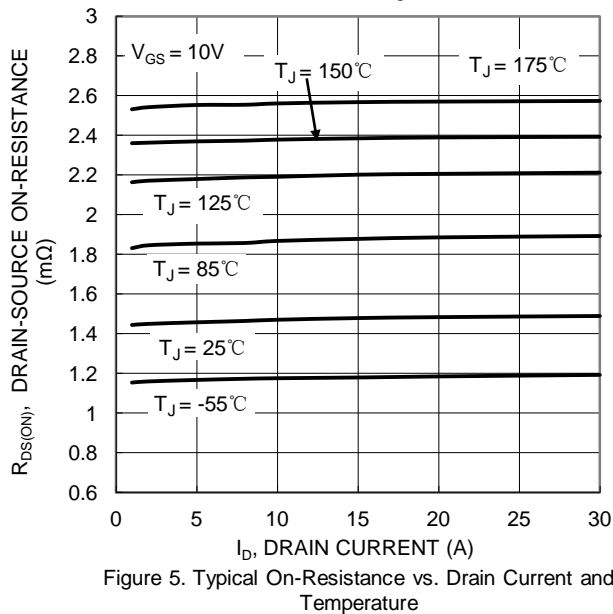
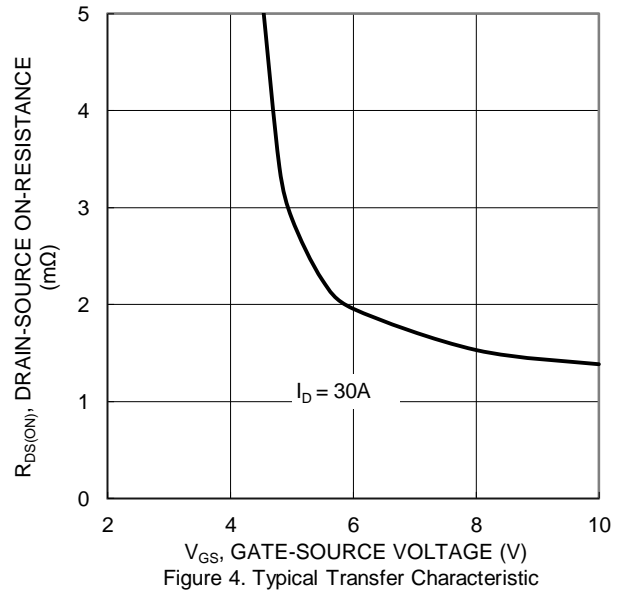
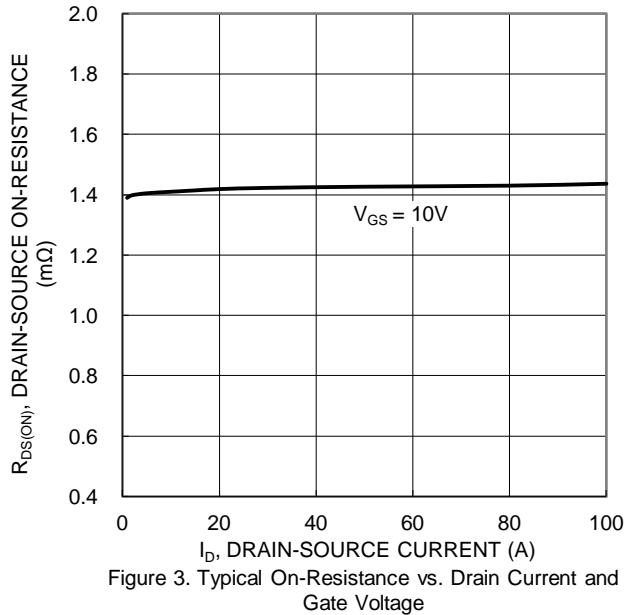
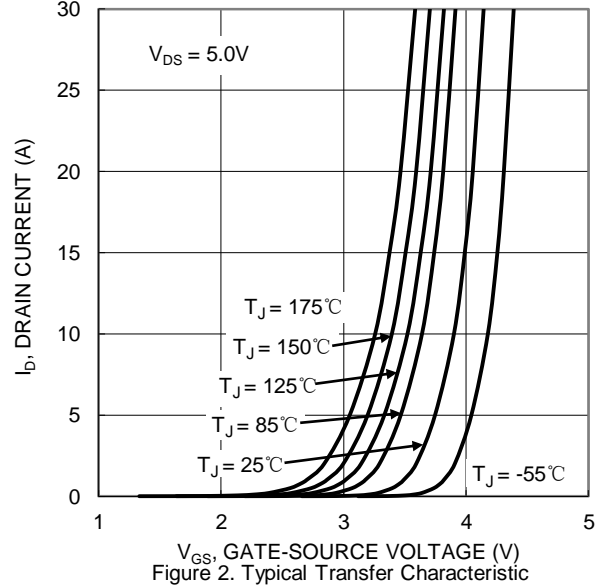
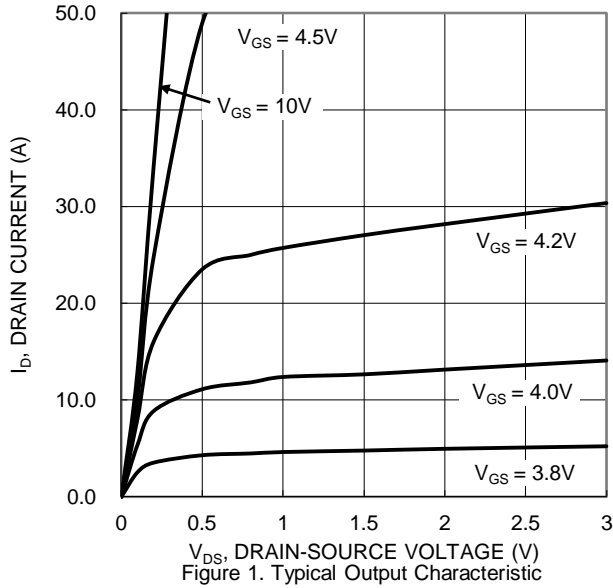
**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	3.03	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	49	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	150	W
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	1.0	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +175	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	40	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 32V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	2	—	4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	1.4	1.8	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 30A
Diode Forward Voltage	V <sub>SD</sub>	—	0.8	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 20A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>ISS</sub>	—	6968	—	pF	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1MHz
Output Capacitance	C <sub>OSS</sub>	—	1812	—		
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	59	—		
Gate Resistance	R <sub>G</sub>	—	1.21	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	—	79.5	—	nC	V <sub>DD</sub> = 20V, I <sub>D</sub> = 90A, V <sub>GS</sub> = 10V
Gate-Source Charge	Q <sub>gs</sub>	—	20.6	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	16.5	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	13.3	—	ns	V <sub>DD</sub> = 20V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 90A, R <sub>G</sub> = 3.5Ω
Turn-On Rise Time	t <sub>r</sub>	—	41.3	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	35.1	—		
Turn-Off Fall Time	t <sub>f</sub>	—	13.7	—		
Reverse Recovery Time	t <sub>RR</sub>	—	62	—	ns	I <sub>F</sub> = 50A, di/dt = 100A/µs
Reverse Recovery Charge	Q <sub>RR</sub>	—	103	—	nC	

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
  6. Thermal resistance from junction to soldering point (on the exposed drain pad).
  7. Short duration pulse test used to minimize self-heating effect.
  8. Guaranteed by design. Not subject to product testing.
  9. Limited by package.



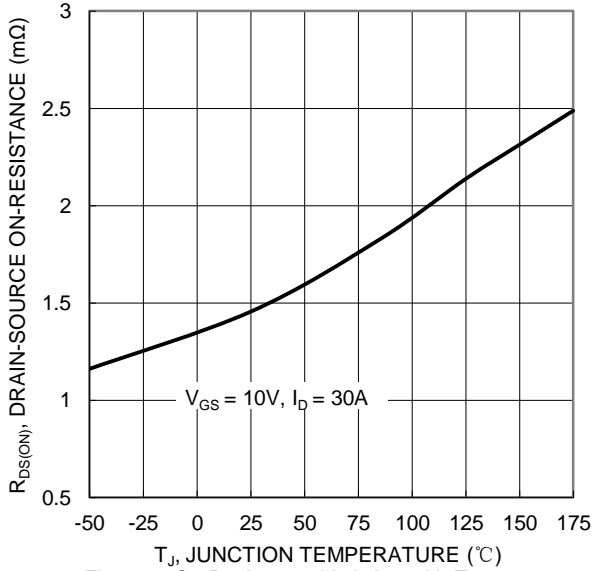


Figure 7. On-Resistance Variation with Temperature

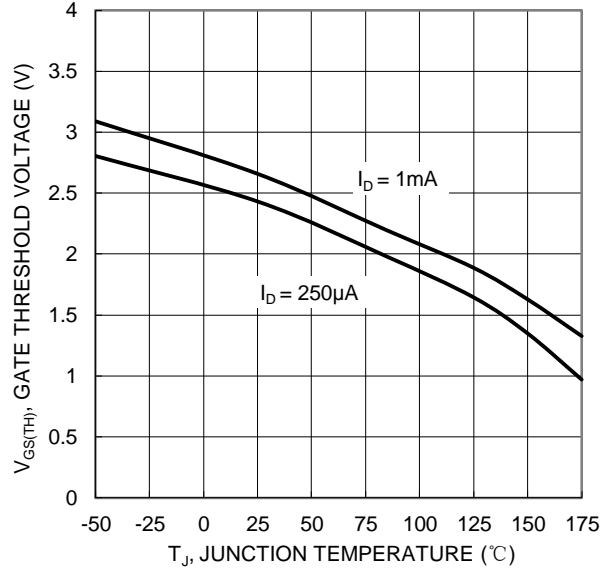


Figure 8. Gate Threshold Variation vs. Junction Temperature

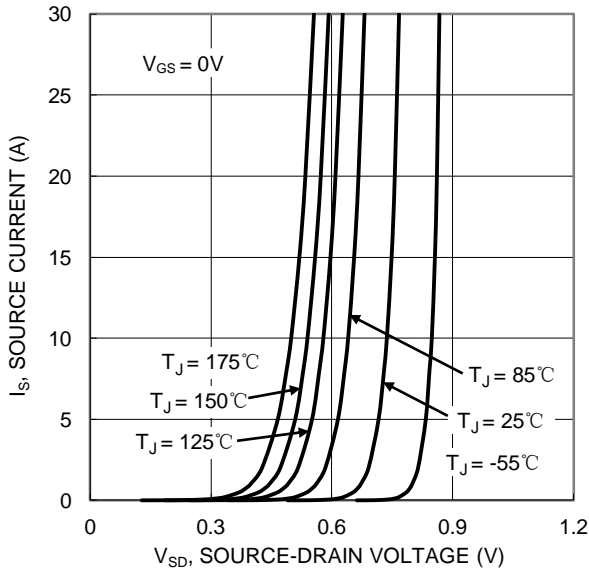


Figure 9. Diode Forward Voltage vs. Current

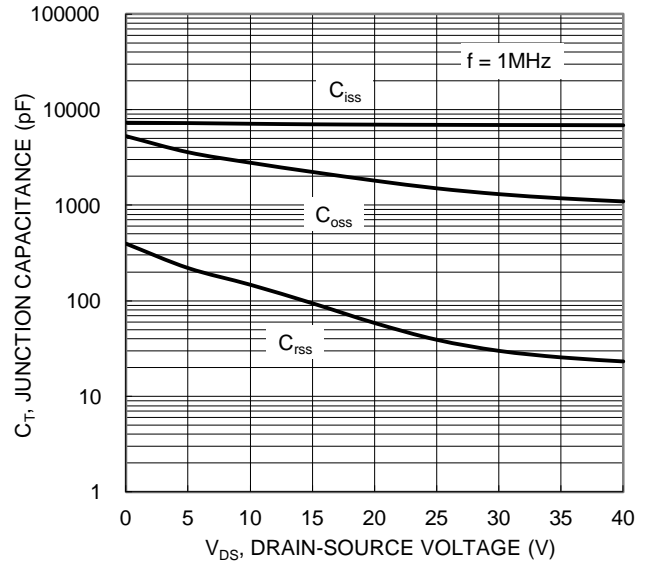


Figure 10. Typical Junction Capacitance

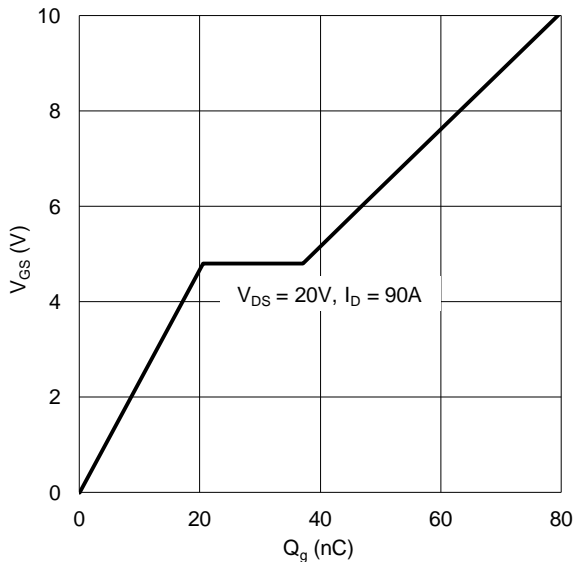


Figure 11. Gate Charge

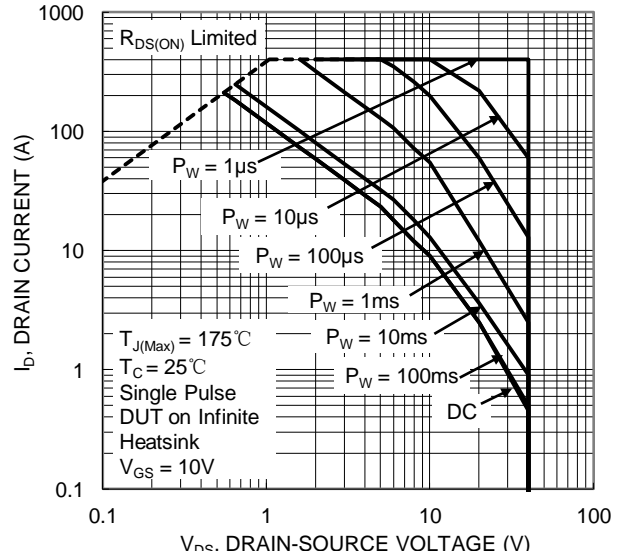


Figure 12. SOA, Safe Operation Area

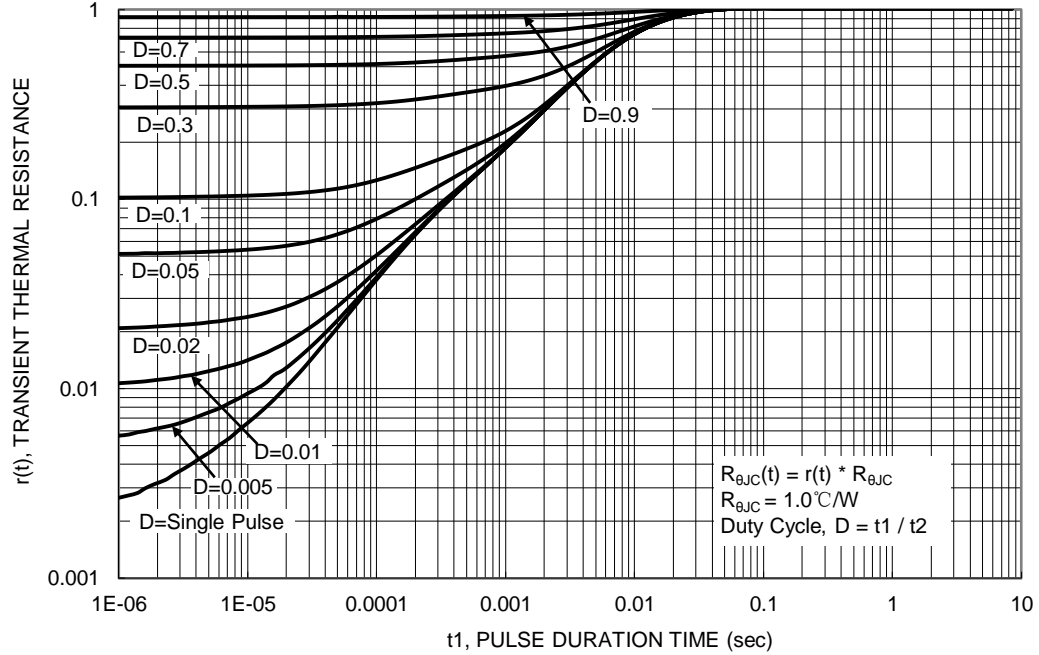
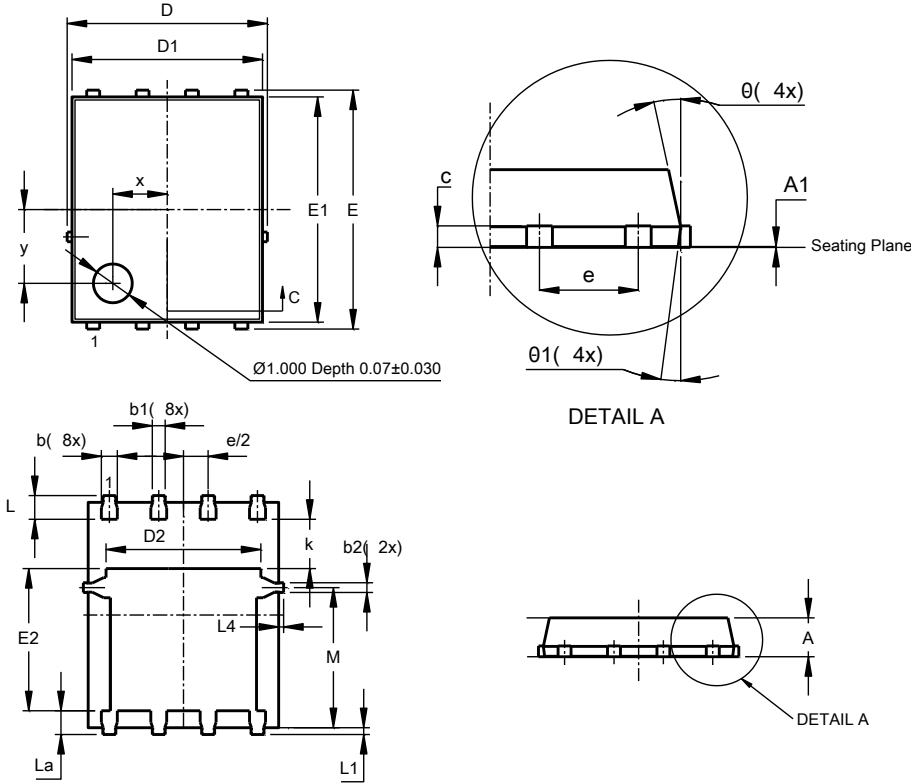


Figure 13. Transient Thermal Resistance

**Package Outline Dimensions**

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**PowerDI5060-8 (Type K)**

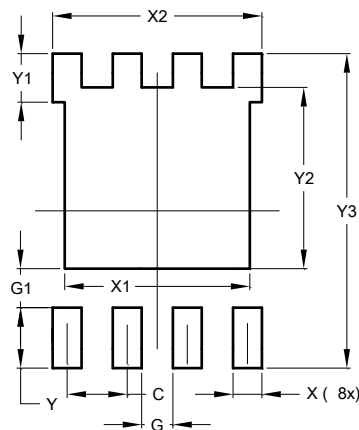


PowerDI5060-8 (Type K)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	0.02
b	0.33	0.51	0.41
b1	0.300	0.366	0.333
b2	0.20	0.35	0.25
c	0.23	0.33	0.277
D	5.15 BSC		
D1	4.85	4.95	4.90
D2	-	-	3.98
E	6.15 BSC		
E1	5.75	5.85	5.80
E2	3.56	3.725	3.66
e	1.27BSC		
k	-	-	1.27
L	0.51	0.71	0.61
La	0.51	0.675	0.61
L1	0.05	0.20	0.175
L4	-	-	0.125
M	3.50	3.71	3.605
x	-	-	1.400
y	-	-	1.900
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI5060-8 (Type K)**



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	3.910
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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