

Ultra Small PLL Clock Generator ICs with Built-In Divider/Multiplier Circuits

■ GENERAL DESCRIPTION

The XC25BS8 series is an ultra small PLL clock generator IC which can generate a high multiplier output up to 4095 from an input frequency as low as 8kHz. The series includes a divider circuit, phase/frequency comparator, charge pump, and VCO so it is possible to configure a fully operational circuit with a few external components like one low-pass filter capacitor. The Input divider ratio (M) can be selected from a range of 1 to 2047, the output divider ratio (N) can be selected from a range of 1 to 4095 and they are set internally by using laser timing technologies. Output frequency (f_{Q0}) is equal to input clock frequency (f_{CLKin}) multiplied by N/M. Output frequency range is 1MHz to 100MHz. Reference clock from 8kHz to 36MHz can be input as the input clock. The IC stops operation and current drain is suppressed when a low level signal is input to the CE pin which greatly reduces current consumption and produces a high impedance output.

The setting of the input divider ratio (M), output divider ratio (N), and charge pump current (I_p) are factory fixed semi-custom. Please advise your Torex sales representative of your particular input/output frequency and supply voltage specifications so that we can see if we will be able to support your requirements. The series is available in small SOT-26W and USP-6C.

■ APPLICATIONS

- Clock for controlling a Imaging dot (LCD)
- DSC (Digital still camera)
- DVC (Digital video camera)
- PND (Car navigation system)
- UMPC (Ultra Mobile Personal Computer)
- SSD (Solid State Disk)
- Digital Photo Frame
- Microcomputer and HDD drives
- Cordless phones & Wireless communication equipment
- Various system clocks

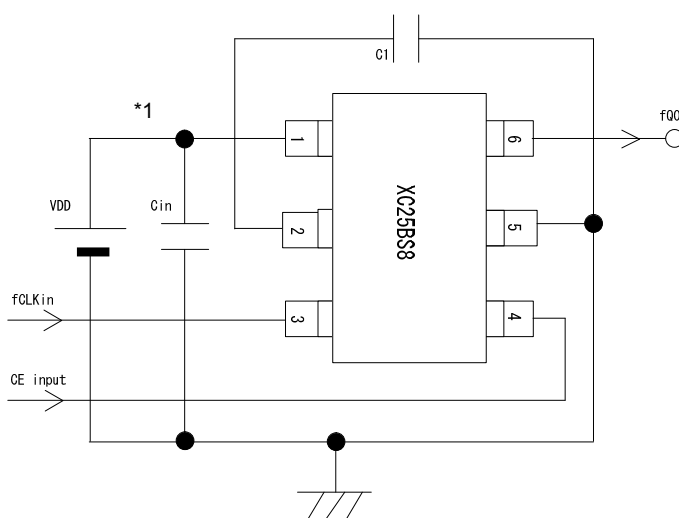
■ FEATURES

| | |
|--------------------------|--|
| Input Frequency Range | : 8kHz ~ 36MHz ^(*) |
| Output Frequency Range | : 1MHz ~ 100MHz |
| | (f _{Q0} =f _{CLKin} × N/M) ^(*) |
| Output Divider (N) Range | : 1 ~ 4095 ^(*) |
| Input Divider (M) Range | : 1 ~ 2047 ^(*) |
| Operating Voltage Range | : 2.50V ~ 5.50V ^(*) |
| Low Power Consumption | : 10 μA MAX. when stand-by ^(**) |
| Small Packages | : SOT-26W, USP-6C |

*1: The series are semi-custom products. Specifications for each product are limited within the above range. The input frequency range is set within ±5% of customer's designated typical frequency. Please note that setting of your some requirements may not be possible due to the specification limits of this series.

*2: When the IC is in stand-by mode, the output becomes high impedance and the IC stops operation.

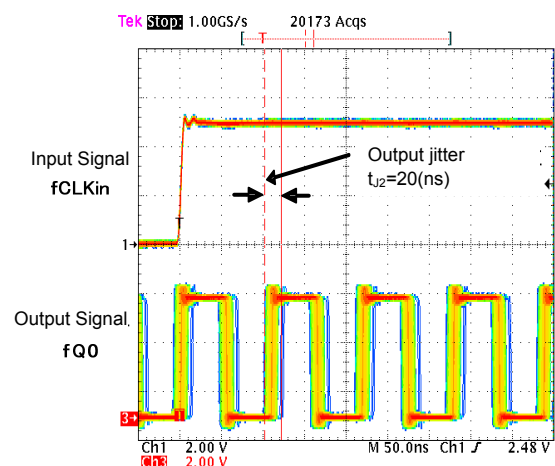
■ TYPICAL APPLICATION CIRCUIT



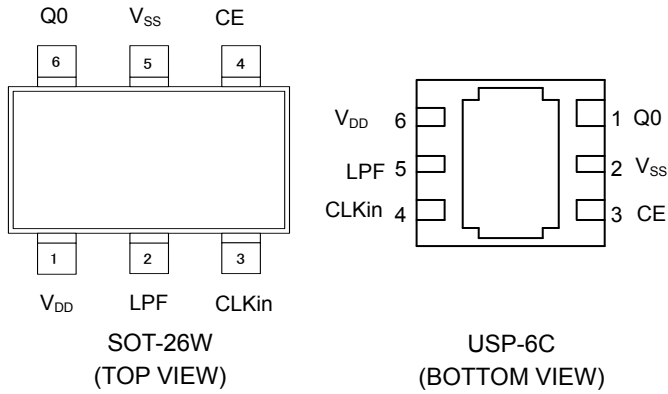
*1: C_{IN} (by-pass capacitor, 0.1 μF) and C1 (LPF capacitor, 0.1 μF) should be connected as close as possible to the IC. Please refer to the pattern reference layout schematics on page 8 for details.

■ TYPICAL PERFORMANCE CHARACTERISTICS

PLL Output signal jitter 2 (t_{j2}) (synchronous to an input signal)
XC25BS8001xx (610 multiplier, input 15kHz (TYP.))



PIN CONFIGURATION



* The dissipation pad (TAB) of the bottom view of the USP-6C package should be connected to the V_{SS} (No. 2) pin.

PIN ASSIGNMENT

| PIN NUMBER | | PIN NAME | FUNCTION |
|------------|--------|-----------------|---------------------------------------|
| SOT-26W | USP-6C | | |
| 6 | 1 | Q0 | Clock Output |
| 5 | 2 | V _{SS} | Ground |
| 4 | 3 | CE | Stand-by Control (*) |
| 3 | 4 | CLKin | Reference Clock Signal Input |
| 2 | 5 | LPF | Device connection for Low Pass Filter |
| 1 | 6 | V _{DD} | Power Input |

FUNCTION LIST

| | | |
|----|---------------|----------------|
| CE | 'H' | 'L' or OPEN |
| Q0 | Signal Output | High Impedance |

*H: High level input

L: Low level input (stand-by mode)

■ PRODUCT CLASSIFICATION

● Ordering Information

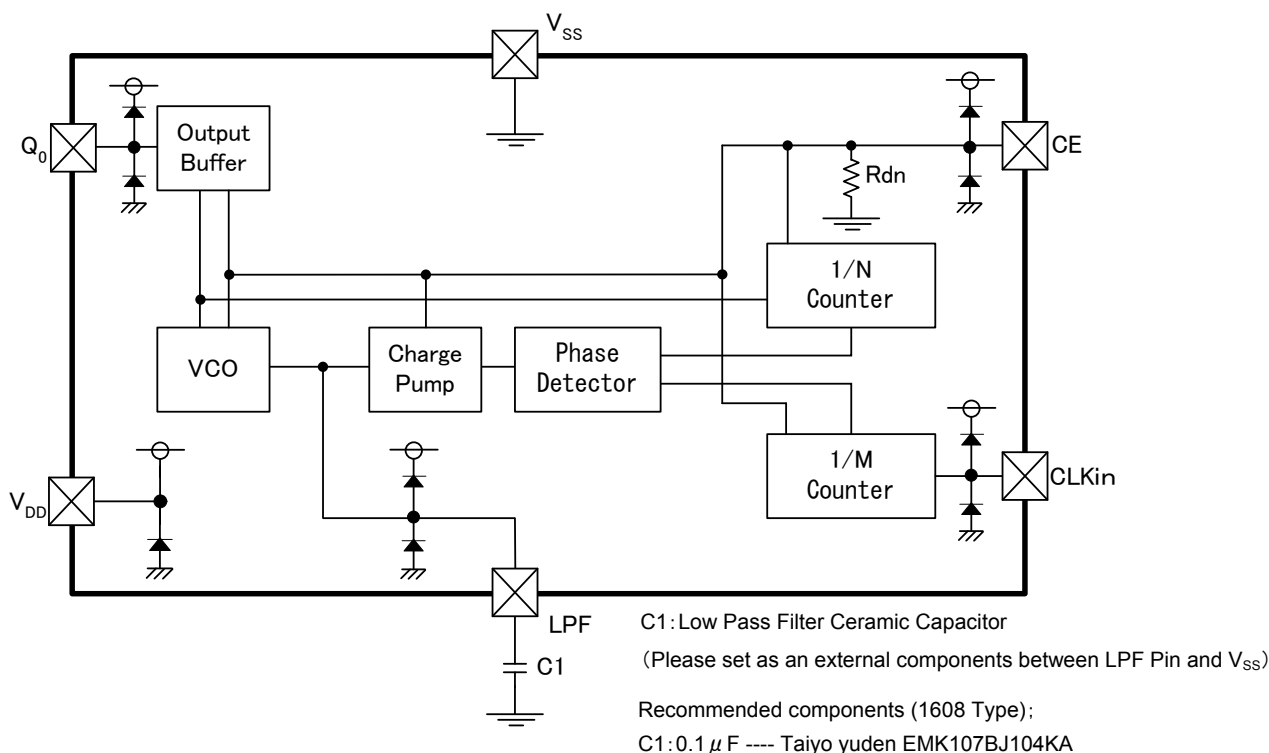
XC25BS8①②③④⑤-⑥ ^{(*)1}

| DESIGNATOR | DESCRIPTION | SYMBOL | DESCRIPTION |
|------------|--------------------------------------|--------|--|
| ①②③ | Product Number | 001~ | Serial number based on internal standards e.g. product number 001→①②③=001 |
| ④⑤-⑥ | Packages Taping Type ^{(*)2} | MR | SOT-26W |
| | | MR-G | SOT-26W (Halogen & Antimony free) |
| | | ER | USP-6C |
| | | ER-G | USP-6C (Halogen & Antimony free) |

^{(*)1} The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.

^{(*)2} The device orientation is fixed in its embossed tape pocket. For reverse orientation, please contact your local Torex sales office or representative. (Standard orientation: ④R-⑥, Reverse orientation: ④L-⑥)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

T_a=25°C

| PARAMETER | SYMBOL | RATINGS | UNITS |
|-----------------------------|------------------|---|-------|
| Supply Voltage | V _{DD} | V _{SS} - 0.3 ~ V _{SS} + 7.0 | V |
| CLKin Pin Input Voltage | V _{CK} | V _{SS} - 0.3 ~ V _{DD} + 0.3 | V |
| CE Pin Input Voltage | V _{CE} | V _{SS} - 0.3 ~ V _{DD} + 0.3 | V |
| Q0 Pin Output Voltage | V _{Q0} | V _{SS} - 0.3 ~ V _{DD} + 0.3 | V |
| Q0 Pin Output Current | I _{Q0} | ± 50 | mA |
| Power Dissipation | SOT-26W | 250 | mW |
| | USP-6C | 100 | mW |
| Operating Temperature Range | T _{opr} | -40 ~ +85 | °C |
| Storage Temperature Range | T _{stg} | -55 ~ +125 | °C |

SELECTION GUIDE

*1: The table below introduces standard products. Please select with seeing the combination of input frequencies and multiplications.
The test condition: $V_{DD}=3.3V\pm 10\%$

*2: For other input frequency and multiplication, please ask your Torex sales contacts.

| Multiplication | Input Frequency | | | Synchronization jitter | Synchronization jitter / Output Period (%) | Product Series |
|----------------|-----------------|---|--------|------------------------|--|----------------|
| | MIN | ~ | MAX | | | |
| 64 | 32kHz | ~ | 192kHz | 36ns | 10% | XC25BS8044 |
| 128 | 32kHz | ~ | 192kHz | 32ns | 18% | XC25BS8027 |
| | 32kHz | ~ | 96kHz | 24ns | 14% | XC25BS8028 |
| | 32kHz | ~ | 48kHz | 20ns | 11% | XC25BS8057 |
| 192 | 32kHz | ~ | 192kHz | 30ns | 25% | XC25BS8030 |
| | 32kHz | ~ | 96kHz | 20ns | 17% | XC25BS8031 |
| | 32kHz | ~ | 48kHz | 16ns | 14% | XC25BS8058 |
| 256 | 32kHz | ~ | 192kHz | 24ns | 27% | XC25BS8033 |
| | 32kHz | ~ | 96kHz | 22ns | 25% | XC25BS8026 |
| | 32kHz | ~ | 48kHz | 18ns | 20% | XC25BS8025 |
| 384 | 32kHz | ~ | 192kHz | 21ns | 36% | XC25BS8035 |
| | 32kHz | ~ | 96kHz | 20ns | 34% | XC25BS8036 |
| | 32kHz | ~ | 48kHz | 18ns | 30% | XC25BS8037 |
| 512 | 32kHz | ~ | 96kHz | 18ns | 41% | XC25BS8039 |
| | 32kHz | ~ | 48kHz | 16ns | 36% | XC25BS8040 |
| 768 | 32kHz | ~ | 96kHz | 16ns | 54% | XC25BS8042 |
| | 32kHz | ~ | 48kHz | 14ns | 47% | XC25BS8043 |

* Synchronization jitters are tested at $f_{CLKIN}=44.1kHz$.

| Multiplication | Input Frequency | | | Amount of Jitter Synchronization | Amount of Jitter Synchronization / Output Period (%) | Product Series |
|----------------|-----------------|---|-------|----------------------------------|--|----------------|
| | MIN | ~ | MAX | | | |
| 64 | 8kHz | ~ | 16kHz | 160ns | 8% | XC25BS8045 |
| 128 | 8kHz | ~ | 16kHz | 140ns | 14% | XC25BS8029 |
| 192 | 8kHz | ~ | 16kHz | 110ns | 17% | XC25BS8032 |
| 256 | 8kHz | ~ | 16kHz | 100ns | 20% | XC25BS8034 |
| 384 | 8kHz | ~ | 16kHz | 96ns | 29% | XC25BS8038 |
| 512 | 8kHz | ~ | 16kHz | 52ns | 21% | XC25BS8041 |
| 768 | 8kHz | ~ | 16kHz | 48ns | 29% | XC25BS8046 |

* Synchronization jitters are tested at $f_{CLKIN}=8kHz$.

| Multiplication | Input Frequency | | | Amount of Jitter Synchronization | Amount of Jitter Synchronization / Output Period (%) | Product Series |
|----------------|-----------------|---|-------|----------------------------------|--|----------------|
| | MIN | ~ | MAX | | | |
| 1 | 8MHz | ~ | 74MHz | 7ns | 8% | XC25BS8047 |
| 2 | 6MHz | ~ | 37MHz | 6ns | 11% | XC25BS8048 |
| 3 | 2MHz | ~ | 24MHz | 12ns | 11% | XC25BS8049 |
| 4 | 2MHz | ~ | 18MHz | 7ns | 8% | XC25BS8050 |
| 5 | 2MHz | ~ | 14MHz | 8ns | 12% | XC25BS8051 |
| 6 | 2MHz | ~ | 12MHz | 7ns | 13% | XC25BS8052 |
| 7 | 2MHz | ~ | 10MHz | 7ns | 15% | XC25BS8053 |
| 8 | 2MHz | ~ | 9MHz | 6ns | 14% | XC25BS8054 |
| 9 | 2MHz | ~ | 8MHz | 6ns | 16% | XC25BS8055 |
| 10 | 2MHz | ~ | 7MHz | 7ns | 21% | XC25BS8056 |

* Synchronization jitters are tested in the condition below.

For the XC258047 (1 Multiplication), $f_{CLKIN}=12MHz$. For the XC258048(2 Multiplication), $f_{CLKIN}=8MHz$

Except above, $f_{CLKIN}=3MHz$ is used.

■ ELECTRICAL CHARACTERISTICS

- Recommended Operating Conditions: XC25BS8050xx (4 multiplication, Input 3MHz (TYP.)) 3.3V (TYP.)

Tested below Ta=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | MAX. | UNITS |
|--|--------------------|--|-------|--------|-------|
| Supply Voltage 3.3V | V _{DD} | 3.3V (TYP.) operation | 2.97 | 3.63 | V |
| Input Frequency | f _{CLKin} | (^{*1}) | 2.000 | 18.500 | MHz |
| Multiplier Ratio | N/M | Typical value is shown (^{*1}) | 4 | | - |
| Output Frequency | f _{Q0} | (^{*1}) | 8.000 | 74.000 | MHz |
| Load Capacity (^{*3}) | CL | | - | 15 | pF |
| Output Start Time (^{*2})(^{*3}) | t _{START} | f _{CLKin} =2.000MHz | 0.05 | 20 | ms |

NOTE:

*1: The values are measured when a capacitor C_{IN}=0.1 μF is connected between V_{DD} and V_{SS} pins, a capacitor C1=0.1 μF is connected between LFP and V_{SS} pins

*2: It is a time to get stable output signal from Q0 pin after the CE pin is turned on while applying supply voltage to the V_{DD} pin and applying the input signal to the CLKin pin.

*3: Values indicated are design values which are not guaranteed 100%.

- DC Characteristics: XC25BS8050xx (4 multiplication, Input 3MHz (TYP.)) 3.3V (TYP.)

Ta=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---------------------------|------------------|---|------|------|------|-------|---------|
| H Level Input Voltage | V _{IH} | | 2.70 | - | - | V | ① |
| L Level Input Voltage | V _{IL} | | - | - | 0.60 | V | ① |
| H Level Input Current | I _{IH} | V _{CLKin} =V _{DD} -0.3V | - | - | 3.0 | μA | ② |
| L Level Input Current | I _{IL} | V _{CLKin} =0.3V | -3.0 | - | - | μA | ② |
| H Level Output Voltage | V _{OH} | V _{DD} =2.97V, I _{OH} =-4mA | 2.38 | - | - | V | ③ |
| L Level Output Voltage | V _{OL} | V _{DD} =2.97V, I _{OL} =4mA | - | - | 0.45 | V | ③ |
| Supply Current 1 | I _{DD1} | V _{DD} =3.63V, CE=3.63V | - | 5.0 | 10.0 | mA | ④ |
| Supply Current 2 | I _{DD2} | V _{DD} =3.63V, CE=0.0V | - | - | 10 | μA | ④ |
| CE H Level Voltage | V _{CEH} | | 2.70 | - | - | V | ① |
| CE L Level Voltage | V _{CEL} | | - | - | 0.45 | V | ① |
| CE Pull-Down Resistance 1 | R _{dn1} | CE=V _{DD} | 0.1 | 0.6 | 1.2 | MΩ | ⑤ |
| CE Pull-Down Resistance 2 | R _{dn2} | CE=0.1*V _{DD} | 5 | 30 | 60 | kΩ | ⑤ |
| Output Off Leak Current | I _{OZ} | V _{DD} =3.63V, CE=0.0V | - | - | 10 | μA | ⑥ |

NOTE:

TEST CONDITION: V_{DD}=3.0V, f_{CLKin}=3MHz, C1=0.1 μF, Multiplier ratio=4, No load

- AC Characteristics: XC25BS8050xx (4 multiplication, 3MHz(TYP.)) 3.3V (TYP.)

Ta=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|--|-----------------|--------------------------------|------|------|------|-------|---------|
| Output Rise Time (^{*1}) | t _R | (20% ~ 80%) | - | 4.0 | 8.0 | ns | ① |
| Output Fall Time (^{*1}) | t _F | (20% ~ 80%) | - | 4.0 | 8.0 | ns | ① |
| Output Signal Duty Cycle (^{*1}) | Duty | | 45 | 50 | 55 | % | ① |
| PLL Output Signal Jitter 1 (^{*1}) | t _{J1} | 1σ (Output Period) | - | 45 | - | ps | ① |
| PLL Output Signal Jitter 2 (^{*1}) | t _{J2} | Peak to Peak (Output Tracking) | - | 8.0 | - | ns | ① |

NOTE:

TEST CONDITION: V_{DD}=3.3V, f_{CLKin}=3MHz, C1=0.1 μF, Multiplier ratio=4, C_L=15pF

*1: Values indicated are design values, which are not guaranteed 100%.

■ ELECTRICAL CHARACTERISTICS (Continued)

● Recommended Operating Conditions: XC25BS8025xx (256 multiplication, Input 44.1kHz (TYP.)) 5.0V (TYP.)

Tested below Ta=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | MAX. | UNITS |
|--|--------------------|--|--------|--------|-------|
| Supply Voltage 5.0V | V _{DD} | 5.0V (TYP.) operation | 4.50 | 5.50 | V |
| Input Frequency | f _{CLKin} | (^{*1}) | 32.000 | 48.000 | kHz |
| Multiplier Ratio | N/M | Typical value is shown (^{*1}) | 256 | | |
| Output Frequency | f _{Q0} | (^{*1}) | 8.693 | 96.075 | MHz |
| Load Capacity (^{*3}) | CL | | - | 15 | pF |
| Output Start Time (^{*2})(^{*3}) | t _{START} | f _{CLKin} =32.000kHz | 0.05 | 20 | ms |

NOTE:

*1: The values are measured when a capacitor C_{IN}=0.1 μF is connected between V_{DD} and V_{SS} pins, a capacitor C1=0.1 μF is connected between LFP and V_{SS} pins.

*2: It is a time to get stable output signal from Q0 pin after the CE pin is turned on while applying supply voltage to the V_{DD} pin and applying the input signal to the CLKin pin.

*3: Values indicated are design values which are not guaranteed 100%.

● DC Characteristics: XC25BS8025xx (256 multiplication, Input 44.1kHz (TYP.)) 5.0V (TYP.)

Ta=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---------------------------|------------------|---|------|------|------|-------|---------|
| H Level Input Voltage | V _{IH} | | 4.00 | - | - | V | ① |
| L Level Input Voltage | V _{IL} | | - | - | 1.00 | V | ① |
| H Level Input Current | I _{IH} | V _{CLKin} =V _{DD} -0.5V | - | - | 5.0 | μA | ② |
| L Level Input Current | I _{IL} | V _{CLKin} =0.5V | -5.0 | - | - | μA | ② |
| H Level Output Voltage | V _{OH} | V _{DD} =4.50V, IOH=-8mA | 3.60 | - | - | V | ③ |
| L Level Output Voltage | V _{OL} | V _{DD} =4.50V, IOL=8mA | - | - | 0.65 | V | ③ |
| Supply Current 1 | I _{DD1} | V _{DD} =5.50V, CE=5.50V | - | 6.5 | 13.0 | mA | ④ |
| Supply Current 2 | I _{DD2} | V _{DD} =5.50V, CE=0.0V | - | - | 20 | μA | ④ |
| CE H Level Voltage | V _{CEH} | | 4.00 | - | - | V | ① |
| CE L Level Voltage | V _{CEL} | | - | - | 1.00 | V | ① |
| CE Pull-Down Resistance 1 | R _{dn1} | CE=V _{DD} | 0.1 | 0.4 | 0.8 | MΩ | ⑤ |
| CE Pull-Down Resistance 2 | R _{dn2} | CE=0.1*V _{DD} | 2 | 20 | 40 | kΩ | ⑤ |
| Output Off Leak Current | I _{oz} | V _{DD} =5.50V, CE=0.0V | - | - | 10 | μA | ⑥ |

NOTE:

TEST CONDITION: V_{DD}=5.0V, f_{CLKin}=44.1kHz, C1=0.1 μF, Multiplier ratio=256, No load

● AC Characteristics: XC25BS8025xx (256 multiplication, Input 44.1kHz (TYP.)) 5.0V (TYP.)

Ta=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|--|-----------------|--------------------------------|------|------|------|-------|---------|
| Output Rise Time (^{*1}) | t _R | (20% ~ 80%) | - | 2.5 | 5.0 | ns | ① |
| Output Fall Time (^{*1}) | t _F | (20% ~ 80%) | - | 2.5 | 5.0 | ns | ① |
| Output Signal Duty Cycle (^{*1}) | Duty | | 45 | 50 | 55 | % | ① |
| PLL Output Signal Jitter 1 (^{*1}) | t _{J1} | 1σ (Output Period) | - | 20 | - | ps | ① |
| PLL Output Signal Jitter 2 (^{*1}) | t _{J2} | Peak to Peak (Output Tracking) | - | 18.0 | - | ns | ① |

NOTE:

TEST CONDITION: V_{DD}=5.0V, f_{CLKin}=44.1kHz, C1=0.1 μF, Multiplier ratio=256, C_L=15pF

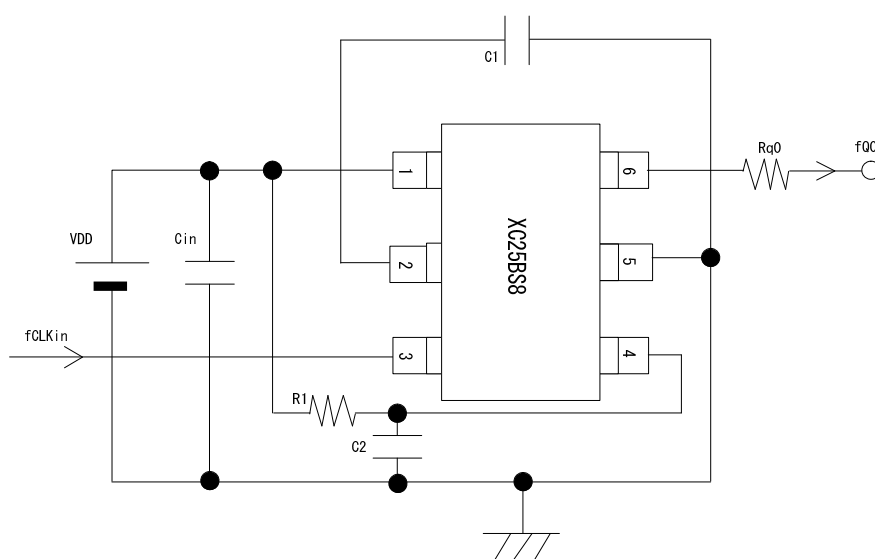
*1: Values indicated are design values, which are not guaranteed 100%.

■ NOTE ON USE

- (1) Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
- (2) The series is an analog IC. Please use a $0.01 \mu\text{F}$ to $0.1 \mu\text{F}$ of a by-pass capacitor.
- (3) The constant of the LPF element of this IC is preset. Always use the capacitance value ($=0.1 \mu\text{F}$) specified by us for the external ceramic capacitor (C1) for LPF. Operating this IC with a capacitor of the wrong capacitance will cause erroneous operation.
- (4) Rq0 shown in the Typical Application Circuit is a matching resistor. The use is recommended in order to counter unwanted radiations.
- (5) Please place the by-pass capacitor and the matching resistor as close to the IC as possible. The IC may not operate normally if the by-pass capacitor is not close enough to the IC. Further, the unwanted radiation may occur between the resistor and the IC pin if the matching resistor is not close enough to the IC.
- (6) When the CE pin is not controlled by external signals, it is recommended that a time constant circuit of $R1=1\text{k}\Omega \times C2 = 0.1 \mu\text{F}$ be added for stability.
- (7) With this IC, output is achieved by dividing and multiplying the reference oscillation by means of the PLL circuit. In cases where this output is further used as a reference oscillation of another PLL circuit, it may be that the final output signal's jitter increases; therefore, all necessary precautions should be taken to avoid this.
- (8) It is recommended that a low noise power supply, such as a series regulator, be used as the series' supply voltage. Using a power supply such as a switching regulator may enlarge the jitter, which in turn may lead to abnormal operation. Please confirm its operation with the actual device.
- (9) For operating the IC normally, please take procedures below when applying voltage to the series' input pin:
 - 1) Apply power source while the CE pin is "L" level with no clock input (high-Impedance or "L"),
 - 2) Input the clock,
 - 3) At least $100 \mu\text{s}$ after applying clock input, change the CE pin into "H" level and then to enable.

The IC has to be started by inputting the clock once the power rises completely. The CE pin, then, should be enabling. If the CE pin becomes enable and the clock is inputted before the power rises completely, an internal reset circuit does not operate normally which may cause to generate extraneous frequency.

●eg.) Matching Resistance (Rq0) and Device for Time constant circuit (R1,C2) are connected,
(Package: SOT-26W)



NOTE ON USE (Continued)

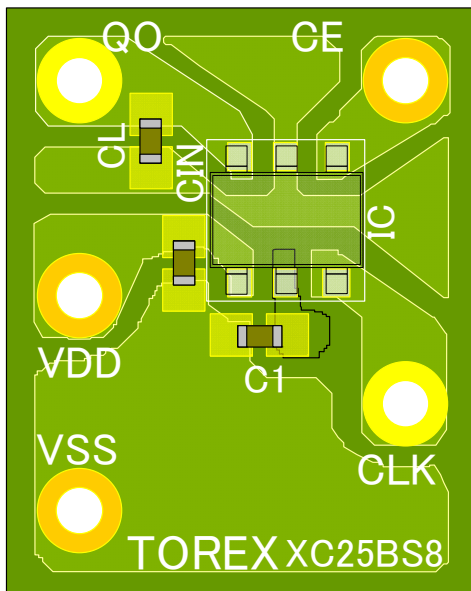
● Instructions on Pattern Layout

1. In order to stabilize V_{DD} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{DD} and V_{SS} pins.
2. Please mount the low pass filter capacitor $C1(=0.1\mu F)$ as close to the IC as possible.
3. Make the pattern as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
4. Make sure that the V_{SS} (GND) traces are as thick as possible, as variations in ground potential caused by noise may result in instability of this product.

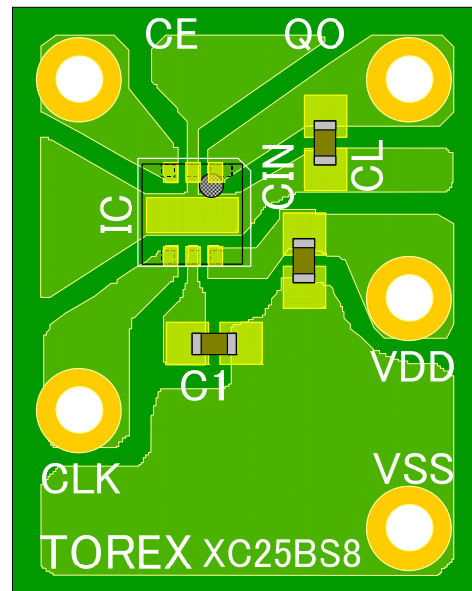
< Reference pattern layout >

* We prepare the evaluation board PCB, which is designed by the below layout pattern.

1. SOT-26W Reference Pattern Layout



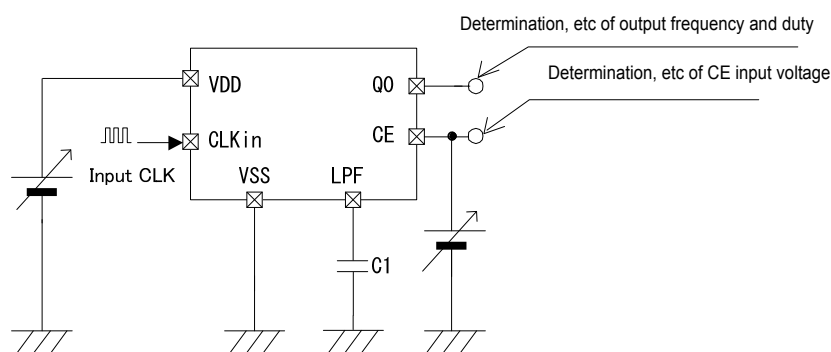
2. USP-6C Reference Pattern Layout



■ TEST CIRCUIT

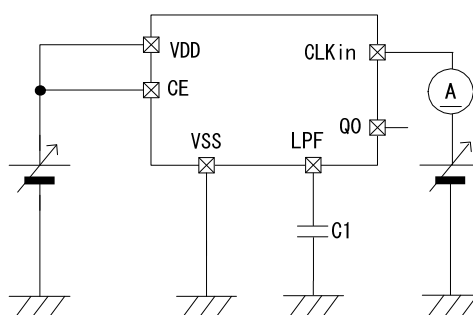
① Operating Supply Voltage

- H Level Input Voltage
- L Level Input Voltage
- CE "H" Level Voltage
- CE "L" Level Voltage
- Output Rise Time
- Output Fall Time
- Output Signal Duty
- PLL Output Signal Jitter 1
- PLL Output Signal Jitter 2



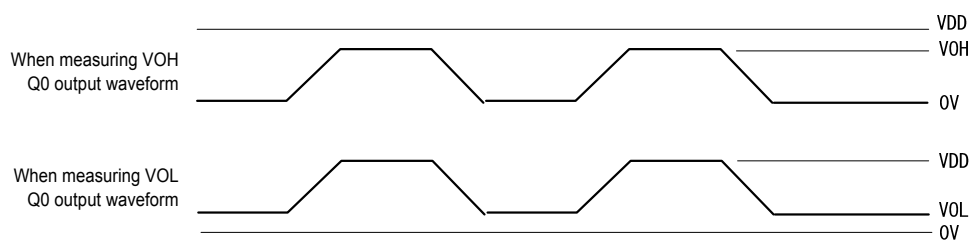
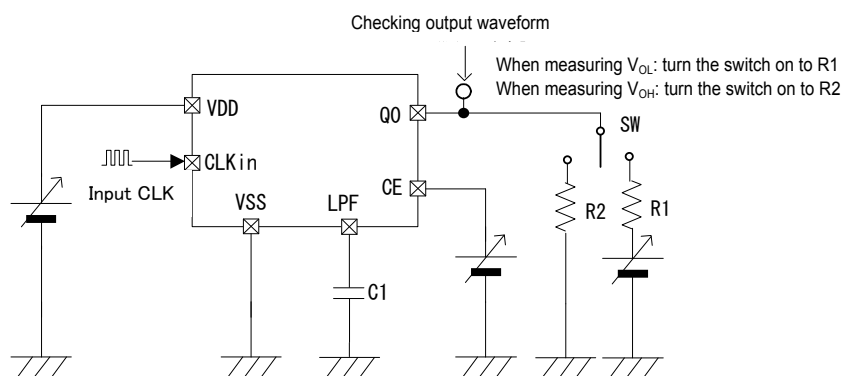
② H Level Input Current

- L Level Input Current



③ H Level Output Voltage

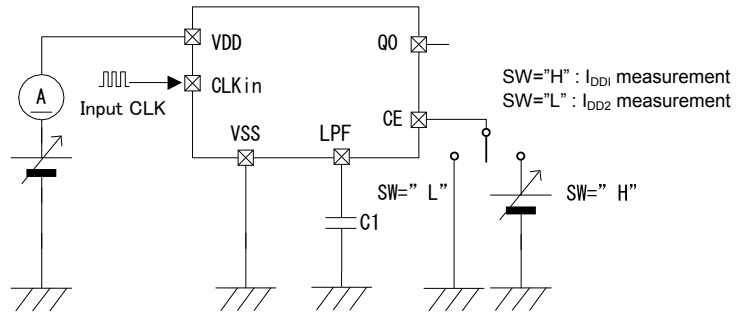
- L Level Output Voltage



TEST CIRCUIT (Continued)

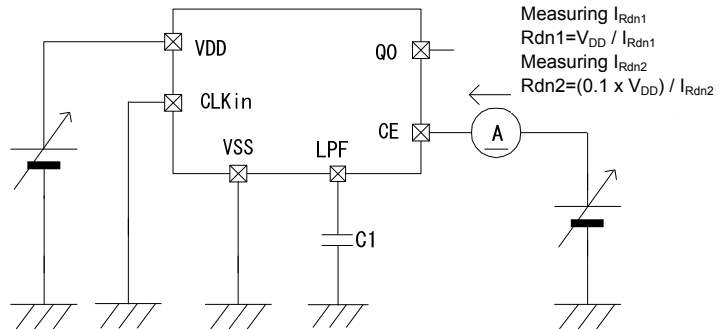
④ Supply Current 1

Supply Current 2

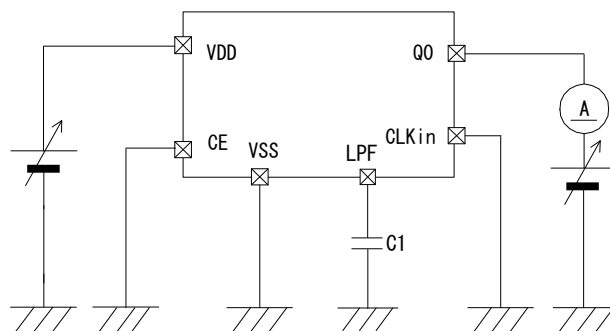


⑤ CE Pull-Down Resistance 1

CE Pull-Down Resistance 2

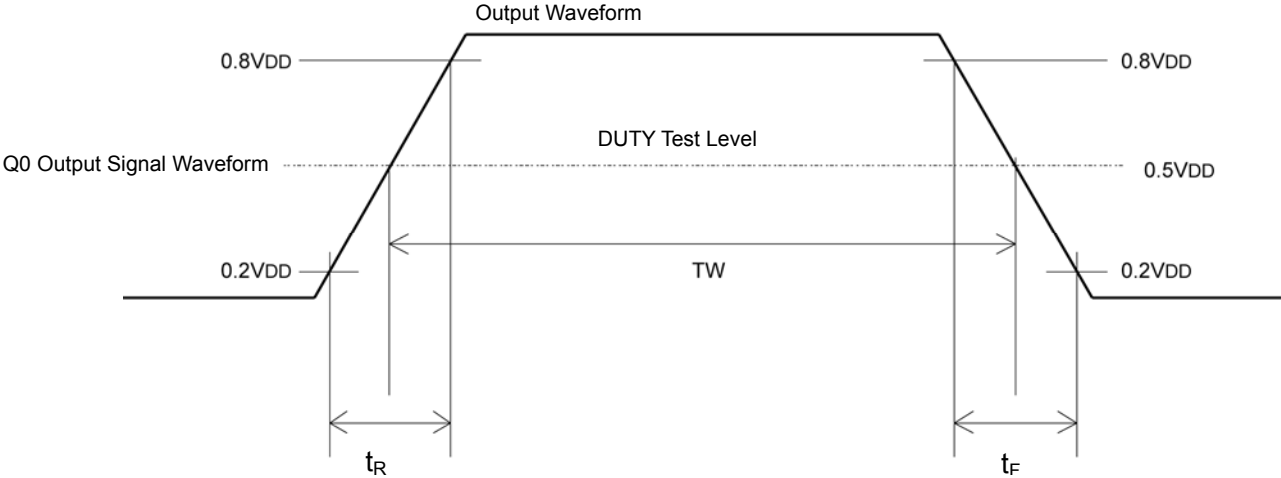


⑥ Output Off Leak Current

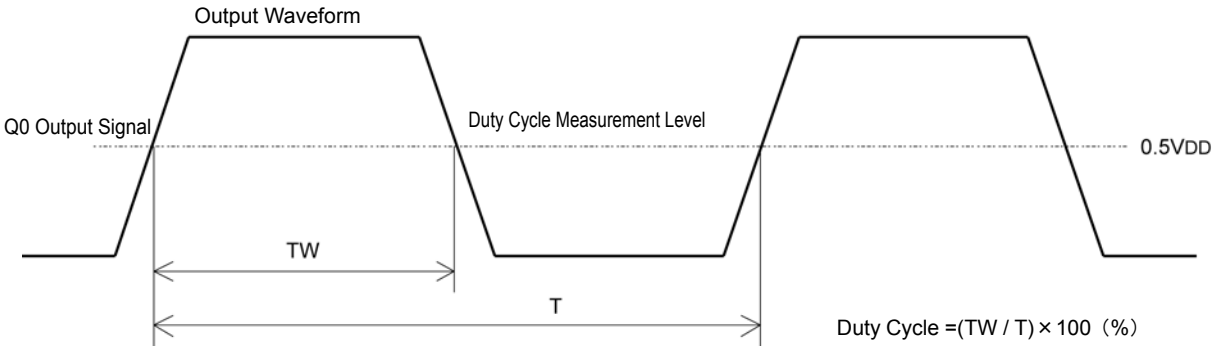


AC CHARACTERISTICS TEST WAVEFORM

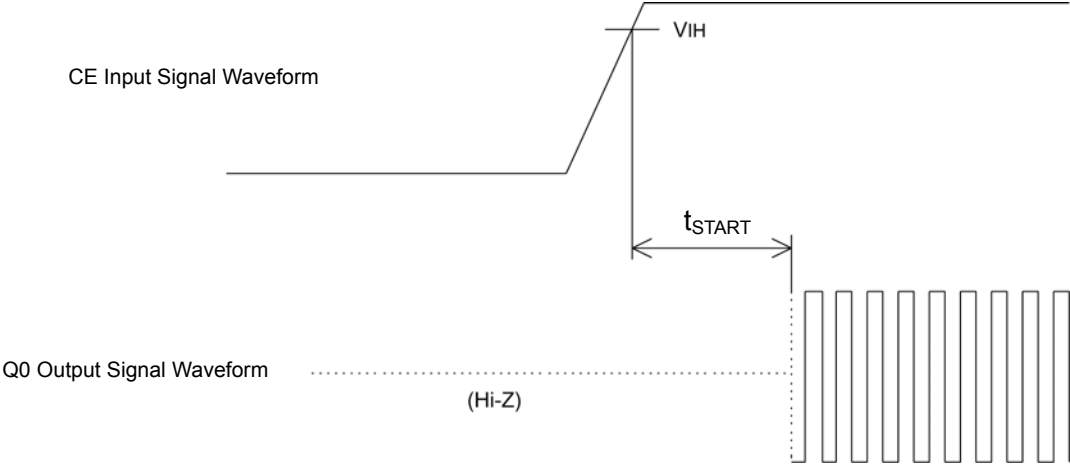
1) Output Rise Time, Output Fall Time



2) Duty Cycle



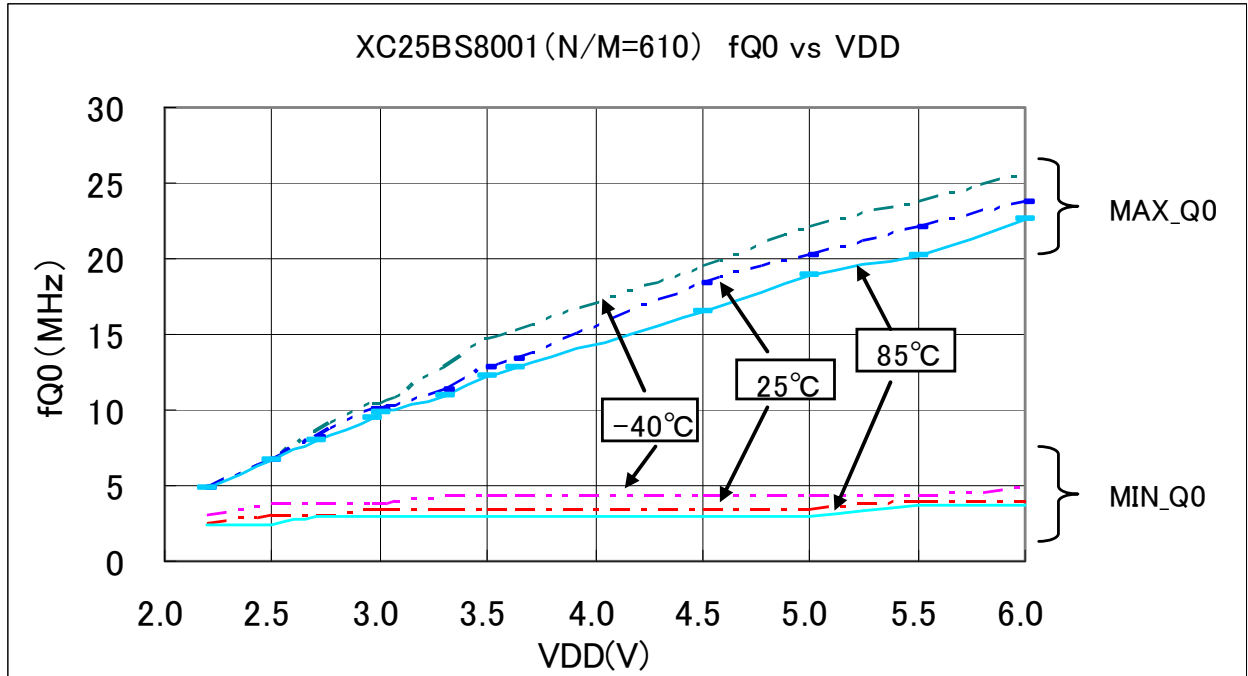
3) Output Start Time



■ TYPICAL PERFORMANCE CHARACTERISTICS

● Synchronous Output Frequency vs. Supply Voltage

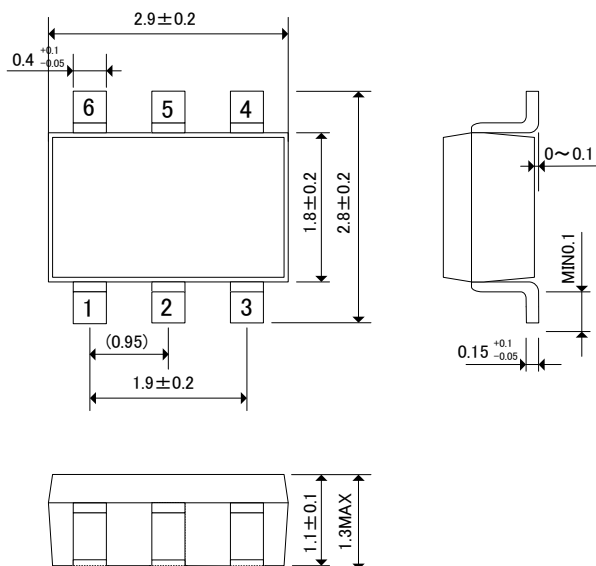
XC25BS8001xx (610 multiplication, Input 15kHz(TYP.))



PACKAGE INFORMATION

●SOT-26W

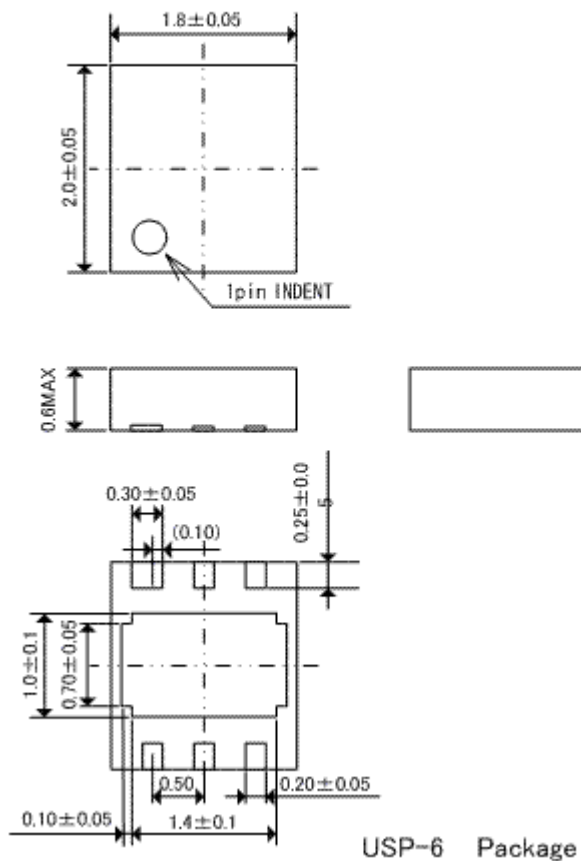
(unit : mm)



SOT-26W Package

●USP-6C

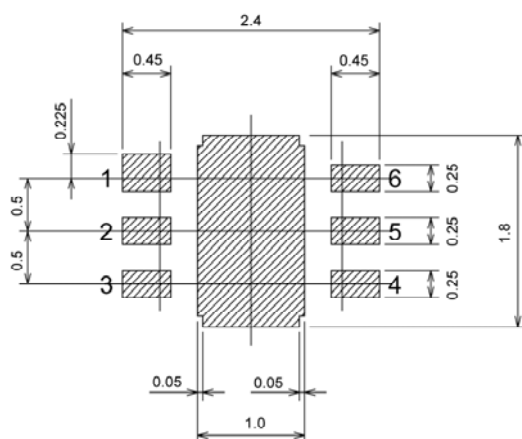
(unit : mm)



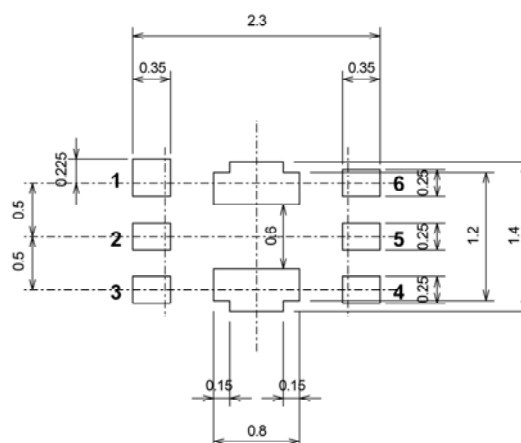
USP-6 Package

* No. 1 pin is wider than the other pins.
Soldering fillet surface is not formed because the sides of the pins are not plated.

●USP-6C Reference Pattern Layout



●USP-6C Reference Metal Mask Design



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