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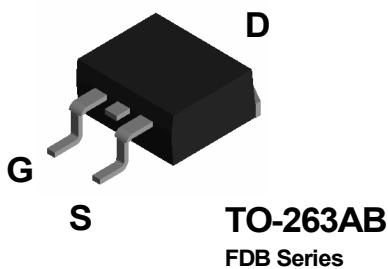
# FDB8447L

## 40V N-Channel PowerTrench® MOSFET

### 40V, 50A, 8.5mΩ

#### Features

- Max  $r_{DS(on)}$  = 8.5mΩ at  $V_{GS} = 10V$ ,  $I_D = 14A$
- Max  $r_{DS(on)}$  = 11mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 11A$
- Fast Switching
- RoHS Compliant

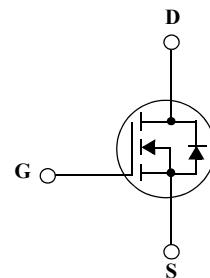


#### General Description

This N-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench® technology to deliver low  $r_{DS(on)}$  and optimized  $BV_{DSS}$  capability to offer superior performance benefit in the application.

#### Application

- Inverter
- Power Supplies



#### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ C$	50	A
	-Continuous (Silicon limited) $T_C = 25^\circ C$ (Note 1)	66	
	-Continuous $T_A = 25^\circ C$ (Note 1a)	15	
	-Pulsed	100	
$E_{AS}$	Drain-Source Avalanche Energy (Note 3)	153	mJ
$P_D$	Power Dissipation $T_C = 25^\circ C$	60	W
	Power Dissipation (Note 1a)	3.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB8447L	FDB8447L	TO-263AB	330mm	24mm	800 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		35		$\text{mV/}^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

**On Characteristics (Note 2)**

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-5		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 14\text{A}$		7.4	8.5	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 11\text{A}$		8.7	11.0	
		$V_{GS} = 10\text{V}, I_D = 14\text{A}, T_J = 125^\circ\text{C}$		10.8	12.4	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 14\text{A}$		58		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1970	2620	pF
$C_{oss}$	Output Capacitance			250	335	pF
$C_{rss}$	Reverse Transfer Capacitance			150	225	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		1.0		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}, I_D = 14\text{A}$ $V_{GS} = 10\text{V}, R_{\text{GEN}} = 6\Omega$		11	20	ns
$t_r$	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			28	45	ns
$t_f$	Fall Time			4	10	ns
$Q_{g(\text{TOT})}$	Total Gate Charge, $V_{GS} = 10\text{V}$	$V_{DD} = 20\text{V}, I_D = 14\text{A}$ $V_{GS} = 10\text{V}$		37	52	nC
$Q_{g(\text{TOT})}$	Total Gate Charge, $V_{GS} = 5\text{V}$			20	28	nC
$Q_{gs}$	Gate to Source Gate Charge			6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 14\text{A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 14\text{A}, di/dt = 100\text{A}/\mu\text{s}$		28	42	ns
$Q_{rr}$	Reverse Recovery Charge				24	36

**Notes:**

1:  $R_{QJA}$  is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{QJC}$  is guaranteed by design while  $R_{QJA}$  is determined by the user's board design.

a.  $40^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper

b.  $62.5^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

2: Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $I_{AS} = 17.5\text{A}$ ,  $V_{DD} = 40\text{V}$ ,  $V_{GS} = 10\text{V}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

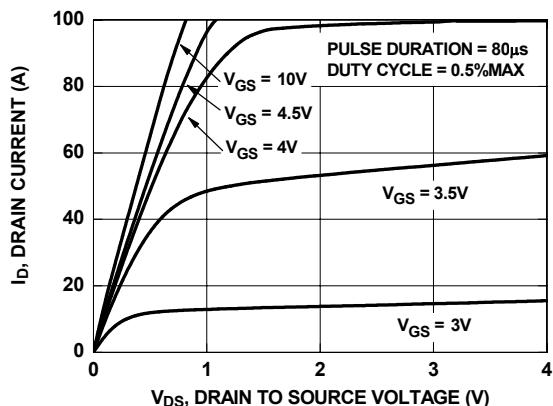


Figure 1. On Region Characteristics

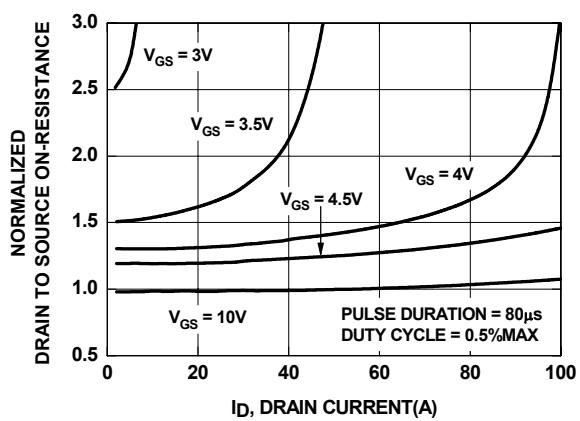


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

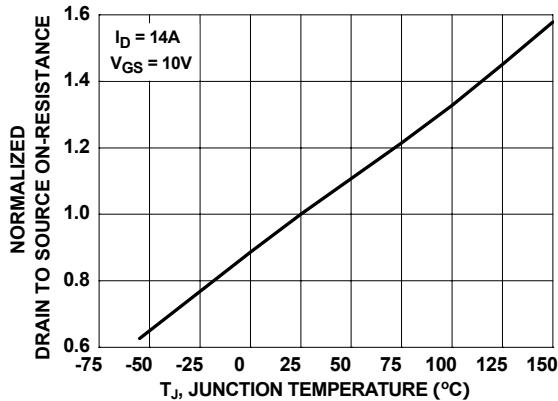


Figure 3. Normalized On Resistance vs Junction Temperature

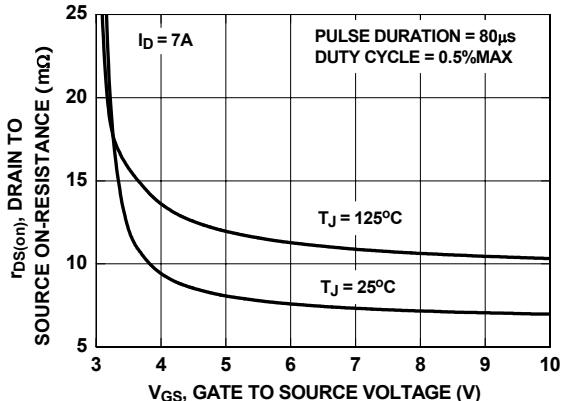


Figure 4. On-Resistance vs Gate to Source Voltage

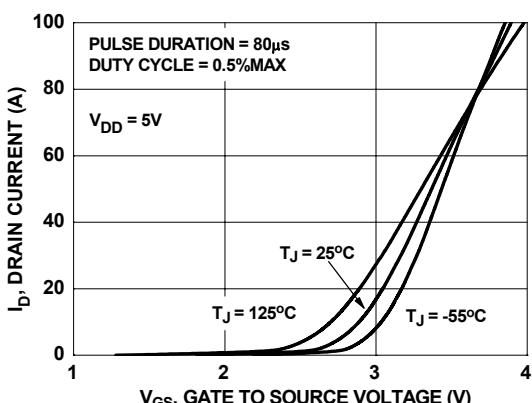


Figure 5. Transfer Characteristics

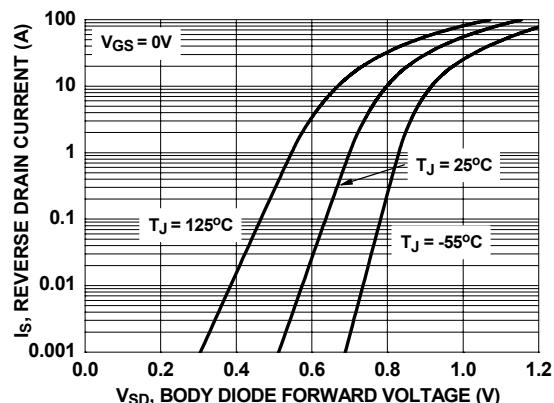
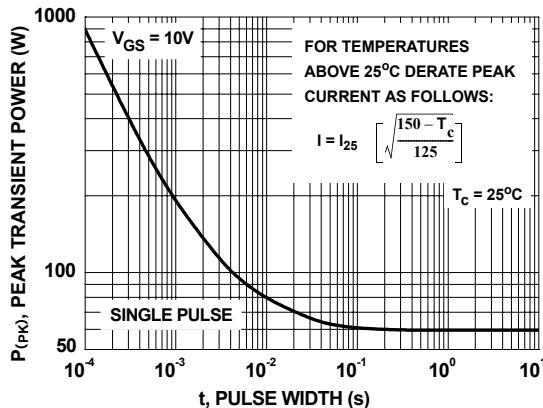
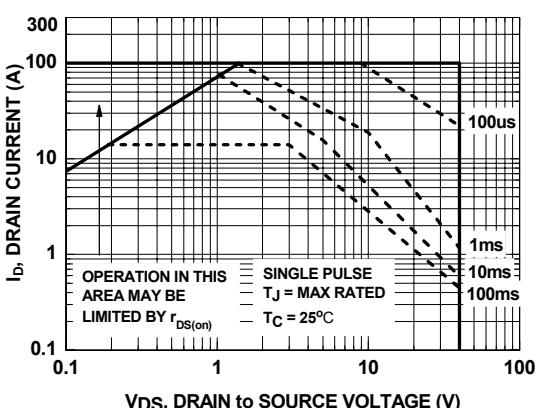
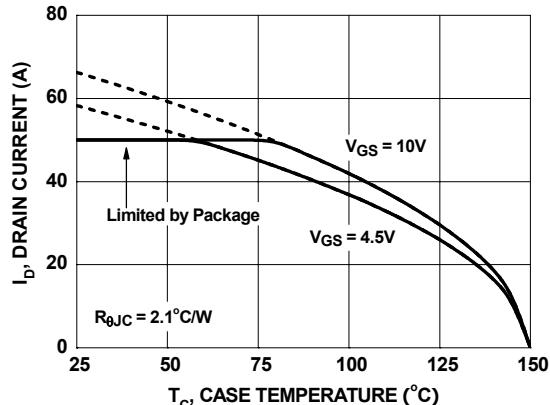
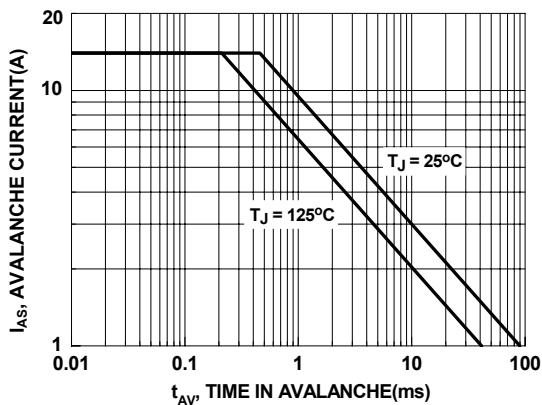
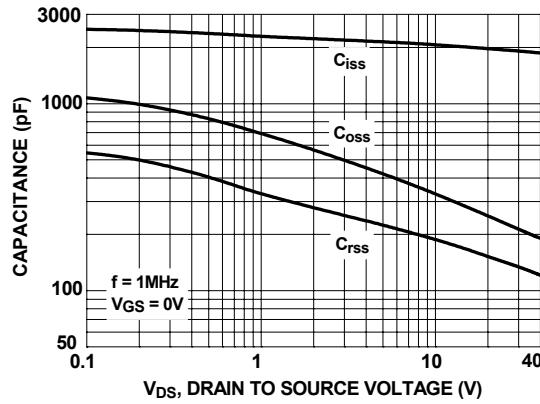
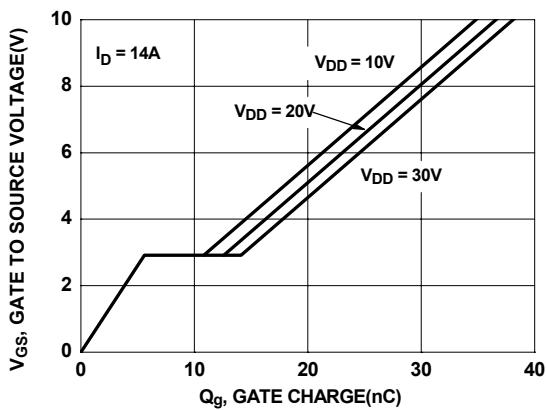
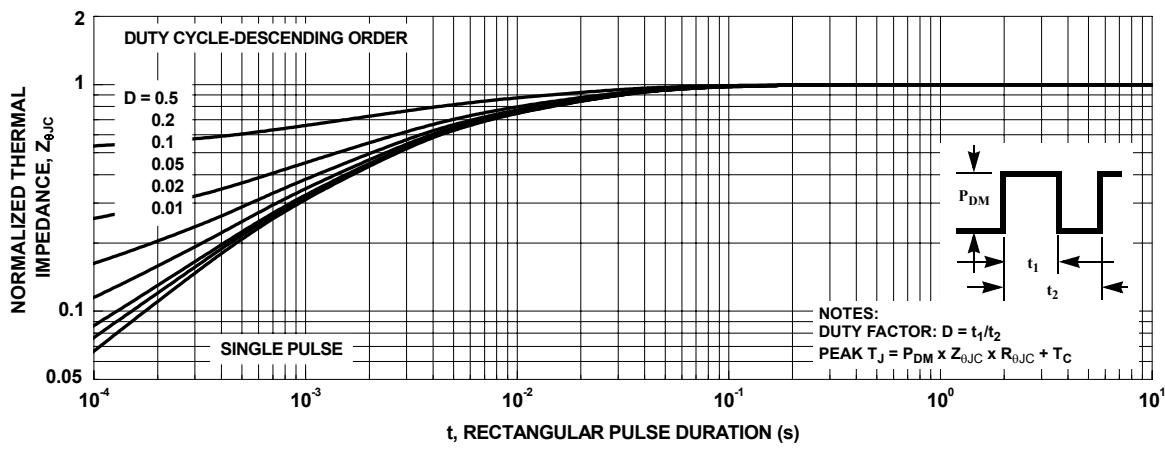


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



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