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# FCD5N60\_F085

## N-Channel SuperFET<sup>®</sup> MOSFET

### 600 V, 4.6 A, 1.1 $\Omega$

July 2015

#### Features

- 600V, 4.6A, typ.  $R_{ds(on)}=860m\Omega@V_{GS}=10V$
- Ultra Low Gate Charge (Typ.  $Q_g = 16$  nC)
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

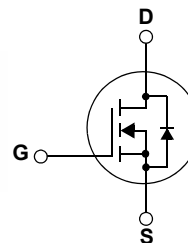
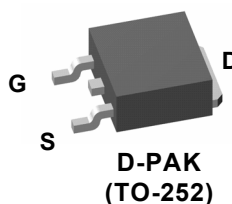
#### Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV

#### Description

SuperFET<sup>™</sup> is Fairchild's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is suitable for various automotive DC/DC power conversion.



For current package drawing, please refer to the Fairchild website at <http://www.fairchildsemi.com/package-drawings/TO/TO252A03.pdf>.

#### MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage	600	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$I_D$	Drain Current - Continuous ( $V_{GS}=10$ ) (Note 1)	$T_C = 25^\circ\text{C}$	A
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$	
		See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	29	mJ
$P_D$	Power Dissipation	54	W
	Derate Above $25^\circ\text{C}$	1.56	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 2)	83	$^\circ\text{C/W}$

#### Notes:

- 1: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 10\text{mH}$ ,  $I_{AS} = 2.4\text{A}$ ,  $V_{DD} = 100\text{V}$  during inductor charging and  $V_{DD} = 0\text{V}$  during time in avalanche.
- 2:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD5N60	FCD5N60_F085	D-PAK(TO-252)	13"	16mm	2500units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$B_{V_{DS}}$	Drain-to-Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	600	-	-	V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{DS} = 600\text{V}$ , $T_J = 25^\circ\text{C}$ $V_{GS} = 0\text{V}$ , $T_J = 150^\circ\text{C}$ (Note 4)	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 30\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 4.6\text{A}$ , $T_J = 25^\circ\text{C}$ $V_{GS} = 10\text{V}$ , $T_J = 150^\circ\text{C}$ (Note 4)	-	0.86	1.1	$\Omega$
			-	2.5	3.2	$\Omega$

**Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz		-	570	-	pF
C <sub>oss</sub>	Output Capacitance			-	280	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			-	20	-	pF
R <sub>g</sub>	Gate Resistance	f = 1MHz		-	1.9	-	Ω
Q <sub>g(ToT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to 10V	V <sub>DD</sub> = 480V I <sub>D</sub> = 4.6A	-	16	21	nC
Q <sub>g(th)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 to 2V		-	1.0	-	nC
Q <sub>gs</sub>	Gate-to-Source Gate Charge			-	3.2	-	nC
Q <sub>gd</sub>	Gate-to-Drain “Miller” Charge			-	7.6	-	nC

**Switching Characteristics**

$t_{on}$	Turn-On Time	$V_{DD} = 300\text{V}$ , $I_D = 4.6\text{A}$ , $V_{GS} = 10\text{V}$ , $R_{GEN} = 25\Omega$	-	-	84	ns
$t_{d(on)}$	Turn-On Delay		-	18	-	ns
$t_r$	Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off Delay		-	48	-	ns
$t_f$	Fall Time		-	13	-	ns
$t_{off}$	Turn-Off Time		-	-	178	ns

**Drain-Source Diode Characteristics**

$V_{SD}$	Source-to-Drain Diode Voltage	$I_{SD} = 4.6\text{A}$ , $V_{GS} = 0\text{V}$	-	-	1.25	V
$t_{rr}$	Reverse-Recovery Time	$V_{DD} = 480\text{V}$ , $I_F = 4.6\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	190	250	ns
$Q_{rr}$	Reverse-Recovery Charge		-	1.7	2.2	$\mu\text{C}$

**Note:**

4: The maximum value is specified by design at  $T_J = 150^\circ\text{C}$ . Product is not tested to this condition in production.

## Typical Characteristics

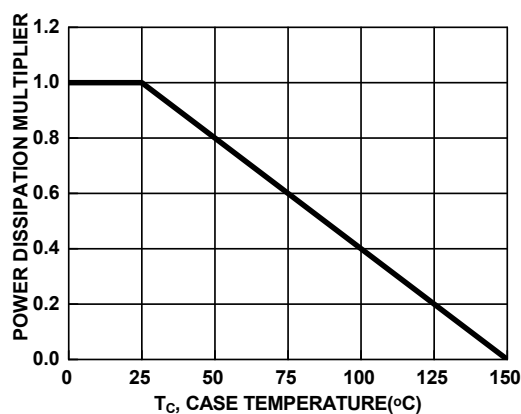


Figure 1. Normalized Power Dissipation vs. Case Temperature

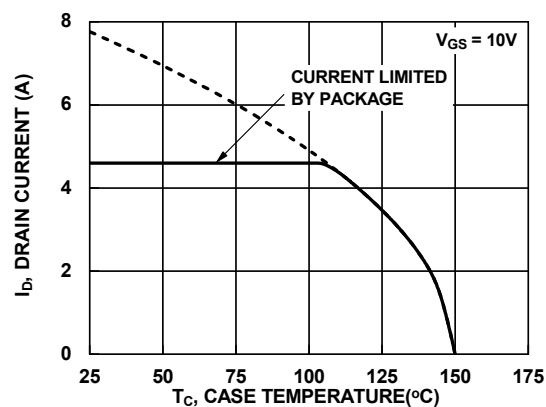


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

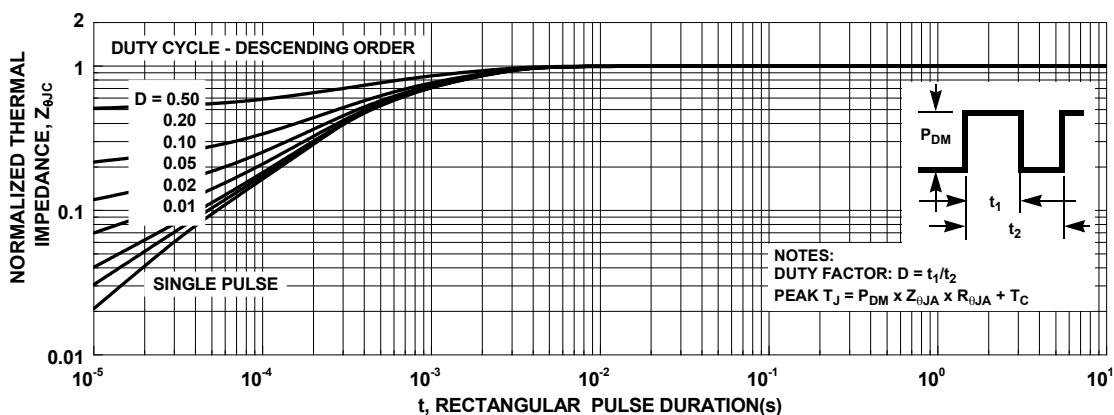


Figure 3. Normalized Maximum Transient Thermal Impedance

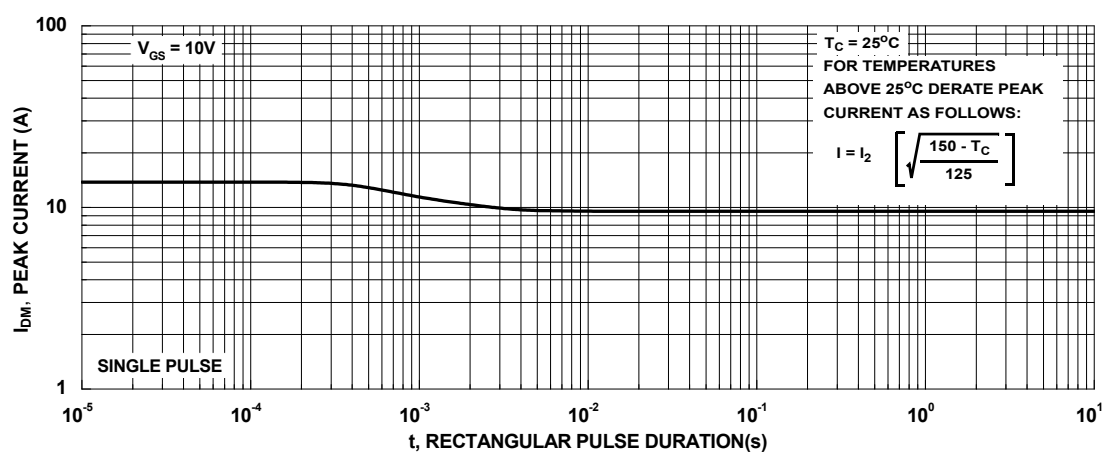


Figure 4. Peak Current Capability

## Typical Characteristics

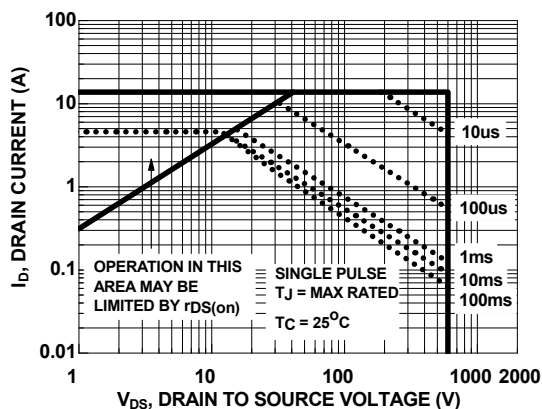


Figure 5. Forward Bias Safe Operating Area

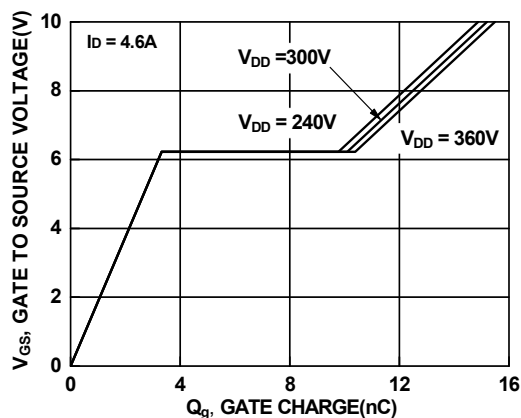


Figure 6. Gate Charge vs. Gate to Source Voltage

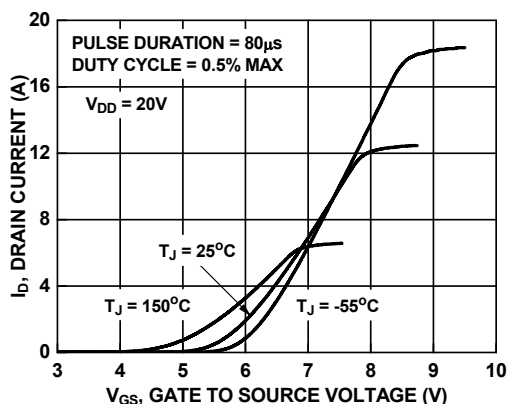


Figure 7. Transfer Characteristics

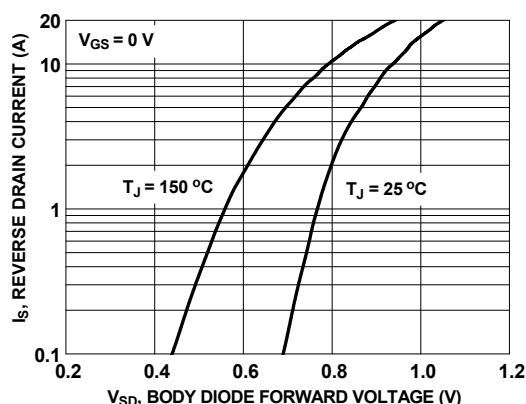


Figure 8. Forward Diode Characteristics

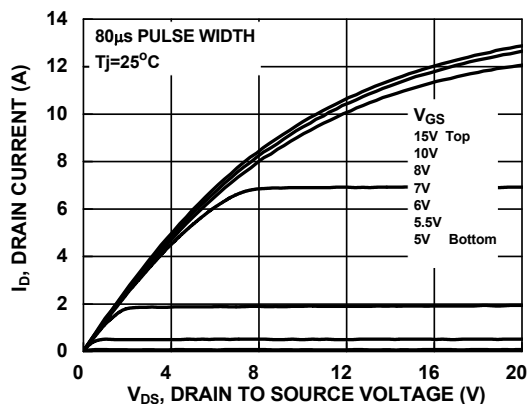


Figure 9. Saturation Characteristics

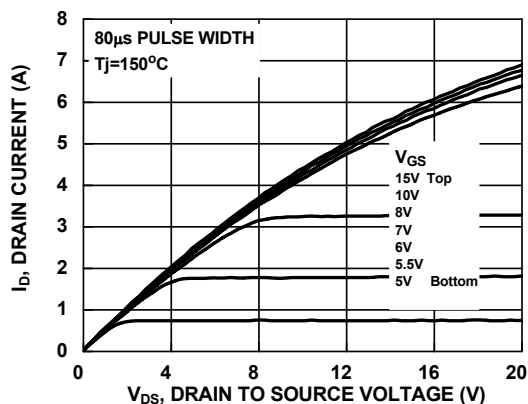


Figure 10. Saturation Characteristics

## Typical Characteristics

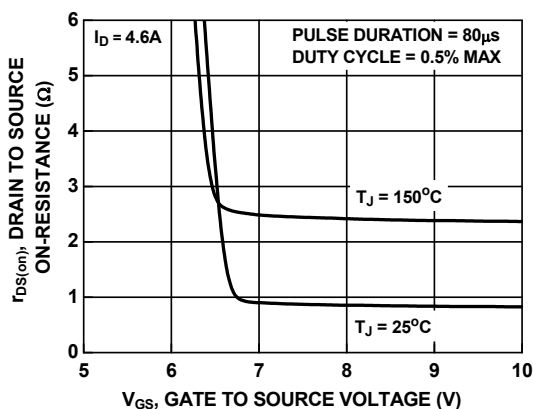


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

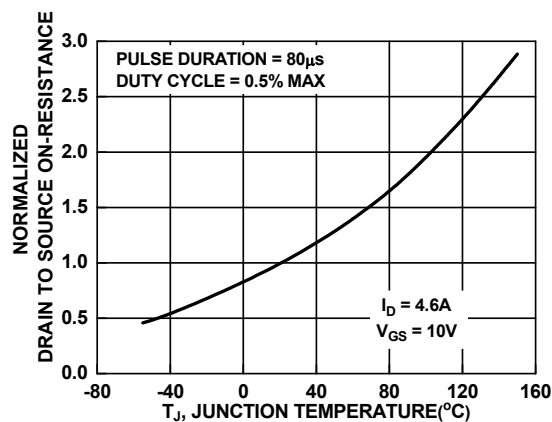


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

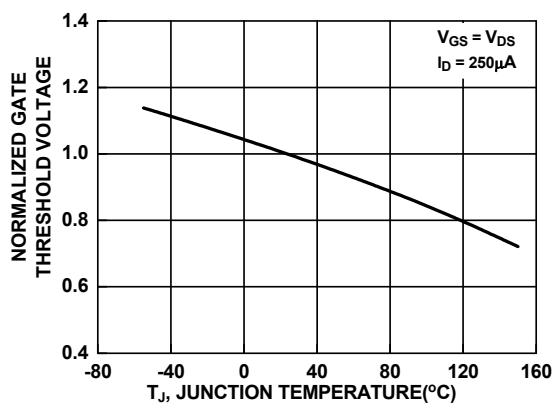


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

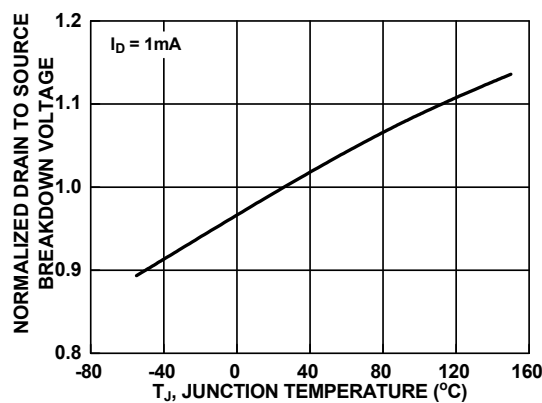


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

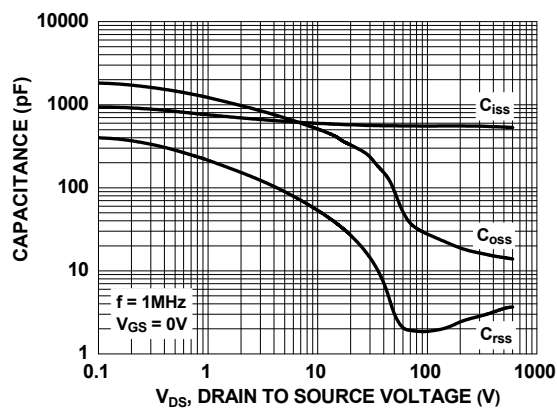


Figure 15. Capacitance vs. Drain to Source Voltage



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