

Summary

The Xilinx® Automotive (XA) Spartan®-3 family of Field-Programmable Gate Arrays meets the needs of high-volume, cost-sensitive automotive electronic applications. The five-member family offers densities ranging from 50,000 to 1.5 million system gates, as shown in [Table 1](#).

Introduction

XA devices are available in both extended-temperature Q-grade (–40°C to +125°C T_J) and I-grade (–40°C to +100°C T_J) and are qualified to the industry-recognized AEC-Q100 standard.

The XA Spartan-3 family builds on the success of the earlier XA Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. These Spartan-3 enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of advanced automotive electronics modules and systems ranging from the latest driver assistance and infotainment systems to instrument clusters and gateways.

The Spartan-3 family is a flexible alternative to ASICs, ASSPs, and microcontrollers. FPGAs avoid the high initial NREs, the lengthy development cycles, and problems with obsolescence. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary.

Table 1: Summary of Spartan-3 FPGA Attributes

| Device | System Gates | Logic Cells | CLB Array (One CLB = Four Slices) | | | Distributed RAM (bits ¹) | Block RAM (bits ¹) | Dedicated Multipliers | DCMs | Maximum User I/O | Maximum Differential I/O Pairs |
|----------|--------------|-------------|--------------------------------------|---------|------------|--------------------------------------|--------------------------------|-----------------------|------|------------------|--------------------------------|
| | | | Rows | Columns | Total CLBs | | | | | | |
| XA3S50 | 50K | 1,728 | 16 | 12 | 192 | 12K | 72K | 4 | 2 | 124 | 56 |
| XA3S200 | 200K | 4,320 | 24 | 20 | 480 | 30K | 216K | 12 | 4 | 173 | 76 |
| XA3S400 | 400K | 8,064 | 32 | 28 | 896 | 56K | 288K | 16 | 4 | 264 | 116 |
| XA3S1000 | 1M | 17,280 | 48 | 40 | 1,920 | 120K | 432K | 24 | 4 | 333 | 149 |
| XA3S1500 | 1.5M | 29,952 | 64 | 52 | 3,328 | 208K | 576K | 32 | 4 | 487 | 221 |

Notes:

- By convention, one Kb is equivalent to 1,024 bits.

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Features

- AEC-Q100 device qualification and full PPAP documentation support available in both extended temperature Q-grade and I-grade
- Guaranteed to meet full electrical specification over the T_J = –40°C to +125°C temperature range
- Revolutionary 90-nanometer process technology
- Low cost, high-performance logic solution for high-volume, automotive applications
 - Three power rails: for core (1.2V), I/Os (1.2V to 3.3V), and auxiliary purposes (2.5V)
- SelectIO™ interface signaling
 - Up to 487 I/O pins
 - 622 Mb/s data transfer rate per I/O
 - Eighteen single-ended signal standards
 - Eight differential signal standards including LVDS
 - Termination by Digitally Controlled Impedance
 - Signal swing ranging from 1.14V to 3.45V
 - Double Data Rate (DDR) support
- Logic resources
 - Abundant logic cells with shift register capability
 - Wide multiplexers

- ◆ Fast look-ahead carry logic
- ◆ Dedicated 18 x 18 multipliers
- ◆ JTAG logic compatible with IEEE 1149.1/1532
- SelectRAM™ hierarchical memory
 - ◆ Up to 576 Kbits of total block RAM
 - ◆ Up to 208 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
 - ◆ Clock skew elimination
 - ◆ Frequency synthesis
 - ◆ High-resolution phase shifting
 - ◆ Maximum clock frequency 125 MHz
- Fully supported by Xilinx ISE® software development system
 - ◆ Synthesis, mapping, placement and routing
- MicroBlaze™ processor, CAN, LIN, MOST, and other cores
- Pb-free packaging options
- Xilinx and all of our production partners are qualified to ISO-TS16949

Please refer to the Spartan-3 complete data sheet ([DS099](#)) for a full product description, AC and DC specifications, and package pinout descriptions

Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available as shown in [Table 2](#). Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in [Figure 1](#). A ring of IOBs surrounds a regular array of CLBs. The XA3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XA3S200 to the XA3S1500 have two columns of block RAM. Each column is made up of several 18 Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XA3S50 has only the block RAM column on the far left.

Figure 1: Spartan-3 Family Architecture

Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust static memory cells that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit-wide SelectMAP port.

I/O Capabilities

The SelectIO feature of Spartan-3 devices supports 18 single-ended standards and eight differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections. Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 2: Signal Standards Supported by the Spartan-3 Family

| Standard Category | Description | V _{CCO} (V) | Class | Symbol | DCI Option |
|---------------------|--|----------------------|----------------------|-----------------|------------|
| Single-Ended | | | | | |
| GTL | Gunning Transceiver Logic | N/A | Terminated | GTL | Yes |
| | | | Plus | GTLP | Yes |
| HSTL | High-Speed Transceiver Logic | 1.5 | I | HSTL_I | Yes |
| | | | III | HSTL_III | Yes |
| | | 1.8 | I | HSTL_I_18 | Yes |
| | | | II | HSTL_II_18 | Yes |
| | | | III | HSTL_III_18 | Yes |
| LVCMOS | Low-Voltage CMOS | 1.2 | N/A | LVCMOS12 | No |
| | | 1.5 | N/A | LVCMOS15 | Yes |
| | | 1.8 | N/A | LVCMOS18 | Yes |
| | | 2.5 | N/A | LVCMOS25 | Yes |
| | | 3.3 | N/A | LVCMOS33 | Yes |
| LVTTTL | Low-Voltage Transistor-Transistor Logic | 3.3 | N/A | LVTTTL | No |
| PCI | Peripheral Component Interconnect | 3.0 | 33 MHz | PCI33_3 | No |
| SSTL | Stub Series Terminated Logic | 1.8 | N/A (± 6.7 mA) | SSTL18_I | Yes |
| | | | N/A (± 13.4 mA) | SSTL18_II | No |
| | | 2.5 | I | SSTL2_I | Yes |
| | | | II | SSTL2_II | Yes |
| Differential | | | | | |
| LDT (ULVDS) | Lightning Data Transport (HyperTransport™) | 2.5 | N/A | LDT_25 | No |
| LVDS | Low-Voltage Differential Signaling | | Standard | LVDS_25 | Yes |
| | | | Bus | BLVDS_25 | No |
| | | | Extended Mode | LVDS_EXT_25 | Yes |
| LVPECL | Low-Voltage Positive Emitter-Coupled Logic | 2.5 | N/A | LVPECL_25 | No |
| RSDS | Reduced-Swing Differential Signaling | 2.5 | N/A | RSDS_25 | No |
| HSTL | Differential High-Speed Transceiver Logic | 1.8 | II | DIFF_HSTL_II_18 | Yes |
| SSTL | Differential Stub Series Terminated Logic | 2.5 | II | DIFF_SSTL2_II | Yes |

Table 3: Spartan-3 XA I/O Chart

| Device | Grade | Available User I/Os and Differential (Diff) I/O Pairs | | | | | | | | | | | |
|----------|-------|---|------|--------|------|--------|------|--------|------|--------|------|--------|------|
| | | VQG100 | | TQG144 | | PQG208 | | FTG256 | | FGG456 | | FGG676 | |
| | | User | Diff | User | Diff | User | Diff | User | Diff | User | Diff | User | Diff |
| XA3S50 | I,Q | 63 | 29 | - | - | 124 | 56 | - | - | - | - | - | - |
| XA3S200 | I,Q | 63 | 29 | 97 | 46 | 141 | 62 | 173 | 76 | - | - | - | - |
| XA3S400 | I,Q | - | - | - | - | 141 | 62 | 173 | 76 | 264 | 116 | - | - |
| XA3S1000 | I,Q | - | - | - | - | - | - | 173 | 76 | 333 | 149 | - | - |
| XA3S1500 | I | - | - | - | - | - | - | - | - | 333 | 149 | 487 | 221 |

Notes:

- All device options listed in a given package column are pin-compatible.

DC Specifications

Table 4: General Recommended Operating Conditions

| Symbol | Description | | Min | Nom | Max | Units |
|--------------------------|--|---------------------|-------|-------|-----------------|-------|
| T_J | Junction temperature | I-Grade | -40 | 25 | 100 | °C |
| | | Q-Grade | -40 | 25 | 125 | °C |
| V_{CCINT} | Internal supply voltage | | 1.140 | 1.200 | 1.260 | V |
| $V_{CCO}^{(1)}$ | Output driver supply voltage | | 1.140 | - | 3.450 | V |
| V_{CCAUX} | Auxiliary supply voltage | | 2.375 | 2.500 | 2.625 | V |
| $\Delta V_{CCAUX}^{(2)}$ | Voltage variance on VCCAUX when using a DCM | | - | - | 10 | mV/ms |
| V_{IN} | Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND | $V_{CCO} = 3.3V$ | -0.3 | - | 3.75 | V |
| | | $V_{CCO} \leq 2.5V$ | -0.3 | - | $V_{CCO}+0.3$ | V |
| | Voltage applied to all Dedicated pins relative to GND | | -0.3 | - | $V_{CCAUX}+0.3$ | V |

Notes:

- The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 34 of [DS099](#), and that specific to the differential standards is given in Table 36 of [DS099](#).
- Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.

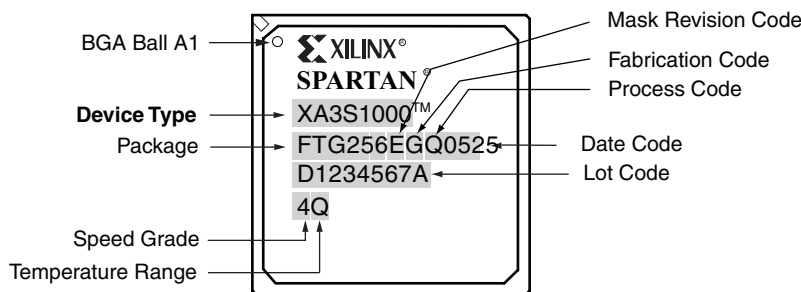
Table 5: Quiescent Supply Current Characteristics

| Symbol | Description | Device | I-Grade Maximum | Q-Grade Maximum | Units |
|---------------------|---|----------|-----------------|-----------------|-------|
| I _{CCINTQ} | Quiescent V _{CCINT} supply current | XA3S50 | 50 | 100 | mA |
| | | XA3S200 | 125 | 200 | mA |
| | | XA3S400 | 180 | 250 | mA |
| | | XA3S1000 | 315 | 400 | mA |
| | | XA3S1500 | 410 | - | mA |
| I _{CCOQ} | Quiescent V _{CCO} supply current | XA3S50 | 12 | 12 | mA |
| | | XA3S200 | 12 | 12 | mA |
| | | XA3S400 | 14 | 14 | mA |
| | | XA3S1000 | 14 | 14 | mA |
| | | XA3S1500 | 16 | - | mA |
| I _{CCAUXQ} | Quiescent V _{CCAUX} supply current | XA3S50 | 22 | 25 | mA |
| | | XA3S200 | 33 | 35 | mA |
| | | XA3S400 | 44 | 50 | mA |
| | | XA3S1000 | 55 | 60 | mA |
| | | XA3S1500 | 85 | - | mA |

Notes:

- The numbers in this table are based on the conditions set forth in Table 31 of [DS099](#). Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at ambient room temperature (T_A of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.45V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a “blank” configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Power Estimator for more accurate estimates. See Note 2.
- There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The XPower Power Estimator at http://www.xilinx.com/ise/power_tools provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
- The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus ICCINT if VCCINT Applied before VCCAUX, page 51 of [DS099](#).

Ordering Information



DS314-1_02_100808

Figure 2: Spartan-3 BGA Package Marking Example for Part Number XA3S1000-4 FTG256Q

Spartan-3 FPGAs are available in Pb-free packaging options for all device/package combinations. The Pb-free packages include a special “G” character in the ordering code.

Pb-Free Packaging

For additional information on Pb-free packaging, see [XAPP427: Implementation and Solder Reflow Guidelines for Pb-Free Packages](#).

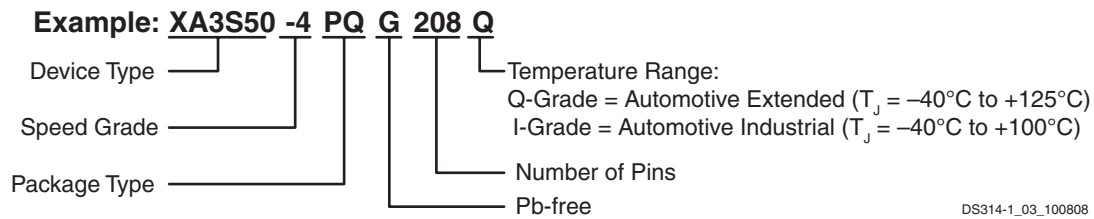


Table 6: Package Types and Number of Pins

| Device | Speed Grade | | Package Type / Number of Pins | | Temperature Range (T_j) | |
|----------|-------------|----------------------|-------------------------------|--|-----------------------------|---|
| | | | | | | |
| XA3S50 | -4 | Standard Performance | VQG100 | 100-pin Very Thin Quad Flat Pack (VQFP) | I | I-Grade (-40°C to $+100^{\circ}\text{C}$) |
| XA3S200 | | | TQG144 | 144-pin Thin Quad Flat Pack (TQFP) | Q | Q-Grade (-40°C to $+125^{\circ}\text{C}$) |
| XA3S400 | | | PQG208 | 208-pin Plastic Quad Flat Pack (PQFP) | | |
| XA3S1000 | | | FTG256 | 256-ball Fine-Pitch Thin Ball Grid Array (FTBGA) | | |
| XA3S1500 | | | FGG456 | 456-ball Fine-Pitch Ball Grid Array (FBGA) | | |
| | | | FGG676 | 676-ball Fine-Pitch Ball Grid Array (FBGA) | | |

Additional Resources

- [DS099](#), Spartan-3 FPGA Family Data Sheet
- [UG331](#), Spartan-3 Generation FPGA User Guide
- [UG332](#), Spartan-3 Generation Configuration User Guide

Revision History

The following table shows the revision history for this document:

| Date | Version | Description |
|----------|---------|---|
| 10/18/04 | 1.0 | Initial Xilinx release. |
| 12/20/04 | 1.1 | Multiple text edits throughout. |
| 10/27/06 | 1.2 | Updated IO standards (Table 2), and link to Spartan-3 Data Sheet, added XA3S1500, TQG144, FGG676, Table 4 , and Table 5 . |
| 11/28/06 | 1.2.1 | Changed order of explanations in Table 6 for TQG144 and PQG208. |
| 11/12/07 | 1.2.2 | Changed all values for the Block RAM (bits) column and two values for the XA3S1000 row in Table 1 . |
| 01/25/08 | 1.2.3 | Changed XA3S1500 Q-Grade Maximum in Table 5 . |
| 06/18/09 | 1.3 | Added UG331 and UG332 to " Additional Resources " section. |

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