RICOH R2221x R2223x

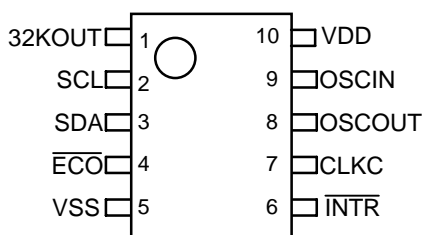## 2-wire Serial Interface Real Time Clock IC

OUTLINE

The R2221x,R2223x is a CMOS real-time clock IC connected to the CPU by two signal lines, SCL, SDA, and configured to perform serial transmission of time and calendar data to the CPU. The periodic interrupt circuit is configured to generate interrupt signals with six selectable interrupts ranging from 0.5 seconds to 1 month. The 2 alarm interrupt circuits generate interrupt signals at preset times. As the oscillation circuit is driven under constant voltage, fluctuation of the oscillator frequency due to supply voltage is small, and the time keeping current is small (TYP. $0.18\mu A$ at 3V). The oscillation halt sensing circuit can be used to judge the validity of internal data in such events as power-on; the supply voltage monitoring circuit is configured to record a drop in supply voltage below supply voltage monitoring threshold settings. The 32.768kHz clock output function (CMOS output with control pin) is intended to output sub-clock pulses for the external microcomputer. The oscillation adjustment circuit is intended to adjust time counts with high precision by correcting deviations in the oscillation frequency of the crystal oscillator. Since the package for these ICs are TSSOP10G (4.0x2.9x1.0:R2221T,R2223T) or QFN018018-12 (1.8x1.8x0.43: R2221L, R2223L), high density mounting of ICs on boards is possible.

FEATURES

- Minimum Timekeeping supply voltage TYP:0.6 to 5.5v (Worst: 0.9V to 5.5v); VDD pin
- Ultra low power consumption $0.18\mu A$ TYP at V_{DD}=3V ($0.65\mu A$ MAX.)
- Two signal lines (SCL, SDA) required for connection to the CPU.
- Time counters (counting hours, minutes, and seconds) and calendar counters (counting years, months, days, and weeks) (in BCD format)
- Interrupt circuit configured to generate interrupt signals (with interrupts ranging from 0.5 seconds to 1 month) to the CPU and provided with an interrupt flag and an interrupt halt
- 2 alarm interrupt circuits (Alarm_W for week, hour, and minute alarm settings and Alarm_D for hour and minute alarm settings)
- With Power-on flag to prove that the power supply starts from 0V
- 32-kHz clock output pin (CMOS push-pull output with control pin)
- Supply voltage monitoring circuit with supply voltage monitoring threshold settings
- Automatic identification of leap years up to the year 2099
- Selectable 12-hour and 24-hour mode settings
- High precision oscillation adjustment circuit
- Built-in oscillation stabilization capacitors (CG and CD)
- Package TSSOP10G (4.0mm x 2.9mm x 1.0mm: R2221T, R2223T)
        QFN018018-12 (1.8mm x 1.8mm x 0.43mm: R2221L, R2223L)
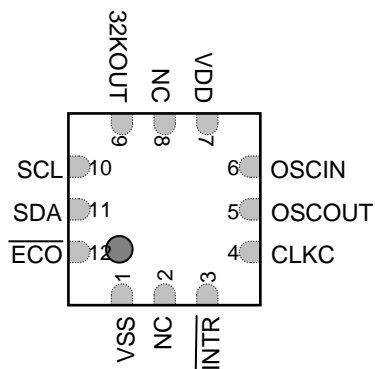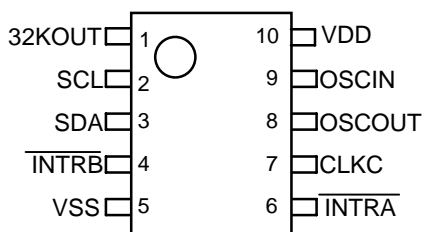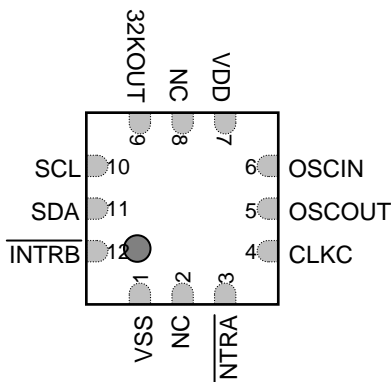- CMOS process

PIN CONFIGURATION

R2221T(TSSOP10G)

32KOUT	1	10 VDD
SCL	2	9 OSCIN
SDA	3	8 OSCOUT
$\overline{ECO}$	4	7 CLKC
VSS	5	6 $\overline{INTR}$

TOP VIEW

R2221L(QFN018018-12)

32KOUT NC VDD
9 8 7

SCL	10	6	OSCIN
SDA	11	5	OSCOUT
$\overline{ECO}$	12 1	4	CLKC

2 3
SSA NC $\overline{INTR}$

TOP VIEW

R2223T(TSSOP10G)

32KOUT	1	10 VDD
SCL	2	9 OSCIN
SDA	3	8 OSCOUT
$\overline{INTRB}$	4	7 CLKC
VSS	5	6 $\overline{INTRA}$

TOP VIEW

R2223L(QFN018018-12)

32KOUT NC VDD
9 8 7

SCL	10	6	OSCIN
SDA	11	5	OSCOUT
$\overline{INTRB}$	12 1	4	CLKC

2 3
VSS NC $\overline{INTRA}$

TOP VIEW

BLOCK DIAGRAM
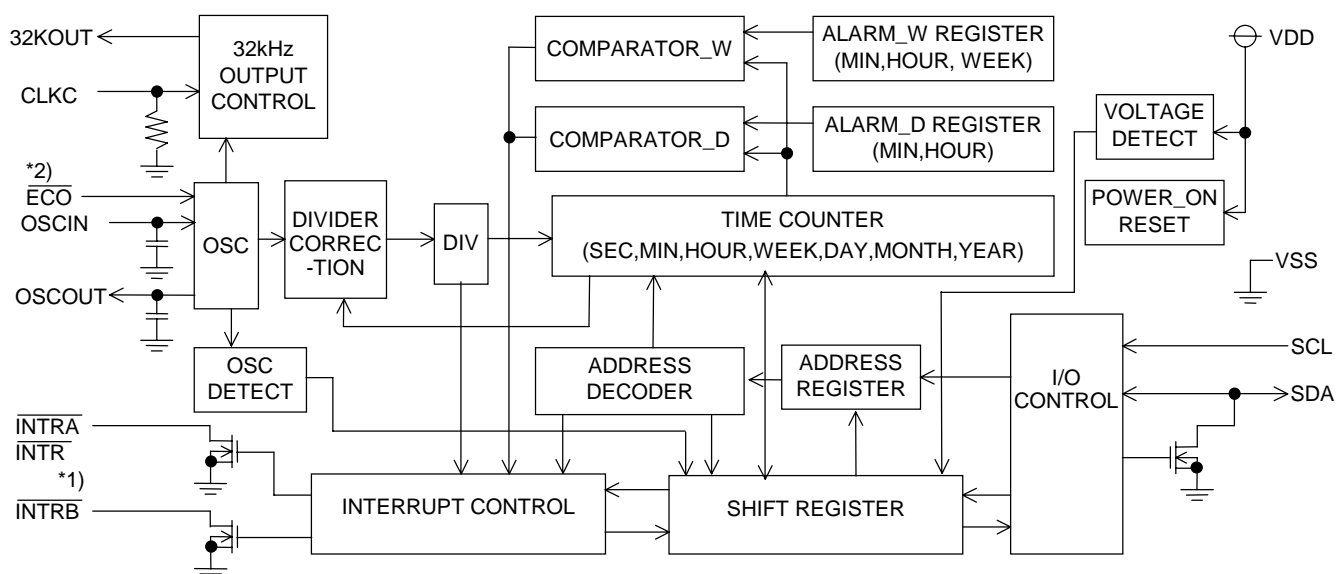
*1) As an interrupt pin, the R2221x has $\overline{INTR}$, the R2223x has $\overline{INTRA}$ pin. The R2221x does not have $\overline{INTRB}$ pin.

*2) The R2221x has $\overline{ECO}$ pin. The R2223x can set ECO mode with the internal resister.

RICOH

SELECTION GUIDE

Product Name	Package	Quantity per Reel	Pb Free
R2221T-E2-F	TSSOP10G	2000 pcs	Yes
R2221L-E2	QFN018018-12	3000 pcs	Yes
R2223T-E2-F	TSSOP10G	2000 pcs	Yes
R2223L-E2	QFN018018-12	3000 pcs	Yes

PIN DESCRIPTION

Symbol	Item	Description
SCL	Serial Clock Line	The SCL pin is used to input clock pulses synchronizing the input and output of data to and from the SDA pin. Allows a maximum input voltage of 5.5v regardless of supply voltage.
SDA	Serial Data Line	The SDA pin is used to input and output data intended for writing and reading in synchronization with the SCL pin. Allows a maximum input voltage of 5.5v regardless of supply voltage. Nch. open drain output.
32KOUT	32kHz Clock Output	The 32KOUT pin is used to output 32.768-kHz clock pulses. The pin is CMOS push-pull output. The output is disabled and held "L" when CLKC pin is set to "L" or open, or certain register setting. This pin is enabled at power-on from 0v. Allows a maximum input voltage of 5.5v regardless of supply voltage.
CLKC	Clock Control	The CLKC pin is used to control output of the 32KOUT pin. The clock output is disabled and held "L" when this pin is set to "L" or open. Incorporated pull down register.
$\overline{\text{INTRA}}$ (R2223x)	Interrupt Output A	The $\overline{\text{INTRA}}$ pin is used to output alarm interrupt (Alarm_D) and periodic interrupt signals to the CPU. Disabled at power-on from 0V. N-channel open drain output. Allows a maximum pull-up voltage of 5.5v regardless of supply voltage.
$\overline{\text{INTRB}}$ (R2223x)	Interrupt Output B	The $\overline{\text{INTRB}}$ pin is used to output alarm interrupt (Alarm_W) to the CPU. Disabled at power-on from 0V. N-channel open drain output. Allows a maximum pull-up voltage of 5.5v regardless of supply voltage.
$\overline{\text{INTR}}$ (R2221x)	Interrupt Output	The $\overline{\text{INTR}}$ pin is used to output alarm interrupt (Alarm_D、Alarm_W) and periodic interrupt signals to the CPU. Disabled at power-on from 0V. N-channel open drain output. Allows a maximum pull-up voltage of 5.5v regardless of supply voltage.
$\overline{\text{ECO}}$ (R2221x)	Oscillator mode select pin	Ultra low consumption oscillator mode (ECO mode) select pin When the $\overline{\text{ECO}}$ pin is "L", the oscillator becomes ultra low consumption oscillator mode. In the actual usage, set this pin at "L" or "H". (R2223x realizes the ultra low consumption oscillator mode by resister.) For further information to know the technical notes, refer to the item "ECO mode" at P.30.
VDD VSS	Positive/Negative Power Supply Input	The VDD pin is connected to the power supply. The VSS pin is grounded.
OSCIN OSCOUT	Oscillation Circuit Input / Output	The OSCIN and OSCOUT pins are used to connect the 32.768-kHz crystal oscillator (with all other oscillation circuit components built into the R2221x, R2223x).
NC	No connection	

RICOH

ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Symbol	Item	Pin Name	Description	Unit
V_{DD}	Supply Voltage	VDD	-0.3 to +6.5	V
V_I	Input Voltage 1	SCL, SDA, CLKC, $\overline{ECO}$ *1)	-0.3 to +6.5	V
V_O	Output Voltage 1	SDA, $\overline{INTRA}$, $\overline{INTRB}$, $\overline{INTR}$*1)	-0.3 to +6.5	V
	Output Voltage 2	32KOUT	-0.3 to V_{DD} + 0.3	
P_D	Power Dissipation	Topt = 25°C	300	mW
Topt	Operating Temperature		-40 to +85	°C
Tstg	Storage Temperature		-55 to +125	°C

*1)R2221x: $\overline{ECO}$, $\overline{INTR}$ R2223x: $\overline{INTRA}$, $\overline{INTRB}$.

RECOMMENDED OPERATING CONDITIONS

(Vss=0V, Topt=-40 to +85°C)

Symbol	Item	Pin Name	Min,	Typ.	Max.	Unit
Vaccess	Supply Voltage	Power supply voltage for interfacing with CPU	1.5		5.5	V
VCLK	Time keeping Voltage	CGout,CDout=0pF *1), *2)	0.9		5.50	V
VCLKL	Minimum Time keeping Voltage	CGout,CDout=0pF *1), *2)		0.6	0.9	
Vxstp	Oscillation halt sensing Voltage	power supply which satisfies the condition XSTP=1 *3) CGout=CDout=0pF *1)*2)		0.6	0.9	V
fXT	Oscillation Frequency			32.768		kHz
VPUP	Pull-up Voltage	$\overline{INTRA}$, $\overline{INTRB}$, $\overline{INTR}$ *4)			5.5	V

*1) CGout is connected between OSCIN and VSS, CDout is connected between OSCOUT and VSS.
R2221x, R2223x incorporates the capacitors between OSCIN and VSS, between OSCOUT and VSS.
Then normally, CGout and CDout are not necessary.
For more detail, refer to the item named "•Configuration of Oscillation Circuit, ECO mode, and Correction of Time Count Deviations" on P.29.

*2) Quartz crystal unit: CL (load capacity)=6 to 12.5pF, R1 (equivalent series resistance)=under 75 to 80KΩ(Max.) The adjustment method depends on the CL value, R1 value, use or not use of ECO mode. For more detail, "•Configuration of Oscillation Circuit, ECO mode, and Correction of Time Count Deviations" on P.29.

*3) XSTP is the crystal oscillation halt sensing flag. When the crystal oscillation halts, XSTP=1.

*4)R2221x: $\overline{ECO}$, $\overline{INTR}$.   R2223x: $\overline{INTRA}$, $\overline{INTRB}$

RICOH

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified: V_{SS}=0V, V_{DD}=3.0V, Topt=-40 to +85°C, Crystal oscillator 32768Hz)

Symbol	Item	Pin Name	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	"H" Input Voltage	SCL, SDA, CLKC,	V_{DD}=1.5 to 5.5V	0.8x VDD		5.5	V
V_{IL}	"L" Input Voltage	$\overline{ECO}$ *1)		-0.3		0.2x VDD	
I_{OH}	"H" Output Current	32KOUT	V_{OH}=V_{DD}-0.5V			-0.5	mA
I_{OL1}	"L" Output Current	32KOUT	V_{OL}=0.4V	0.5			mA
I_{OL2}		$\overline{INTRA}$ $\overline{INTRB}$ $\overline{INTR}$ *1)		2.0			
I_{OL3}		SDA		3.0			
I_{IL}	Input Leakage Current	SCL, $\overline{ECO}$ *1)	V_I=5.5V or V_{SS} V_{DD}=5.5V	-0.2		0.2	μA
I_{CLKC}	Pull-down Resister Input Leakage Current	CLKC	V_I=5.5V		0.2	1.00	μA
I_{OZ}	Output Off-state Current	SDA, $\overline{INTRA}$, $\overline{INTRB}$, $\overline{INTR}$ *1)	V_O=5.5V or V_{SS} V_{DD}=5.5V	-0.2		0.2	μA
I_{DD1}	Time Keeping Current (ECO mode =ON)	VDD	V_{DD}=3V, Topt=-40 to +85°C *2) *3) *4)		0.18	0.65	μA
			V_{DD}=3V, Topt=-30 to +70°C *2) *3) *4)		0.18	0.5	μA
I_{DD2}	Time Keeping Current (ECO mode =OFF)	VDD	V_{DD}=3V, Topt=-40 to +85°C *2) *3) *5)		0.35	0.9	μA
			V_{DD}=3V, Topt=-30 to +70°C *2) *3) *5)		0.35	0.75	μA
V_{DET}	Supply Voltage Monitoring Voltage	VDD	Topt=-30 to +70°C	1.20	1.35	1.50	V

*1) R2221x: $\overline{ECO}$, $\overline{INTR}$ R2223x: $\overline{INTRA}$, $\overline{INTRB}$

*2) CGout,CDout=0pFFor time keeping current when outputting 32.768kHz from the 32KOUT pin, see "P.44 •TYPICAL CHARACTERISTICS".   For time keeping current when CGOUT, CDOUT is not equal to 0pF, see "P.31 •Adjustment of oscillation frequency".

*3) V_{DD}=3V,SCL=SDA=0V, CLKC=0V(32KOUT=OFF), OUTPUT=OPEN, CGout=CDout=0pf

*4) R1 of Crystal=30kΩ

*5) R1 of Crystal=55kΩ

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{SS}=0V,Topt=-40 to +85°C

Input and Output Conditions: V_{IH}=0.8×V_{DD},V_{IL}=0.2×V_{DD},V_{OH}=0.8×V_{DD},V_{OL}=0.2×V_{DD},CL=50pF

Sym-bol	Item	Condi-Tions	V_{DD}≥1.5V *1)			Unit
			Min.	Typ.	Max.	
f_{SCL}	SCL Clock Frequency				400	kHz
t_{LOW}	SCL Clock Low Time		1.3			μs
t_{HIGH}	SCL Clock High Time		0.6			μs
$t_{HD;STA}$	Start Condition Hold Time		0.6			μs
$t_{SU;STO}$	Stop Condition Set Up Time		0.6			μs
$t_{SU;STA}$	Start Condition Set Up Time		0.6			μs
$t_{SU;DAT}$	Data Set Up Time		100			ns
$t_{HD;DAT}$	Data Hold Time		0			ns
$t_{PL;DAT}$	SDA "L" Stable Time After Falling of SCL				0.9	μs
$t_{PZ;DAT}$	SDA off Stable Time After Falling of SCL				0.9	μs
t_R	Rising Time of SCL and SDA (input)				300	ns
t_F	Falling Time of SCL and SDA (input)				300	ns
t_{SP}	Spike Width that can be removed with Input Filter				50	ns
t_{RCV}	Recovery Time from Stop Condition to Start Condition *)		31			μs

*) For , Recovery Time see "P.28 Interfacing with the CPU •Data Transmission under Special Conditions".

| S | Start Condition | P | Stop Condition |

| Sr | Repeated Start Condition |

RICOH
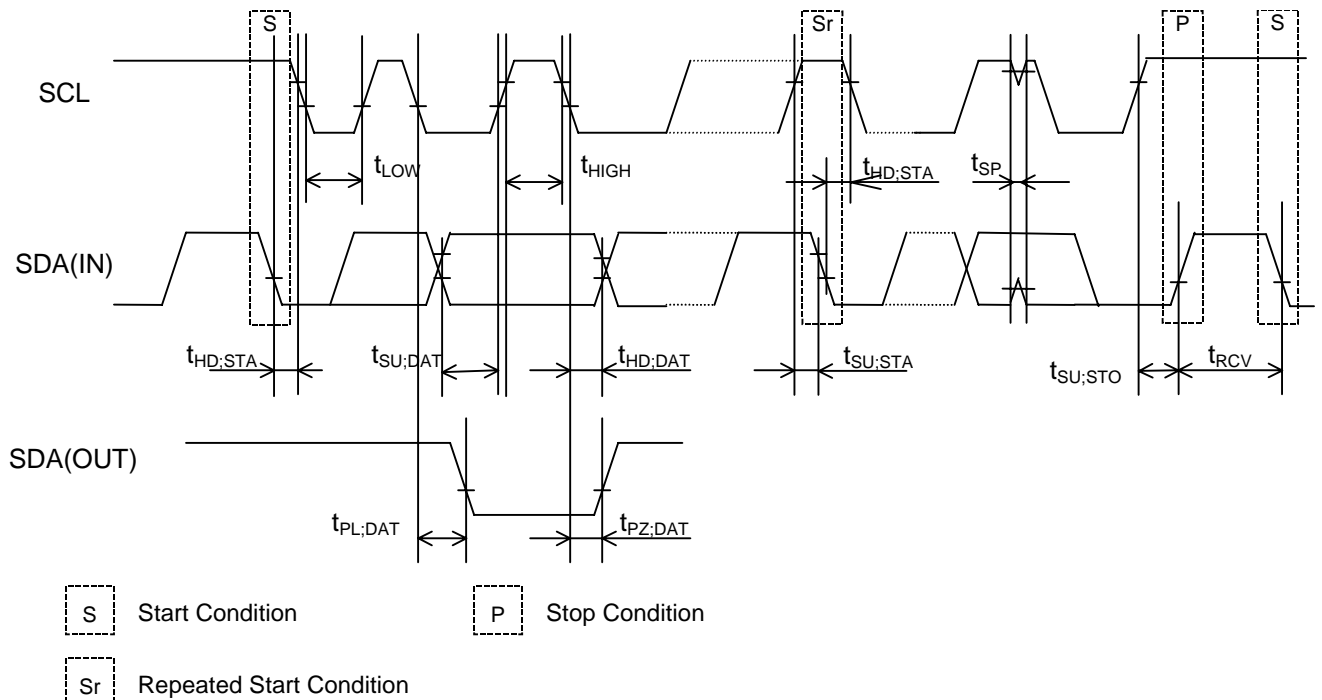
PACKAGE DIMENSIONS

- **R2221L, R2223L**
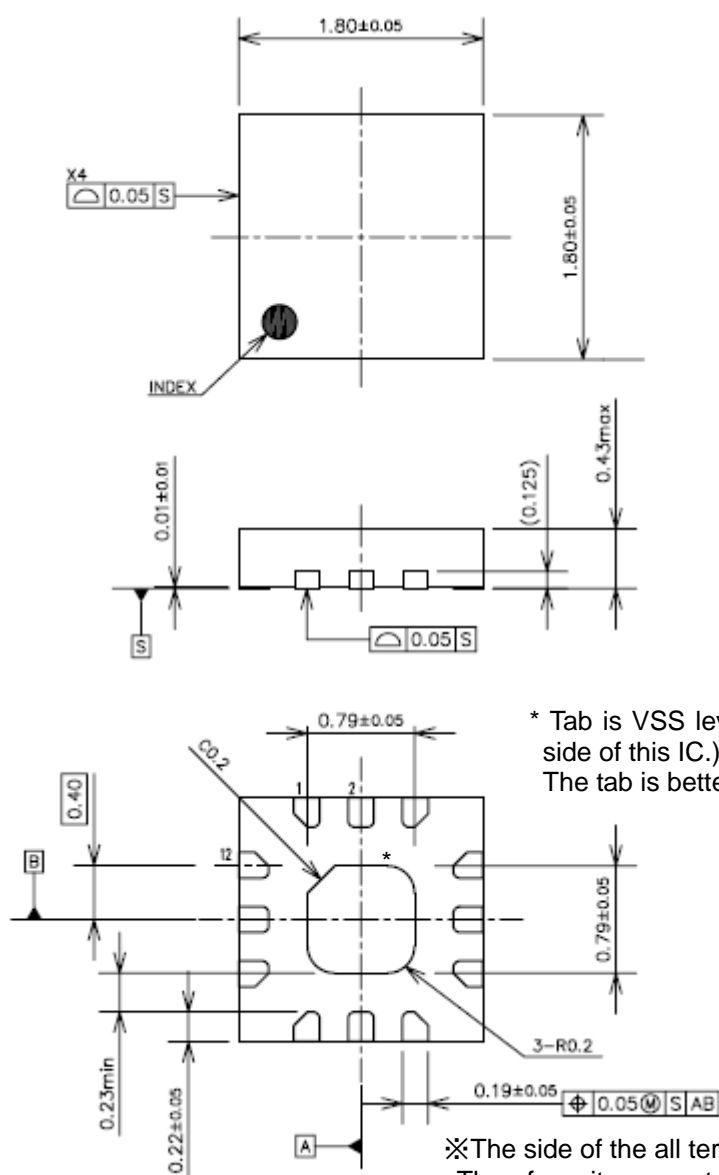
* Tab is VSS level. (They are connected to the reverse side of this IC.)
The tab is better to be connected to the VSS.

※The side of the all terminals have no plating treatment. Therefore, it may not be able to form solder fillet on the side of the terminals.

unit: mm

● **R2221T, R2223T**

2.9±0.2

10   6

1   5

0.5

2.8±0.2

4.0±0.2

0 to 10°

0.55±0.2

0.13 +0.1 -0.05

(0.75)

0.85±0.15

0.1 +0.1 -0.05

⌓ 0.1

0.2±0.1   ⊕ 0.15 Ⓜ

unit: mm

RICOH

GENERAL DESCRIPTION

- **Interface with CPU**

The R2221x,R2223x is connected to the CPU by two signal lines, SCL and SDA, through which it reads and writes data from and to the CPU.   Since the I/O pin of SDA is open drain, data interfacing with a CPU different supply voltage is possible by applying pull-up resistors on the circuit board.   The maximum clock frequency of 400kHz (at VDD$\geq$1.5V) of SCL enables data transfer in I^{2}C bus fast mode.

- **Clock and Calendar Function**

The R2221x, R2223x reads and writes time data from and to the CPU in units ranging from seconds to the last two digits of the calendar year. The calendar year will automatically be identified as a leap year when its last two digits are a multiple of 4.   Consequently, leap years up to the year 2099 can automatically be identified as such.

*) The year 2000 is a leap year while the year 2100 is not a leap year.

- **Alarm Function**

The R2221x, R2223x incorporates the alarm interrupt circuit configured to generate interrupt signals to the CPU at preset times. The alarm interrupt circuit allows two types of alarm settings specified by the Alarm_W registers and the Alarm_D registers. The Alarm_W registers allow week, hour, and minute alarm settings including combinations of multiple day-of-week settings such as "Monday, Wednesday, and Friday" and "Saturday and Sunday". The Alarm_D registers allow hour and minute alarm settings. In case of R2221x the Alarm outputs from $\overline{\text{INTR}}$ In case of R2223x the Alarm_W outputs from $\overline{\text{INTRB}}$ pin, and the Alarm_D outputs from $\overline{\text{INTRA}}$ pin. Each alarm function can be checked from the CPU by using a polling function.

- **High-precision Oscillation Adjustment Function**

The R2221x, R2223x has built-in oscillation stabilization capacitors (CG and CD), which can be connected to an external crystal oscillator to configure an oscillation circuit. Two kinds of accuracy for this function are alternatives. To correct deviations in the oscillator frequency of the crystal, the oscillation adjustment circuit is configured to allow correction of a time count gain or loss (up to $\pm$1.5ppm or $\pm$0.5ppm at 25$°$C) from the CPU. The maximum range is approximately $\pm$189ppm (or $\pm$63ppm) in increments of approximately 3ppm (or 1ppm).   Such oscillation frequency adjustment in each system has the following advantages:
* Allows timekeeping with much higher precision than conventional RTCs while using a crystal oscillator with a wide range of precision variations.
* Corrects seasonal frequency deviations through seasonal oscillation adjustment.
* Allows timekeeping with higher precision particularly with a temperature sensing function out of RTC, through oscillation adjustment in tune with temperature fluctuations.

- **Power-on Reset, Oscillation Halt Sensing Function and Supply Voltage Monitoring Function**

The R2221x, R2223x incorporates an oscillation halt sensing circuit equipped with internal registers configured to record any past oscillation halt.
Power on reset function reset the control resisters when the system is powered on from 0V. At the same time, the fact is memorized to the resister as a flag, thereby identifying whether they are powered on from 0V or battery backed-up.
The R2221x, R2223x also incorporates a supply voltage monitoring circuit equipped with internal registers configured to record any drop in supply voltage below a certain threshold value. Supply voltage monitoring threshold is V$_{\text{DET}}$.
The oscillation halt sensing circuit and the power-on reset flag are configured to confirm the established invalidation of time data in contrast to the supply voltage monitoring circuit intended to confirm the potential invalidation of time data. Further, the supply voltage monitoring circuit can be applied to battery supply voltage monitoring.

● Periodic Interrupt Function

The R2221x, R2223x incorporates the periodic interrupt circuit configured to generate periodic interrupt signals aside from interrupt signals generated by the alarm interrupt circuit for output from the $\overline{\text{INTR}}$ (R2221x) or $\overline{\text{INTRA}}$ (R2223x) pin. Periodic interrupt signals have five selectable frequency settings of 2 Hz (once per 0.5 seconds), 1 Hz (once per 1 second), 1/60 Hz (once per 1 minute), 1/3600 Hz (once per 1 hour), and monthly (the first day of every month). Further, periodic interrupt signals also have two selectable waveforms, a normal pulse form (with a frequency of 2 Hz or 1 Hz) and special form adapted to interruption from the CPU in the level mode (with second, minute, hour, and month interrupts). The condition of periodic interrupt signals can be monitored with using a polling function.

● 32kHz Clock Output

The R2221x, R2223x incorporates a 32-kHz clock circuit configured to generate clock pulses with the oscillation frequency of a 32.768kHz crystal oscillator for output from the 32KOUT pin. The 32KOUT pin is CMOS push-pull output and the output is enabled and disabled when the CLKC pin is held high, and low or open, respectively. The 32-kHz clock output can be disabled by certain register settings but cannot be disabled without manipulation of any two registers with different addresses to prevent disabling in such events as the runaway of the CPU. The 32-kHz clock circuit is enabled at power-on, when the CLKC pin is held high.

● ECO mode

In the case that the equivalent series resistance of the crystal oscillator:R1 is small, （approximately, R1 equal or less than 60kΩ to 65kΩ）, by the pin or setting of the resister, ECO mode can be active, and time keeping consumption current can be reduced. ECO mode is realized by pin as for the R2221x, by the resister as for the R2223x. In terms of the R2223x, if the power supply starts up from 0V, ECO mode turns off. If ECO mode is inactive, if the equivalent series resistance of the crystal oscillator: R1 is large, (approximately equal or less than R1=75 kΩ to 80kΩ), it is possible to use with. When the ECO mode is inactive, time keeping current increases a little. And the oscillation frequency might change slightly whether the ECO mode being turned on or turned off.

RICOH

Address Mapping

	Address [A3:A0]	Register Name	Data								Default *7)
			D7	D6	D5	D4	D3	D2	D1	D0	
0	[0000]	Second Counter	-*2)	S40	S20	S10	S8	S4	S2	S1	xxh
1	[0001]	Minute Counter	-	M40	M20	M10	M8	M4	M2	M1	xxh
2	[0010]	Hour Counter	-	-	H20 P/$\overline{A}$	H10	H8	H4	H2	H1	xxh
3	[0011]	Day-of-week Counter	-	-	-	-	-	W4	W2	W1	xxh
4	[0100]	Day-of-month Counter	-	-	D20	D10	D8	D4	D2	D1	xxh
5	[0101]	Month Counter and Century Bit	-	-	-	MO10	MO8	MO4	MO2	MO1	xxh
6	[0110]	Year Counter	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	xxh
7	[0111]	Oscillation Adjustment Register *3)	DEV *4)	F6	F5	F4	F3	F2	F1	F0	00h
8	[1000]	Alarm_W (Minute Register)	-	WM40	WM20	WM10	WM8	WM4	WM2	WM1	xxh
9	[1001]	Alarm_W (Hour Register)	-	-	WH20 WP/$\overline{A}$	WH10	WH8	WH4	WH2	WH1	xxh
A	[1010]	Alarm_W (Day-of-week Register)	-	WW6	WW5	WW4	WW3	WW2	WW1	WW0	xxh
B	[1011]	Alarm_D (Minute Register)	-	DM40	DM20	DM10	DM8	DM4	DM2	DM1	xxh
C	[1100]	Alarm_D (Hour Register)	-	-	DH20 DP/$\overline{A}$	DH10	DH8	DH4	DH2	DH1	xxh
D	[1101]	User RAM	RAM7	RAM6	RAM5	RAM4	RAM3	RAM2	RAM1	RAM0	00h
E	[1110]	Control Register 1 *3)	WALE	DALE	$\overline{12}$/24	$\overline{CLEN2}$	TEST	CT2	CT1	CT0	00h
F	[1111]	Control Register 2 *3)	ECO *6)	VDET	XSTP	PON *5)	$\overline{CLEN1}$	CTFG	WAFG	DAFG	70h

Notes:

* 1) All the data listed above accept both reading and writing.
* 2) The data marked with "-" is invalid for writing and reset to 0 for reading.
* 3) When the PON bit is set to 1 in Control Register 2, all the bits are reset to 0 in Oscillation Adjustment Register, Control Register 1 and Control Register 2 excluding the XSTP bit and VDET bit.
* 4) When DEV=0, the oscillation adjustment circuit is configured to allow correction of a time count gain or loss up to ±1.5ppm. When DEV=1, the oscillation adjustment circuit is configured to allow correction of a time count gain or loss up to or ±0.5ppm.
* 5) PON is a power-on-reset flag.
* 6) R2221x=SCRATCH, R2223x=ECO
* 7) Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt. "xxh" means indifinite.

RICOH

Register Settings

● **Control Register 1 (ADDRESS Eh)**

D7	D6	D5	D4	D3	D2	D1	D0	
WALE	DALE	$\overline{12}$ /24	$\overline{CLEN2}$	TEST	CT2	CT1	CT0	(For Writing)
WALE	DALE	$\overline{12}$ /24	$\overline{CLEN2}$	TEST	CT2	CT1	CT0	(For Reading)
0	0	0	0	0	0	0	0	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

(1) WALE, DALE Alarm_W Enable Bit, Alarm_D Enable Bit

WALE,DALE	Description	
0	Disabling the alarm interrupt circuit (under the control of the settings of the Alarm_W registers and the Alarm_D registers).	(Default)
1	Enabling the alarm interrupt circuit (under the control of the settings of the Alarm_W registers and the Alarm_D registers)	

(2) $\overline{12}$ /24 $\overline{12}$ /24-hour Mode Selection Bit

$\overline{12}$ /24	Description	
0	Selecting the 12-hour mode with a.m. and p.m. indications.	(Default)
1	Selecting the 24-hour mode	

Setting the $\overline{12}$ /24 bit to 0 and 1 specifies the 12-hour mode and the 24-hour mode, respectively.

24-hour mode	12-hour mode	24-hour mode	12-hour mode
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

Setting the $\overline{12}$ /24 bit should precede writing time data

(3) $\overline{CLEN2}$ 32kHz Clock Output Bit 2

$\overline{CLEN2}$	Description	
0	Enabling the 32-kHz clock circuit	(Default)
1	Disabling the 32-kHz clock circuit	

Setting the $\overline{CLEN2}$ bit or the $\overline{CLEN1}$ bit (D3 in the control register 2) to 0, and the CLKC pin to high specifies generating clock pulses with the oscillation frequency of the 32.768-kHz crystal oscillator for output from the 32KOUT pin. Conversely, setting both the $\overline{CLEN1}$ and $\overline{CLEN2}$ bit to 1 or CLKC pin to low specifies disabling ("L") such output.

(4) TEST   Test Bit

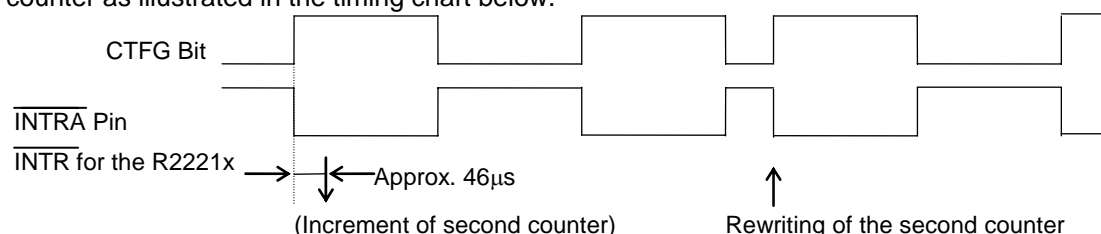| TEST	Description	
0	Normal operation mode.	(Default)
1	Test mode.	

The TEST bit is used only for testing in the factory and should normally be set to 0.

RICOH

(5) CT2, CT1, and CT0   Periodic Interrupt Selection Bits

CT2	CT1	CT0	Description	
			Wave form mode	**Interrupt Cycle and Falling Timing**
0	0	0	-	OFF(H) (Default)
0	0	1	-	Fixed at "L"
0	1	0	Pulse Mode *1)	2Hz (Duty50%)
0	1	1	Pulse Mode *1)	1Hz (Duty50%)
1	0	0	Level Mode *2)	Once per 1 second (Synchronized with second counter increment)
1	0	1	Level Mode *2)	Once per 1 minute (at 00 seconds of every minute)
1	1	0	Level Mode *2)	Once per hour (at 00 minutes and 00 seconds of every hour)
1	1	1	Level Mode *2)	Once per month (at 00 hours, 00 minutes, and 00 seconds of first day of every month)

* 1) Pulse Mode: 2-Hz and 1-Hz clock pulses are output in synchronization with the increment of the second counter as illustrated in the timing chart below.

CTFG Bit

$\overline{\text{INTRA}}$ Pin
$\overline{\text{INTR}}$ for the R2221x →   Approx. 46μs
(Increment of second counter)   Rewriting of the second counter

In the pulse mode, the increment of the second counter is delayed by approximately 46 μs from the falling edge of clock pulses.   Consequently, time readings immediately after the falling edge of clock pulses may appear to lag behind the time counts of the real-time clocks by approximately 1 second.   Rewriting the second counter will reset the other time counters of less than 1 second, driving the $\overline{\text{INTRA}}$ ($\overline{\text{INTR}}$) pin low.

* 2) Level Mode: Periodic interrupt signals are output with selectable interrupt cycle settings of 1 second, 1 minute, 1 hour, and 1 month.   The increment of the second counter is synchronized with the falling edge of periodic interrupt signals.   For example, periodic interrupt signals with an interrupt cycle setting of 1 second are output in synchronization with the increment of the second counter as illustrated in the timing chart below.

CTFG Bit

$\overline{\text{INTRA}}$ Pin

Setting CTFG bit to 0   Setting CTFG bit to 0
(Increment of   (Increment of   (Increment of
second counter)   second counter)   second counter)

At the level mode, the moment right after writing CT2-CT0, $\overline{\text{INTRA}}$ ($\overline{\text{INTR}}$) pin becomes "L" in very short moment. In such a case, ignore it or confirm it by CTFG bit.

*1), *2) When the oscillation adjustment circuit is used, the interrupt cycle will fluctuate once per 20sec. or 60sec. as follows:
Pulse Mode: The "L" period of output pulses will increment or decrement by a maximum of ±3.784 ms. For example, 1-Hz clock pulses will have a duty cycle of 50 ±0.3784%.
Level Mode: A periodic interrupt cycle of 1 second will increment or decrement by a maximum of ±3.784 ms.

● **Control Register 2 (Address Fh)**

D7	D6	D5	D4	D3	D2	D1	D0	
ECO or Scratch	VDET	XSTP	PON	$\overline{\text{CLEN1}}$	CTFG	WAFG	DAFG	(For Writing)
ECO or Scratch	VDET	XSTP	PON	$\overline{\text{CLEN1}}$	CTFG	WAFG	DAFG	(For Reading)
0	1	1	1	0	0	0	0	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

(1) ECO(R2223x),SCRATCH(R2221x)   Oscillation Mode Selection Bit

ECO	Description	
0	.Normal mode	(Default)
1	Low current mode.	

When "1" is written on this bit, the IC mode becomes ultra low consumption current oscillation mode (ECO mode). In terms of the selection of ECO mode, refer to the item "ECO mode" on P.30. This bit is available only for the R2223x. As for the R2221x, "write" and "read" on this bit is possible just same as RAM, but the result has no influence on any function, or SCRATCH bit.

(2) VDET   Supply Voltage Monitoring Result Indication Bit

VDET	Description	
0	Indicating supply voltage above the supply voltage monitoring threshold settings.	
1	Indicating supply voltage below the supply voltage monitoring threshold settings.	(Default)

Once the VDET bit is set to 1, the supply voltage monitoring circuit will be disabled while the VDET bit will hold the setting of 1. The VDET bit accepts only the writing of 0, which restarts the supply voltage monitoring circuit. Conversely, setting the VDET bit to 1 causes no event.

(3) XSTP   Oscillation Halt Sensing Monitor Bit

XSTP	Description	
0	Sensing a normal condition of oscillation	
1	Sensing a halt of oscillation	(Default)

The XSTP bit will be set to "1" when the oscillation halt is detected. Once this bit becomes "1", unless otherwise "0" is written, this bit never return to "0". If "1" is written, nothing will change.

(4) PON   Power-on-reset Flag Bit

PON	Description	
0	Normal condition	
1	Detecting VDD power-on -reset	(Default)

The PON bit is for sensing power-on reset condition.

* The PON bit will be set to 1 when VDD power-on from 0 volt. The PON bit will hold the setting of 1 even after power-on.
* When the PON bit is set to 1, all bits will be reset to 0, in the Oscillation Adjustment Register, Control Regist1, and Control Register 2, except PON,XSTP and VDET . As a result, $\overline{\text{INTRA}}$ and $\overline{\text{INTRB}}$ ($\overline{\text{INTR}}$ for the R2221x) pin stops outputting.
* The PON bit accepts only the writing of 0. Conversely, setting the PON bit to 1 causes no event.

RICOH

(5) $\overline{\text{CLEN1}}$ **32kHz Clock Output Bit 1**

$\overline{\text{CLEN1}}$	Description	
0	Enabling the 32-kHz clock circuit	(Default)
1	Disabling the 32-kHz clock circuit	

Setting the $\overline{\text{CLEN1}}$ bit or the $\overline{\text{CLEN2}}$ bit (D4 in the control register 1) to 0, and the CLKC pin to high specifies generating clock pulses with the oscillation frequency of the 32.768-kHz crystal oscillator for output from the 32KOUT pin. Conversely, setting both the $\overline{\text{CLEN1}}$ and $\overline{\text{CLEN2}}$ bit to 1 or CLKC pin to low specifies disabling ("L") such output.

(6) CTFG   **Periodic Interrupt Flag Bit**

CTFG	Description	
0	Periodic interrupt output = "H"	(Default)
1	Periodic interrupt output = "L"	

The CTFG bit is set to 1 when the periodic interrupt signals are output from the $\overline{\text{INTRA}}$ ($\overline{\text{INTR}}$ for the R2221x) pin ("L"). The CTFG bit accepts only the writing of 0 in the level mode, which disables ("H") the $\overline{\text{INTRA}}$ ($\overline{\text{INTR}}$ for the R2221x) pin until it is enabled ("L") again in the next interrupt cycle. Conversely, setting the CTFG bit to 1 causes no event.

(7) WAFG,DAFG   **Alarm_W Flag Bit and Alarm_D Flag Bit**

WAFG,DAFG	Description	
0	Indicating a mismatch between current time and preset alarm time	(Default)
1	Indicating a match between current time and preset alarm time	

The WAFG and DAFG bits are valid only when the WALE and DALE have the setting of 1, which is caused approximately 15μs after any match between current time and preset alarm time specified by the Alarm_W registers and the Alarm_D registers. The WAFG (DAFG) bit accepts only the writing of 0.
$\overline{\text{INTRA}}$ / $\overline{\text{INTRB}}$ ($\overline{\text{INTR}}$ for the R2221x) pin outputs off ("H") when this bit is set to 0. And $\overline{\text{INTRA}}$ / $\overline{\text{INTRB}}$ ($\overline{\text{INTR}}$ for the R2221x) pin outputs "L" again at the next preset alarm time. Conversely, setting the WAFG and DAFG bits to 1 causes no event. The WAFG and DAFG bits will have the reading of 0 when the alarm interrupt circuit is disabled with the WALE and DALE bits set to 0. The settings of the WAFG and DAFG bits are synchronized with the output of the $\overline{\text{INTRA}}$ / $\overline{\text{INTRB}}$ ($\overline{\text{INTR}}$ for the R2221x) pin as shown in the timing chart below.
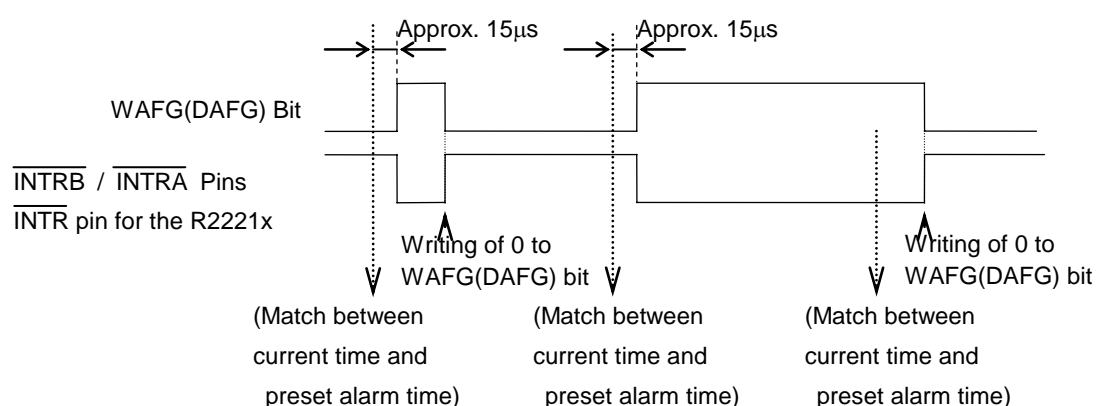
- **Time Counter (Address 0-2h)**

Second Counter (Address 0h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	S40	S20	S10	S8	S4	S2	S1	(For Writing)
0	S40	S20	S10	S8	S4	S2	S1	(For Reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

Minute Counter (Address 1h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	M40	M20	M10	M8	M4	M2	M1	(For Writing)
0	M40	M20	M10	M8	M4	M2	M1	(For Reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

Hour Counter (Address 2h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	P/$\overline{A}$ or H20	H10	H8	H4	H2	H1	(For Writing)
0	0	P/$\overline{A}$ or H20	H10	H8	H4	H2	H1	(For Reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

* Time digit display (BCD format) as follows:
   The second digits range from 00 to 59 and are carried to the minute digit in transition from 59 to 00.
   The minute digits range from 00 to 59 and are carried to the hour digits in transition from 59 to 00.
   The hour digits range as shown in "P12 • Control Register 1 (ADDRESS Eh) (2) $\overline{12}$ /24: $\overline{12}$ /24-hour Mode Selection Bit" and are carried to the day-of-month and day-of-week digits in transition from PM11 to AM12 or from 23 to 00.
* Any writing to the second counter resets divider units of less than 1 second.
* Any carry from lower digits with the writing of non-existent time may cause the time counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent time data.

- **Day-of-week Counter (Address 3h)**

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	W4	W2	W1	(For Writing)
0	0	0	0	0	W4	W2	W1	(For Reading)
0	0	0	0	0	Indefinite	Indefinite	Indefinite	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

* The day-of-week counter is incremented by 1 when the day-of-week digits are carried to the day-of-month digits.
* Day-of-week display (incremented in septimal notation):
   (W4, W2, W1) = (0, 0, 0) → (0, 0, 1)→…→(1, 1, 0) → (0, 0, 0)
* Correspondence between days of the week and the day-of-week digits are user-definable (e.g. Sunday = 0,

RICOH

0, 0)
* The writing of (1, 1, 1) to (W4, W2, W1) is prohibited except when days of the week are unused.

● **Calendar Counter (Address 4-6h)**

Day-of-month Counter (Address 4h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	D20	D10	D8	D4	D2	D1	(For Writing)
0	0	D20	D10	D8	D4	D2	D1	(For Reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

Month Counter + Century Bit (Address 5h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	MO10	MO8	MO4	MO2	MO1	(For Writing)
0	0	0	MO10	MO8	MO4	MO2	MO1	(For Reading)
0	0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

Year Counter (Address 6h)

D7	D6	D5	D4	D3	D2	D1	D0	
Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	(For Writing)
Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	(For Reading)
Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

* The calendar counters are configured to display the calendar digits in BCD format by using the automatic calendar function as follows:
The day-of-month digits (D20 to D1) range from 1 to 31 for January, March, May, July, August, October, and December; from 1 to 30 for April, June, September, and November; from 1 to 29 for February in leap years; from 1 to 28 for February in ordinary years. The day-of-month digits are carried to the month digits in reversion from the last day of the month to 1.   The month digits (MO10 to MO1) range from 1 to 12 and are carried to the year digits in reversion from 12 to 1.
The year digits (Y80 to Y1) range from 00 to 99 (00, 04, 08, …, 92, and 96 in leap years) .
* Any carry from lower digits with the writing of non-existent calendar data may cause the calendar counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent calendar data.

● **Oscillation Adjustment Register (Address 7h)**

D7	D6	D5	D4	D3	D2	D1	D0	
DEV	F6	F5	F4	F3	F2	F1	F0	(For Writing)
DEV	F6	F5	F4	F3	F2	F1	F0	(For Reading)
0	0	0	0	0	0	0	0	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

DEV bit

When DEV is set to 0, the Oscillation Adjustment Circuit operates 00, 20, 40 seconds.

When DEV is set to 1, the Oscillation Adjustment Circuit operates 00 seconds.

F6 to F0 bits

The Oscillation Adjustment Circuit is configured to change time counts of 1 second on the basis of the settings of the Oscillation Adjustment Register at the timing set by DEV.

* The Oscillation Adjustment Circuit will not operate with the same timing (00, 20, or 40 seconds) as the timing of writing to the Oscillation Adjustment Register.

* The F6 bit setting of 0 causes an increment of time counts by $((F5, F4, F3, F2, F1, F0) - 1) \times 2$.

The F6 bit setting of 1 causes a decrement of time counts by $((\overline{F_5}.\overline{F_4}.\overline{F_3}.\overline{F_2}.\overline{F_1}.\overline{F_0}) + 1) \times 2$.

The settings of "*, 0, 0, 0, 0, 0, *" ("*" representing either "0" or "1") in the F6, F5, F4, F3, F2, F1, and F0 bits cause neither an increment nor decrement of time counts.

Example:

If (DEV, F6, F5, F4, F3, F2, F1, F0) is set to (0, 0, 0, 0, 0, 1, 1, 1), when the second digits read 00, 20, or 40, an increment of the current time counts of $32768 + (7 - 1) \times 2$ to 32780 (a current time count loss).

If (DEV, F6, F5, F4, F3, F2, F1, F0) is set to (0, 0, 0, 0, 0, 0, 0, 1), when the second digits read 00, 20, 40, neither an increment nor a decrement of the current time counts of 32768.

If (DEV, F6, F5, F4, F3, F2, F1, F0) is set to (1, 1, 1, 1, 1, 1, 1, 0), when the second digits read 00, a decrement of the current time counts of $32768 + (- 2) \times 2$ to 32764 (a current time count gain).

An increase of two clock pulses once per 20 seconds causes a time count loss of approximately 3 ppm ($2 / (32768 \times 20 = 3.051$ ppm). Conversely, a decrease of two clock pulses once per 20 seconds causes a time count gain of 3 ppm. Consequently, when DEV is set to "0", deviations in time counts can be corrected with a precision of ± 1.5 ppm. In the same way, when DEV is set to "1", deviations in time counts can be corrected with a precision of ± 0.5 ppm. Note that the oscillation adjustment circuit is configured to correct deviations in time counts and not the oscillation frequency of the 32.768-kHz clock pulses. For further details, see "P.33 Configuration of Oscillation Circuit, ECO mode and Correction of Time Count Deviations ● Oscillation Adjustment Circuit".

RICOH

● **Alarm_W Registers (Address 8-Ah)**

Alarm_W Minute Register (Address 8h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	WM40	WM20	WM10	WM8	WM4	WM2	WM1	(For Writing)
0	WM40	WM20	WM10	WM8	WM4	WM2	WM1	(For Reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

Alarm_W Hour Register (Address 9h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	WH20 WP/$\overline{A}$	WH10	WH8	WH4	WH2	WH1	(For Writing)
0	0	WH20 WP/$\overline{A}$	WH10	WH8	WH4	WH2	WH1	(For Reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

Alarm_W Day-of-week Register (Address Ah)

D7	D6	D5	D4	D3	D2	D1	D0	
-	WW6	WW5	WW4	WW3	WW2	WW1	WW0	(For Writing)
0	WW6	WW5	WW4	WW3	WW2	WW1	WW0	(For Reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

* The D5 bit of the Alarm_W Hour Register represents WP/$\overline{A}$ when the 12-hour mode is selected (0 for a.m. and 1 for p.m.) and WH20 when the 24-hour mode is selected (tens in the hour digits).

* The Alarm_W Registers should not have any non-existent alarm time settings.

(Note that any mismatch between current time and preset alarm time specified by the Alarm_W registers may disable the alarm interrupt circuit.)

* When the 12-hour mode is selected, the hour digits read 12 and 32 for 0 a.m. and 0 p.m., respectively. (See "P12 ●Control Register 1 (ADDRESS Eh) (2) $\overline{12}$/24: $\overline{12}$/24-hour Mode Selection Bit")

* WW0 to WW6 correspond to W4, W2, and W1 of the day-of-week counter with settings ranging from (0, 0, 0) to (1, 1, 0).

* WW0 to WW6 with respective settings of 0 disable the outputs of the Alarm_W Registers.

Example of Alarm Time Setting

Alarm Preset alarm time	Day-of-week							12-hour mode				24-hour mode			
	Sun.	Mon.	Tue.	Wed.	Th.	Fri.	Sat.	10 hr.	hr.	10 min.	min.	10 hr.	hr.	10 min.	min.
	WW0	WW1	WW2	WW3	WW4	WW5	WW6								
00:00 a.m. on all days	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
01:30 a.m. on all days	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
11:59 a.m. on all days	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00 p.m. on Mon. to Fri.	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
01:30 p.m. on Sun.	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
11:59 p.m. on Mon., Wed., and Fri.	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

Note that the correspondence between WW0 to WW6 and the days of the week shown in the above table is just an example and not mandatory.

RICOH

● **Alarm_D Register (Address B-Ch)**

Alarm_D Minute Register (Address Bh)

D7	D6	D5	D4	D3	D2	D1	D0	
-	DM40	DM20	DM10	DM8	DM4	DM2	DM1	(For Writing)
0	DM40	DM20	DM10	DM8	DM4	DM2	DM1	(For Reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

Alarm_D Hour Register (Address Ch)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	DH20 DP/$\overline{A}$	DH10	DH8	DH4	DH2	DH1	(For Writing)
0	0	DH20 DP/$\overline{A}$	DH10	DH8	DH4	DH2	DH1	(For Reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

* The D5 bit represents DP/$\overline{A}$ when the 12-hour mode is selected (0 for a.m. and 1 for p.m.) and DH20 when the 24-hour mode is selected (tens in the hour digits).
* The Alarm_D registers should not have any non-existent alarm time settings.
(Note that any mismatch between current time and preset alarm time specified by the Alarm_D registers may disable the alarm interrupt circuit.)
* When the 12-hour mode is selected, the hour digits read 12 and 32 for 0a.m. and 0p.m., respectively.
(See "P.12 ●Control Register 1 (ADDRESS Eh) (2) $\overline{12}$ /24: $\overline{12}$ /24-hour Mode Selection Bit")

● **User RAM(Address Dh)**

D7	D6	D5	D4	D3	D2	D1	D0	
RAM7	RAM6	RAM5	RAM4	RAM3	RAM2	RAM1	RAM0	(For Writing)
RAM7	RAM6	RAM5	RAM4	RAM3	RAM2	RAM1	RAM0	(For Reading)
0	0	0	0	0	0	0	0	Default Settings *)

*) Default settings: Default value means read / written values when the PON bit is set to "1" due to VDD power-on from 0 volt.

RAM7-RAM0 bit accepts the reading and writing of 0 and 1.

RICOH

Interfacing with the CPU

The R2221x, R2223x employs the I2C-Bus system to be connected to the CPU via 2-wires. Connection and system of I2C-Bus are described in the following sections.

● **Connection of I2C-Bus**

2-wires, SCL and SDA pins that are connected to I2C-Bus are used for transmit clock pulses and data respectively. All ICs that are connected to these lines are designed that will not be clamped when a voltage beyond supply voltage is applied to input or output pins. Open drain pins are used for output. This construction allows communication of signals between ICs with different supply voltages by adding a pull-up resistor to each signal line as shown in the figure below. Each IC is designed not to affect SCL and SDA signal lines when power to each of these is turned off separately.
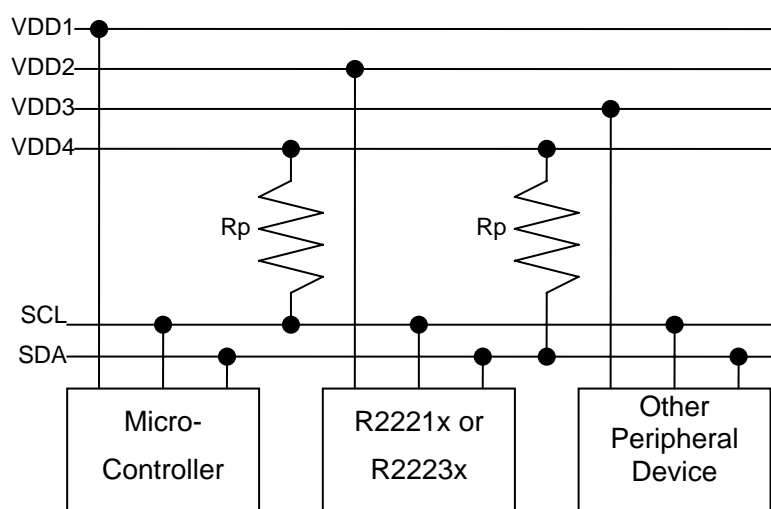
* For data interface, the following conditions must be met:
VCC4≥VCC1
VCC4≥VCC2
VCC4≥VCC3

* When the master is one, the micro-controller is ready for driving SCL to "H" and Rp of SCL may not be required.

Cautions on determining Rp resistance,
(1) Dropping voltage at Rp due to sum of input current or output current at off conditions on each IC pin connected to the I2C-Bus shall be adequately small.
(2) Rising time of each signal be kept short even when all capacity of the bus is driven.
(3) Current consumed in I2C-Bus is small compared to the consumption current permitted for the entire system.

When all ICs connected to I2C-Bus are CMOS type, condition (1) may usually be ignored since input current and off-state output current is extremely small for the many CMOS type ICs. Thus the maximum resistance of Rp may be determined based on (2), while the minimum on (3) in most cases.
In actual cases a resistor may be place between the bus and input/output pins of each IC to improve noise margins in which case the Rp minimum value may be determined by the resistance.
Consumption current in the bus to review (3) above may be expressed by the formula below:

Bus consumption current ≈

$$\frac{\text{(Sum of input current and off state output current of all devices in standby mode)} \times \text{Bus standby duration}}{\text{Bus stand-by duration + the Bus operation duration}}$$

$$+\frac{\text{Supply voltage} \times \text{Bus operation duration} \times 2}{\text{Rp resistance} \times 2 \times \text{(Bus stand-by duration + bus operation duration)}}$$

+ Supply voltage × Bus capacity × Charging/Discharging times per unit time

Operation of "× 2" in the second member denominator in the above formula is derived from assumption that "L"

RICOH

21

duration of SDA and SCL pins are the half of bus operation duration. "× 2" in the numerator of the same member is because there are two pins of SDA and SCL. The third member, (charging/discharging times per unit time) means number of transition from "H" to "L" of the signal line.

Calculation example is shown below:
Pull-up resistor (Rp) = 2kΩ, Bus capacity = 50pF(both for SCL, SDA), V_{DD}=3V,
In a system with sum of input current and off-state output current of each pin = 0.1μA,
I^2C-Bus is used for 10ms every second while the rest of 990ms in the stand-by mode,
In this mode, number of transitions of the SCL pin from "H" to "L" state is 100 while SDA 50, every second.

$$\text{Bus consumption current} \approx \frac{0.1\mu A \times 990msec}{990msec + 10msec}$$

$$+ \frac{3V \times 10msec \times 2}{2K\Omega \times 2 \times (990msec + 10msec)}$$

$$+ 3V \times 50pF \times (100 + 50)$$

$$\approx 0.099\mu A + 15.0\mu A + 0.0225\mu A \approx 15.12\mu A$$

Generally, the second member of the above formula is larger enough than the first and the third members bus consumption current may be determined by the second member is many cases.

RICOH

● **Transmission System of I²C-Bus**

(1) Start Condition and Stop Condition

In I²C-Bus, SDA must be kept at a certain state while SCL is at the "H" state during data transmission as shown below.
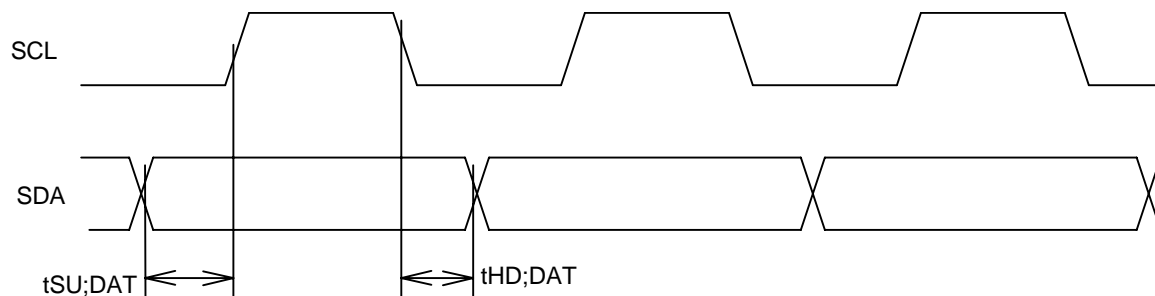
The SCL and SDA pins are at the "H" level when no data transmission is made. Changing the SDA from "H" to "L" when the SCL and the SDA are "H" activates the Start Condition and access is started. Changing the SDA from "L" to "H" when the SCL is "H" activates Stop Condition and accessing stopped. Generation of Start and Stop Conditions is always made by the master (see the figure below).
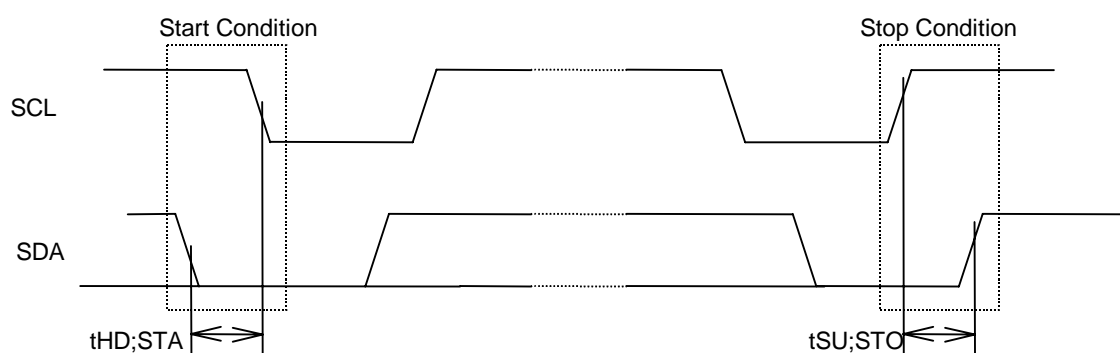
(2) Data transmission and its acknowledge

After Start condition is entered, data is transmitted by 1byte (8bits).   Any bytes of data may be serially transmitted. The receiving side will send an acknowledge signal to the transmission side each time 8bit data is transmitted. The acknowledge signal is sent immediately after falling to "L" of SCL 8bit clock pulses of data is transmitted, by releasing the SDA by the transmission side that has asserted the bus at that time and by turning SDA to "L" by receiving side.   When transmission of 1byte data next to preceding 1byte of data is received the receiving side releases the SDA pin at falling edge of the SCL 9bit of clock pulses or when the receiving side switches to the transmission side it starts data transmission.   When the master is receiving side, it generates no acknowledge signal after last 1byte of data from the slave to tell the transmitter that data transmission has completed.   The slave side (transmission side) continues to release the SDA pin so that the master will be able to generate Stop Condition, after falling edge of the SCL 9bit of clock pulses.

RICOH
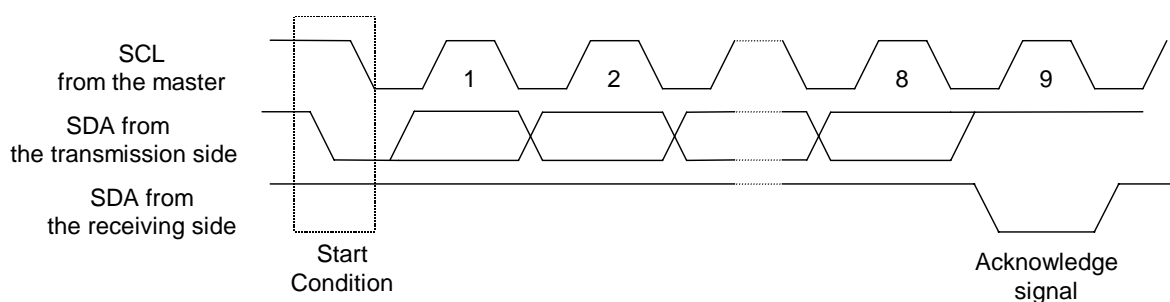
(3) Data Transmission Format in I²C-Bus

I²C-Bus has no chip enable signal line.   In place of it, each device has a 7bit Slave Address allocated. The first 1byte is allocated to this 7bit address and to the command (R/W) for which data transmission direction is designated by the data transmission thereafter.   7bit address is sequentially transmitted from the MSB and 2 and after bytes are read, when 8bit is "H" and when write "L".

The Slave Address of the R2221x, R2223x is specified at (0110010).

At the end of data transmission / receiving, Stop Condition is generated to complete transmission. However, if start condition is generated without generating Stop Condition, Repeated Start Condition is met and transmission / receiving data may be continue by setting the Slave Address again. Use this procedure when the transmission direction needs to be change during one transmission.

Data is written to the slave from the master

| S | Slave Address | 0 | A | | Data | | A | | Data | | A | P |

(0110010)   R/W=0(Write)
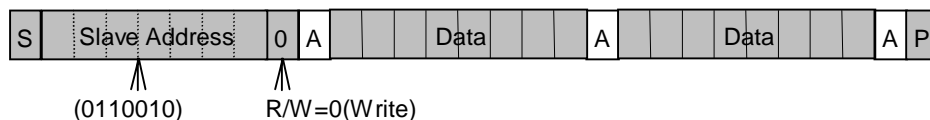
When data is read from the slave immediately after 7bit addressing from the master

| S | Slave Address | 1 | A | | Data | | A | | Data | | /A | P |

(0110010)   R/W=1(Read)

Inform read has been completed by not generate an acknowledge signal to the slave side.
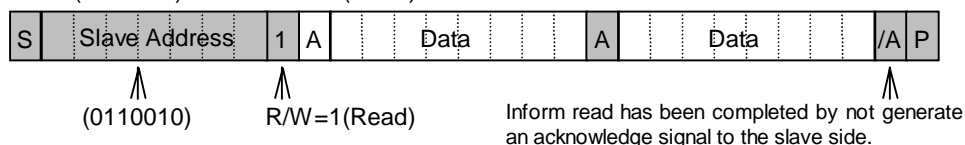
When the transmission direction is to be changed during transmission.
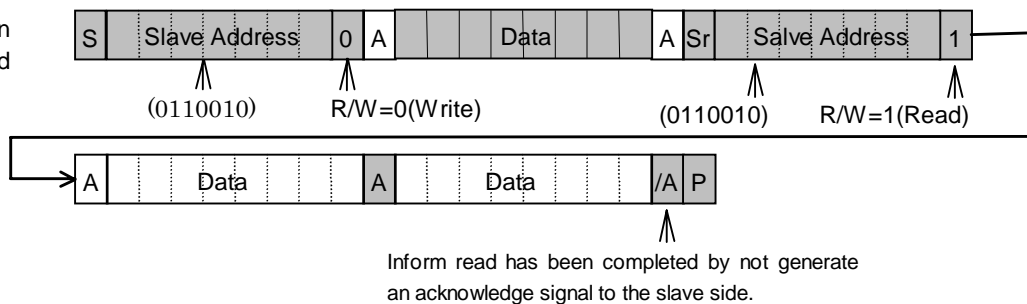
| S | Slave Address | 0 | A | | Data | | A | Sr | Salve Address | 1 |

(0110010)   R/W=0(Write)   (0110010)   R/W=1(Read)

| A | | Data | | A | | Data | | /A | P |

Inform read has been completed by not generate an acknowledge signal to the slave side.

| ▦ Master to slave | □ Slave to master | A A /A Acknowledge Signal |
| S Start Condition | P Stop Condition | Sr Repeated Start Condition |

RICOH

(4) Data Transmission Write Format in the R2221x, R2223x

Although the I²C-Bus standard defines a transmission format for the slave allocated for each IC, transmission method of address information in IC is not defined. The R2221x, R2223x transmits data the internal address pointer (4bit) and the Transmission Format Register (4bit) at the 1byte next to one which transmitted a Slave Address and a write command. For write operation only one transmission format is available and (0000) is set to the Transmission Format Register. The 3byte transmits data to the address specified by the internal address pointer written to the 2byte. Internal address pointer setting are automatically incremented for 4byte and after. Note that when the internal address pointer is Fh, it will change to 0h on transmitting the next byte.

Example of data writing (When writing to internal address Eh to Fh)

R/W=0(Write)

| S | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | A | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | A | Data | A | Data | A | P |

Slave Address	Address	Transmission	Writing of data to the	Writing of data to the
←(0110010)	Pointer	Format	internal address Eh	internal address Fh
	←Eh	Register ←		
		0h		

	Master to slave		Slave to master
S	Start Condition	P	Stop Condition
A A /A	Acknowledge signal		

RICOH

25
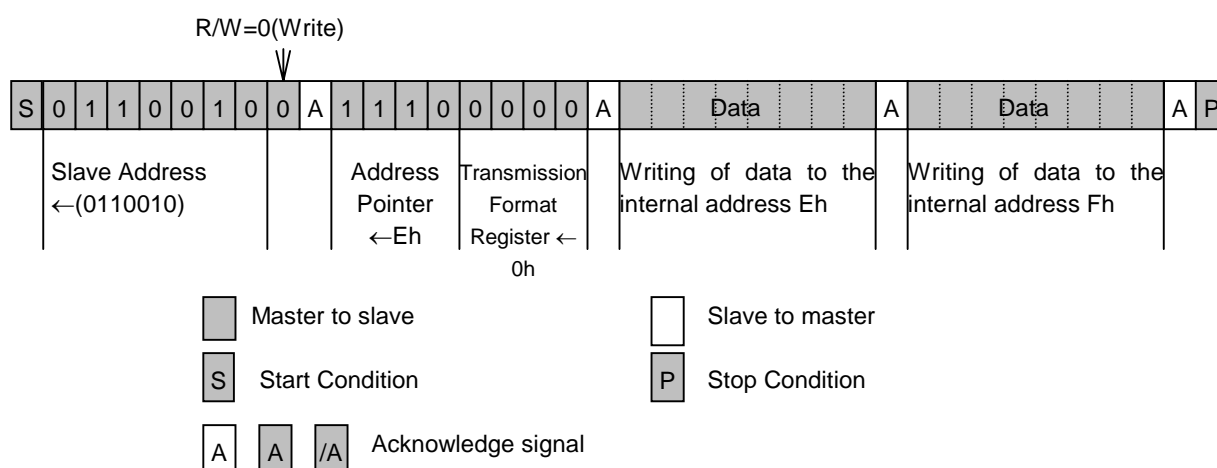
(5) Data transmission read format of the R2221x, R2223x

The R2221x, R2223x allows the following three read out method of data an internal register.

The first method to reading data from the internal register is to specify an internal address by setting the internal address pointer and the transmission format register described P25 (4), generate the Repeated Start Condition (See P24 (3)) to change the data transmission direction to perform reading. The internal address pointer is set to Fh when the Stop Condition is met. Therefore, this method of reading allows no insertion of Stop Condition before the Repeated Start Condition. Set 0h to the Transmission Format Register when this method used.

Example 1 of Data Read (when data is read from 2h to 4h)

RICOH
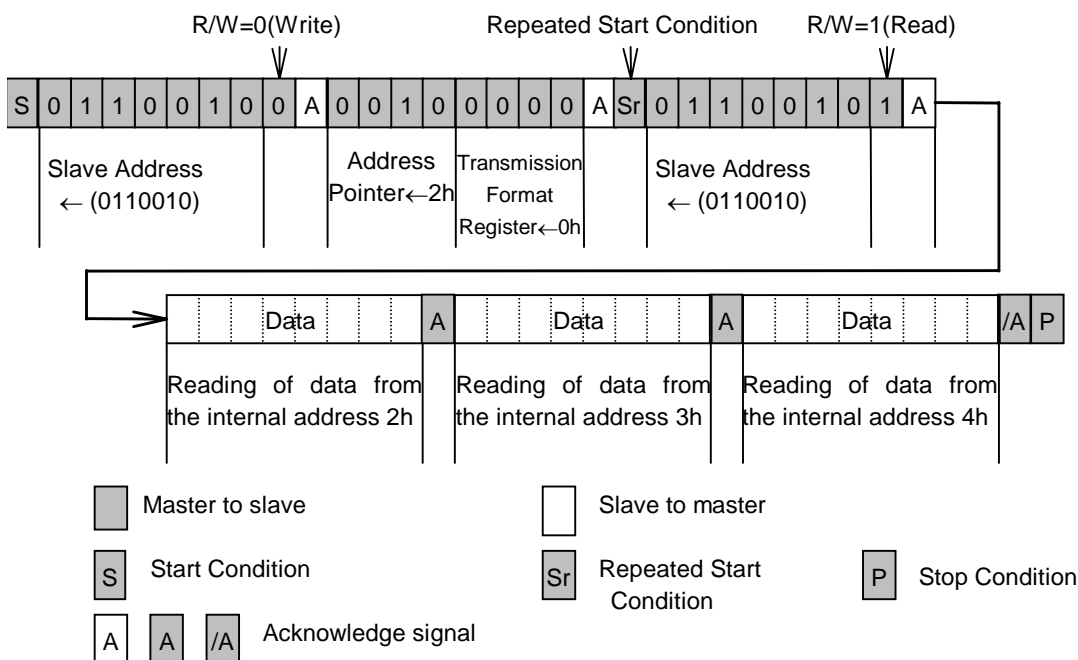
The second method to reading data from the internal register is to start reading immediately after writing to the Internal Address Pointer and the Transmission Format Register. Although this method is not based on I²C-Bus standard in a strict sense it still effective to shorten read time to ease load to the master. Set 4h or 5h to the transmission format register when this method used.

Example 2 of data read (when data is read from internal addresses Eh to 1h)

R/W=0(Write)

S	0	1	1	0	0	1	0	0	A	1	1	1	0	0	1	0	X	A	Data	A

| Slave Address ← (0110010) | | Address Pointer ←Eh | Transmission Format Register←4h or 5h | Reading of data from the internal address Eh |

Data	A	Data	A	Data	/A	P

| Reading of data from the internal address Fh | Reading of data from the internal address 0h | Reading of data from the internal address 1h |

▨	Master to slave	□	Slave to Master
S	Start Condition	P	Stop Condition
A A /A	Acknowledge Signal		

The third method to reading data from the internal register is to start reading immediately after writing to the Slave Address and R/W bit. Since the Internal Address Pointer is set to Fh by default as described in the first method, this method is only effective when reading is started from the Internal Address Fh.

Example 3 of data read (when data is read from internal addresses Fh to 3h)

R/W=1(Read)

S	0	1	1	0	0	1	0	1	A	Data	A	Data	A

| Slave Address ← (0110010) | | Reading of data from the Internal Address Fh | Reading of data from the Internal Address 0h |

Data	A	Data	A	Data	/A	P

| Reading of data from the Internal Address 1h | Reading of data from the Internal Address 2h | Reading of data from the Internal Address 3h |

▨	Master to slave	□	Slave to master
S	Start Condition	P	Stop Condition
A A /A	Acknowledge Signal		

RICOH
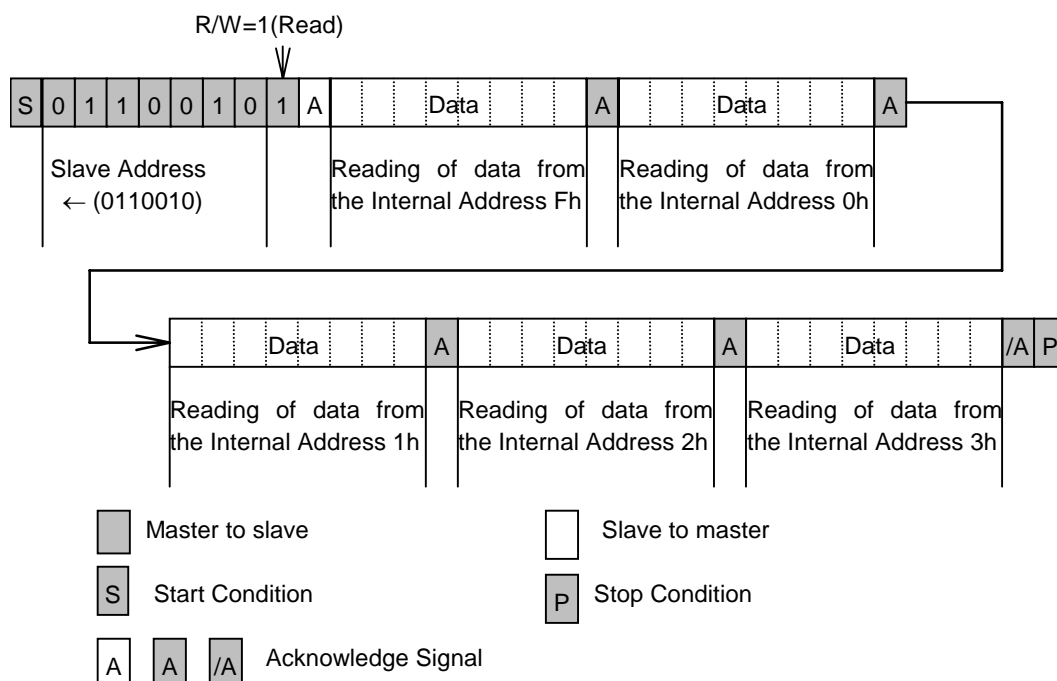
● **Data Transmission under Special Condition**

The R2221x, R2223x holds the clock tentatively for duration from Start Condition to avoid invalid read or write clock on carrying clock. When clock carried during this period, which will be adjusted within approx. 31µs from Stop Condition. To prevent invalid read or write, clock and calendar data shall be made during one transmission operation (from Start Condition to Stop Condition). When 0.5 to 1.0 second elapses after Start Condition, any access to the R2221x, R2223x is automatically released to release tentative hold of the clock, and access from the CPU is forced to be terminated (The same action as made Stop Condition is received: automatic resume function from I²C-Bus interface). Therefore, one access must be complete within 0.5 seconds. The automatic resume function prevents delay in clock even if SCL is stopped from sudden failure of the system during clock read operation.

Also a second Start Condition after the first Start Condition and before the Stop Condition is regarded "Repeated Start Condition". Therefore, when 0.5 seconds passed after the first Start Condition, an access to the R2221x, R2223x is automatically released.

If access is tried after automatic resume function is activated, no acknowledge signal will be output for writing while FFh will be output for reading.

The user shall always be able to access the real-time clock as long as three conditions are met.

No Stop Condition shall be generated until clock and calendar data read/write is started and completed.

One cycle read/write operation shall be complete within 0.5 seconds.

Do not make Start Condition within 31µs from Stop Condition. When clock is carried during the access, which will be adjusted within approx. 31µs from Stop Condition.

Bad example of reading from seconds to hours (invalid read)

(Start Condition) → (Read of seconds) → (Read of minutes) → (Stop Condition) → (Start Condition) → (Read of hour) → (Stop Condition)

Assuming read was started at 05:59:59 P.M. and while reading seconds and minutes the time advanced to 06:00:00 P.M. At this time second digit is hold so read the read as 05:59:59. Then the R2221x, R2223x confirms (Stop Condition) and carries second digit being hold and the time change to 06:00:00 P.M. Then, when the hour digit is read, it changes to 6. The wrong results of 06:59:59 will be read.

RICOH

Configuration of Oscillation Circuit, ECO mode, and Correction of Time Count Deviations

● **Configuration of Oscillation Circuit**
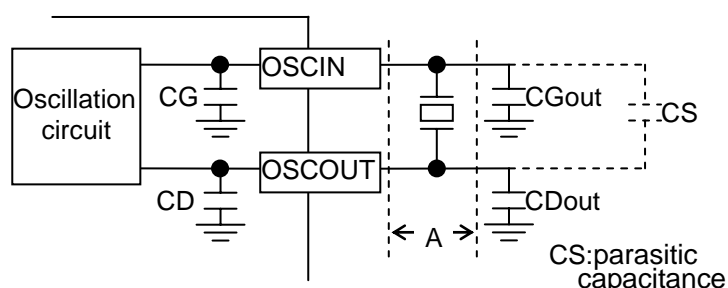
Typical externally-equipped element
X'tal : 32.768kHz
ECO mode OFF: Max. R1 up to 80kΩ
ECO mode ON : Max. R1 up to 65kΩ
CL=6 to 12.5pF
CGOUT＝CDOUT＝0pF
Standard values of internal elements
CG, CD 10pF typ.

The oscillation circuit is driven at a constant voltage of approximately 0.9 volts relative to the level of the VSS pin input.   As such, it is configured to generate an oscillating waveform with a peak-to-peak voltage on the order of 0.9 volts on the positive side of the VSS pin input.

< Considerations in Handling quartz crystal unit >
Generally, quartz crystal units have basic characteristics including an equivalent series resistance (R1) indicating the oscillation margin and a load capacitance (CL) indicating the degree of their center frequency. Particularly, recommended characteristics of quartz crystal units intended for use in the R2221x, R2223x are as follows:
   (1) Max. R1 is up to 80kΩ. (ECO mode: off) or up to 65kΩ (ECO mode: on)
   (2) CL value of 6 to 8pF.
The stability of quarts crystal units' oscillation depends on a parasitic capacitance of the circuit board (CS shown in the figure above.) and external oscillator capacitors. (CGout, CDout shown in the figure above.)
Especially, in terms of R1 and CL, to confirm these recommended values, contact the manufacturers of quartz crystal units intended for use in these particular models to make them matching error evaluation and decide the appropriate values. We recommend CL value of 6 to 8pF,but a case that CL value is more than 8pF use the oscillation adjustment circuit (see " P.33   ● Oscillation Adjustment Circuit").

< Considerations in Installing Components around the Oscillation Circuit >
1) Install the quartz crystal unit in the closest possible vicinity to the real-time clock ICs.
2) Avoid laying any signal lines or power lines in the vicinity of the oscillation circuit (particularly in the area marked "A" in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN and OSCOUT pins and the printed circuit board.
4) Avoid using any long parallel lines to wire the OSCIN and OSCOUT pins.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

< Other Relevant Considerations >
1) We cannot recommend connecting the external input of 32.768-kHz clock pulses to the OSCIN pin.
2) To maintain stable characteristics of the quartz crystal unit, avoid driving any other IC through 32.768-kHz clock pulses output from the OSCOUT pin.

● **Measurement of Oscillation Frequency**
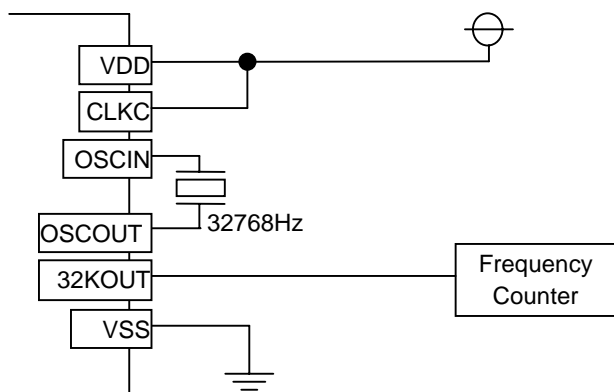
* 1) The R2221x, R2223x is configured to generate 32.768-kHz clock pulses for output from the 32KOUT pin.

* 2) A frequency counter with 6 (more preferably 7) or more digits on the order of 1ppm is recommended for use in the measurement of the oscillation frequency of the oscillation circuit.

● **ECO mode**

In the R2223x, by writing "1" on ECO bit, the IC becomes into ECO mode or, time keeping operation at ultra low power consumption is realized. As for R2221x, by setting the ECO pin to "L", the IC becomes into ECO mode. If ECO mode is necessary, consider the conditions shown below, and confirm the oscillation margin by matching evaluation.

  1) The maximum R1 of the quarts crystal units must be up to 65kΩ.

  2) Do not set external capacitances (CGout/CDout) between OSCIN-VSS and OSCOUT-VSS. Consider the PCB layout to reduce the parasitic capacitance. Especially, if signal lines of OSCIN/OSCOUT are crossed over the multi-layer PCB, bad effect may occur to the operation.

If the R1 of the quartz crystal unit is larger than 65kΩ, turn off ECO mode, and as for the R2223x, to fix the mode off, write "0" to the ECO bit in case of the power supply turns on from 0V and in case of setting time.

<R1 (Equivalent Series Resistance) of quartz crystal units and supply current>

In terms of the time keeping current of R2221x and R2223x is relevant with the R1 (equivalent series resistance) of quartz crystal units. If R1 value is large, the loss becomes also large, as a result, time keeping current may increase. The relation between R1 and time keeping current, refer to the typical characteristics on p. 44.

<ECO mode/ Normal Mode/ Boost Mode>

There are three types of oscillation mode of quartz crystal units with R2221x and R2223x.

ECO mode: Time keeping current decreases extremely.

Normal mode (ECO mode "off"): Time keeping current becomes normal or larger than time keeping current of ECO mode.

Boost mode: At initial power-on (PON=1), or when the quartz crystal oscillation stops (XSTP=1), the oscillation circuit of quartz crystal unit is boosted and the oscillation starting time becomes fast.
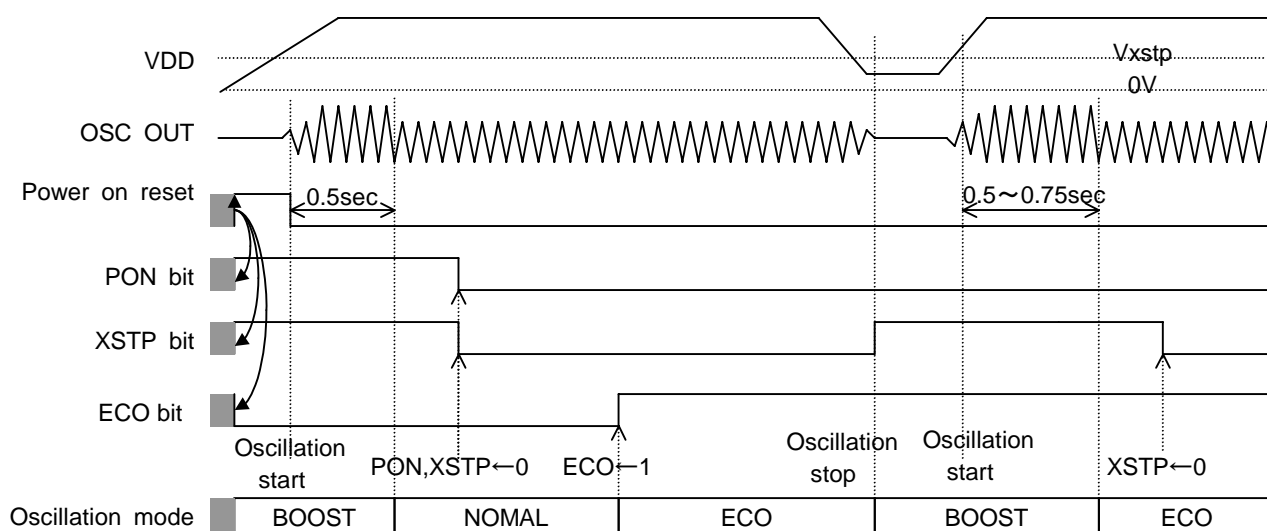
RICOH

| Oscillation mode | BOOST | NOMAL | ECO | BOOST | ECO |

*) The power on reset shown above is an internal signal and the signal is generated from right after the VDD turns on until the oscillation of quartz crystal unit starts. While the term of the power-on reset signal is out, or the time until the oscillation of quarts crystal unit starts, approximately 0.1s to 1.0s, access of I2C bus is impossible.

● **Adjustment of Oscillation frequency**

The oscillation frequency of the oscillation circuit can be adjusted by varying procedures depending on the usage of Model R2221x, R2223x in the system into which they are to be built and on the allowable degree of time count errors. The flow chart below serves as a guide to selecting an optimum oscillation frequency adjustment procedure for the relevant system.
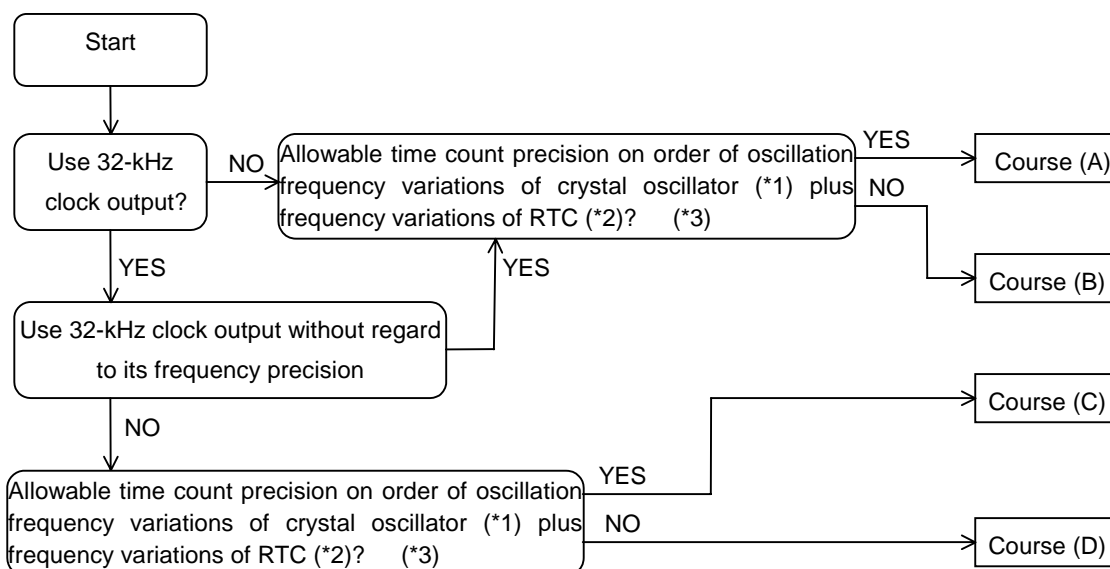
* 1) Generally, quartz crystal units for commercial use are classified in terms of their center frequency depending on their load capacitance (CL) and further divided into ranks on the order of ±10, ±20, and ±50ppm depending on the degree of their oscillation frequency variations.

* 2) Basically, Model R2221x, R2223x is configured to cause frequency variations on the order of ±5 to ±10ppm at 25°C.

* 3) Time count precision as referred to in the above flow chart is applicable to normal temperature and actually affected by the temperature characteristics and other properties of quartz crystal units.

RICOH

Course (A)

When the time count precision of each RTC is not to be adjusted, the quartz crystal unit intended for use in that RTC may have any CL value requiring no presetting. The quartz crystal unit may be subject to frequency variations which are selectable within the allowable range of time count precision. Several quartz crystal units and RTCs should be used to find the center frequency of the quartz crystal units by the method described in "P.30 • Measurement of Oscillation Frequency" and then calculate an appropriate oscillation adjustment value by the method described in "P.33 • Oscillation Adjustment Circuit" for writing this value to the R2221x, R2223x.

Course (B)

When the time count precision of each RTC is to be adjusted within the oscillation frequency variations of the quartz crystal unit plus the frequency variations of the real-time clock ICs, it becomes necessary to correct deviations in the time count of each RTC by the method described in " P.33 • Oscillation Adjustment Circuit". Such oscillation adjustment provides quartz crystal units with a wider range of allowable settings of their oscillation frequency variations and their CL values. The real-time clock IC and the quartz crystal unit intended for use in that real-time clock IC should be used to find the center frequency of the quartz crystal unit by the method described in " P.30 • Measurement of Oscillation Frequency" and then confirm the center frequency thus found to fall within the range adjustable by the oscillation adjustment circuit before adjusting the oscillation frequency of the oscillation circuit. At normal temperature, the oscillation frequency of the oscillator circuit can be adjusted by up to approximately ±0.5ppm.

Course (C)

Course (C) together with Course (D) requires adjusting the time count precision of each RTC as well as the frequency of 32.768-kHz clock pulses output from the 32KOUT pin. Normally, the oscillation frequency of the crystal oscillator intended for use in the RTCs should be adjusted by adjusting the oscillation stabilizing capacitors CG and CD connected to both ends of the crystal oscillator. The R2221x, R2223x, which incorporate the CG and the CD, require adjusting the oscillation frequency of the crystal oscillator through its CL value.

Generally, the relationship between the CL value and the CG and CD values can be represented by the following equation:

$CL = (CG \times CD)/(CG + CD) + CS$ where "CS" represents the floating capacity of the printed circuit board.

The crystal oscillator intended for use in the R2221x, R2223x is recommended to have the CL value on the order of 6 to 8pF. Its oscillation frequency should be measured by the method described in " P.30 • Measurement of Oscillation Frequency ". Any crystal oscillator found to have an excessively high or low oscillation frequency (causing a time count gain or loss, respectively) should be replaced with another one having a smaller and greater CL value, respectively until another one having an optimum CL value is selected. In this case, the bit settings disabling the oscillation adjustment circuit (see " P.33 • Oscillation Adjustment Circuit") should be written to the oscillation adjustment register.

Incidentally, the high oscillation frequency of the crystal oscillator can also be adjusted by adding an external oscillation stabilization capacitor CGOUT or/and CDOUT as illustrated in the diagram below.
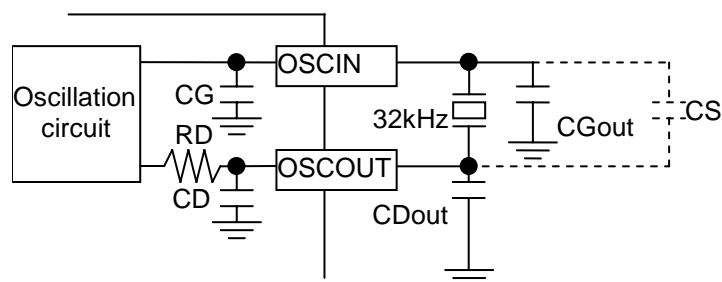
*1) The CGOUT or/and CDOUT should have a capacitance ranging from 0 to 6 pF.
(Including parasitic capacitance of the printed circuit board)

RICOH

However, if adding CGOUT and/or CDOUT, Time keeping Voltage and Current will be worse, and it will be hard to oscillate. For reference, the data of Time keeping voltage and current when adding CGOUT=CDOUT=5pF are shown in the table below.

(Topt=-40 to 85°C, Vss=0v)

PIN	Item	Condition	Min.	TYP.	MAX.	UNITS
Vclk	Time Keeping Voltage (ECO mode =OFF)	CGout=CDout=5pF R1 of quartz crystal unit=55kΩ	(1.1)		5.5	V
I_{DD}	Time Keeping Current (ECO mode =OFF)	V_{DD}=3V, SCL, SDA, CLKC=0V 32KOUT=OPEN OUTPUT=OPEN CGout=CDout=5pF R1 of quartz crystal unit=55kΩ		0.35	(1.0)	μA

Course (D)

It is necessary to select the crystal oscillator in the same manner as in Course (C) as well as correct errors in the time count of each RTC in the same manner as in Course (B) by the method described in " P.33 • Oscillation Adjustment Circuit ".

• Oscillation Adjustment Circuit

The oscillation adjustment circuit can be used to correct a time count gain or loss with high precision by varying the number of 1-second clock pulses once per 20 seconds or 60 seconds. When DEV bit in the Oscillation Adjustment Register is set to 0, R2221x,R2223x varies number of 1-second clock pulses once per 20 seconds. When DEV bit is set to 1, R2221x,R2223x varies number of 1-second clock pulses once per 60 seconds. The oscillation adjustment circuit can be disabled by writing the settings of "*, 0, 0, 0, 0, 0, *" ("*" representing "0" or "1") to the F6, F5, F4, F3, F2, F1, and F0 bits in the oscillation adjustment circuit. Conversely, when such oscillation adjustment is to be made, an appropriate oscillation adjustment value can be calculated by the equation below for writing to the oscillation adjustment circuit.

(1) When Oscillation Frequency (* 1) Is Higher Than Target Frequency (* 2) (Causing Time Count Gain)

When DEV=0:

Oscillation adjustment value (*3) = $\dfrac{\text{(Oscillation frequency - Target Frequency + 0.1)}}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$

≈ (Oscillation Frequency – Target Frequency) × 10 + 1

When DEV=1:

Oscillation adjustment value (*3) = $\dfrac{\text{(Oscillation frequency - Target Frequency + 0.0333)}}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$

≈ (Oscillation Frequency – Target Frequency) × 30 + 1

* 1) Oscillation frequency:

Frequency of clock pulse output from the 32KOUT pin at normal temperature in the manner described in " P30 • Measurement of Oscillation Frequency".

* 2) Target frequency:

Desired frequency to be set. Generally, a 32.768-kHz quartz crystal unit has such temperature characteristics as to have the highest oscillation frequency at normal temperature. Consequently, the quartz crystal unit is recommended to have target frequency settings on the order of 32.768 to 32.76810 kHz (+3.05ppm relative to 32.768 kHz). Note that the target frequency differs depending on the environment or location where the equipment incorporating the RTC is expected to be operated.

* 3) Oscillation adjustment value:

Value that is to be finally written to the F0 to F6 bits in the Oscillation Adjustment Register and is

represented in 7-bit coded decimal notation.

(2) When Oscillation Frequency Is Equal To Target Frequency (Causing Time Count neither Gain nor Loss)

Oscillation adjustment value = 0, +1, -64, or –63

(3) When Oscillation Frequency Is Lower Than Target Frequency (Causing Time Count Loss)

When DEV=0:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\approx (\text{Oscillation Frequency – Target Frequency}) \times 10$$

When DEV=1:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$$

$$\approx (\text{Oscillation Frequency – Target Frequency}) \times 30$$

Oscillation adjustment value calculations are exemplified below

(A) For an oscillation frequency = 32768.85Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = (32768.85 - 32768.05 + 0.1) / (32768.85 \times 3.051 \times 10^{-6})$$

$$\approx (32768.85 - 32768.05) \times 10 + 1$$

$$= 9.001 \approx 9$$

In this instance, write the settings (DEV,F6,F5,F4,F3,F2,F1,F0)=(0,0,0,0,1,0,0,1) in the oscillation adjustment register.   Thus, an appropriate oscillation adjustment value in the presence of any time count gain represents a distance from 01h.

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = (32768.85 - 32768.05 + 0.0333) / (32768.85 \times 1.017 \times 10^{-6})$$

$$\approx (32768.85 - 32768.05) \times 30 + 1$$

$$= 25.00 \approx 25$$

In this instance, write the settings (DEV,F6,F5,F4,F3,F2,F1,F0)=(1,0,0,1,1,0,0,1) in the oscillation adjustment register.

(B) For an oscillation frequency = 32762.22Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = (32762.22 - 32768.05) / (32762.22 \times 3.051 \times 10^{-6})$$

$$\approx (32762.22 - 32768.05) \times 10$$

$$= -58.325 \approx -58$$

To represent an oscillation adjustment value of - 58 in 7-bit coded decimal notation, subtract 58 (3Ah) from 128 (80h) to obtain 46h.   In this instance, write the settings of (DEV,F6,F5,F4,F3,F2,F1,F0) = (0,1,0,0,0,1,1,0) in the oscillation adjustment register.   Thus, an appropriate oscillation adjustment value in the presence of any time count loss represents a distance from 80h.

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = (32762.22 - 32768.05) / (32762.22 \times 1.017 \times 10^{-6})$$

$$\approx (32762.22 - 32768.05) \times 30$$

$$= -174.97 \approx -175$$

Oscillation adjustment value can be set from -62 to 63.   Then, in this case, Oscillation adjustment value is out of range.

RICOH

(4) Difference between DEV=0 and DEV=1

Difference between DEV=0 and DEV=1 is following,

	DEV=0	DEV=1
Maximum value range	-189.2ppm to 189.2ppm	--62ppm to 63ppm
Minimum resolution	3ppm	1ppm

● **How to evaluate the clock gain or loss**

The oscillator adjustment circuit is configured to change time counts of 1 second on the basis of the settings of the oscillation adjustment register once in 20 seconds or 60 seconds. The oscillation adjustment circuit does not effect the frequency of 32768Hz-clock pulse output from the 32KOUT pin. Therefore, after writing the oscillation adjustment register, we cannot measure the clock error with probing 32KOUT clock pulses. The way to measure the clock error as follows:

(1) Output a 1Hz clock pulse of Pulse Mode from the interrupt pin
Set (xxxx0011) to Control Register 1 at address Eh, then 1Hz clock with 50% duty is output from $\overline{\text{INTRA}}$ pin. ($\overline{\text{INTR}}$ pin for R2221x)

 After setting the oscillation adjustment register, 1Hz clock period changes every 20seconds(DEV=0) or every 60 seconds (DEV=1) like next page figure.
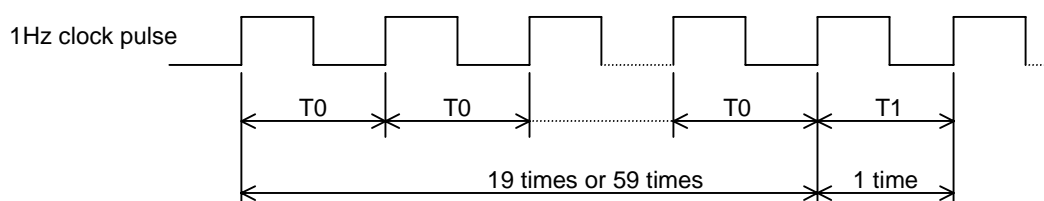
Measure the interval of T0 and T1 with frequency counter. A frequency counter with 7 or more digits is recommended for the measurement.

(2) Calculate the typical period from T0 and T1
   DEV=0
   T = (19×T0+1×T1)/20
   DEV=1
   T = (59×T0+1×T1)/60
Calculate the time error from T.

This method is used at the evaluation stage, however, at the mass production stage, the method is time-consuming and impractical. To confirm the result in a short time, the operation may be complicated, but time error adjustment is digital-wise. Therefore, the time gain and the loss can be estimated precisely by the calculation of 32K clock frequency and adjustment value.

Power-on Reset, Oscillation Halt Sensing, and Supply Voltage Monitoring

The power-on reset circuit is configured to reset control register1, 2, and clock adjustment register when VDD power up from 0v. The oscillation halt sensing circuit is configured to record a halt on oscillation by 32.768kHz clock pulses. The supply voltage monitoring circuit is configured to record a drop in supply voltage below a threshold voltage (V_{DET})

Each function has a monitor bit. For example, the PON bit is for the power-on reset circuit, and XSTP bit is for the oscillation halt sensing circuit, and VDET is for the supply voltage monitoring circuit.

XSTP bit is becomes "1" when the oscillation halts. The resister value is maintained until the "0" is written. It is impossible to write "1" to this XSTP bit. As for the VDET, the flag for monitoring supply voltage becomes "1" if PON, the flag for power-on reset becomes "1".

The relation among the condition of the PON, XSTP, and VDET, and power supply condition, and time data is shown in the table below.

	PON	XSTP	VDET	Conditions of power supply and oscillation circuit	Conditions of time function and back-up status
I	0	0	0	Normal	Normal
II	0	0	1	VDD supply voltage becomes below threshold voltage, but oscillation continues.	Time data is normal. However, the back-up battery voltage becomes close to minimum voltage for time keeping.
III	0	1	0	Oscillation halts, however, the power supply does not become lower than the threshold	Oscillation may halt by condensation or other reasons.
IV	0	1	1	VDD supply voltage becomes lower than the threshold voltage but higher than 0V, oscillation halts	Time function stops caused by the backup battery voltage drops.
V	1	1	1	Drop in supply voltage to 0v	Time data is unreliable.
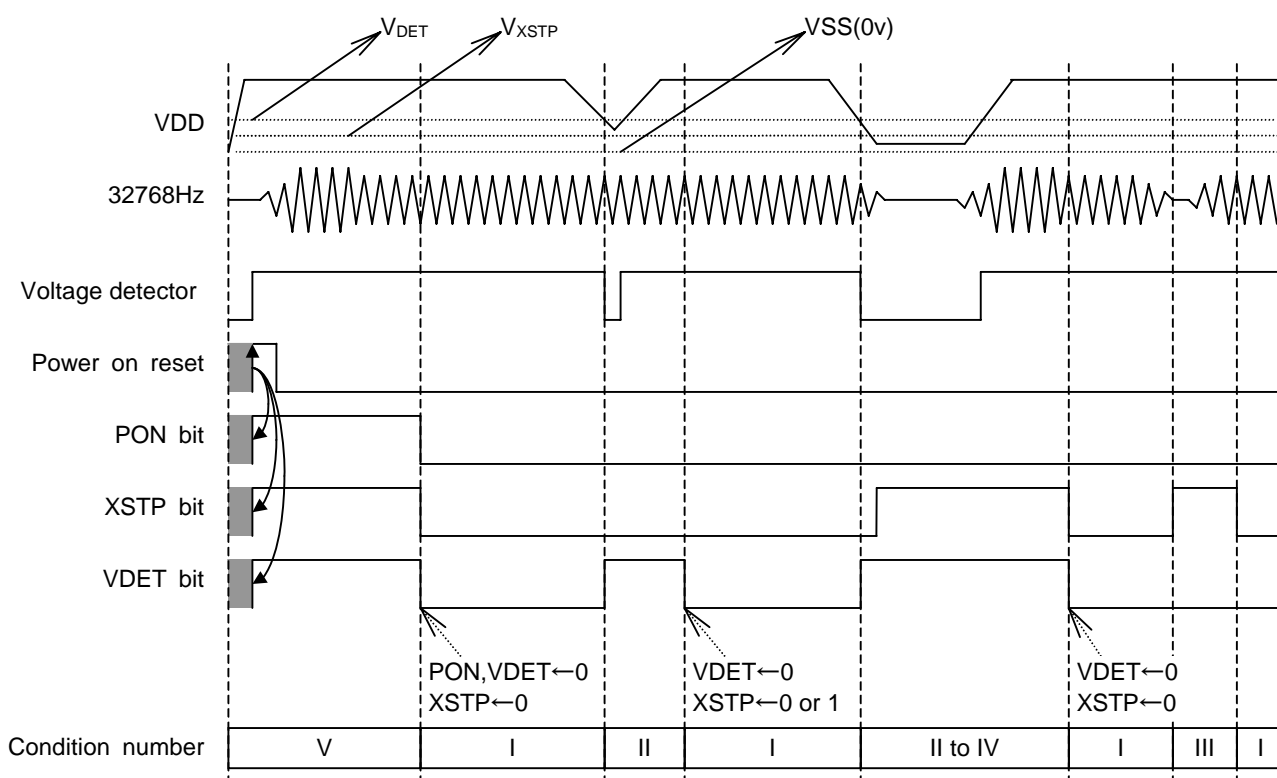
RICOH

*) The power on reset shown above is an internal signal and the signal is generated from right after the VDD turns on until the oscillation of quartz crystal unit starts. While the term of the power-on reset signal is out, or the time until the oscillation of quarts crystal unit starts, approximately 0.1s to 1.0s, access of I2C bus is impossible.

<Voltage Monitoring Circuit>

The supply monitoring circuit is configured to conduct a sampling operation during an interval of 7.8ms per second to reduce the supply current. The threshold voltage is V_{DET}. Once VDET bit becomes "1", sampling operation is suspended and unless otherwise writing "0" to this bit, the device does not restart. If the power supply starts up from 0V and if the PON becomes "1", VDET bit becomes "1", therefore, initially, sampling operation is suspended.

Once the power supply turns on and when "0" is written on the VDET bit, the operation starts. When the VDD becomes equal or less than V_{DET}, or threshold voltage is detected, VDET bit becomes "1" and operation is suspended. This function operates once every second, therefore instantaneous shutdown of the power supply may not be able to be detected.
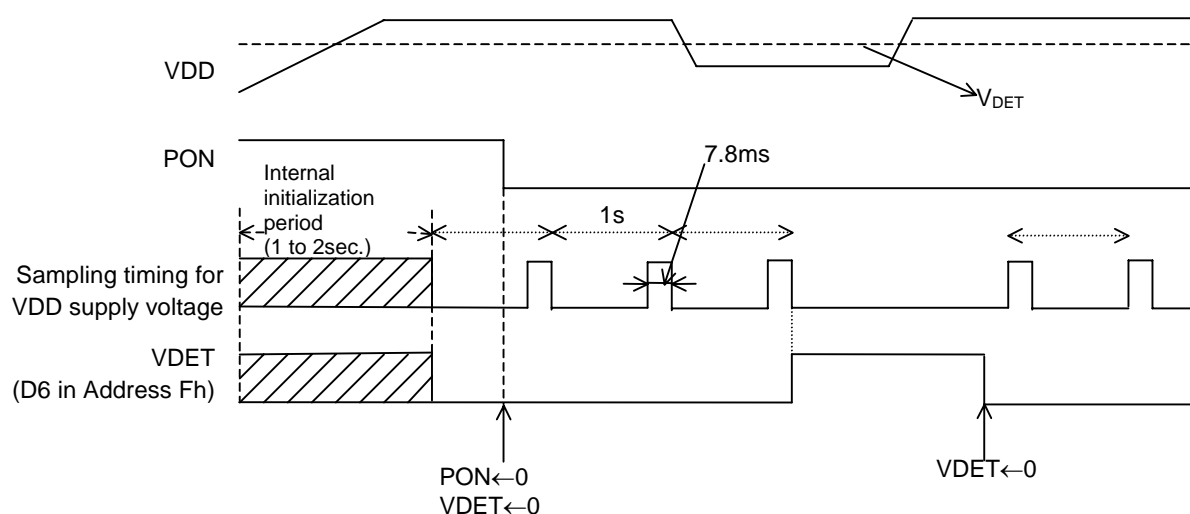
< Considerations in Using Power on Reset, Oscillation Halt Sensing, Power Supply Monitoring Circuit >
If instantaneous shutdown of VDD happens, these functions may not work.
To prevent the spike noise of the power supply line, mount a bypass capacitor as close as possible to VDD.
On-board noise to the quartz crystal unit must be avoided.
Applying to individual pins voltage exceeding their respective maximum ratings must be avoided.

Malfunction of detecting or others caused by noise must be cared as much as possible.
In particular, note that if a supply voltage as illustrated below in such events as backup battery installation, even if PON/XSTP bit may not shift from 0 to 1, internal data may be broken. Further, give special considerations to prevent excessive chattering in the oscillation halt sensing circuit.

Alarm and Periodic Interrupt

The R2221x, R2223x incorporates the alarm interrupt circuit and the periodic interrupt circuit that are configured to generate alarm signals and periodic interrupt signals for output from the $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ (R2223x) $\overline{\text{INTR}}$ (R2221x) pin as described below.

(1) Alarm Interrupt Circuit

The alarm interrupt circuit is configured to generate alarm signals for output from the $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$, which is driven low (enabled) upon the occurrence of a match between current time read by the time counters (the day-of-week, hour, and minute counters) and alarm time preset by the alarm registers (the Alarm_W registers intended for the day-of-week, hour, and minute digit settings and the Alarm_D registers intended for the hour and minute digit settings). In case of R2223x the Alarm_W is output from the $\overline{\text{INTRB}}$ pin, the Alarm_D is output from $\overline{\text{INTRA}}$ pin. In case of R2221x the Alarm_W and Alarm_D is output from $\overline{\text{INTR}}$ pin

(2) Periodic Interrupt Circuit

The periodic interrupt circuit is configured to generate either clock pulses in the pulse mode or interrupt signals in the level mode for output from the $\overline{\text{INTRA}}$ (R2223x), $\overline{\text{INTR}}$ (R2221x) pin depending on the CT2, CT1, and CT0 bit settings in the control register 1.

The above two types of interrupt signals are monitored by the flag bits (i.e. the WAFG, DAFG, and CTFG bits in the Control Register 2) and enabled or disabled by the enable bits (i.e. the WALE, DALE, CT2, CT1, and CT0 bits in the Control Register 1) as listed in the table below.

	Flag bits	Enable bits	Output Pin (R2223x)	Output Pin (R2221x)
Alarm_W	WAFG (D1 at Address Fh)	WALE (D7 at Address Eh)	$\overline{\text{INTRB}}$	$\overline{\text{INTR}}$
Alarm_D	DAFG (D0 at Address Fh)	DALE (D6 at Address Eh)	$\overline{\text{INTRA}}$	$\overline{\text{INTR}}$
Periodic interrupt	CTFG (D2 at Address Fh)	CT2=CT1=CT0=0 (These bit setting of "0" disable the Periodic interrupt) (D2 to D0 at Address Eh)	$\overline{\text{INTRA}}$	$\overline{\text{INTR}}$

* At power-on, when the WALE, DALE, CT2, CT1, and CT0 bits are set to 0 in the Control Register 1, the $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ (R2223x), $\overline{\text{INTR}}$ (R2221x) pin is driven high (disabled).
* When two types of interrupt signals are output simultaneously from the $\overline{\text{INTRA}}$ (R2221x= $\overline{\text{INTR}}$) pin, the output from the $\overline{\text{INTRA}}$ (R2221x= $\overline{\text{INTR}}$) pin becomes an OR waveform of their negative logic.

Example: Combined Output to $\overline{\text{INTRA}}$ Pin Under Control of
$\overline{\text{ALARM\_D}}$ and Periodic Interrupt

Alarm_D

Periodic Interrupt
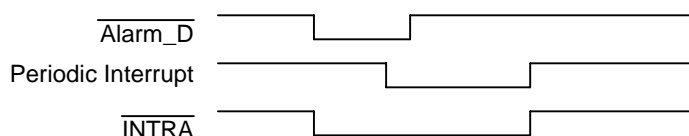
$\overline{\text{INTRA}}$

In this event, which type of interrupt signal is output from the $\overline{\text{INTRA}}$ (R2221x= $\overline{\text{INTR}}$) pin can be confirmed by reading the DAFG, and CTFG bit settings in the Control Register 2.
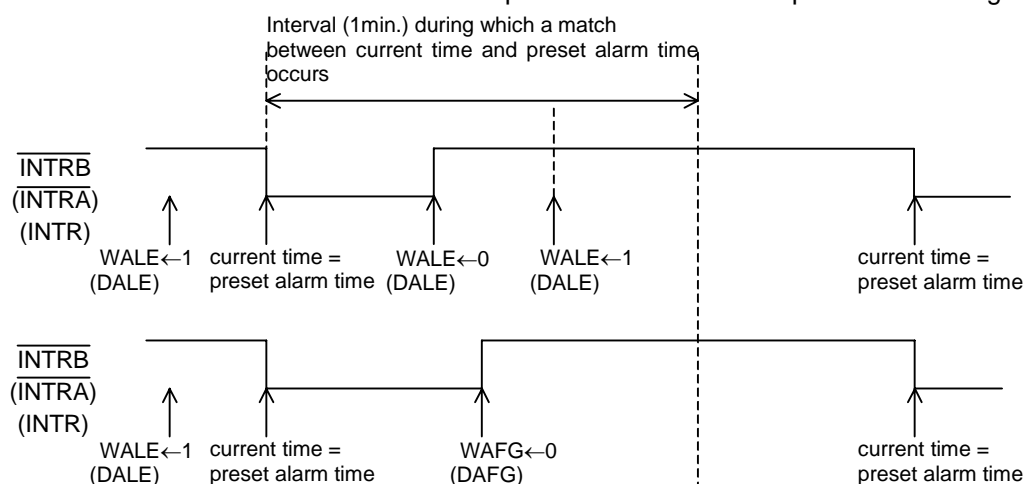
● **Alarm Interrupt**

The alarm interrupt circuit is controlled by the enable bits (i.e. the WALE and DALE bits in the Control Register 1) and the flag bits (i.e. the WAFG and DAFG bits in the Control Register 2). The enable bits can be used to enable

RICOH

this circuit when set to 1 and to disable it when set to 0.   When intended for reading, the flag bits can be used to monitor alarm interrupt signals.   When intended for writing, the flag bits will cause no event when set to 1 and will drive high (disable) the alarm interrupt circuit when set to 0.

The enable bits will not be affected even when the flag bits are set to 0.   In this event, therefore, the alarm interrupt circuit will continue to function until it is driven low (enabled) upon the next occurrence of a match between current time and preset alarm time.

The alarm function can be set by presetting desired alarm time in the alarm registers (the Alarm_W Registers for the day-of-week digit settings and both the Alarm_W Registers and the Alarm_D Registers for the hour and minute digit settings) with the WALE and DALE bits once set to 0 and then to 1 in the Control Register 1.   Note that the WALE and DALE bits should be once set to 0 in order to disable the alarm interrupt circuit upon the coincidental occurrence of a match between current time and preset alarm time in the process of setting the alarm function.

After setting WALE(DALW) to 0, Alarm registers is set to current time, and WALE(DALE) is set to 1, $\overline{INTRB}$ ($\overline{INTRA}$) will be not driven to "L" immediately, $\overline{INTRB}$ ($\overline{INTRA}$, $\overline{INTR}$) will be driven to "L" at next alarm setting time.

● **Periodic Interrupt**

Setting of the periodic selection bits (CT2 to CT0) enables periodic interrupt to the CPU. There are two waveform modes: pulse mode and level mode.   In the pulse mode, the output has a waveform duty cycle of around 50%. In the level mode, the output is cyclically driven low and, when the CTFG bit is set to 0, the output is return to High (OFF).

CT2	CT1	CT0	Description	
			Wave form mode	Interrupt Cycle and Falling Timing
0	0	0	-	OFF(H)
0	0	1	-	Fixed at "L"
0	1	0	Pulse Mode *1)	2Hz(Duty50%)
0	1	1	Pulse Mode *1)	1Hz(Duty50%)
1	0	0	Level Mode *2)	Once per 1 second (Synchronized with Second counter increment)
1	0	1	Level Mode *2)	Once per 1 minute (at 00 seconds of every Minute)
1	1	0	Level Mode *2)	Once per hour (at 00 minutes and 00 Seconds of every hour)
1	1	1	Level Mode *2)	Once per month (at 00 hours, 00 minutes, and 00 seconds of first day of every month)

(The first row "0 0 0" is marked as (Default))

*1) Pulse Mode:

2-Hz and 1-Hz clock pulses are output in synchronization with the increment of the second counter as illustrated in the timing chart below.

In the pulse mode, the increment of the second counter is delayed by approximately 46 μs from the falling edge of clock pulses. Consequently, time readings immediately after the falling edge of clock pulses may appear to lag behind the time counts of the real-time clocks by approximately 1 second. Rewriting the second counter will reset the other time counters of less than 1 second, driving the $\overline{\text{INTRA}}$ ($\overline{\text{INTR}}$) pin low.

*2) Level Mode:
Periodic interrupt signals are output with selectable interrupt cycle settings of 1 second, 1 minute, 1 hour, and 1 month. The increment of the second counter is synchronized with the falling edge of periodic interrupt signals. For example, periodic interrupt signals with an interrupt cycle setting of 1 second are output in synchronization with the increment of the second counter as illustrated in the timing chart below.

*1), *2) When the oscillation adjustment circuit is used, the interrupt cycle will fluctuate once per 20sec. as follows:

Pulse Mode: The "L" period of output pulses will increment or decrement by a maximum of ±3.784ms. For example, 1-Hz clock pulses will have a duty cycle of 50 ±0.3784%.

Level Mode: A periodic interrupt cycle of 1 second will increment or decrement by a maximum of ±3.784 ms.

RICOH

- **32-kHz CLOCK OUTPUT**

For the R2221x, R2223x 32.768-kHz clock pulses are output from the 32KOUT pin when either the $\overline{\text{CLEN1}}$ bit in the Control Register 2 or the $\overline{\text{CLEN2}}$ bit in the Control Register 1 is set to 0 when the CLKC pin is set to high. If the condition is not satisfied, the output is set to low.

$\overline{\text{CLEN1}}$ (D3 at Address Fh)	$\overline{\text{CLEN2}}$ (D4 at Address Eh)	CLKC pin input	32KOUT PIN (CMOS push-pull output)
1	1	*	"L"
*	*	L	
0(Default)	*	H	Clock pulses
*	0(Default)	H	

The 32KOUT pin output is synchronized with the $\overline{\text{CLEN1}}$ and $\overline{\text{CLEN2}}$ bit and CLKC pin settings as illustrated in the timing chart below.
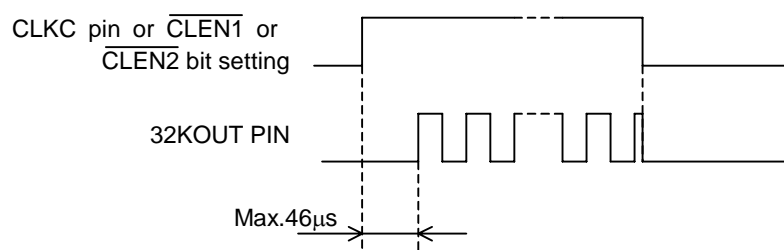
Typical Applications

Sample circuit configuration1
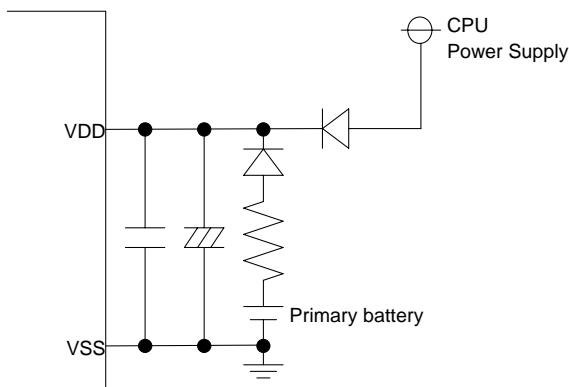
Sample circuit configuration2
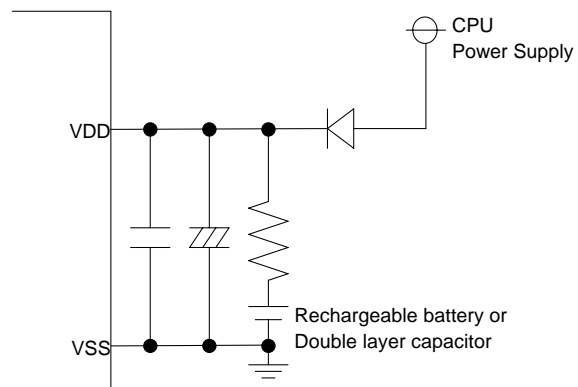
*Set bypass capacitors as close as possible to the IC, use a capacitor for high frequency and another capacitor for low frequency in parallel.

● **Connection of $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$(R2223x), $\overline{\text{INTR}}$ (R2221x) Pin**

The $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ (R2223x), $\overline{\text{INTR}}$ (R2221x) pin follows the N-channel open drain output logic and contains no protective diode on the power supply side. As such, it can be connected to a pull-up resistor of up to 5.5v regardless of supply voltage.
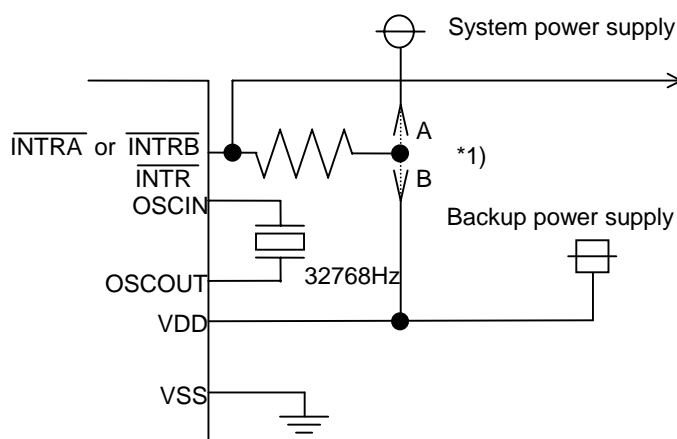
*1) Depending on whether the $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ (R2223x), $\overline{\text{INTR}}$ (R2221x) pin is used during battery backup, it should be connected to a pull-up resistor at the following different positions:

(1) Position A in the left diagram when it is not to be used during battery backup.

(2) Position B in the left diagram when it is to be used during battery backup.

RICOH

● **Connection of 32KOUT Pin**

As the 32KOUT pin is CMOS output, the supply voltage of the R2221x, R2223x and any devices to be connected should be the same.   When the device is powered down, the 32KOUT output pin should be disabled.

When the CLKC pin is connected to the system power supply through the pull-up resistor, the pull-up resistor should be 0Ω to 10kΩ, and the 32KOUT pin should be connect to the host device through the resistor (approx. 10kΩ)
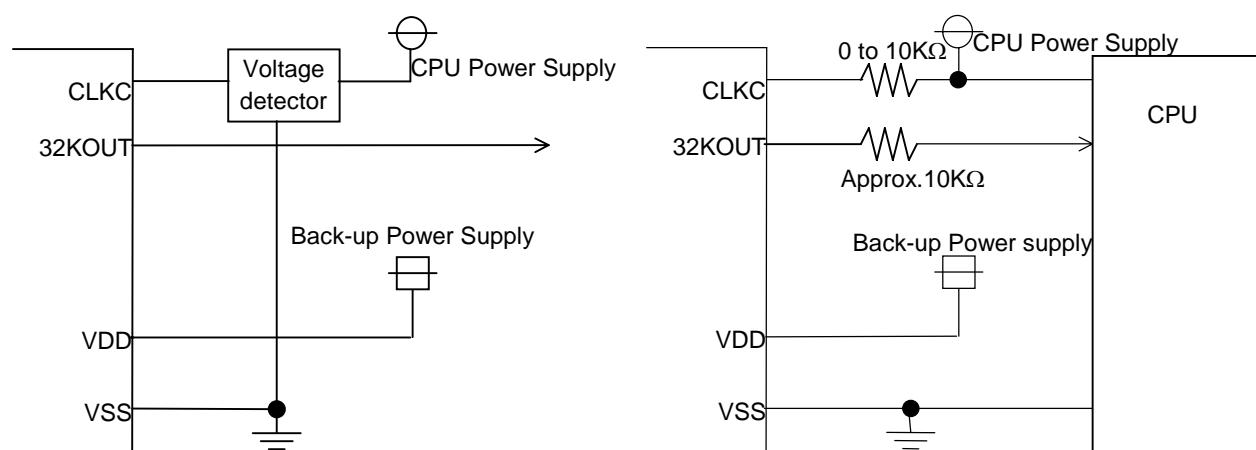
Typical Characteristics

Test circuit
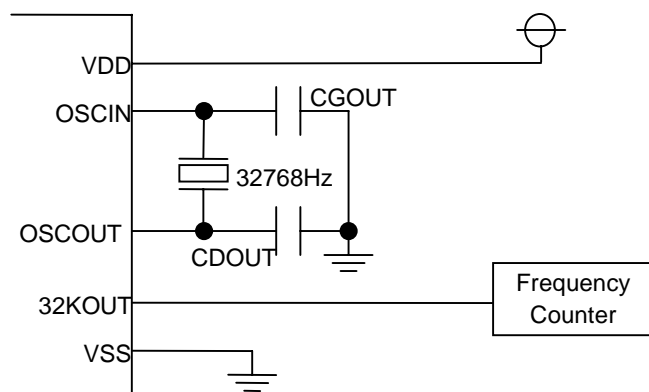
X'tal : 32.768kHz
(R1=30kΩ typ)
(CL=7pF)
Topt : 25°C
Output pins : Open

Timekeeping Current vs. Supply Voltage
(with no 32kHz clock output)
(ECO=ON, SCL=SDA=CLKC=Vss)
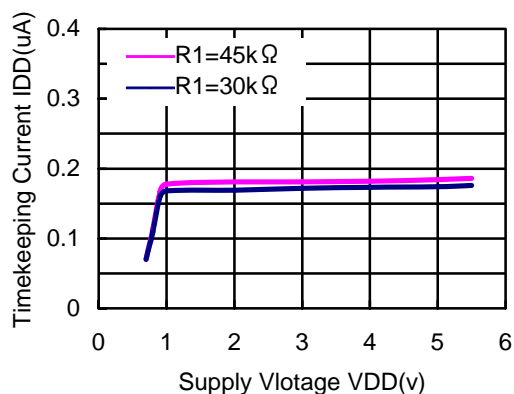
Timekeeping Current vs. Supply Voltage
(with no 32kHz clock output)
(ECO=OFF,SCL=SDA=CLKC=Vss)
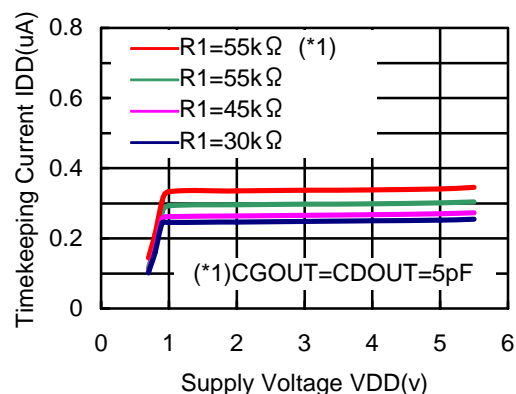
Timekeeping Current vs. Supply Voltage
(ECO=ON, SCL=SDA=Vss, CLKC=VDD,)
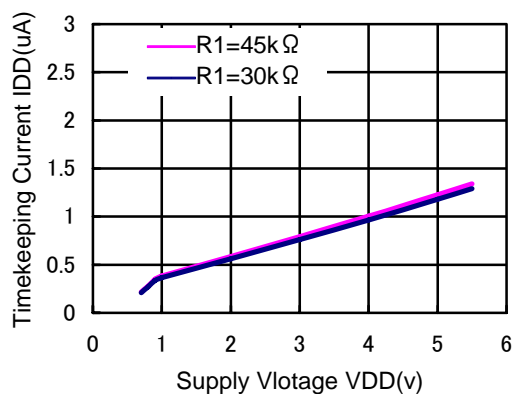
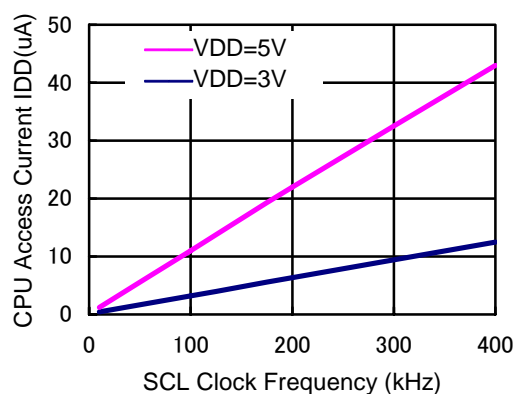Timekeeping Current vs. Supply Voltage
(ECO=OFF, SCL=SDA=Vss, CLKC=VDD,)

RICOH
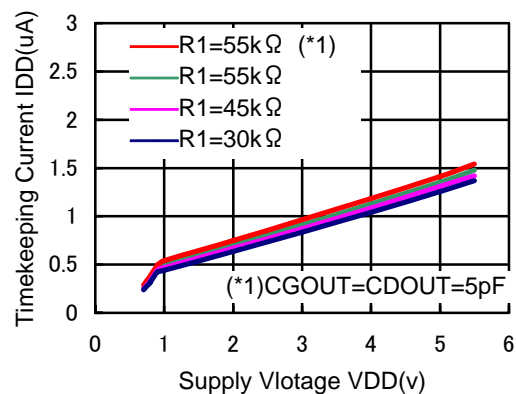
Timekeeping Current vs. Operating Temperature
(ECO=ON, V$_{DD}$=3V, SCL=SDA=CLKC=V$_{SS}$)
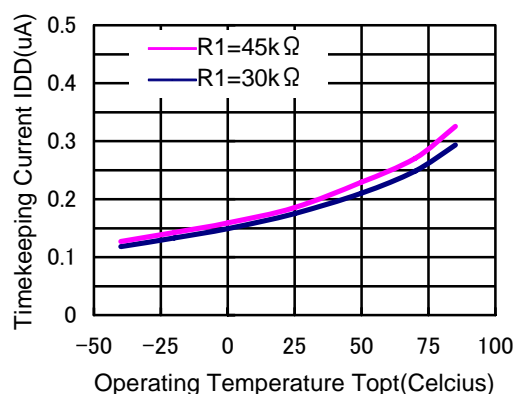
Timekeeping Current vs. Operating Temperature
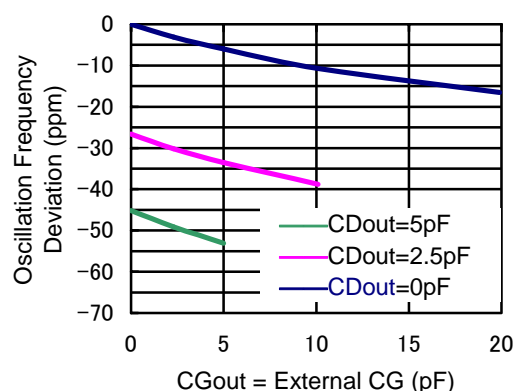(ECO=OFF, V$_{DD}$=3V, SCL=SDA=CLKC=V$_{SS}$)
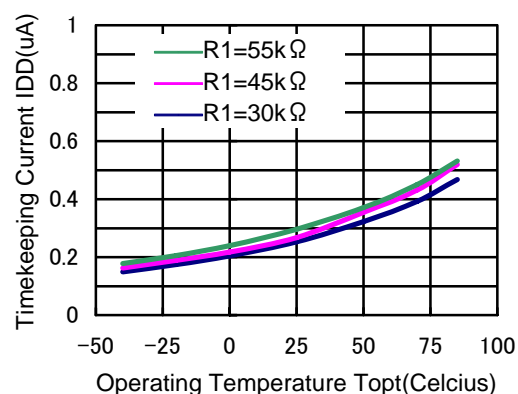
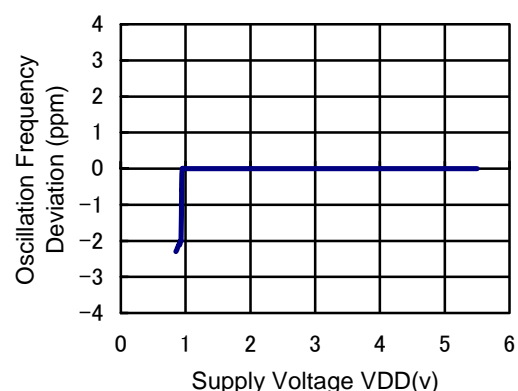CPU Access Current vs. SCL Clock Frequency
(CLKC=V$_{SS}$)

Supply Voltage Monitoring Voltage (VDET) vs
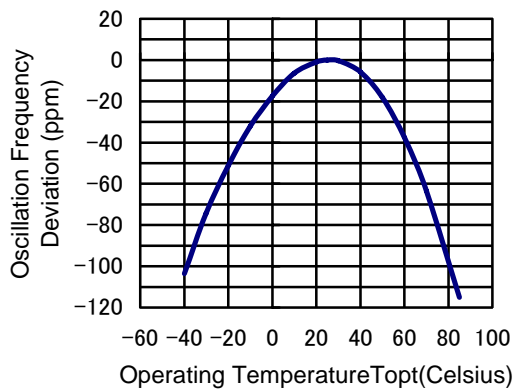Operating Temperature   (-30 to +70°C)
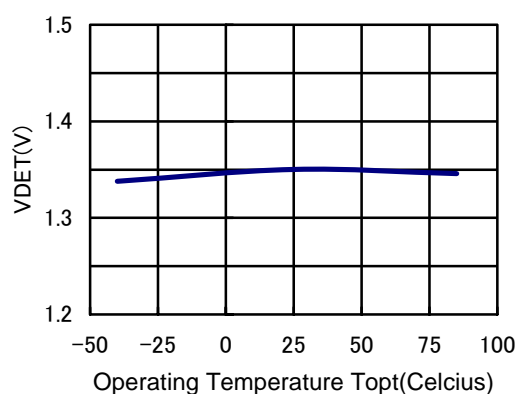
Oscillation Frequency Deviation vs. External CG,CD
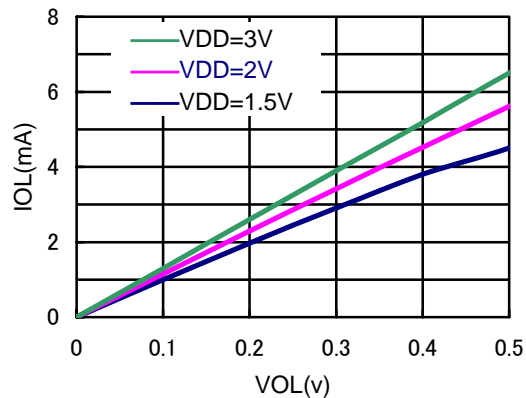(V$_{DD}$=3v, CGout=CDout=0pF as standard)

Oscillation Frequency Deviation vs. Supply Voltage
(VDD=3v as standard)

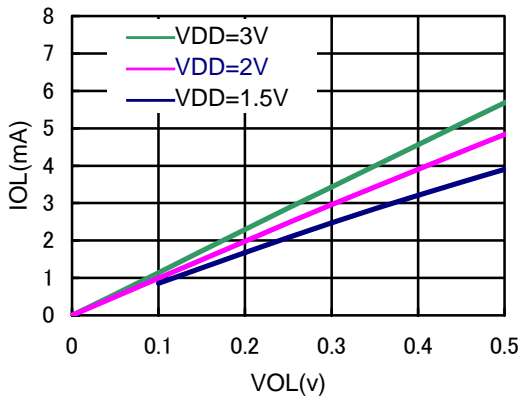Oscillation Frequency Deviation vs.
Operating Temperature
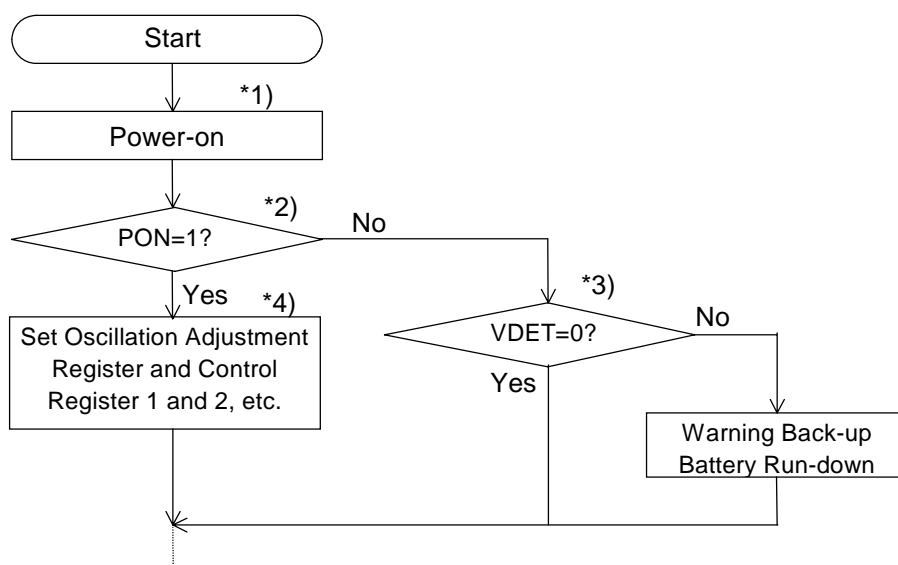(V_DD=3V, Topt=25°C as standard)

V_{OL} vs I_{OL}
(SDA pin)

V_{OL} vs I_{OL}
($\overline{INTRA}$, $\overline{INTRB}$, $\overline{INTR}$ pin)

RICOH

Typical Software-based Operations

- **Initialization at Power-on**

*1) After power-on from 0 volt, the start of oscillation and the process of internal initialization require a time span on 1to 2seconds, so that access should be done after the lapse of this time span or more.

*2) The PON bit setting of 0 in the Control Register 1 indicates power-on from backup battery and not from 0v. For further details, see "P.36 • Power-on Reset, Oscillation Halt Sensing, and Supply Voltage Monitoring".

*3) This step is not required when the supply voltage monitoring circuit is not used.

*4) This step involves ordinary initialization including the Oscillation Adjustment Register and interrupt cycle settings, etc.

- **Writing of Time and Calendar Data**
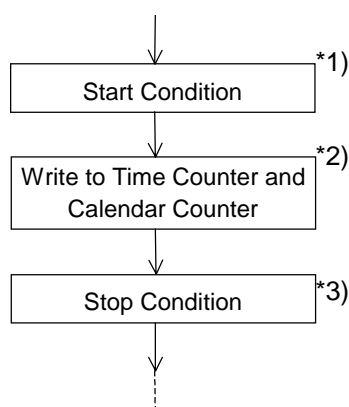
*1) When writing to clock and calendar counters, do not insert Stop Condition until all times from second to year have been written to prevent error in writing time. (Detailed in "P.28 Data Transmission under Special Condition".
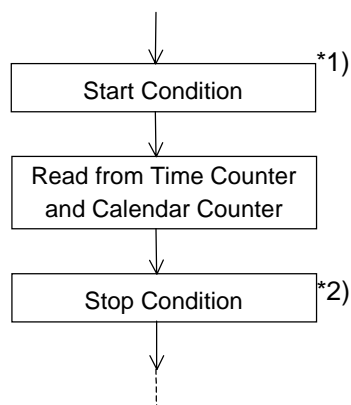
*2) Any writing to the second counter will reset divider units lower than the second digits.

*3) Take care so that process from Start Condition to Stop Condition will be complete within 0.5sec. (Detailed in "P.28 Data Transmission under Special Condition".

The R2221x,R2223x may also be initialized not at power-on but in the process of writing time and calendar data.
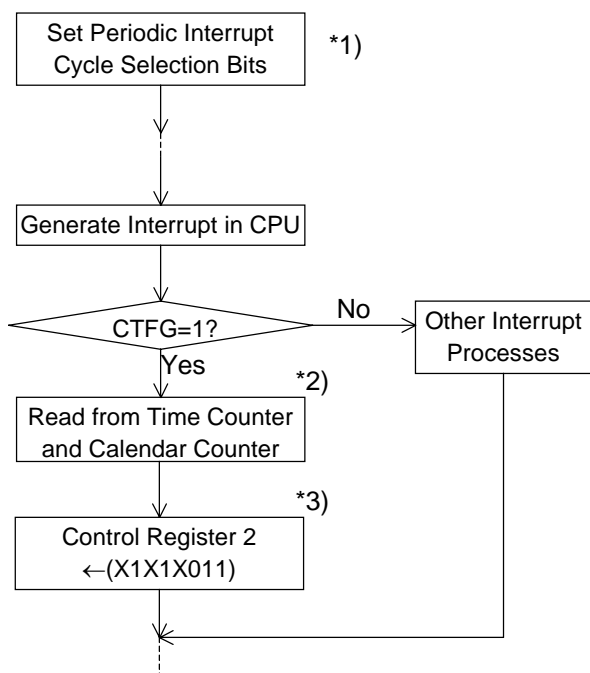
● **Reading Time and Calendar Data**

(1) Ordinary Process of Reading Time and Calendar Data

```
              │
              ▼              *1)
    ┌───────────────────┐
    │  Start Condition  │
    └───────────────────┘
              │
              ▼
    ┌───────────────────┐
    │ Read from Time Counter │
    │  and Calendar Counter  │
    └───────────────────┘
              │
              ▼
    ┌───────────────────┐
    │  Stop Condition   │  *2)
    └───────────────────┘
              │
              ▼ (dashed)
```

*1) When reading to clock and calendar counters, do not insert Stop Condition until all times from second to year have been written to prevent error in writing time. (Detailed in "P.28 Data Transmission under Special Condition".

*2) Take care so that process from Start Condition to Stop Condition will be complete within 0.5sec. (Detailed in "P.28 Data Transmission under Special Condition".

(2) Basic Process of Reading Time and Calendar Data with Periodic Interrupt Function

```
    ┌───────────────────┐
    │ Set Periodic Interrupt │   *1)
    │ Cycle Selection Bits   │
    └───────────────────┘
              │ (dashed)
              ▼
    ┌───────────────────┐
    │ Generate Interrupt in CPU │
    └───────────────────┘
              │
              ▼
          ╱ CTFG=1? ╲ ──No──> ┌──────────────┐
          ╲         ╱          │ Other Interrupt │
            Yes                │   Processes     │
              │      *2)       └──────────────┘
              ▼                        │
    ┌───────────────────┐              │
    │ Read from Time Counter │         │
    │  and Calendar Counter  │         │
    └───────────────────┘              │
              │      *3)               │
              ▼                        │
    ┌───────────────────┐              │
    │  Control Register 2  │           │
    │   ←(X1X1X011)        │           │
    └───────────────────┘              │
              │◄──────────────────────┘
              ▼ (dashed)
```

*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.
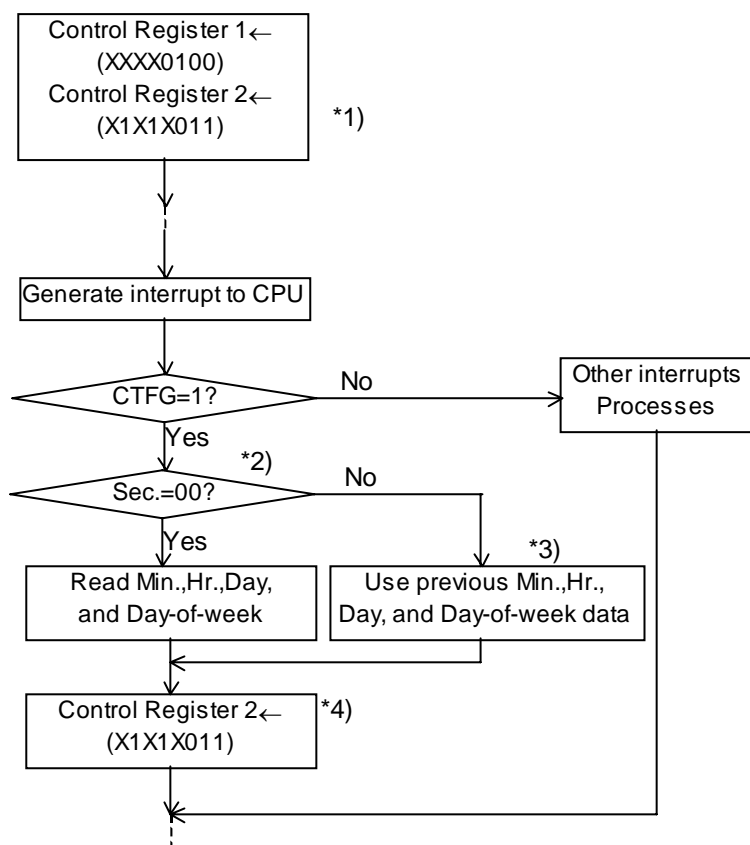
*2) This step must be completed within 0.5 second.

*3) This step is intended to set the CTFG bit to 0 in the Control Register 2 to cancel an interrupt to the CPU.

RICOH

(3) Applied Process of Reading Time and Calendar Data with Periodic Interrupt Function

Time data need not be read from all the time counters when used for such ordinary purposes as time count indication.   This applied process can be used to read time and calendar data with substantial reductions in the load involved in such reading.

For Time Indication in "Day-of-Month, Day-of-week, Hour, Minute, and Second"   Format:

```
  ┌─────────────────────────┐
  │ Control Register 1←      │
  │    (XXXX0100)            │
  │ Control Register 2←      │  *1)
  │    (X1X1X011)            │
  └─────────────────────────┘
              │
              ↓
  ┌─────────────────────────┐
  │ Generate interrupt to CPU│
  └─────────────────────────┘
              │
              ↓              No    ┌──────────────────┐
          < CTFG=1? >──────────────│ Other interrupts │
              │ Yes                │    Processes     │
              ↓        *2)         └──────────────────┘
          < Sec.=00? >──── No
              │ Yes          │
              ↓              ↓  *3)
  ┌──────────────────┐  ┌──────────────────────┐
  │ Read Min.,Hr.,Day,│  │ Use previous Min.,Hr.,│
  │ and Day-of-week   │  │ Day, and Day-of-week │
  └──────────────────┘  │      data            │
              │          └──────────────────────┘
              ↓
  ┌──────────────────┐  *4)
  │ Control Register 2←│
  │    (X1X1X011)     │
  └──────────────────┘
              │
              ↓
```

*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.
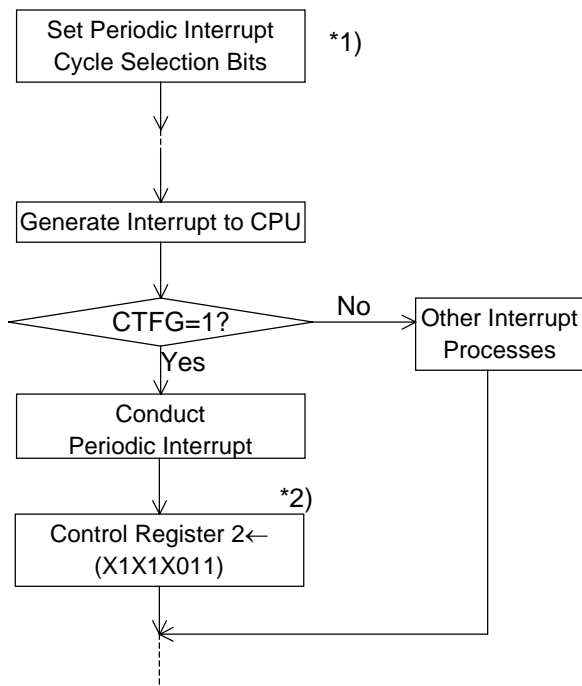
*2) This step must be completed within 0.5 sec.

*3) This step is intended to read time data from all the time counters only in the first session of reading time data after writing time data.

*4) This step is intended to set the CTFG bit to 0 in the Control Register 2 to cancel an interrupt to the CPU.
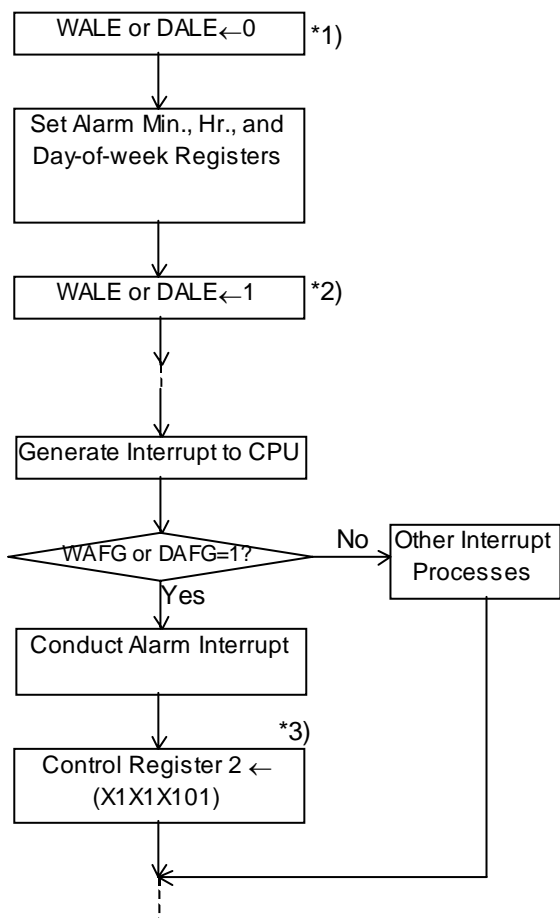
- **Interrupt Process**

(1) Periodic Interrupt

```
┌─────────────────────┐
│ Set Periodic Interrupt │  *1)
│ Cycle Selection Bits │
└─────────────────────┘
          ┆
┌─────────────────────┐
│ Generate Interrupt to CPU │
└─────────────────────┘
          │
       ╱CTFG=1?╲───No──→┌──────────────┐
       ╲       ╱        │ Other Interrupt │
          │Yes          │  Processes    │
          ▼             └──────────────┘
┌─────────────────────┐
│     Conduct         │
│ Periodic Interrupt  │
└─────────────────────┘
          │        *2)
┌─────────────────────┐
│ Control Register 2← │
│    (X1X1X011)       │
└─────────────────────┘
          ┆
```

*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.

*2) This step is intended to set the CTFG bit to 0 in the Control Register 2 to cancel an interrupt to the CPU.

(2) Alarm Interrupt

```
┌─────────────────────┐
│  WALE or DALE←0     │  *1)
└─────────────────────┘
          │
┌─────────────────────┐
│ Set Alarm Min., Hr., and │
│ Day-of-week Registers │
└─────────────────────┘
          │
┌─────────────────────┐
│  WALE or DALE←1     │  *2)
└─────────────────────┘
          ┆
┌─────────────────────┐
│ Generate Interrupt to CPU │
└─────────────────────┘
          │
   ╱WAFG or DAFG=1?╲──No─→┌──────────────┐
   ╲              ╱       │ Other Interrupt │
          │Yes            │  Processes    │
          ▼               └──────────────┘
┌─────────────────────┐
│ Conduct Alarm Interrupt │
└─────────────────────┘
          │        *3)
┌─────────────────────┐
│ Control Register 2 ← │
│    (X1X1X101)       │
└─────────────────────┘
          ┆
```

*1) This step is intended to once disable the alarm interrupt circuit by setting the WALE or DALE bits to 0 in anticipation of the coincidental occurrence of a match between current time and preset alarm time in the process of setting the alarm interrupt function.

*2) This step is intended to enable the alarm interrupt function after completion of all alarm interrupt settings.

*3) This step is intended to once cancel the alarm interrupt function by writing the settings of "X,1,X, 1,X,1,0,1" and "X,1,X,1,X,1,1,0" to the Alarm_W Registers and the Alarm_D Registers, respectively.

RICOH

RoHS Compliant
Halogen Free

Ricoh is committed to reducing the environmental loading materials in electrical devices with a view to contributing to the protection of human health and the environment.
Ricoh has been providing RoHS compliant products since April 1, 2006 and Halogen-free products since April 1, 2012.

RICOH RICOH ELECTRONIC DEVICES CO., LTD.

http://www.e-devices.ricoh.co.jp/en/

Sales & Support Offices

RICOH ELECTRONIC DEVICES CO., LTD.
Higashi-Shinagawa Office (International Sales)
3-32-3, Higashi-Shinagawa, Shinagawa-ku, Tokyo 140-8655, Japan
Phone: +81-3-5479-2857 Fax: +81-3-5479-0502

RICOH EUROPE (NETHERLANDS) B.V.
Semiconductor Support Centre
Prof. W.H. Keesomlaan 1, 1183 DJ Amstelveen, The Netherlands
Phone: +31-20-5474-309

RICOH ELECTRONIC DEVICES KOREA CO., LTD.
3F, Haesung Bldg, 504, Teheran-ro, Gangnam-gu, Seoul, 135-725, Korea
Phone: +82-2-2135-5700 Fax: +82-2-2051-5713

RICOH ELECTRONIC DEVICES SHANGHAI CO., LTD.
Room 403, No.2 Building, No.690 Bibo Road, Pu Dong New District, Shanghai 201203, People's Republic of China
Phone: +86-21-5027-3200 Fax: +86-21-5027-3299

RICOH ELECTRONIC DEVICES CO., LTD.
Taipei office
Room 109, 10F-1, No.51, Hengyang Rd., Taipei City, Taiwan (R.O.C.)
Phone: +886-2-2313-1621/1622 Fax: +886-2-2313-1623

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Ricoh Electronics](#):
 [R2221L-E2](#) [R2223L-E2](#) [R2223T-E2-F](#) [R2221T-E2-F](#)

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А