




## Thyristor/Diode and Thyristor/Thyristor (SUPER MAGN-A-PAK Power Modules), 500 A



SUPER MAGN-A-PAK

### FEATURES

- High current capability
- High surge capability
- Industrial standard package
- 3000 V<sub>RMS</sub> isolating voltage with non-toxic substrate
- UL approved file E78996 
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level



RoHS COMPLIANT

### PRODUCT SUMMARY

I<sub>T(AV)</sub>, I<sub>F(AV)</sub>

500 A

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
I <sub>T(AV)</sub> , I <sub>F(AV)</sub>	82 °C	500	A
I <sub>T(RMS)</sub>		785	A
	T <sub>C</sub>	82	°C
I <sub>TSM</sub>	50 Hz	17.8	kA
	60 Hz	18.7	
I <sup>2</sup> t	50 Hz	1591	kA <sup>2</sup> s
	60 Hz	1452	
I <sup>2</sup> √t		15 910	kA <sup>2</sup> √s
V <sub>RRM</sub>	Range	800 to 1600	V
T <sub>Stg</sub>	Range	- 40 to 150	°C
T <sub>J</sub>	Range	- 40 to 130	

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> MAXIMUM AT T <sub>J</sub> = T <sub>J</sub> MAXIMUM mA
VSK.500	08	800	900	100
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

ON-STATE CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$ , $I_{F(AV)}$	180° conduction, half sine wave		500	A
				82	°C
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave at $T_C = 82\text{ °C}$		785	A
Maximum peak, one-cycle, non-repetitive on-state surge current	$I_{TSM}$ , $I_{FSM}$	t = 10 ms	No voltage reappplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	kA
		t = 8.3 ms			
		t = 10 ms	100 % $V_{RRM}$ reappplied		
		t = 8.3 ms			
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reappplied	1591	kA <sup>2</sup> s
		t = 8.3 ms			
		t = 10 ms	100 % $V_{RRM}$ reappplied	1452	
		t = 8.3 ms		1125	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied		1027	kA <sup>2</sup> √s
Low level value or threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		15910	V
High level value of threshold voltage	$V_{T(TO)2}$	(I $> \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		0.85	
Low level value on-state slope resistance	$r_{t1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		0.93	mΩ
High level value on-state slope resistance	$r_{t2}$	(I $> \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum		0.36	
Maximum on-state voltage drop	$V_{TM}$	$I_{pk} = 1500\text{ A}$ , $T_J = 25\text{ °C}$ , $t_p = 10\text{ ms}$ sine pulse		1.50	V
Maximum forward voltage drop	$V_{FM}$	$I_{pk} = 1500\text{ A}$ , $T_J = 25\text{ °C}$ , $t_p = 10\text{ ms}$ sine pulse		1.50	V
Maximum holding current	$I_H$	$T_J = 25\text{ °C}$ , anode supply 12 V resistive load		500	mA
Maximum latching current	$I_L$			1000	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum rate of rise of turned-on current	$di/dt$	$T_J = T_J$ maximum, $I_{TM} = 400\text{ A}$ , $V_{DRM}$ applied		1000	A/μs
Typical delay time	$t_d$	Gate current 1 A, $di_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$ , $T_J = 25\text{ °C}$		2.0	μs
Typical turn-off time	$t_q$	$I_{TM} = 750\text{ A}$ ; $T_J = T_J$ maximum, $di/dt = -60\text{ A}/\mu\text{s}$ , $V_R = 50\text{ V}$ , $dV/dt = 20\text{ V}/\mu\text{s}$ , gate 0 V 100 Ω		200	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = 130\text{ °C}$ , linear to $V_D = 80\% V_{DRM}$		1000	V/μs
RMS insulation voltage	$V_{INS}$	t = 1 s		3000	V
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied		100	mA



# VSKT500-..PbF, VSKH500-..PbF, VSKL500-..PbF

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TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	W
Maximum peak average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0	
Maximum peak positive gate current	$+I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0	A
Maximum peak positive gate voltage	$+V_{GM}$		20	V
Maximum peak negative gate voltage	$-V_{GM}$		5.0	
Maximum DC gate current required to trigger	$I_{GT}$	$T_J = 25$ °C, $V_{ak} 12$ V	200	mA
DC gate voltage required to trigger	$V_{GT}$		3.0	V
DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum	10	mA
DC gate voltage not to trigger	$V_{GD}$		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	$T_J$		- 40 to 130	°C
Maximum storage temperature range	$T_{Stg}$		- 40 to 150	
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation	0.065	K/W
Maximum thermal resistance, case to heatsink	$R_{thC-hs}$		0.02	
Mounting torque $\pm 10$ %	SMAP to heatsink busbar to SMAP	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	6 to 8	Nm
			12 to 15	
Approximate weight			1500	g
Case style		See dimensions - link at the end of datasheet	SUPER MAGN-A-PAK	

$\Delta R_{thJC}$ CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.009	0.006	$T_J = T_J$ maximum	K/W
120°	0.011	0.011		
90°	0.014	0.015		
60°	0.021	0.022		
30°	0.037	0.038		

**Note**

- Table shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

# VSKT500-..PbF, VSKH500-..PbF, VSKL500-..PbF



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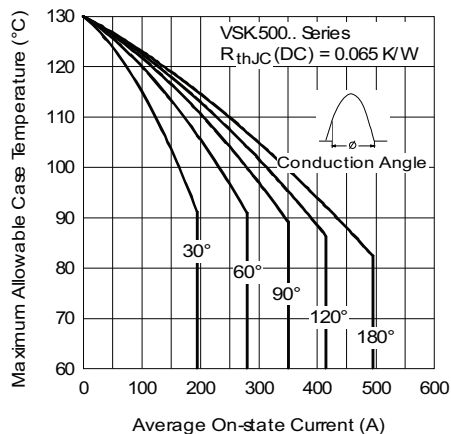


Fig. 1 - Current Ratings Characteristics

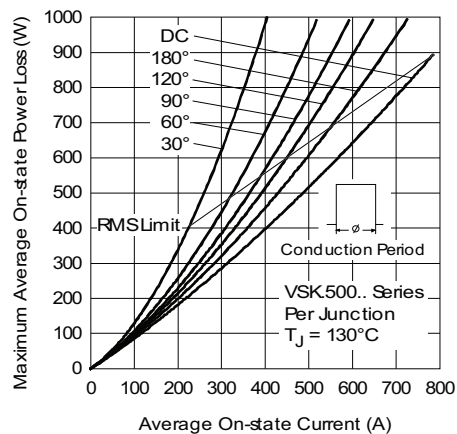


Fig. 4 - On-State Power Loss Characteristics

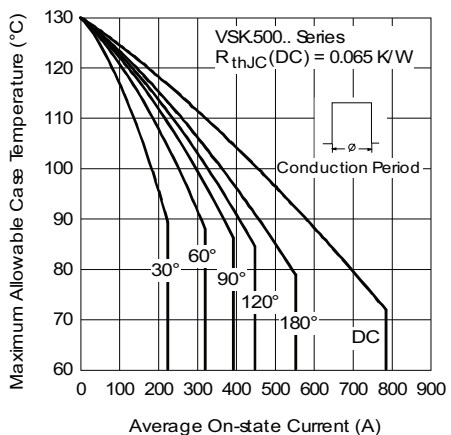


Fig. 2 - Current Ratings Characteristics

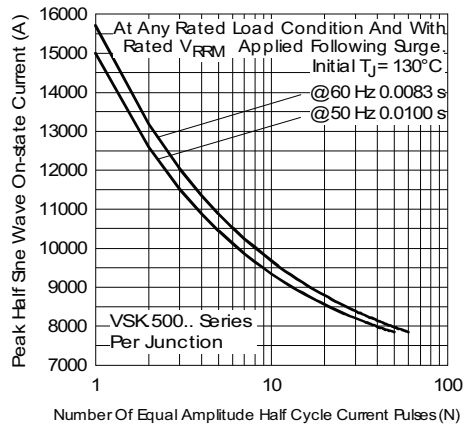


Fig. 5 - Maximum Non-Repetitive Surge Current

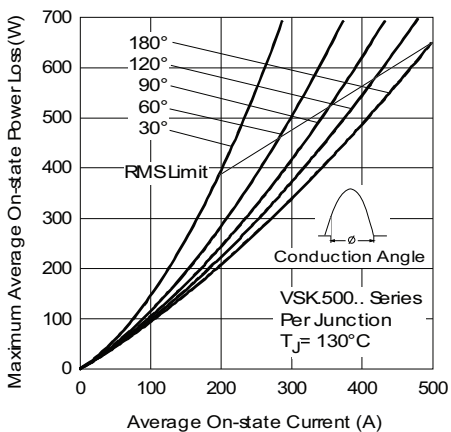


Fig. 3 - On-State Power Loss Characteristics

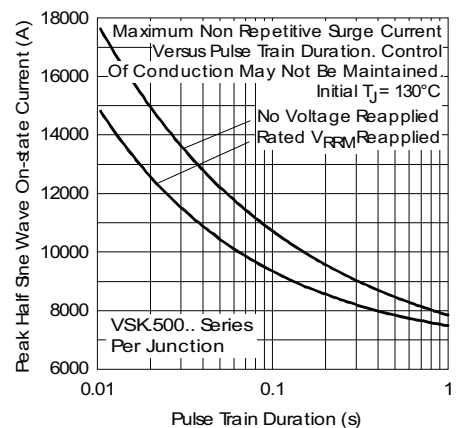


Fig. 6 - Maximum Non-Repetitive Surge Current



# VSKT500-..PbF, VSKH500-..PbF, VSKL500-..PbF

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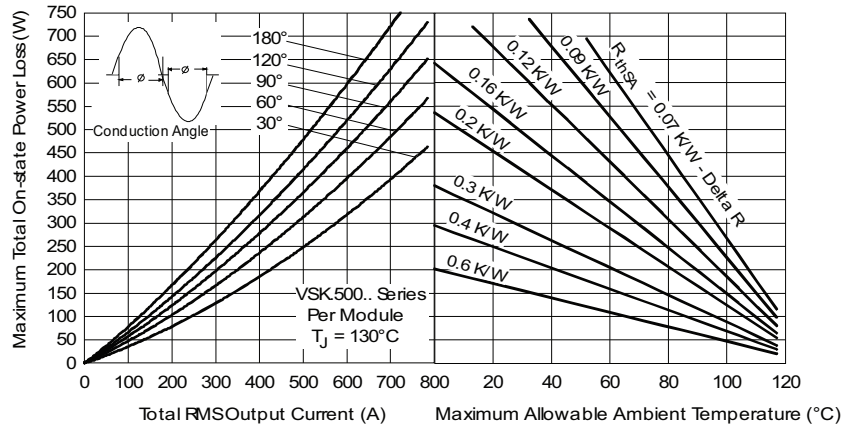


Fig. 7 - On-State Power Loss Characteristics

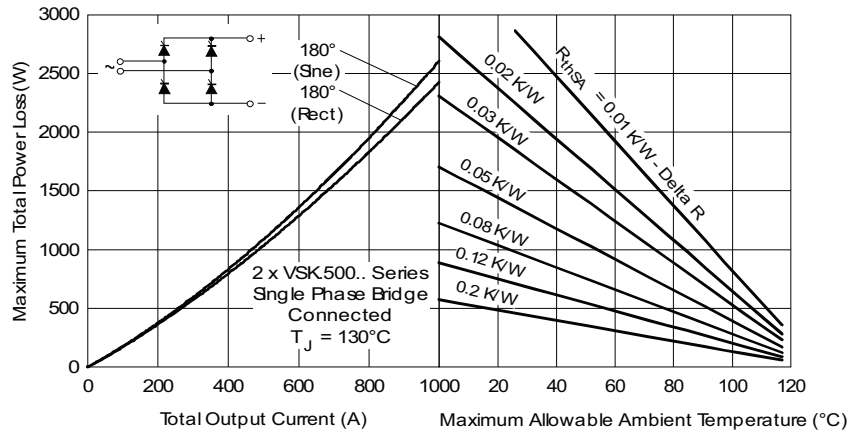


Fig. 8 - On-State Power Loss Characteristics

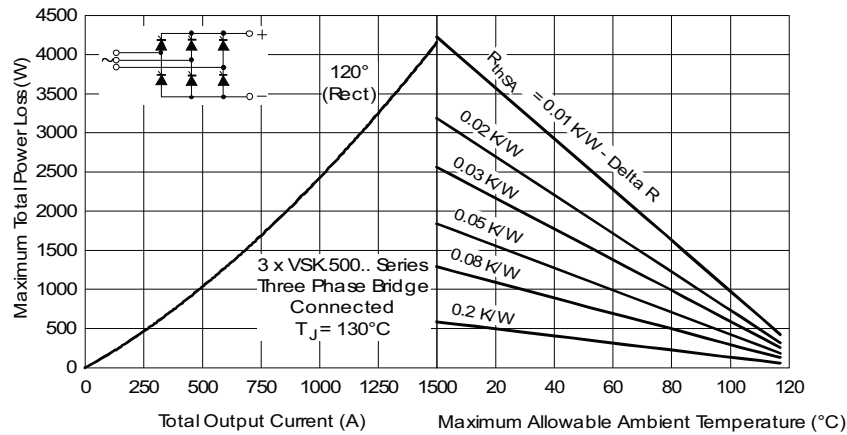


Fig. 9 - On-State Power Loss Characteristics

# VSKT500-..PbF, VSKH500-..PbF, VSKL500-..PbF



Vishay Semiconductors Thyristor/Diode and Thyristor/Thyristor  
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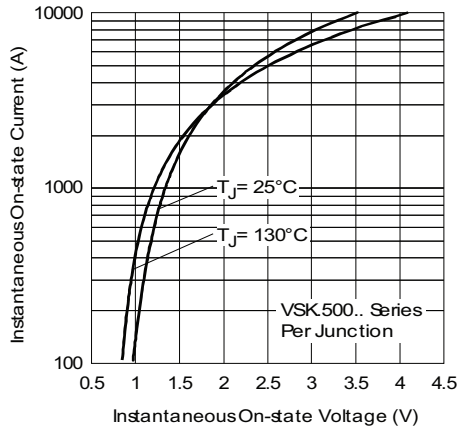


Fig. 10 - On-State Voltage Drop Characteristics

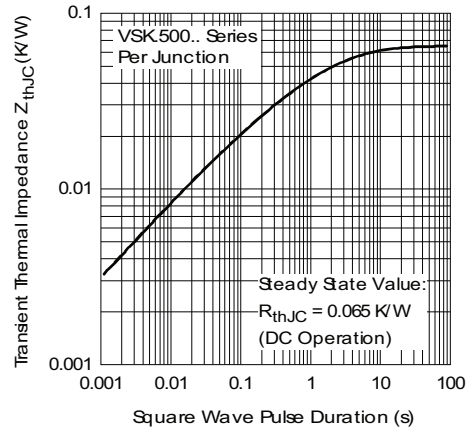


Fig. 11 - Thermal Impedance  $Z_{thJC}$  Characteristics

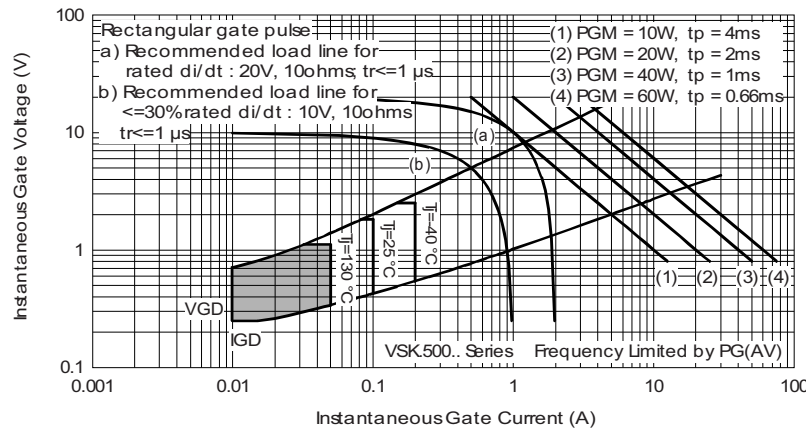


Fig. 12 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code	<b>VSK</b>	<b>T</b>	<b>500</b>	<b>-</b>	<b>16</b>	<b>PbF</b>
	①	②	③		④	⑤
	<b>1</b>	-	Module type			
	<b>2</b>	-	Circuit configuration (see end of datasheet)			
	<b>3</b>	-	Current rating			
	<b>4</b>	-	Voltage code x 100 = $V_{RRM}$ (see Voltage Ratings table)			
	<b>5</b>	-	Lead (Pb)-free			

### Note

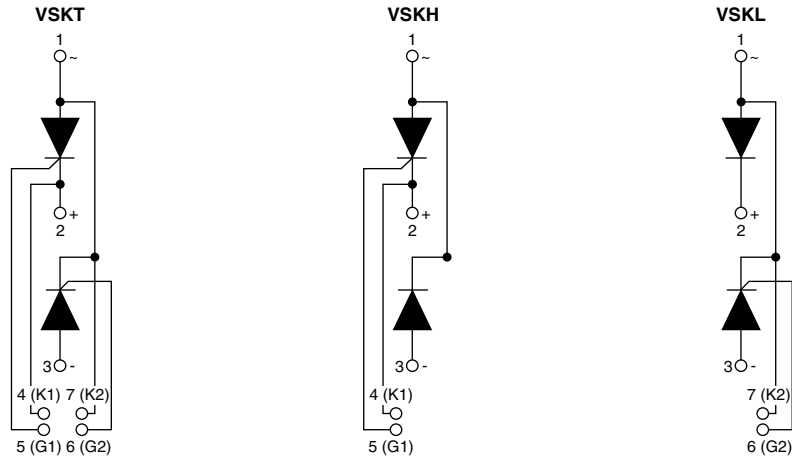
- To order the optional hardware go to [www.vishay.com/doc?95172](http://www.vishay.com/doc?95172)



# VSKT500-..PbF, VSKH500-..PbF, VSKL500-..PbF

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## CIRCUIT CONFIGURATION



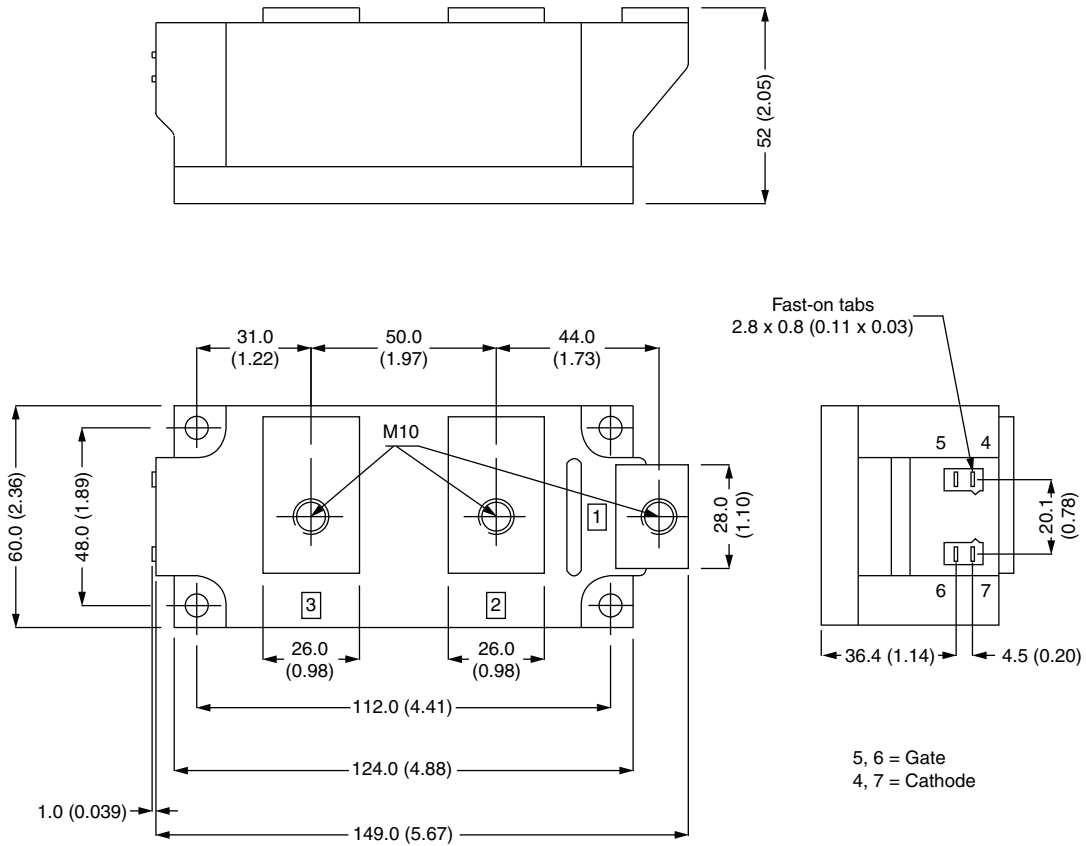
### LINKS TO RELATED DOCUMENTS

Dimensions

[www.vishay.com/doc?95283](http://www.vishay.com/doc?95283)

## Super MAGN-A-PAK Thyristor/Diode

**DIMENSIONS** in millimeters (inches)







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