

74HC109; 74HCT109

Dual JK flip-flop with set and reset; positive-edge-trigger

Rev. 4 — 1 April 2020

Product data sheet

1. General description

The 74HC109; 74HCT109 is a dual positive edge triggered $J\bar{K}$ flip-flop featuring individual nJ and n \bar{K} inputs. It has clock (nCP) inputs, set (n \bar{S} D) and reset (n \bar{R} D) inputs and complementary nQ and n \bar{Q} outputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The nJ and n \bar{K} inputs control the state changes of the flip-flops as described in the mode select function table. The nJ and n \bar{K} inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. The $J\bar{K}$ design allows operation as a D-type flip-flop by connecting the nJ and n \bar{K} inputs together. Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features and benefits

- Input levels:
 - For 74HC109: CMOS level
 - For 74HCT109: TTL level
- J and \bar{K} inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC109D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT109D				
74HC109DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT109DB				
74HCT109PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

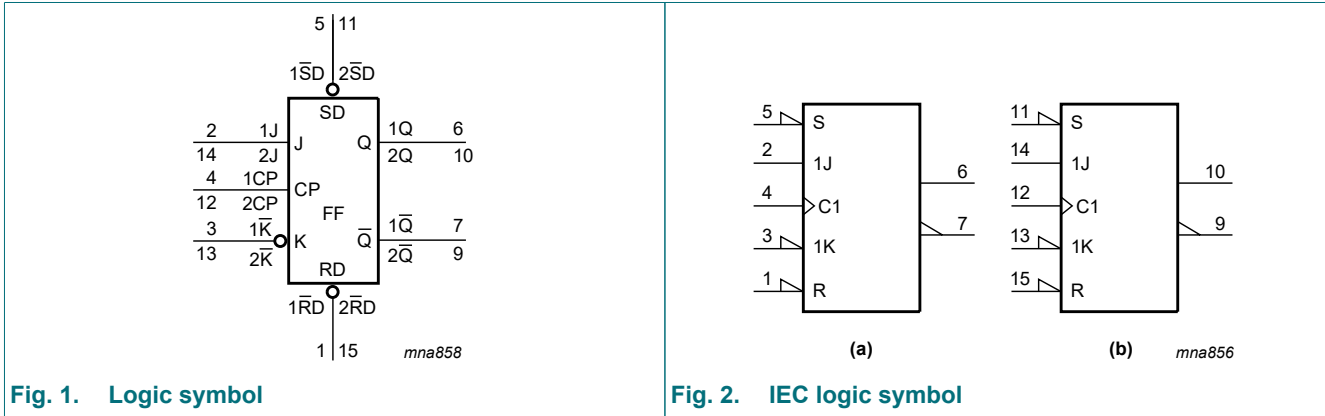


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

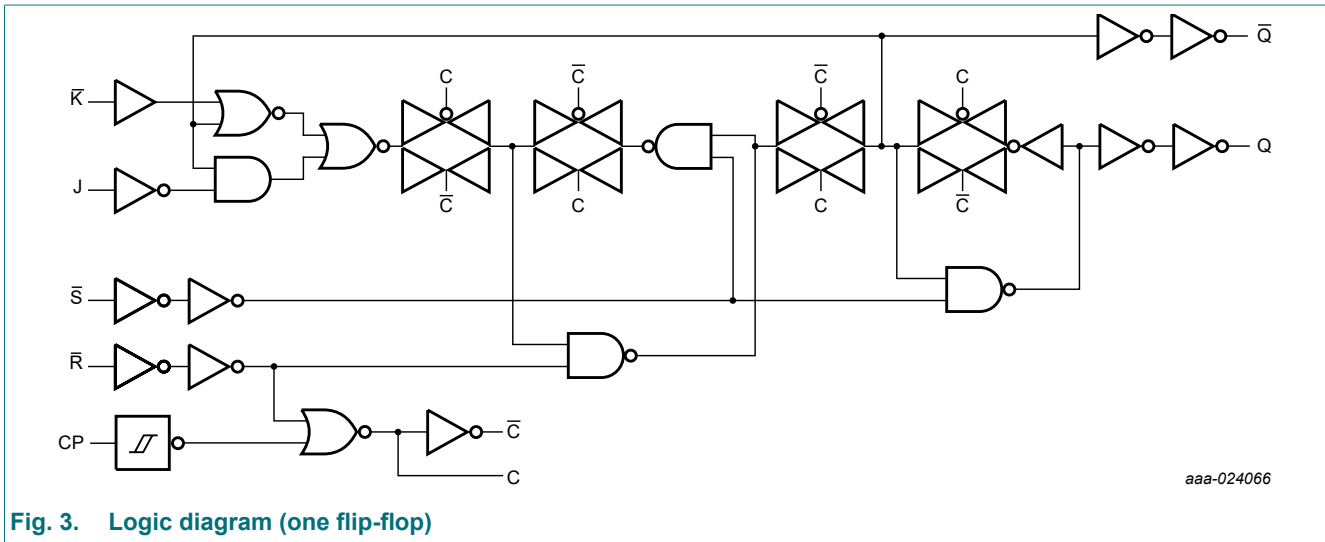
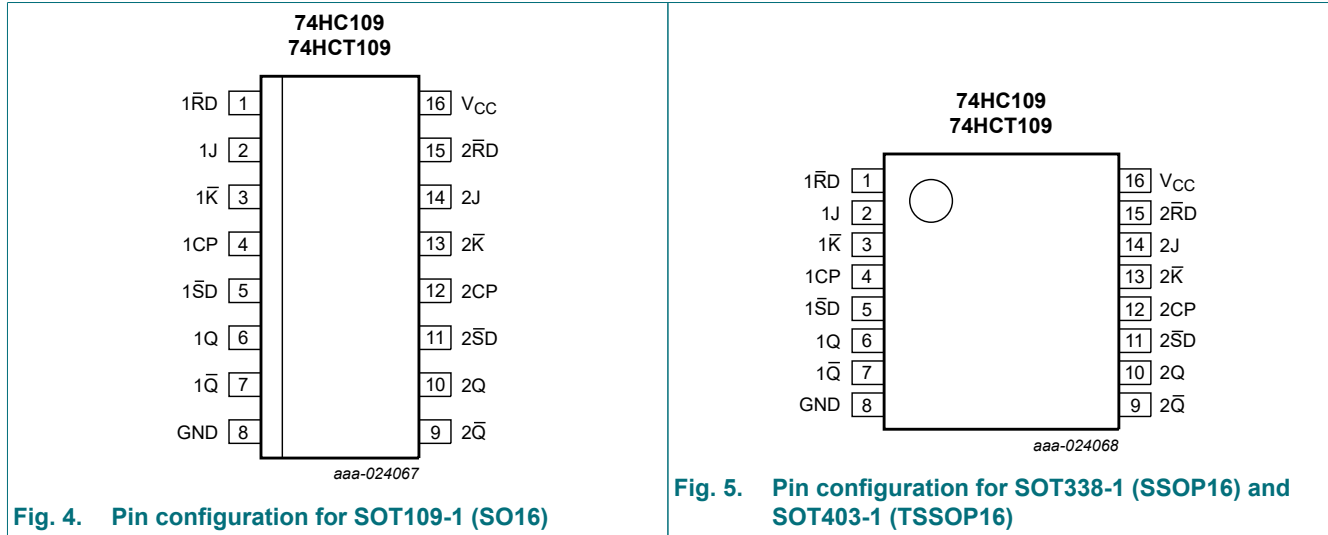


Fig. 3. Logic diagram (one flip-flop)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1 $\bar{R}D$, 2 $\bar{R}D$	1, 15	asynchronous reset input (active LOW)
1J, 2J	2, 14	synchronous input
1 \bar{K} , 2 \bar{K}	3, 13	synchronous input
1CP, 2CP	4, 12	clock input (LOW-to-HIGH; edge-triggered)
1 $\bar{S}D$, 2 $\bar{S}D$	5, 11	asynchronous set input (active LOW)
1Q, 2Q	6, 10	true flip-flop output
1 \bar{Q} , 2 \bar{Q}	7, 9	complement flip-flop output
GND	8	ground (0 V)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; h = HIGH voltage level one set-up time before the LOW-to-HIGH CP transition;

L = LOW voltage level; l = LOW voltage level one set-up time before the LOW-to-HIGH CP transition;

q = lower case letters indicate the state of the referenced output one set-up time before the LOW-to-HIGH CP transition;

X = don't care; ↑ = LOW-to-HIGH CP transition

Operating modes	Input					Output	
	nSD	nRD	nCP	nJ	nK	nQ	nQ̄
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	q̄	q
Load 0 (reset)	H	H	↑	l	l	L	H
Load 1 (set)	H	H	↑	h	h	H	L
Hold no change	H	H	↑	l	h	q	q̄

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
 For SOT338-1 (SSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
 For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC109			74HCT109			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC109										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$I_O = -5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
		$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
I_I	input leakage current	$I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	-	4.0	-	40	-	80	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Dual JK flip-flop with set and reset; positive-edge-trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT109										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		nJ, nK̄, nSD, nRD and nCP inputs	-	35	126	-	157.5	-	171.5	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74HC109										
t _{pd}	propagation delay	nCP to nQ, nQ̄; see Fig. 6 [2]								
		V _{CC} = 2.0 V	-	50	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	18	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	30	-	37	-	45	ns
t _{PLH}	LOW to HIGH propagation delay	nSD to nQ, see Fig. 7								
		V _{CC} = 2.0 V	-	30	120	-	150	-	180	ns
		V _{CC} = 4.5 V	-	11	24	-	30	-	36	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	9	20	-	26	-	31	ns

Dual JK flip-flop with set and reset; positive-edge-trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	n \overline{S} D to n \overline{Q} ; see Fig. 7								
		V _{CC} = 2.0 V	-	41	155	-	195	-	235	ns
		V _{CC} = 4.5 V	-	15	31	-	39	-	47	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	26	-	33	-	40	ns
t _{PHL}	HIGH to LOW propagation delay	n \overline{R} D to n \overline{Q} ; see Fig. 7								
		V _{CC} = 2.0 V	-	41	185	-	230	-	280	ns
		V _{CC} = 4.5 V	-	15	37	-	46	-	56	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	31	-	39	-	48	ns
t _{PLH}	LOW to HIGH propagation delay	n \overline{R} D to n \overline{Q} ; see Fig. 7								
		V _{CC} = 2.0 V	-	39	170	-	215	-	255	ns
		V _{CC} = 4.5 V	-	14	34	-	43	-	51	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	29	-	37	-	43	ns
t _t	transition time	n \overline{Q} , n \overline{Q} ; see Fig. 6 [3]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	nCP HIGH or LOW; see Fig. 6								
		V _{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		n \overline{S} D, n \overline{R} D HIGH or LOW; see Fig. 7								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	ns	
t _{rec}	recovery time	n \overline{S} D, n \overline{R} D to nCP; see Fig. 7								
		V _{CC} = 2.0 V	70	19	-	90	-	105	-	ns
		V _{CC} = 4.5 V	14	7	-	18	-	21	-	ns
		V _{CC} = 6.0 V	12	6	-	15	-	18	-	ns

Dual JK flip-flop with set and reset; positive-edge-trigger

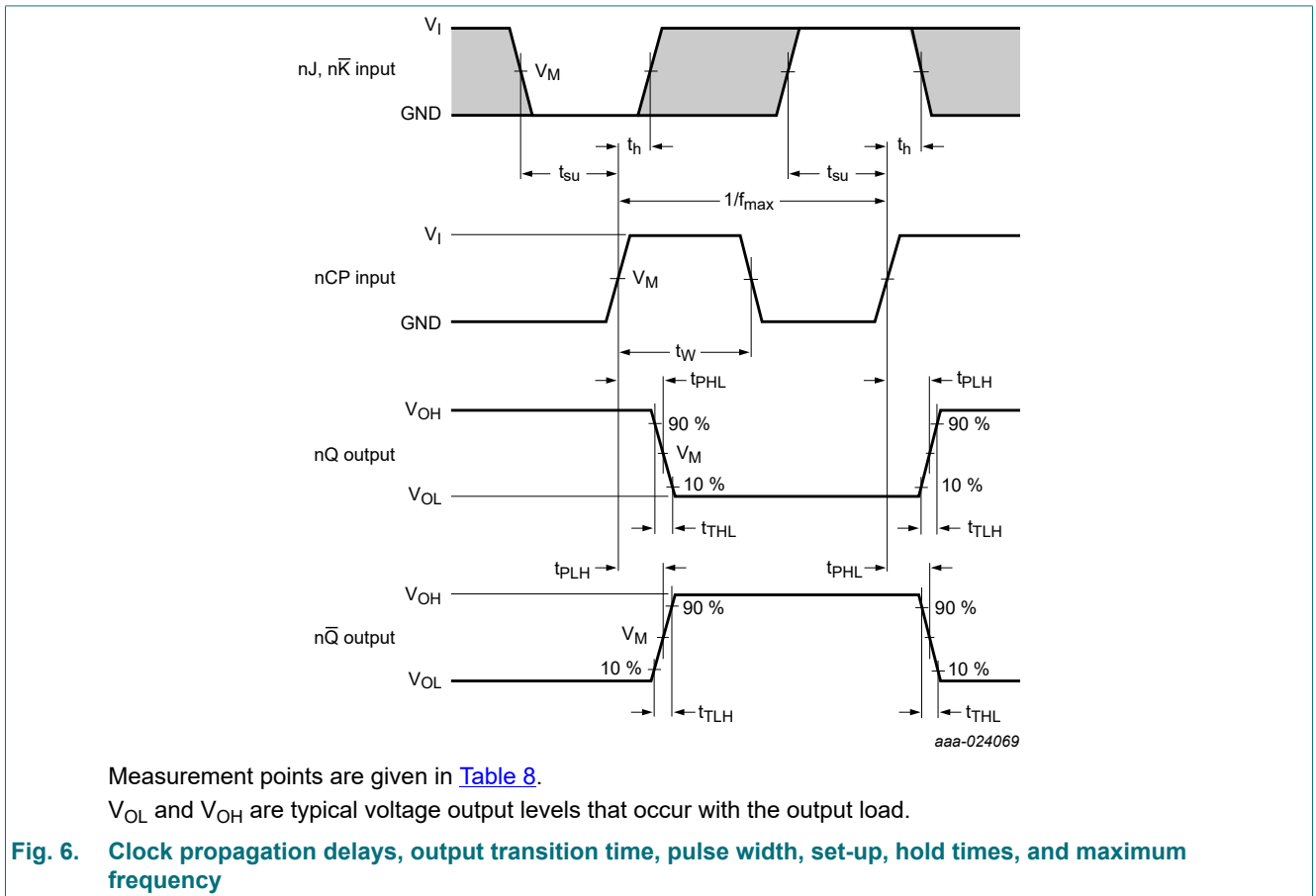
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _{su}	set-up time	nJ and n \bar{K} to nCP; see Fig. 6								
		V _{CC} = 2.0 V	70	17	-	90	-	105	-	ns
		V _{CC} = 4.5 V	14	6	-	18	-	21	-	ns
		V _{CC} = 6.0 V	12	5	-	15	-	18	-	ns
t _h	hold time	nJ and n \bar{K} to nCP; see Fig. 6								
		V _{CC} = 2.0 V	5	0	-	5	-	5	-	ns
		V _{CC} = 4.5 V	5	0	-	5	-	5	-	ns
		V _{CC} = 6.0 V	5	0	-	5	-	5	-	ns
f _{max}	maximum frequency	nCP; see Fig. 6								
		V _{CC} = 2.0 V	6	22	-	5	-	4	-	MHz
		V _{CC} = 4.5 V	30	68	-	24	-	20	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	75	-	-	-	-	-	MHz
	V _{CC} = 6.0 V	35	81	-	28	-	24	-	MHz	
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [4]	-	20	-	-	-	-	-	pF
74HCT109										
t _{pd}	propagation delay	nCP to nQ, n \bar{Q} ; see Fig. 6 [2]								
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
t _{PLH}	LOW to HIGH propagation delay	n \bar{S} D to nQ, see Fig. 7								
		V _{CC} = 4.5 V	-	13	26	-	33	-	39	ns
		V _{CC} = 5 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW propagation delay	n \bar{S} D to n \bar{Q} ; see Fig. 7								
		V _{CC} = 4.5 V	-	19	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW propagation delay	n \bar{R} D to nQ; see Fig. 7								
		V _{CC} = 4.5 V	-	19	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _{PLH}	LOW to HIGH propagation delay	n \bar{R} D to n \bar{Q} ; see Fig. 7								
		V _{CC} = 4.5 V	-	16	32	-	40	-	48	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _t	transition time	nQ, n \bar{Q} ; V _{CC} = 4.5 V; see Fig. 6 [3]	-	7	15	-	19	-	22	ns
t _w	pulse width	nCP HIGH or LOW; V _{CC} = 4.5 V; see Fig. 6	18	9	-	23	-	27	-	ns
		n \bar{S} D, n \bar{R} D HIGH or LOW; V _{CC} = 4.5 V; see Fig. 7	16	8	-	20	-	24	-	ns
t _{rec}	recovery time	n \bar{S} D, n \bar{R} D to nCP; V _{CC} = 4.5 V; see Fig. 7	16	8	-	20	-	24	-	ns

Dual JK flip-flop with set and reset; positive-edge-trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _{su}	set-up time	nJ and nK̄ to nCP; V _{CC} = 4.5 V; see Fig. 6	18	8	-	23	-	27	-	ns
t _h	hold time	nJ and nK̄ to nCP; V _{CC} = 4.5 V; see Fig. 6	3	-3	-	3	-	3	-	ns
f _{max}	maximum frequency	nCP; see Fig. 6								
		V _{CC} = 4.5 V	27	55	-	22	-	18	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	61	-	-	-	-	-	-
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [4]	-	22	-	-	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] t_t is the same as t_{THL} and t_{TLH}.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of outputs.

10.1. Waveforms and test circuit



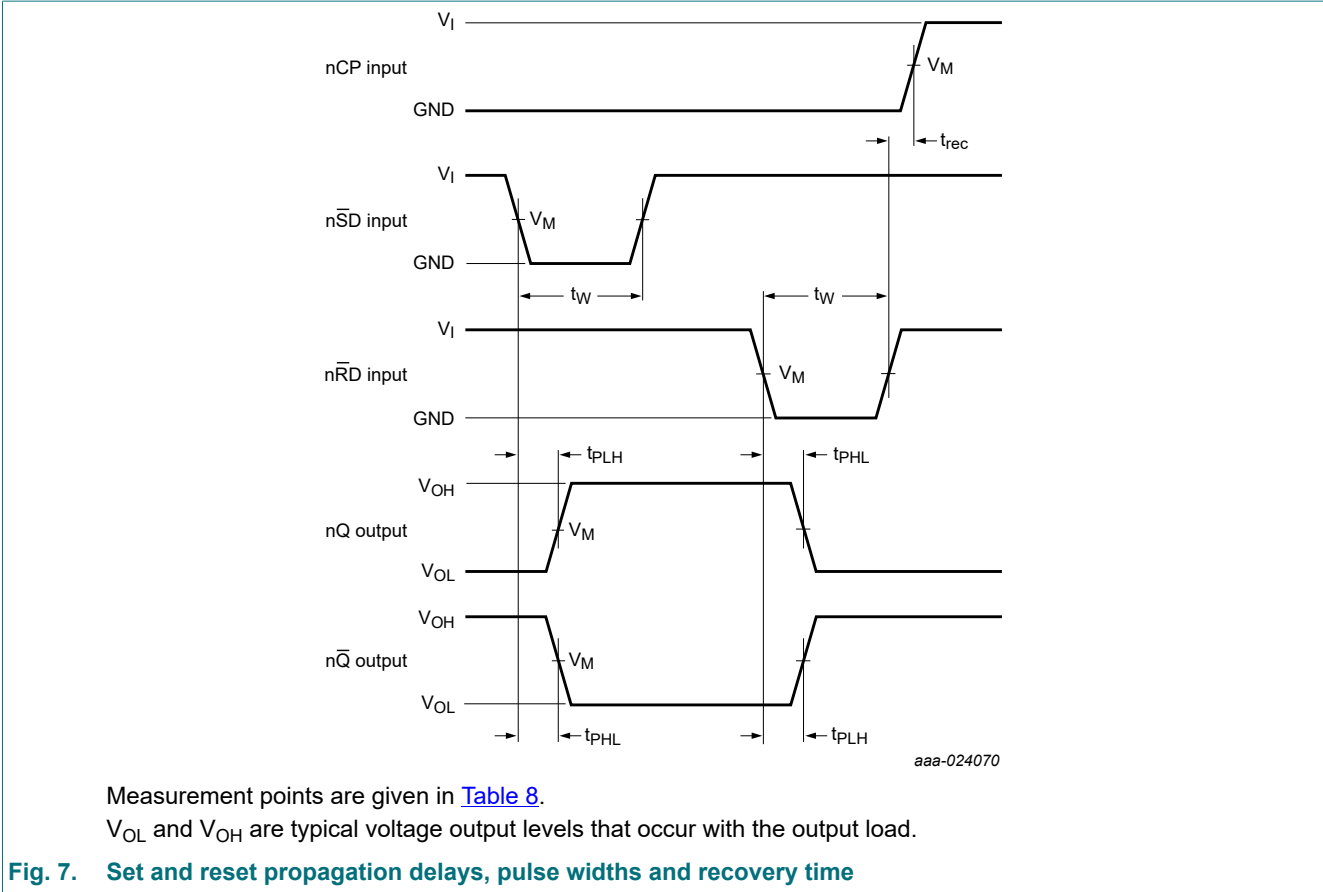
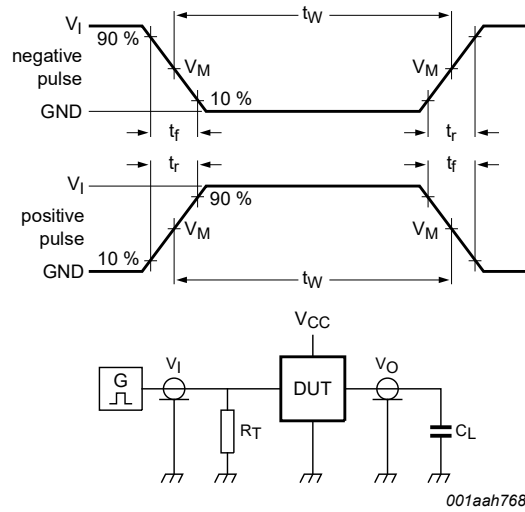


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC109	$0.5V_{CC}$	$0.5V_{CC}$
74HCT109	1.3 V	1.3 V

Dual JK flip-flop with set and reset; positive-edge-trigger



001aah768

Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC109	V_{CC}	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT109	3 V	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

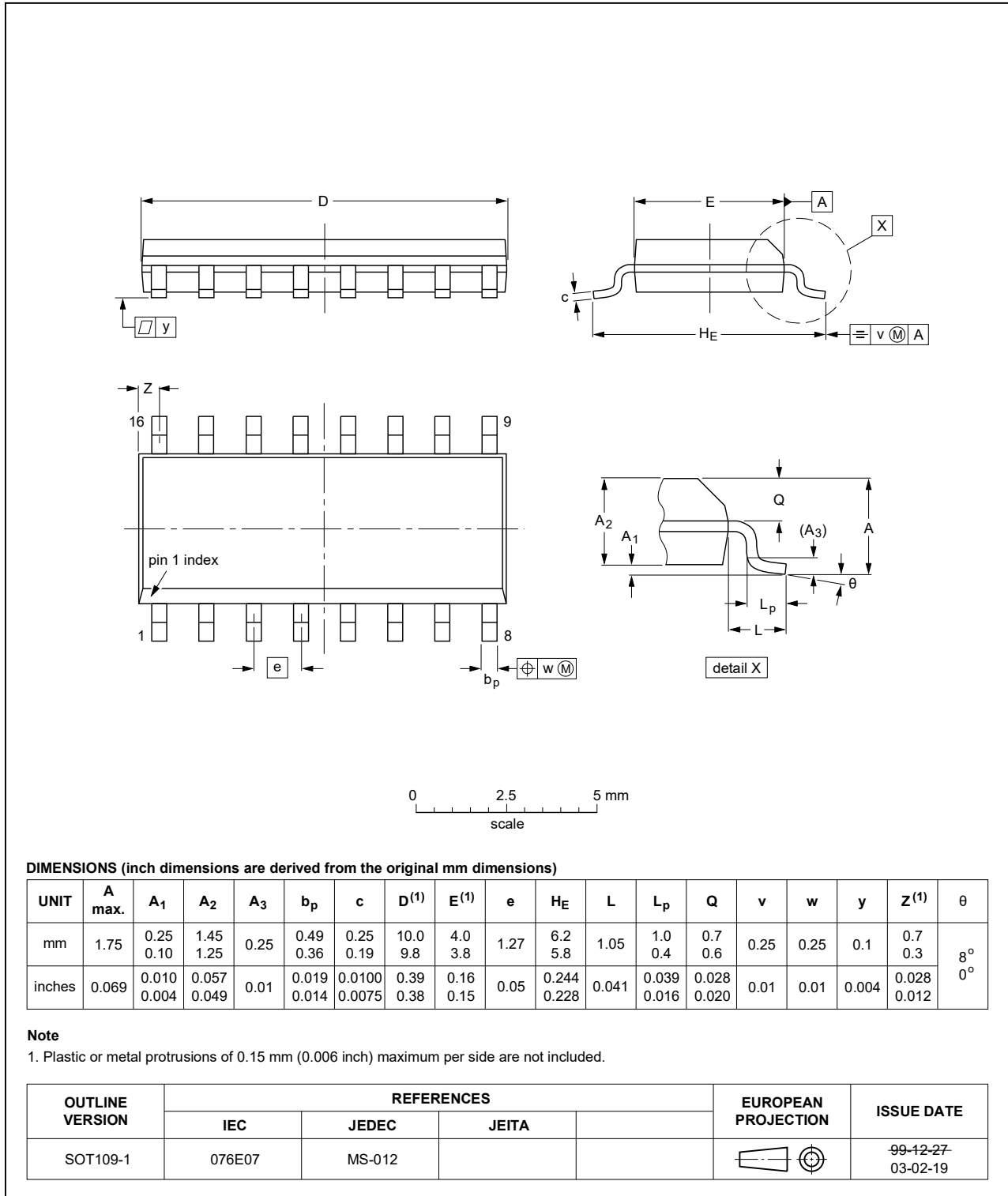


Fig. 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

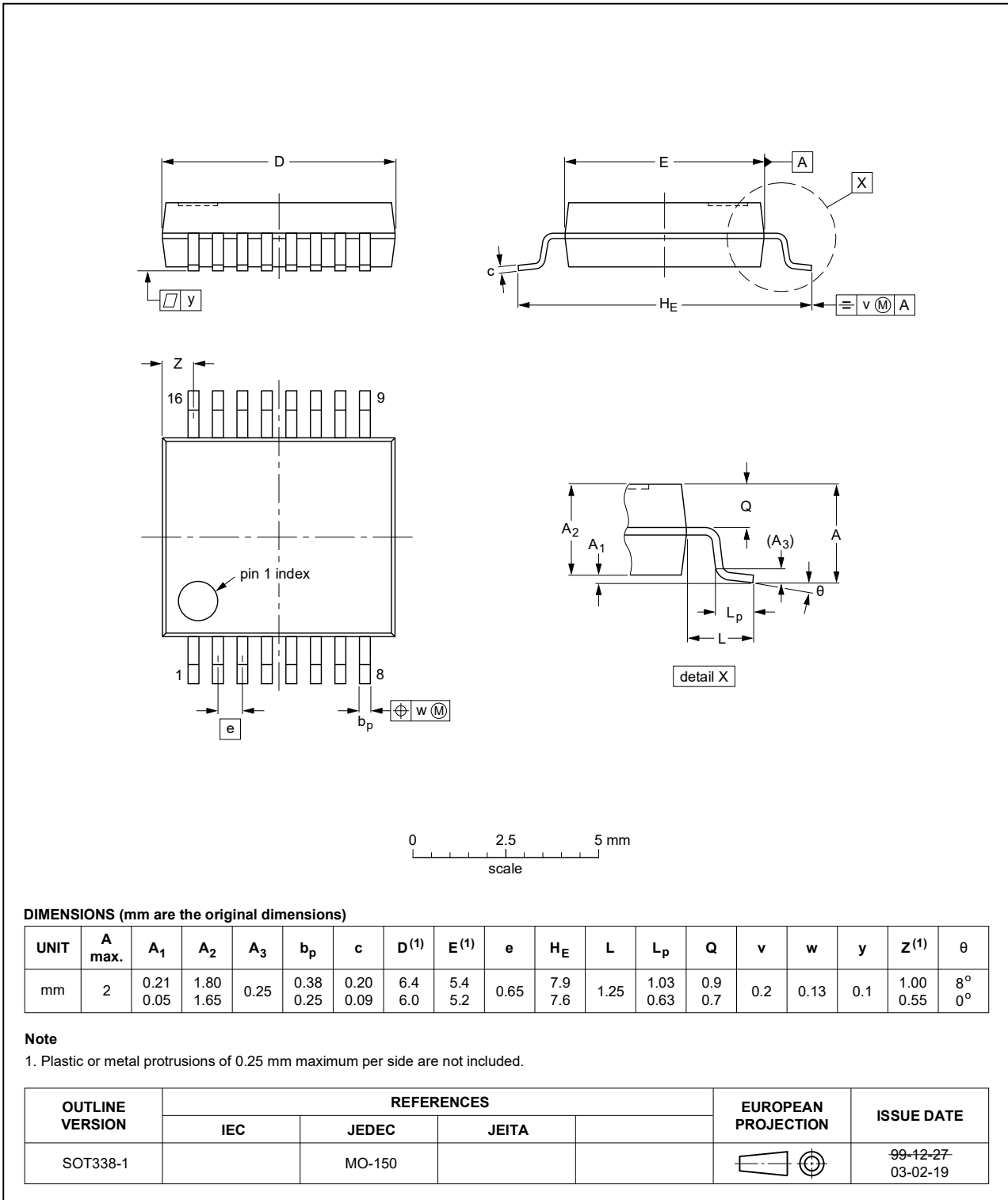


Fig. 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

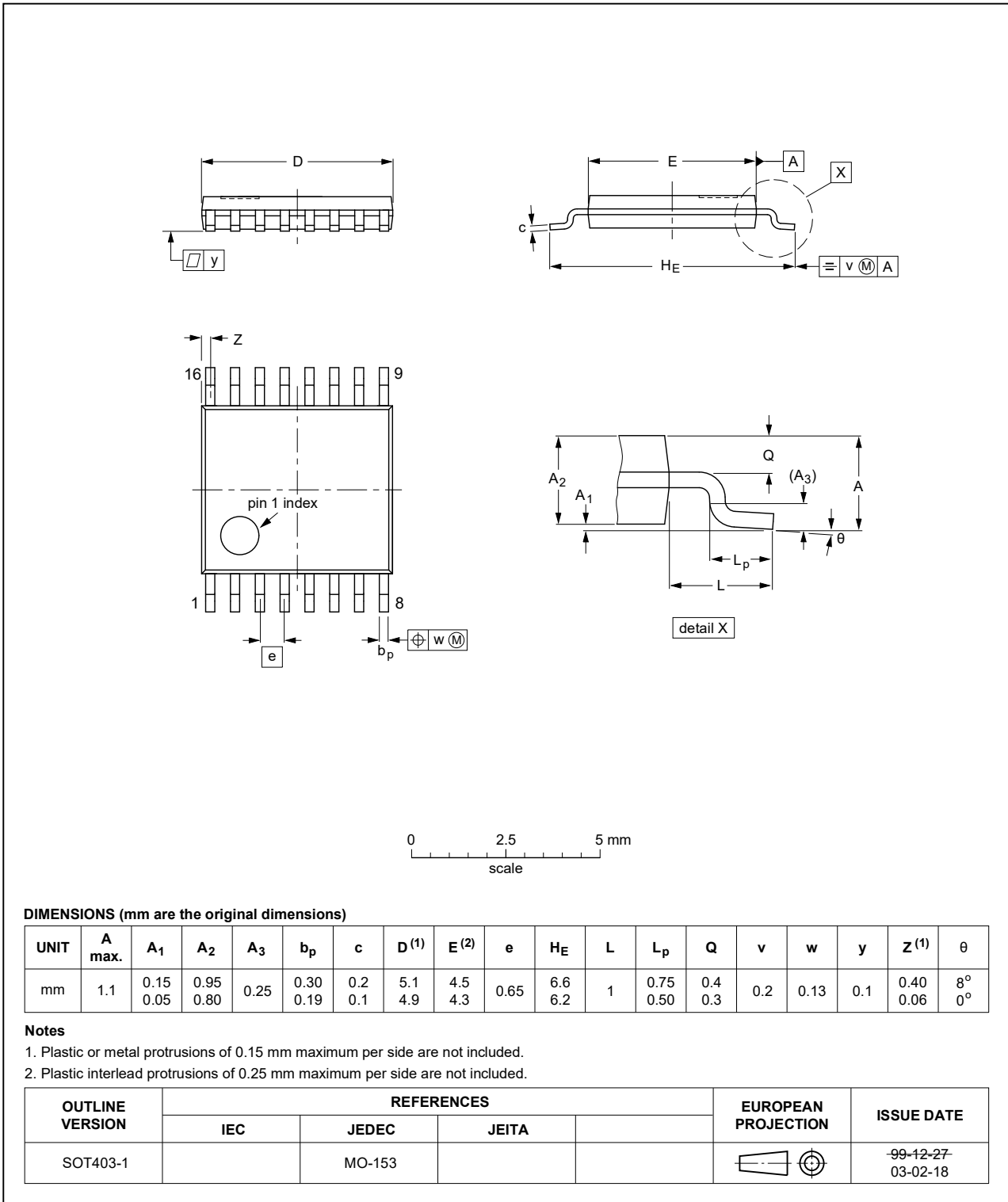


Fig. 11. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT109 v.4	20200401	Product data sheet	-	74HC_HCT109 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Table 4: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT109 v.3	20160801	Product data sheet	-	74HC_HCT109_CNV v.2
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74HC_HCT109_CNV v.2	19971125	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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