The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

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About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

MB95710M Series
MB95770M Series

New 8FX 8-bit Microcontrollers

The MB95710M/770M Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

Features

- F²MC-8FX CPU core
  - Instruction set optimized for controllers
    - Multiplication and division instructions
    - 16-bit arithmetic operations
    - Bit test branch instructions
    - Bit manipulation instructions, etc.
- Clock
  - Selectable main clock source
    - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    - Main CR clock (4 MHz ±2%)
    - Main CR PLL clock
      - The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.
      - The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.
      - The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.
      - The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.

      •Main PLL clock (up to 16.25 MHz, maximum machine clock frequency: 16.25 MHz)
  - Selectable subclock source
    - Suboscillation clock (32.768 kHz)
    - External clock (32.768 kHz)
    - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)
- Timer
  - 8/16-bit composite timer × 2 channels
  - 8/16-bit PPG × 2 channels
  - 16-bit reload timer × 1 channel
  - Event counter × 1 channel
  - Time-base timer × 1 channel
  - Watch counter × 1 channel
  - Watch prescaler × 1 channel
- UART/SIO × 3 channels
  - Full duplex double buffer
  - Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer
- I²C bus interface × 1 channel
  - Built-in wake-up function
- External interrupt × 8 channels
  - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/12-bit A/D converter × 8 channels
  - 8-bit or 12-bit resolution can be selected.
- LCD controller (LCDC)
  - On MB95F714J/F714M/F716J/F716M/F718J/F718M, LCD output can be selected from 40 SEG × 4 COM and 36 SEG × 8 COM.
  - On MB95F774J/F774M/F776J/F776M/F778J/F778M, LCD output can be selected from 32 SEG × 4 COM and 28 SEG × 8 COM.
  - Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software
  - Interrupt in sync with the LCD module frame frequency
  - Blinking function
  - Inverted display function
- Low power consumption (standby) modes
  - There are four standby modes as follows:
    - Stop mode
    - Sleep mode
    - Watch mode
    - Time-base timer mode
- I/O port
  - MB95F714J/F716J/F718J (number of I/O ports: 75)
    - General-purpose I/O ports (CMOS I/O): 71
    - General-purpose I/O ports (N-ch open drain): 4
  - MB95F714M/F716M/F718M (number of I/O ports: 74)
    - General-purpose I/O ports (CMOS I/O): 71
    - General-purpose I/O ports (N-ch open drain): 3
  - MB95F774J/F776J/F778J (number of I/O ports: 59)
    - General-purpose I/O ports (CMOS I/O): 55
    - General-purpose I/O ports (N-ch open drain): 4
  - MB95F774M/F776M/F778M (number of I/O ports: 58)
    - General-purpose I/O ports (CMOS I/O): 55
    - General-purpose I/O ports (N-ch open drain): 3
- On-chip debug
  - 1-wire serial control
  - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
  - Built-in hardware watchdog timer
  - Built-in software watchdog timer
- Power-on reset
  - A power-on reset is generated when the power is switched on.

- Low-voltage detection (LVD) circuit (only available on MB95F714J/F716J/F718J/F774J/F776J/F778J)
  - Built-in low-voltage detection function
- Comparator × 1 channel
- Clock supervisor counter
  - Built-in clock supervisor counter
- Dual operation Flash memory
  - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  - Protects the content of the Flash memory.

Contents

1. Product Line-up

1.1 MB95710M Series

Part number / Parameter	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	512 bytes	1 Kbyte	2 Kbyte	512 bytes	1 Kbyte	2 Kbyte
Power-on reset	Yes					
Low-voltage detection reset	Yes			No		
Reset input	Selected through software			With dedicated reset input		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O port : 75 • CMOS I/O : 71 • N-ch open drain : 4			• I/O port : 74 • CMOS I/O : 71 • N-ch open drain : 3		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (min) • The sub-CR clock can be used as the source clock of the software watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
8/12-bit A/D converter	8 channels					
	8-bit or 12-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					

Part number / Parameter	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M
UART/SIO	3 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.					
I^2C bus interface	1 channel					
	• Master/slave transmission and reception • It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.					
8/16-bit PPG	2 channels					
	• Each channel can be used as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • The counter operating clock can be selected from eight clock sources.					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes are available to use. • It can output square wave. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode					
Event counter	• The event counter function is implemented by configuring the 16-bit reload timer and 8/16-bit composite timer ch. 1. • When the event counter function is used, the 16-bit reload timer and 8/16-bit composite timer ch. 1 become unavailable.					
LCD controller (LCDC)	• COM output: 4 or 8 (max) (selectable) • SEG output: 36 or 40 (max) (selectable) - If the number of COM outputs is 4, the maximum number of SEG outputs is 40, and the maximum number of pixels that can be displayed 160 (4 × 40). - If the number of COM outputs is 8, the maximum number of SEG outputs is 36, and the maximum number of pixels that can be displayed 288 (8 × 36). • LCD drive power supply (bias) pins: 5 (max)					
	• Duty LCD mode • LCD standby mode • Blinking function • Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software • Interrupt in sync with the LCD module frame frequency • Inverted display function					
Watch counter	• Count clock: four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source is one second and the counter value is set to 60.)					
Watch prescaler	Eight different time intervals can be selected.					
Comparator	1 channel					

<table>
<tr><th>Part number
Parameter</th><th>MB95F714J</th><th>MB95F716J</th><th>MB95F718J</th><th>MB95F714M</th><th>MB95F716M</th><th>MB95F718M</th></tr>
<tr><td>Flash memory</td><td colspan="6">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="6">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="6">LQH080</td></tr>
</table>

1.2 MB95770M Series

Part number / Parameter	MB95F774J	MB95F776J	MB95F778J	MB95F774M	MB95F776M	MB95F778M
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	512 bytes	1 Kbyte	2 Kbyte	512 bytes	1 Kbyte	2 Kbyte
Power-on reset	Yes					
Low-voltage detection reset	Yes			No		
Reset input	Selected through software			Dedicated		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O port : 59 • CMOS I/O : 55 • N-ch open drain : 4			• I/O port : 58 • CMOS I/O : 55 • N-ch open drain : 3		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (min) • The sub-CR clock can be used as the source clock of the software watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
8/12-bit A/D converter	8 channels					
	8-bit or 12-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					

Part number / Parameter	MB95F774J	MB95F776J	MB95F778J	MB95F774M	MB95F776M	MB95F778M
UART/SIO	3 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.					
I^2C bus interface	1 channel					
	• Master/slave transmission and reception • It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.					
8/16-bit PPG	2 channels					
	• Each channel can be used as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • The counter operating clock can be selected from eight clock sources.					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes are available to use. • It can output square wave. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode					
Event counter	• The event counter function is implemented by configuring the 16-bit reload timer and 8/16-bit composite timer ch. 1. • When the event counter function is used, the 16-bit reload timer and 8/16-bit composite timer ch. 1 become unavailable.					
LCD controller (LCDC)	• COM output: 4 or 8 (max) (selectable) • SEG output: 28 or 32 (max) (selectable) - If the number of COM outputs is 4, the maximum number of SEG outputs is 32, and the maximum number of pixels that can be displayed 128 (4 × 32). - If the number of COM outputs is 8, the maximum number of SEG outputs is 28, and the maximum number of pixels that can be displayed 224 (8 × 28). • LCD drive power supply (bias) pins: 4 (max)					
	• Duty LCD mode • LCD standby mode • Blinking function • Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software • Interrupt in sync with the LCD module frame frequency • Inverted display function					
Watch counter	• Count clock: four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source is one second and the counter value is set to 60.)					
Watch prescaler	Eight different time intervals can be selected.					
Comparator	1 channel					

<table>
<tr><th>Part number
Parameter</th><th>MB95F774J</th><th>MB95F776J</th><th>MB95F778J</th><th>MB95F774M</th><th>MB95F776M</th><th>MB95F778M</th></tr>
<tr><td>Flash memory</td><td colspan="6">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="6">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="6">LQD064
LQG064</td></tr>
</table>

2. Packages And Corresponding Products

Part number / Package	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M
LQH080	O	O	O	O	O	O

Part number / Package	MB95F774J	MB95F776J	MB95F778J	MB95F774M	MB95F776M	MB95F778M
LQD064	O	O	O	O	O	O
LQG064	O	O	O	O	O	O

O: Available

3. Differences Among Products And Notes On Product Selection

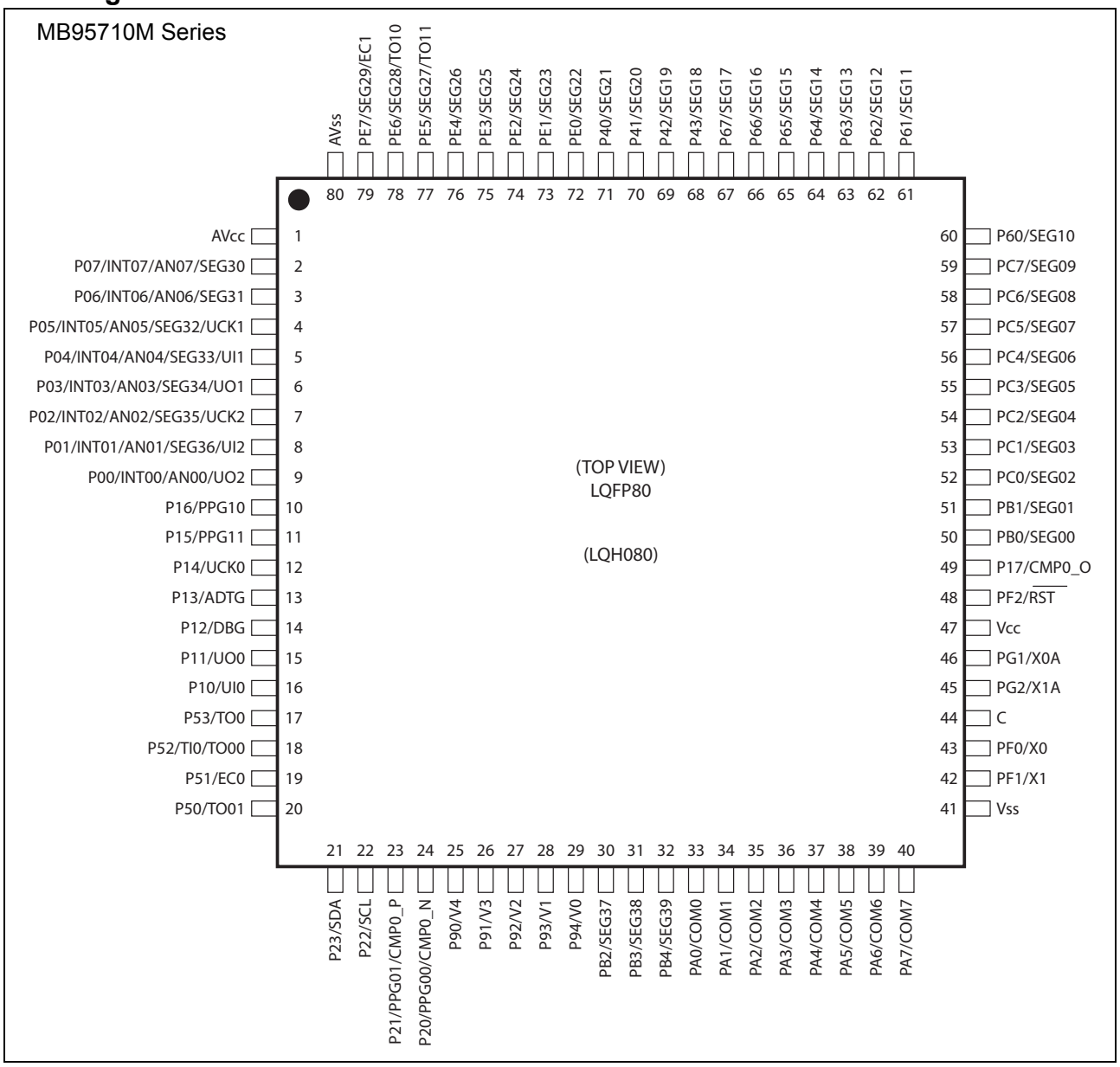
- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

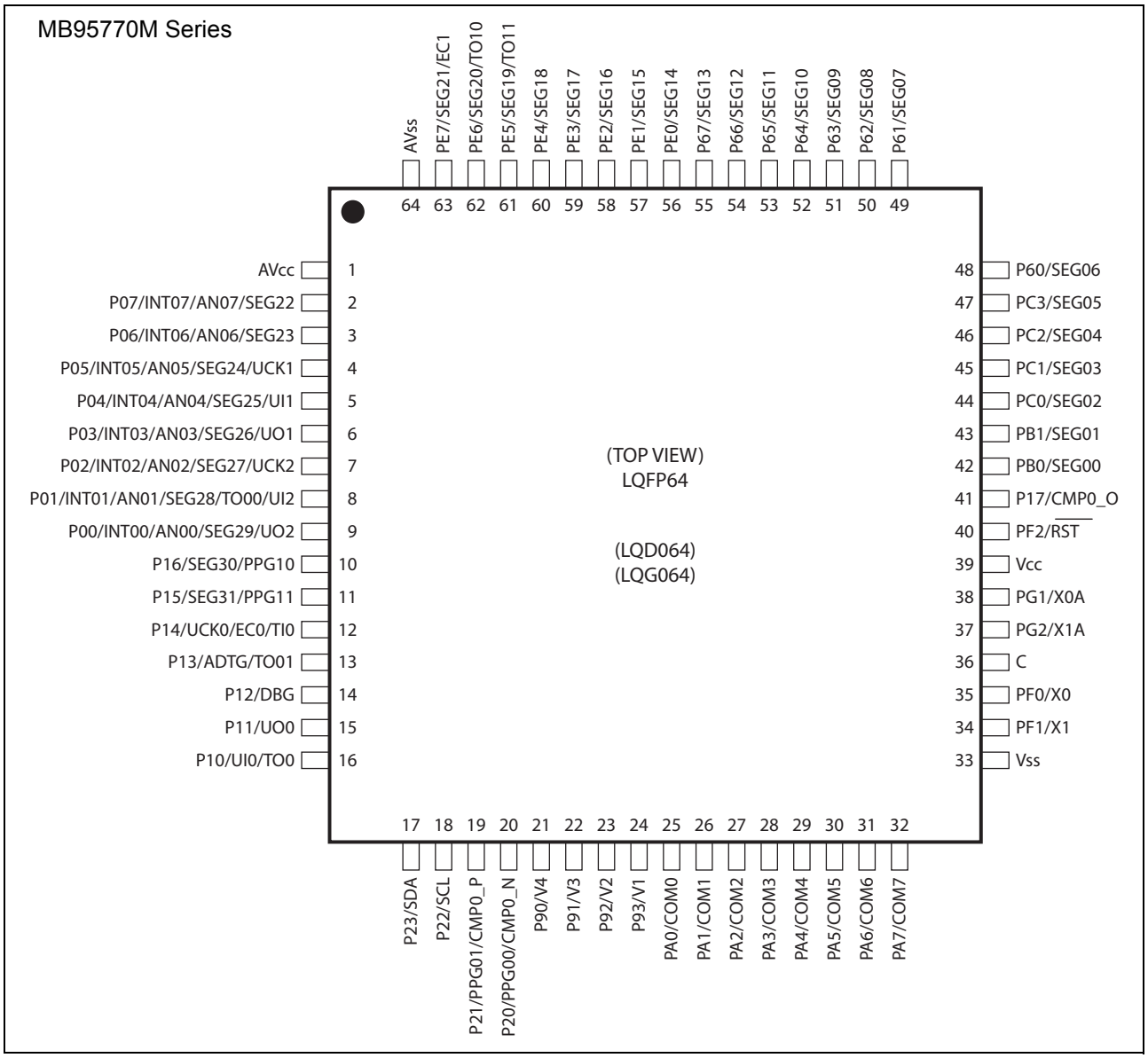
- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “Electrical Characteristics”.

- On-chip debug function
  The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 26 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95710M/770M Series Hardware Manual”.

4. Pin Assignment




MB95770M Series
AVss
PE7/SEG21/EC1
PE6/SEG20/TO10
PE5/SEG19/TO11
PE4/SEG18
PE3/SEG17
PE2/SEG16
PE1/SEG15
PE0/SEG14
P67/SEG13
P66/SEG12
P65/SEG11
P64/SEG10
P63/SEG09
P62/SEG08
P61/SEG07
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
P07/INT07/AN07/SEG22 2
P06/INT06/AN06/SEG23 3
P05/INT05/AN05/SEG24/UCK1 4
P04/INT04/AN04/SEG25/UI1 5
P03/INT03/AN03/SEG26/UO1 6
P02/INT02/AN02/SEG27/UCK2 7
P01/INT01/AN01/SEG28/TO00/UI2 8
P00/INT00/AN00/SEG29/UO2 9
P16/SEG30/PPG10 10
P15/SEG31/PPG11 11
P14/UCK0/EC0/TI0 12
P13/ADTG/TO01 13
P12/DBG 14
P11/UO0 15
P10/UI0/TO0 16
(TOP VIEW)
LQFP64
(LQD064)
(LQG064)
48 P60/SEG06
47 PC3/SEG05
46 PC2/SEG04
45 PC1/SEG03
44 PC0/SEG02
43 PB1/SEG01
42 PB0/SEG00
41 P17/CMP0_O
40 PF2/RST
39 Vcc
38 PG1/X0A
37 PG2/X1A
36 C
35 PF0/X0
34 PF1/X1
33 Vss
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
P23/SDA
P22/SCL
P21/PPG01/CMP0_P
P20/PPG00/CMP0_N
P90/V4
P91/V3
P92/V2
P93/V1
PA0/COM0
PA1/COM1
PA2/COM2
PA3/COM3
PA4/COM4
PA5/COM5
PA6/COM6
PA7/COM7

5. Pin Functions (MB95710M Series)

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
1	AVCC	—	Power supply pin for 8/12-bit A/D converter and comparator	—	—	—	—
2	P07	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT07		External interrupt input pin				
	AN07		8/12-bit A/D converter analog input pin				
	SEG30		LCDC SEG30 output pin				
3	P06	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT06		External interrupt input pin				
	AN06		8/12-bit A/D converter analog input pin				
	SEG31		LCDC SEG31 output pin				
4	P05	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT05		External interrupt input pin				
	AN05		8/12-bit A/D converter analog input pin				
	SEG32		LCDC SEG32 output pin				
	UCK1		UART/SIO ch. 1 clock I/O pin				
5	P04	V	General-purpose I/O port	CMOS/ analog	CMOS/ LCD	—	—
	INT04		External interrupt input pin				
	AN04		8/12-bit A/D converter analog input pin				
	SEG33		LCDC SEG33 output pin				
	UI1		UART/SIO ch. 1 data input pin				
6	P03	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT03		External interrupt input pin				
	AN03		8/12-bit A/D converter analog input pin				
	SEG34		LCDC SEG34 output pin				
	UO1		UART/SIO ch. 1 data output pin				
7	P02	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT02		External interrupt input pin				
	AN02		8/12-bit A/D converter analog input pin				
	SEG35		LCDC SEG35 output pin				
	UCK2		UART/SIO ch. 2 clock I/O pin				
8	P01	V	General-purpose I/O port	CMOS/ analog	CMOS/ LCD	—	—
	INT01		External interrupt input pin				
	AN01		8/12-bit A/D converter analog input pin				
	SEG36		LCDC SEG36 output pin				
	UI2		UART/SIO ch. 2 data input pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
9	P00	W	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT00		External interrupt input pin				
	AN00		8/12-bit A/D converter analog input pin				
	UO2		UART/SIO ch. 2 data output pin				
10	P16	Y	General-purpose I/O port	Hysteresis	CMOS	—	—
	PPG10		8/16-bit PPG ch. 1 output pin				
11	P15	Y	General-purpose I/O port	Hysteresis	CMOS	—	—
	PPG11		8/16-bit PPG ch. 1 output pin				
12	P14	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	UCK0		UART/SIO ch. 0 clock I/O pin				
13	P13	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	ADTG		8/12-bit A/D converter trigger input pin				
14	P12	D	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
15	P11	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	UO0		UART/SIO ch. 0 data output pin				
16	P10	G	General-purpose I/O port	CMOS	CMOS	—	O
	UI0		UART/SIO ch. 0 data input pin				
17	P53	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO0		16-bit reload timer ch. 0 output pin				
18	P52	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	TI0		16-bit reload timer ch. 0 input pin				
	TO00		8/16-bit composite timer ch. 0 output pin				
19	P51	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	EC0		8/16-bit composite timer ch. 0 clock input pin				
20	P50	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO01		8/16-bit composite timer ch. 0 output pin				
21	P23	I	General-purpose I/O port	CMOS	CMOS	O	—
	SDA		I^2C bus interface ch. 0 data I/O pin				
22	P22	I	General-purpose I/O port	CMOS	CMOS	O	—
	SCL		I^2C bus interface ch. 0 clock I/O pin				
23	P21	T	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	PPG01		8/16-bit PPG ch. 0 output pin				
	CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
24	P20	T	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	PPG00		8/16-bit PPG ch. 0 output pin				
	CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				
25	P90	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V4		LCD drive power supply pin				
26	P91	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V3		LCD drive power supply pin				
27	P92	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V2		LCD drive power supply pin				
28	P93	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V1		LCD drive power supply pin				
29	P94	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V0		LCD drive power supply pin				
30	PB2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG37		LCDC SEG37 output pin				
31	PB3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG38		LCDC SEG38 output pin				
32	PB4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG39		LCDC SEG39 output pin				
33	PA0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM0		LCDC COM0 output pin				
34	PA1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM1		LCDC COM1 output pin				
35	PA2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM2		LCDC COM2 output pin				
36	PA3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM3		LCDC COM3 output pin				
37	PA4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM4		LCDC COM4 output pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
38	PA5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM5		LCDC COM5 output pin				
39	PA6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM6		LCDC COM6 output pin				
40	PA7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM7		LCDC COM7 output pin				
41	V_{SS}	—	Power supply pin (GND)	—	—	—	—
42	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
43	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
44	C	—	Decoupling capacitor connection pin	—	—	—	—
45	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
46	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
47	V_{CC}	—	Power supply pin	—	—	—	—
48	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F714M/F716M/F718M				
49	P17	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	CMP0_O		Comparator ch. 0 digital output pin				
50	PB0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG00		LCDC SEG00 output pin				
51	PB1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG01		LCDC SEG01 output pin				
52	PC0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG02		LCDC SEG02 output pin				
53	PC1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG03		LCDC SEG03 output pin				
54	PC2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG04		LCDC SEG04 output pin				
55	PC3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG05		LCDC SEG05 output pin				
56	PC4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG06		LCDC SEG06 output pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
57	PC5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG07		LCDC SEG07 output pin				
58	PC6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG08		LCDC SEG08 output pin				
59	PC7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG09		LCDC SEG09 output pin				
60	P60	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG10		LCDC SEG10 output pin				
61	P61	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG11		LCDC SEG11 output pin				
62	P62	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG12		LCDC SEG12 output pin				
63	P63	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG13		LCDC SEG13 output pin				
64	P64	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG14		LCDC SEG14 output pin				
65	P65	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG15		LCDC SEG15 output pin				
66	P66	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG16		LCDC SEG16 output pin				
67	P67	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG17		LCDC SEG17 output pin				
68	P43	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG18		LCDC SEG18 output pin				
69	P42	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG19		LCDC SEG19 output pin				
70	P41	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG20		LCDC SEG20 output pin				
71	P40	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG21		LCDC SEG21 output pin				
72	PE0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG22		LCDC SEG22 output pin				
73	PE1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG23		LCDC SEG23 output pin				
74	PE2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG24		LCDC SEG24 output pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
75	PE3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG25		LCDC SEG25 output pin				
76	PE4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG26		LCDC SEG26 output pin				
77	PE5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG27		LCDC SEG27 output pin				
	TO11		8/16-bit composite timer ch. 1 output pin				
78	PE6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG28		LCDC SEG28 output pin				
	TO10		8/16-bit composite timer ch. 1 output pin				
79	PE7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG29		LCDC SEG27 output pin				
	EC1		8/16-bit composite timer ch. 1 clock input pin				
80	AV_{SS}	—	Power supply pin (GND) for 8/12-bit A/D converter and comparator	—	—	—	—

O: Available

*1: For the I/O circuit types, see “I/O Circuit Type”.
*2: N-ch open drain
*3: Pull-up

6. Pin Functions (MB95770M Series)

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
1	AVcc	—	Power supply pin for 8/12-bit A/D converter and comparator	—	—	—	—
2	P07	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT07		External interrupt input pin				
	AN07		8/12-bit A/D converter analog input pin				
	SEG22		LCDC SEG22 output pin				
3	P06	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT06		External interrupt input pin				
	AN06		8/12-bit A/D converter analog input pin				
	SEG23		LCDC SEG23 output pin				
4	P05	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT05		External interrupt input pin				
	AN05		8/12-bit A/D converter analog input pin				
	SEG24		LCDC SEG24 output pin				
	UCK1		UART/SIO ch. 1 clock I/O pin				
5	P04	V	General-purpose I/O port	CMOS/ analog	CMOS/ LCD	—	—
	INT04		External interrupt input pin				
	AN04		8/12-bit A/D converter analog input pin				
	SEG25		LCDC SEG25 output pin				
	UI1		UART/SIO ch. 1 data input pin				
6	P03	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT03		External interrupt input pin				
	AN03		8/12-bit A/D converter analog input pin				
	SEG26		LCDC SEG26 output pin				
	UO1		UART/SIO ch. 1 data output pin				
7	P02	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT02		External interrupt input pin				
	AN02		8/12-bit A/D converter analog input pin				
	SEG27		LCDC SEG27 output pin				
	UCK2		UART/SIO ch. 2 clock I/O pin				
8	P01	V	General-purpose I/O port	CMOS/ analog	CMOS/ LCD	—	—
	INT01		External interrupt input pin				
	AN01		8/12-bit A/D converter analog input pin				
	SEG28		LCDC SEG28 output pin				
	TO00		8/16-bit composite timer ch. 0 output pin				
	UI2		UART/SIO ch. 2 data input pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
9	P00	S	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT00		External interrupt input pin				
	AN00		8/12-bit A/D converter analog input pin				
	SEG29		LCDC SEG29 output pin				
	UO2		UART/SIO ch. 2 data output pin				
10	P16	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG30		LCDC SEG30 output pin				
	PPG10		8/16-bit PPG ch. 1 output pin				
11	P15	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG31		LCDC SEG31 output pin				
	PPG11		8/16-bit PPG ch. 1 output pin				
12	P14	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	UCK0		UART/SIO ch. 0 clock I/O pin				
	EC0		8/16-bit composite timer ch. 0 clock input pin				
	TI0		16-bit reload timer ch. 0 input pin				
13	P13	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	ADTG		8/12-bit A/D converter trigger input pin				
	TO01		8/16-bit composite timer ch. 0 output pin				
14	P12	D	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
15	P11	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	UO0		UART/SIO ch. 0 data output pin				
16	P10	G	General-purpose I/O port	CMOS	CMOS	—	O
	UI0		UART/SIO ch. 0 data input pin				
	TO0		16-bit reload timer ch. 0 output pin				
17	P23	I	General-purpose I/O port	CMOS	CMOS	O	—
	SDA		I^2C bus interface ch. 0 data I/O pin				
18	P22	I	General-purpose I/O port	CMOS	CMOS	O	—
	SCL		I^2C bus interface ch. 0 clock I/O pin				
19	P21	T	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	PPG01		8/16-bit PPG ch. 0 output pin				
	CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				
20	P20	T	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	PPG00		8/16-bit PPG ch. 0 output pin				
	CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
21	P90	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V4		LCD drive power supply pin				
22	P91	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V3		LCD drive power supply pin				
23	P92	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V2		LCD drive power supply pin				
24	P93	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V1		LCD drive power supply pin				
25	PA0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM0		LCDC COM0 output pin				
26	PA1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM1		LCDC COM1 output pin				
27	PA2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM2		LCDC COM2 output pin				
28	PA3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM3		LCDC COM3 output pin				
29	PA4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM4		LCDC COM4 output pin				
30	PA5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM5		LCDC COM5 output pin				
31	PA6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM6		LCDC COM6 output pin				
32	PA7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM7		LCDC COM7 output pin				
33	V_{SS}	—	Power supply pin (GND)	—	—	—	—
34	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
35	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
36	C	—	Decoupling capacitor connection pin	—	—	—	—
37	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				

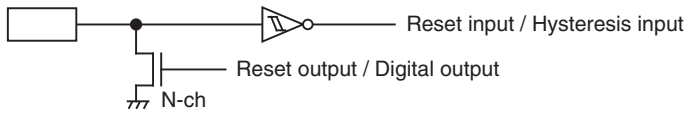
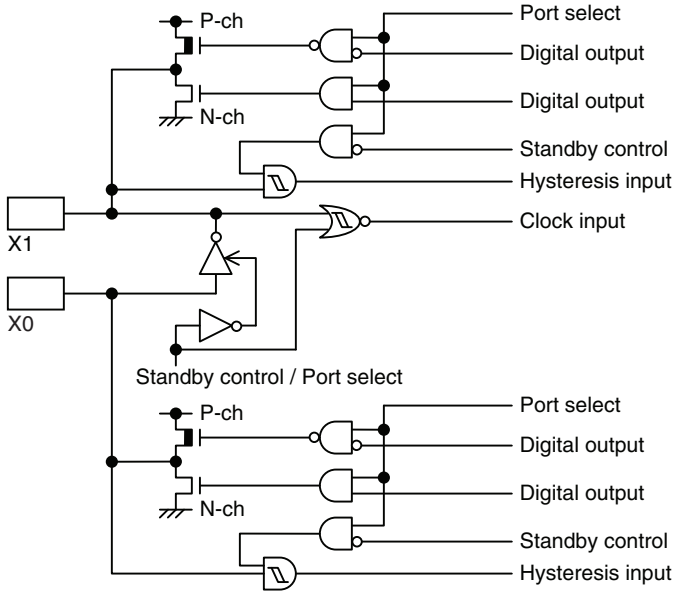
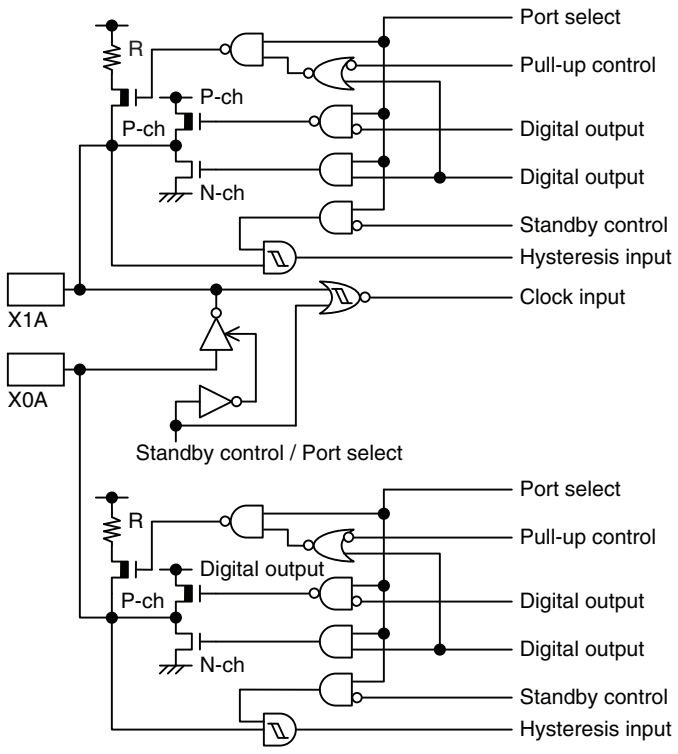
Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
38	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
39	V_{CC}	—	Power supply pin	—	—	—	—
40	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F774M/F776M/F778M				
41	P17	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	CMP0_O		Comparator ch. 0 digital output pin				
42	PB0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG00		LCDC SEG00 output pin				
43	PB1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG01		LCDC SEG01 output pin				
44	PC0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG02		LCDC SEG02 output pin				
45	PC1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG03		LCDC SEG03 output pin				
46	PC2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG04		LCDC SEG04 output pin				
47	PC3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG05		LCDC SEG05 output pin				
48	P60	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG06		LCDC SEG06 output pin				
49	P61	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG07		LCDC SEG07 output pin				
50	P62	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG08		LCDC SEG08 output pin				
51	P63	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG09		LCDC SEG09 output pin				
52	P64	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG10		LCDC SEG10 output pin				
53	P65	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG11		LCDC SEG11 output pin				
54	P66	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG12		LCDC SEG12 output pin				
55	P67	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG13		LCDC SEG13 output pin				

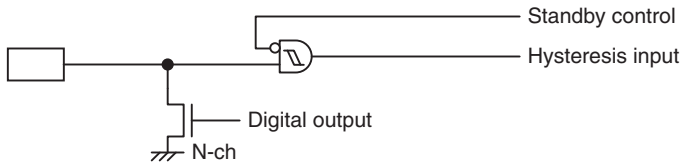
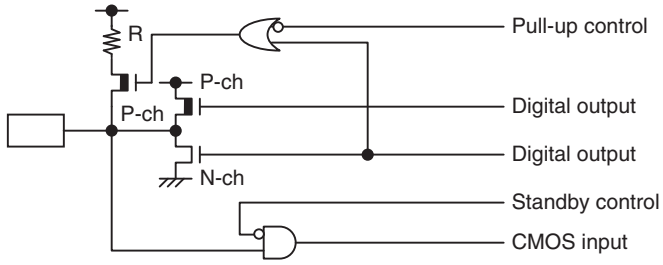
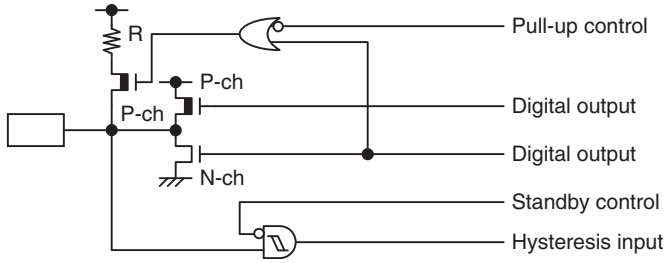
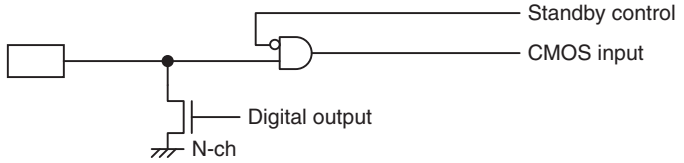
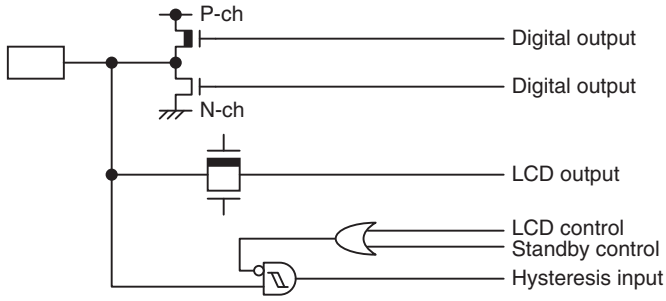
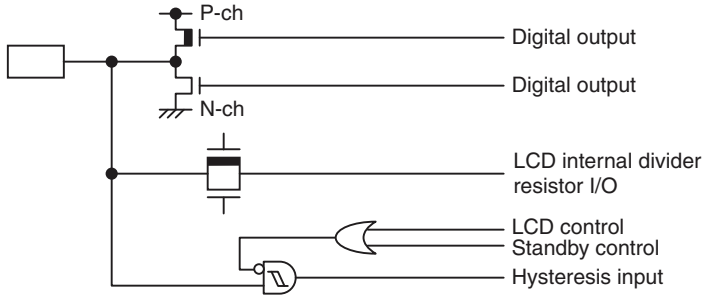
Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
56	PE0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG14		LCDC SEG14 output pin				
57	PE1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG15		LCDC SEG15 output pin				
58	PE2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG16		LCDC SEG16 output pin				
59	PE3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG17		LCDC SEG17 output pin				
60	PE4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG18		LCDC SEG18 output pin				
61	PE5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG19		LCDC SEG19 output pin				
	TO11		8/16-bit composite timer ch. 1 output pin				
62	PE6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG20		LCDC SEG20 output pin				
	TO10		8/16-bit composite timer ch. 1 output pin				
63	PE7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG21		LCDC SEG21 output pin				
	EC1		8/16-bit composite timer ch. 1 clock input pin				
64	AVSS	—	Power supply pin (GND) for 8/12-bit A/D converter and comparator	—	—	—	—

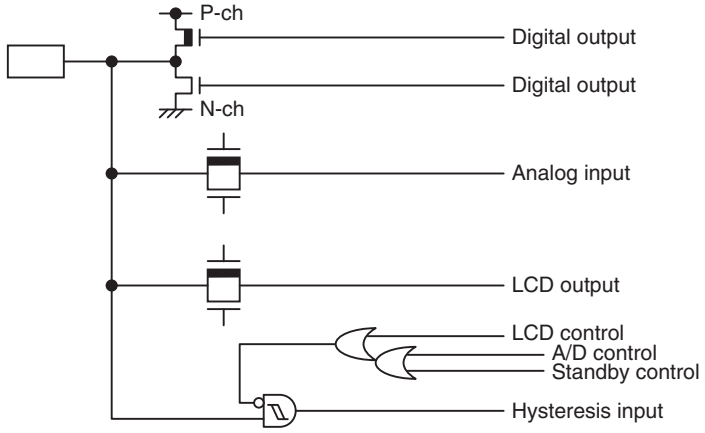
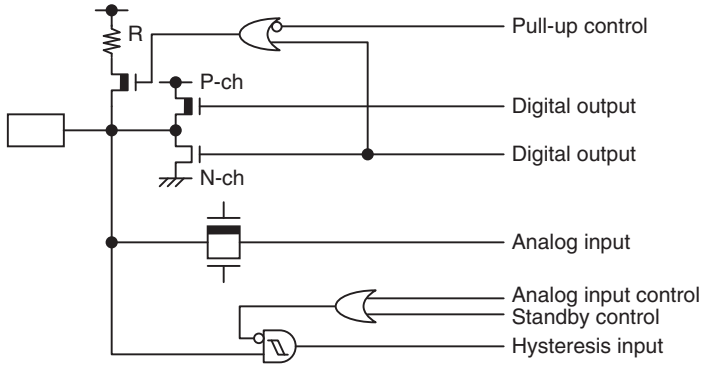
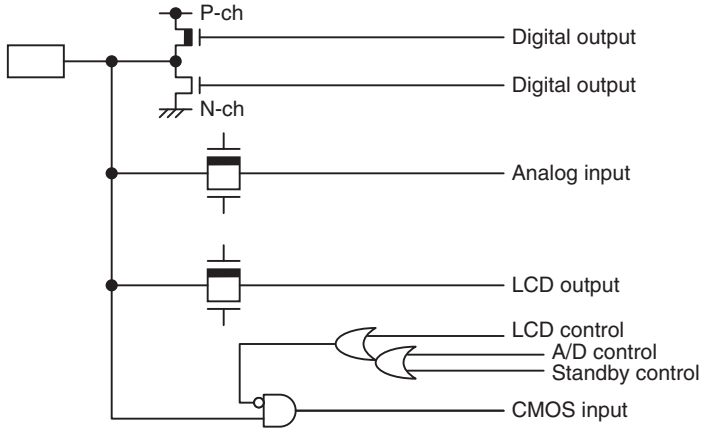
O: Available

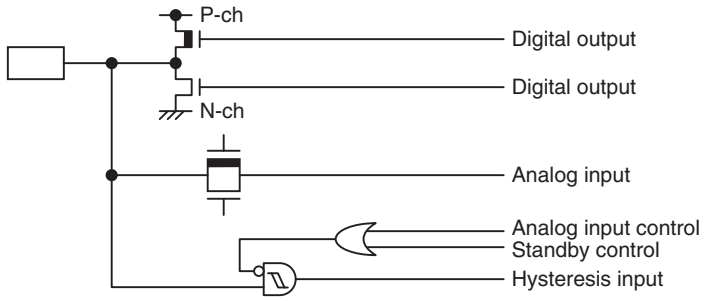
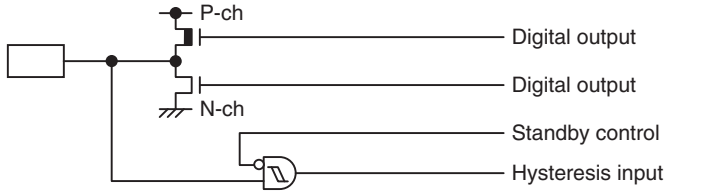
*1: For the I/O circuit types, see “I/O Circuit Type”.
*2: N-ch open drain
*3: Pull-up

7. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control

Type	Circuit	Remarks
D		• N-ch open drain output • Hysteresis input
G		• CMOS output • CMOS input • Pull-up control
H		• CMOS output • Hysteresis input • Pull-up control
I		• N-ch open drain output • CMOS input
M		• CMOS output • LCD output • Hysteresis input
R		• CMOS output • LCD power supply • Hysteresis input

Type	Circuit	Remarks
S		• CMOS output • LCD output • Hysteresis input • Analog input
T		• CMOS output • Hysteresis input • Analog input • Pull-up control
V		• CMOS output • CMOS input • LCD output • Analog input

Type	Circuit	Remarks
W		• CMOS output • Hysteresis input • Analog input
Y		• CMOS output • Hysteresis input

8. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

  Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- **Lead-Free Packaging**

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

  Condition: 125°C/24 h

- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%.
  Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

8.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

9. Notes On Device Handling

- Preventing latch-ups
  When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
  In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “22.1 Absolute Maximum Ratings” of “Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
  When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage
  Supply voltage must be stabilized.
  A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
  As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock
  When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub-clock mode or stop mode.

10. Pin Connection

- Treatment of unused pins
  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins
  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 1.0 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin
  Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.
  After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.
  The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

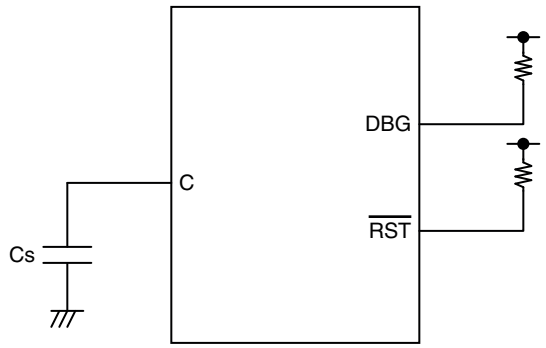
- $\overline{\text{RST}}$ pin
  Connect the $\overline{\text{RST}}$ pin to an external pull-up resistor of 2 kΩ or above.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{\text{RST}}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.
  The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general-purpose I/O function can be selected by the RSTEN bit in the SYSC register.

- Analog power supply
  Always set the same potential to the AV_{CC} pin and the V_{CC} pin. When V_{CC} is larger than AV_{CC}, the current may flow through the AN00 to AN07 pins.

- Treatment of power supply pins on the 8/12-bit A/D converter
  Ensure that AV_{CC} is equal to V_{CC} and AV_{SS} equal to V_{SS} even when the 8/12-bit A/D converter is not in use.
  Noise riding on the AV_{CC} pin may cause accuracy degradation. Therefore, connect a ceramic capacitor of 0.1 µF (approx.) as a bypass capacitor between the AV_{CC} pin and the AV_{SS} pin in the vicinity of this device.

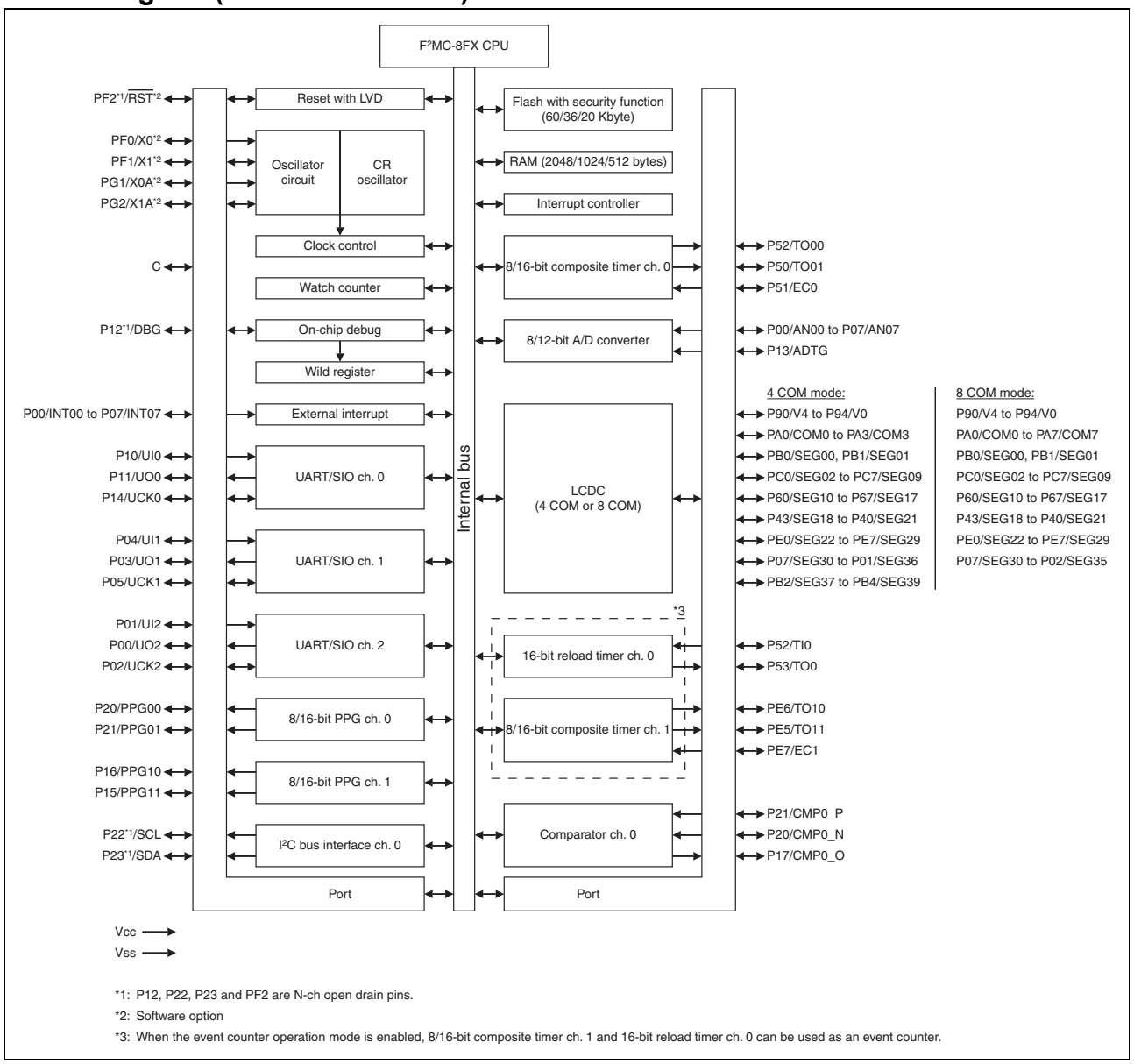
- C pin
  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/$\overline{\text{RST}}$/C pins connection diagram



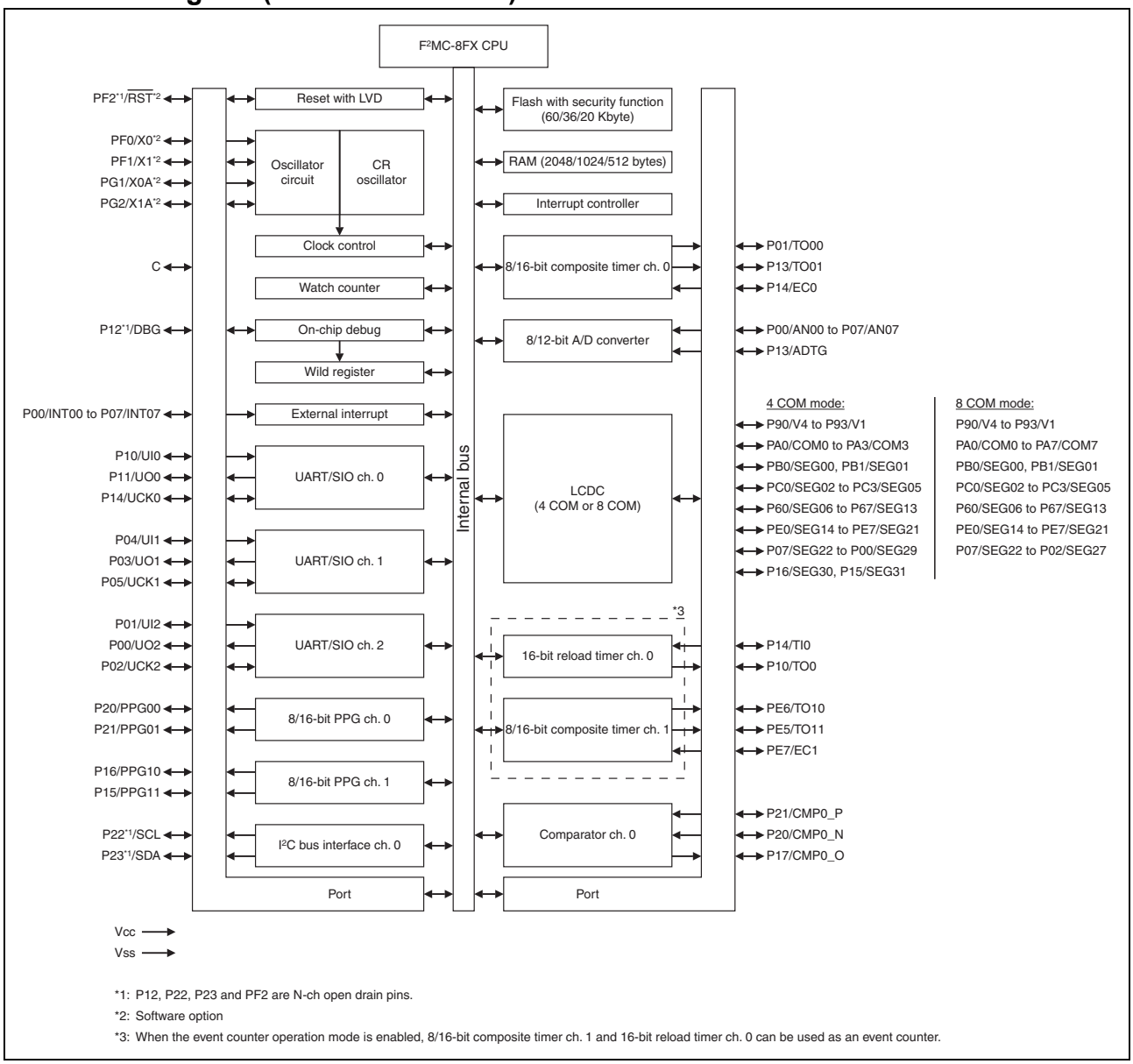
- Note on serial communication
  In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

11. Block Diagram (MB95710M Series)



*1: P12, P22, P23 and PF2 are N-ch open drain pins.
*2: Software option
*3: When the event counter operation mode is enabled, 8/16-bit composite timer ch. 1 and 16-bit reload timer ch. 0 can be used as an event counter.

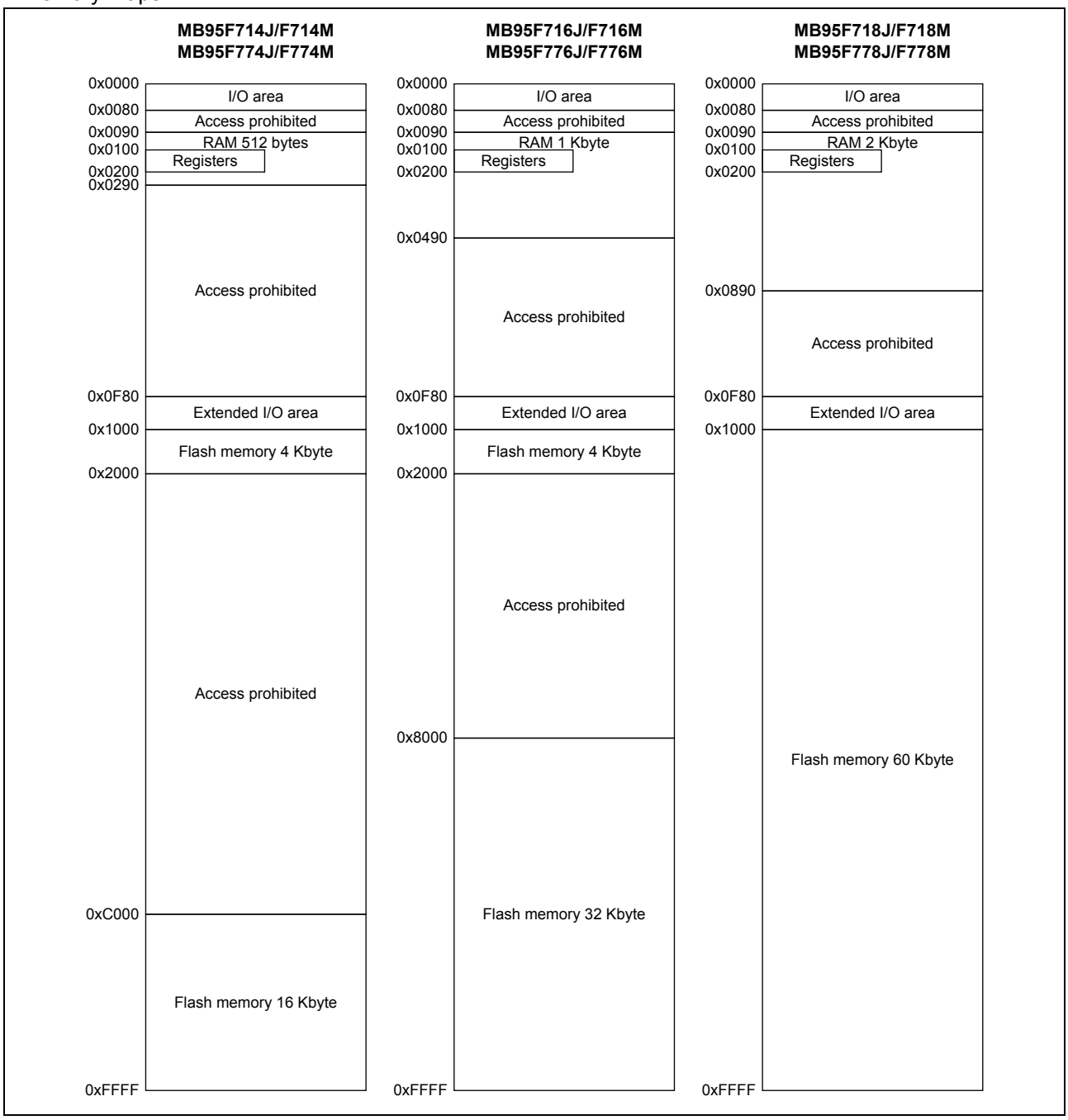
12. Block Diagram (MB95770M Series)



*1: P12, P22, P23 and PF2 are N-ch open drain pins.
*2: Software option
*3: When the event counter operation mode is enabled, 8/16-bit composite timer ch. 1 and 16-bit reload timer ch. 0 can be used as an event counter.

13. CPU Core

- Memory space
  The memory space of the MB95710M/770M Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95710M/770M Series are shown below.
- Memory maps



14. Memory Space

The memory space of the MB95710M/770M Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas for specific applications such as general-purpose registers and a vector table.

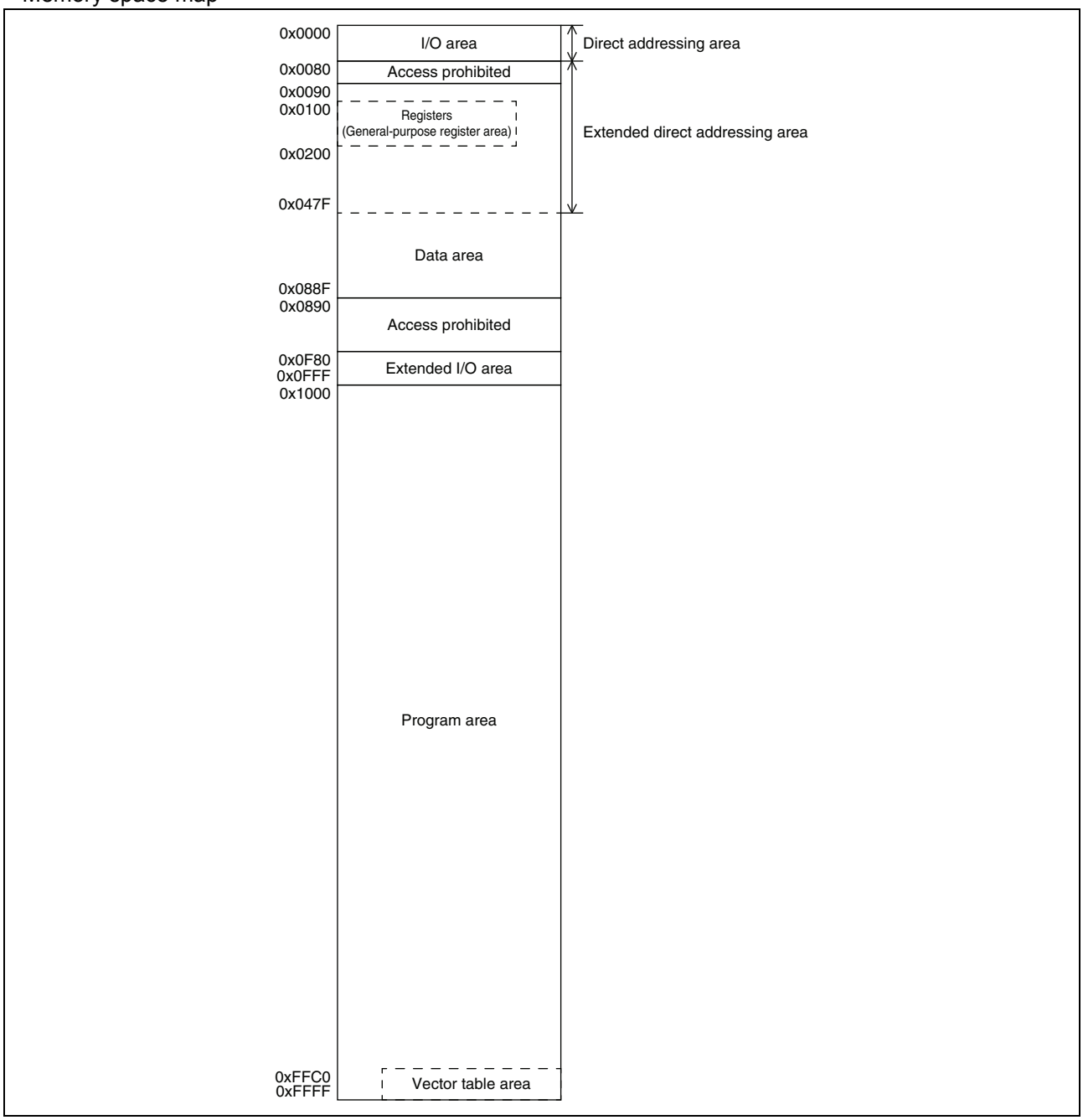
- I/O area (addresses: 0x0000 to 0x007F)
  - This area contains the control registers and data registers for built-in peripheral functions.
  - As the I/O area forms part of the memory space, it can be accessed in the same way as the memory. It can also be accessed at high-speed by using direct addressing instructions.

- Extended I/O area (addresses: 0x0F80 to 0x0FFF)
  - This area contains the control registers and data registers for built-in peripheral functions.
  - As the extended I/O area forms part of the memory space, it can be accessed in the same way as the memory.

- Data area
  - Static RAM is incorporated in the data area as the internal data area.
  - The internal RAM size varies according to product.
  - The RAM area from 0x0090 to 0x00FF can be accessed at high-speed by using direct addressing instructions.
  - In MB95F716J/F716M/F718J/F718M/F776J/F776M/F778J/F778M, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
  - In MB95F714J/F714M/F774J/F774M, the area from 0x0090 to 0x028F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
  - The area from 0x0100 to 0x01FF can be used as a general-purpose register area.

- Program area
  - The Flash memory is incorporated in the program area as the internal program area.
  - The Flash memory size varies according to product.
  - The area from 0xFFC0 to 0xFFFF is used as the vector table.
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register.

- Memory space map



15. Areas For Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

- General-purpose register area (Addresses: 0x0100 to 0x01FF)
  - This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
  - As this area forms part of the RAM area, it can also be used as conventional RAM.
  - When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.

- Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to “CHAPTER 28 NON-VOLATILE REGISTER (NVR) INTERFACE” in “New 8FX MB95710M/770M Series Hardware Manual”

- Vector table area (Addresses: 0xFFC0 to 0xFFFF)
  - This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
  - The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

  “Interrupt Source Table” lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.
  For details, refer to “CHAPTER 4 RESET”, “CHAPTER 5 INTERRUPTS”, and “A.2 Special Instruction ■ Special Instruction ● CALLV #vct” in “APPENDIX” in “New 8FX MB95710M/770M Series Hardware Manual”.

- Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (Initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001	0x0080 to 0x00FF	0x0100 to 0x017F
0b010		0x0180 to 0x01FF
0b011		0x0200 to 0x027F
0b100		0x0280 to 0x02FF*
0b101		0x0300 to 0x037F
0b110		0x0380 to 0x03FF
0b111		0x0400 to 0x047F

*: Due to the memory size limit, the available access area is up to “0x028F” in MB95F714J/F714M/F774J/F774M.

16. I/O Map (MB95710M Series)

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	PDR2	Port 2 data register	R/W	0b00000000
0x000F	DDR2	Port 2 direction register	R/W	0b00000000
0x0010, 0x0011	—	(Disabled)	—	—
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014	PDR5	Port 5 data register	R/W	0b00000000
0x0015	DDR5	Port 5 direction register	R/W	0b00000000
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x001B	—	(Disabled)	—	—
0x001C	PDR9	Port 9 data register	R/W	0b00000000
0x001D	DDR9	Port 9 direction register	R/W	0b00000000
0x001E	PDRA	Port A data register	R/W	0b00000000
0x001F	DDRA	Port A direction register	R/W	0b00000000
0x0020	PDRB	Port B data register	R/W	0b00000000
0x0021	DDRB	Port B direction register	R/W	0b00000000
0x0022	PDRC	Port C data register	R/W	0b00000000
0x0023	DDRC	Port C direction register	R/W	0b00000000
0x0024, 0x0025	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x0026	PDRE	Port E data register	R/W	0b00000000
0x0027	DDRE	Port E direction register	R/W	0b00000000
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	—	(Disabled)	—	—
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E	PUL2	Port 2 pull-up register	R/W	0b00000000
0x002F, 0x0030	—	(Disabled)	—	—
0x0031	PUL5	Port 5 pull-up register	R/W	0b00000000
0x0032 to 0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	TMCSRH0	16-bit reload timer control status register (upper) ch. 0	R/W	0b00000000
0x003F	TMCSRL0	16-bit reload timer control status register (lower) ch. 0	R/W	0b00000000
0x0040 to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	—	(Disabled)	—	—
0x004E	LVDC	LVD control register	R/W	0b00000100
0x004F	LCDCC2	LCDC control register 2	R/W	0b00010100
0x0050	CMR0	Comparator control register ch. 0	R/W	0b00000001

Address	Register abbreviation	Register name	R/W	Initial value
0x0051 to 0x0055	—	(Disabled)	—	—
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	0b00000000
0x005C	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	0b00100000
0x005D	SSR1	UART/SIO serial status and data register ch. 1	R/W	0b00000001
0x005E	TDR1	UART/SIO serial output data register ch. 1	R/W	0b00000000
0x005F	RDR1	UART/SIO serial input data register ch. 1	R	0b00000000
0x0060	IBCR00	I²C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I²C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I²C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I²C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I²C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I²C clock control register ch. 0	R/W	0b00000000
0x0066	SMC12	UART/SIO serial mode control register 1 ch. 2	R/W	0b00000000
0x0067	SMC22	UART/SIO serial mode control register 2 ch. 2	R/W	0b00100000
0x0068	SSR2	UART/SIO serial status and data register ch. 2	R/W	0b00000001
0x0069	TDR2	UART/SIO serial output data register ch. 2	R/W	0b00000000
0x006A	RDR2	UART/SIO serial input data register ch. 2	R	0b00000000
0x006B	ADC3	8/12-bit A/D converter control register 3	R/W	0b01111100
0x006C	ADC1	8/12-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/12-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/12-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/12-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111

Address	Register abbreviation	Register name	R/W	Initial value
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6	TMRH0	16-bit reload timer timer register (upper) ch. 0	R/W	0b00000000
	TMRLRH0	16-bit reload timer reload register (upper) ch. 0		
0x0FA7	TMRL0	16-bit reload timer timer register (lower) ch. 0	R/W	0b00000000
	TMRLRL0	16-bit reload timer reload register (lower) ch. 0		
0x0FA8	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FA9	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FAA	PSSR1	UART/SIO dedicated baud rate generator prescaler select register ch. 1	R/W	0b00000000
0x0FAB	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	0b00000000
0x0FAC	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	0b00000000
0x0FAD	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	0b00000000
0x0FAE	—	(Disabled)	—	—
0x0FAF	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FB0	LCDCC1	LCDC control register 1	R/W	0b00000000
0x0FB1	—	(Disabled)	—	—
0x0FB2	LCDCE1	LCDC enable register 1	R/W	0b00111110
0x0FB3	LCDCE2	LCDC enable register 2	R/W	0b00000000
0x0FB4	LCDCE3	LCDC enable register 3	R/W	0b00000000
0x0FB5	LCDCE4	LCDC enable register 4	R/W	0b00000000
0x0FB6	LCDCE5	LCDC enable register 5	R/W	0b00000000
0x0FB7	LCDCE6	LCDC enable register 6	R/W	0b00000000
0x0FB8	LCDCE7	LCDC enable register 7	R/W	0b00000000
0x0FB9	LCDCB1	LCDC blinking setting register 1	R/W	0b00000000
0x0FBA	LCDCB2	LCDC blinking setting register 2	R/W	0b00000000
0x0FBB, 0x0FBC	—	(Disabled)	—	—
0x0FBD to 0x0FE0	LCDRAM	LCDC display RAM (36 bytes)	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0FE1	—	(Disabled)	—	—
0x0FE2	EVCR	Event counter control register	R/W	0b00000000
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	SYSC2	System configuration register 2	R/W	0b00000000
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b00111111
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

- R/W access symbols
  R/W : Readable/Writable
  R : Read only
- Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

17. I/O Map (MB95770M Series)

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	PDR2	Port 2 data register	R/W	0b00000000
0x000F	DDR2	Port 2 direction register	R/W	0b00000000
0x0010 to 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x001B	—	(Disabled)	—	—
0x001C	PDR9	Port 9 data register	R/W	0b00000000
0x001D	DDR9	Port 9 direction register	R/W	0b00000000
0x001E	PDRA	Port A data register	R/W	0b00000000
0x001F	DDRA	Port A direction register	R/W	0b00000000
0x0020	PDRB	Port B data register	R/W	0b00000000
0x0021	DDRB	Port B direction register	R/W	0b00000000
0x0022	PDRC	Port C data register	R/W	0b00000000
0x0023	DDRC	Port C direction register	R/W	0b00000000
0x0024, 0x0025	—	(Disabled)	—	—
0x0026	PDRE	Port E data register	R/W	0b00000000
0x0027	DDRE	Port E direction register	R/W	0b00000000
0x0028	PDRF	Port F data register	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	—	(Disabled)	—	—
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E	PUL2	Port 2 pull-up register	R/W	0b00000000
0x002F to 0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	TMCSRH0	16-bit reload timer control status register (upper) ch. 0	R/W	0b00000000
0x003F	TMCSRL0	16-bit reload timer control status register (lower) ch. 0	R/W	0b00000000
0x0040 to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	—	(Disabled)	—	—
0x004E	LVDC	LVD control register	R/W	0b00000100
0x004F	LCDCC2	LCDC control register 2	R/W	0b00010100
0x0050	CMR0	Comparator control register ch. 0	R/W	0b00000001
0x0051 to 0x0055	—	(Disabled)	—	—
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	0b00000000
0x005C	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	0b00100000
0x005D	SSR1	UART/SIO serial status and data register ch. 1	R/W	0b00000001
0x005E	TDR1	UART/SIO serial output data register ch. 1	R/W	0b00000000
0x005F	RDR1	UART/SIO serial input data register ch. 1	R	0b00000000
0x0060	IBCR00	I²C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I²C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I²C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I²C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I²C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I²C clock control register ch. 0	R/W	0b00000000
0x0066	SMC12	UART/SIO serial mode control register 1 ch. 2	R/W	0b00000000
0x0067	SMC22	UART/SIO serial mode control register 2 ch. 2	R/W	0b00100000
0x0068	SSR2	UART/SIO serial status and data register ch. 2	R/W	0b00000001
0x0069	TDR2	UART/SIO serial output data register ch. 2	R/W	0b00000000
0x006A	RDR2	UART/SIO serial input data register ch. 2	R	0b00000000
0x006B	ADC3	8/12-bit A/D converter control register 3	R/W	0b01111100
0x006C	ADC1	8/12-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/12-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/12-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/12-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111

Address	Register abbreviation	Register name	R/W	Initial value
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6	TMRH0	16-bit reload timer timer register (upper) ch. 0	R/W	0b00000000
	TMRLRH0	16-bit reload timer reload register (upper) ch. 0		

Address	Register abbreviation	Register name	R/W	Initial value
0x0FA7	TMRL0	16-bit reload timer timer register (lower) ch. 0	R/W	0b00000000
	TMRLRL0	16-bit reload timer reload register (lower) ch. 0		
0x0FA8	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FA9	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FAA	PSSR1	UART/SIO dedicated baud rate generator prescaler select register ch. 1	R/W	0b00000000
0x0FAB	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	0b00000000
0x0FAC	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	0b00000000
0x0FAD	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	0b00000000
0x0FAE	—	(Disabled)	—	—
0x0FAF	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FB0	LCDCC1	LCDC control register 1	R/W	0b00000000
0x0FB1	—	(Disabled)	—	—
0x0FB2	LCDCE1	LCDC enable register 1	R/W	0b00111110
0x0FB3	LCDCE2	LCDC enable register 2	R/W	0b00000000
0x0FB4	LCDCE3	LCDC enable register 3	R/W	0b00000000
0x0FB5	LCDCE4	LCDC enable register 4	R/W	0b00000000
0x0FB6	LCDCE5	LCDC enable register 5	R/W	0b00000000
0x0FB7	LCDCE6	LCDC enable register 6	R/W	0b00000000
0x0FB8	—	(Disabled)	—	—
0x0FB9	LCDCB1	LCDC blinking setting register 1	R/W	0b00000000
0x0FBA	LCDCB2	LCDC blinking setting register 2	R/W	0b00000000
0x0FBB, 0x0FBC	—	(Disabled)	—	—
0x0FBD to 0x0FD8	LCDRAM	LCDC display RAM (28 bytes)	R/W	0b00000000
0x0FD9 to 0x0FE1	—	(Disabled)	—	—
0x0FE2	EVCR	Event counter control register	R/W	0b00000000
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	SYSC2	System configuration register 2	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b00111111
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

- R/W access symbols
  R/W : Readable/Writable
  R : Read only
- Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

18. I/O Ports (MB95710M Series)

- List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 2 data register	PDR2	R, RM/W	0b00000000
Port 2 direction register	DDR2	R/W	0b00000000
Port 4 data register	PDR4	R, RM/W	0b00000000
Port 4 direction register	DDR4	R/W	0b00000000
Port 5 data register	PDR5	R, RM/W	0b00000000
Port 5 direction register	DDR5	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 9 data register	PDR9	R, RM/W	0b00000000
Port 9 direction register	DDR9	R/W	0b00000000
Port A data register	PDRA	R, RM/W	0b00000000
Port A direction register	DDRA	R/W	0b00000000
Port B data register	PDRB	R, RM/W	0b00000000
Port B direction register	DDRB	R/W	0b00000000
Port C data register	PDRC	R, RM/W	0b00000000
Port C direction register	DDRC	R/W	0b00000000
Port E data register	PDRE	R, RM/W	0b00000000
Port E direction register	DDRE	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 1 pull-up register	PUL0	R/W	0b00000000
Port 2 pull-up register	PUL1	R/W	0b00000000
Port 5 pull-up register	PUL5	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

18.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- A/D input disable register (lower) (AIDRL)

18.1.2 Block diagrams of port 0

- P00/INT00/AN00/UO2 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT00)
  - 8/12-bit A/D converter analog input pin (AN00)
  - UART/SIO ch. 2 data output pin (UO2)

- P02/INT02/AN02/SEG35/UCK2 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT02)
  - 8/12-bit A/D converter analog input pin (AN02)
  - LCDC SEG35 output pin (SEG35)
  - UART/SIO ch. 2 clock I/O pin (UCK2)

- P03/INT03/AN03/SEG34/UO1 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT03)
  - 8/12-bit A/D converter analog input pin (AN03)
  - LCDC SEG34 output pin (SEG34)
  - UART/SIO ch. 1 data output pin (UO1)

- P05/INT05/AN05/SEG32/UCK1 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT05)
  - 8/12-bit A/D converter analog input pin (AN05)
  - LCDC SEG32 output pin (SEG32)
  - UART/SIO ch. 1 clock I/O pin (UCK1)

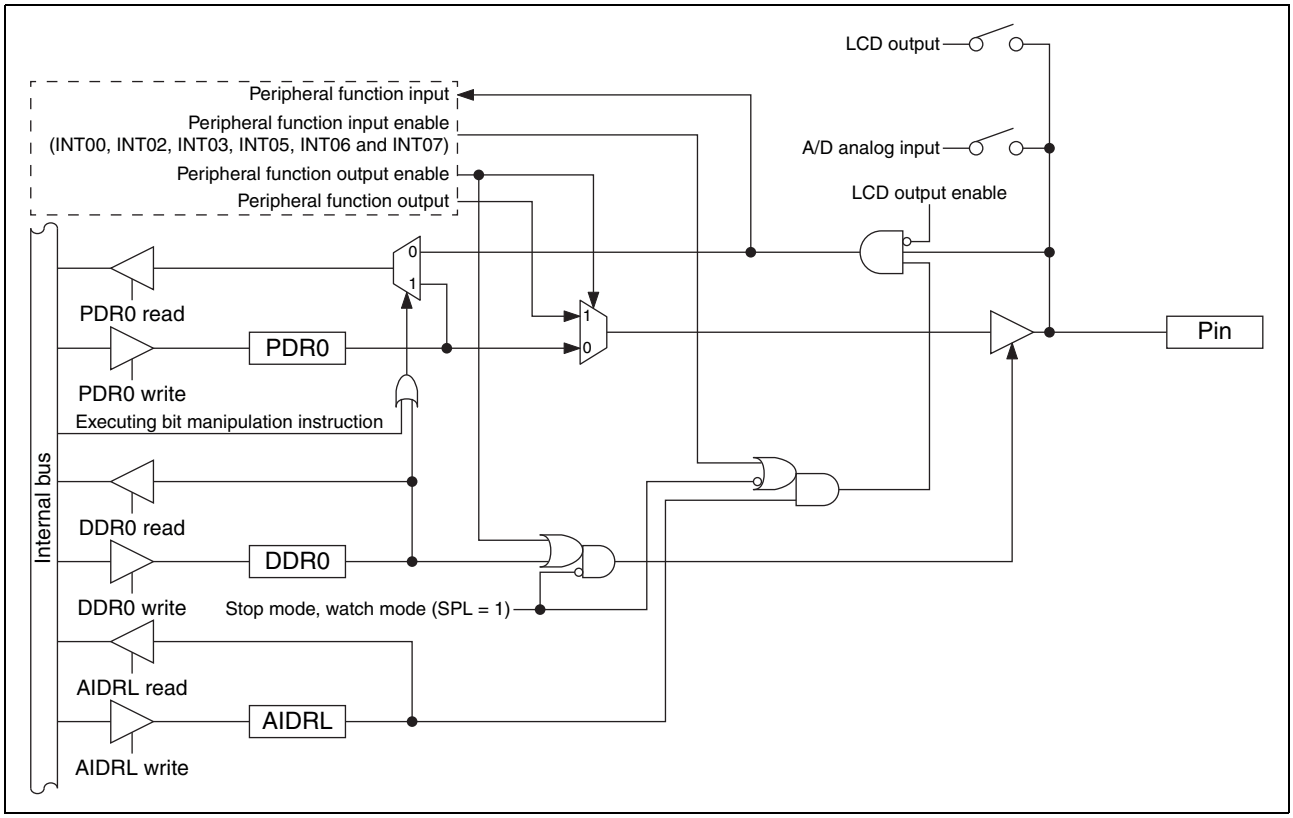
- P06/INT06/AN06/SEG31 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT06)
  - 8/12-bit A/D converter analog input pin (AN06)
  - LCDC SEG31 output pin (SEG31)

- P07/INT07/AN07/SEG30 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT07)
  - 8/12-bit A/D converter analog input pin (AN07)
  - LCDC SEG30 output pin (SEG30)

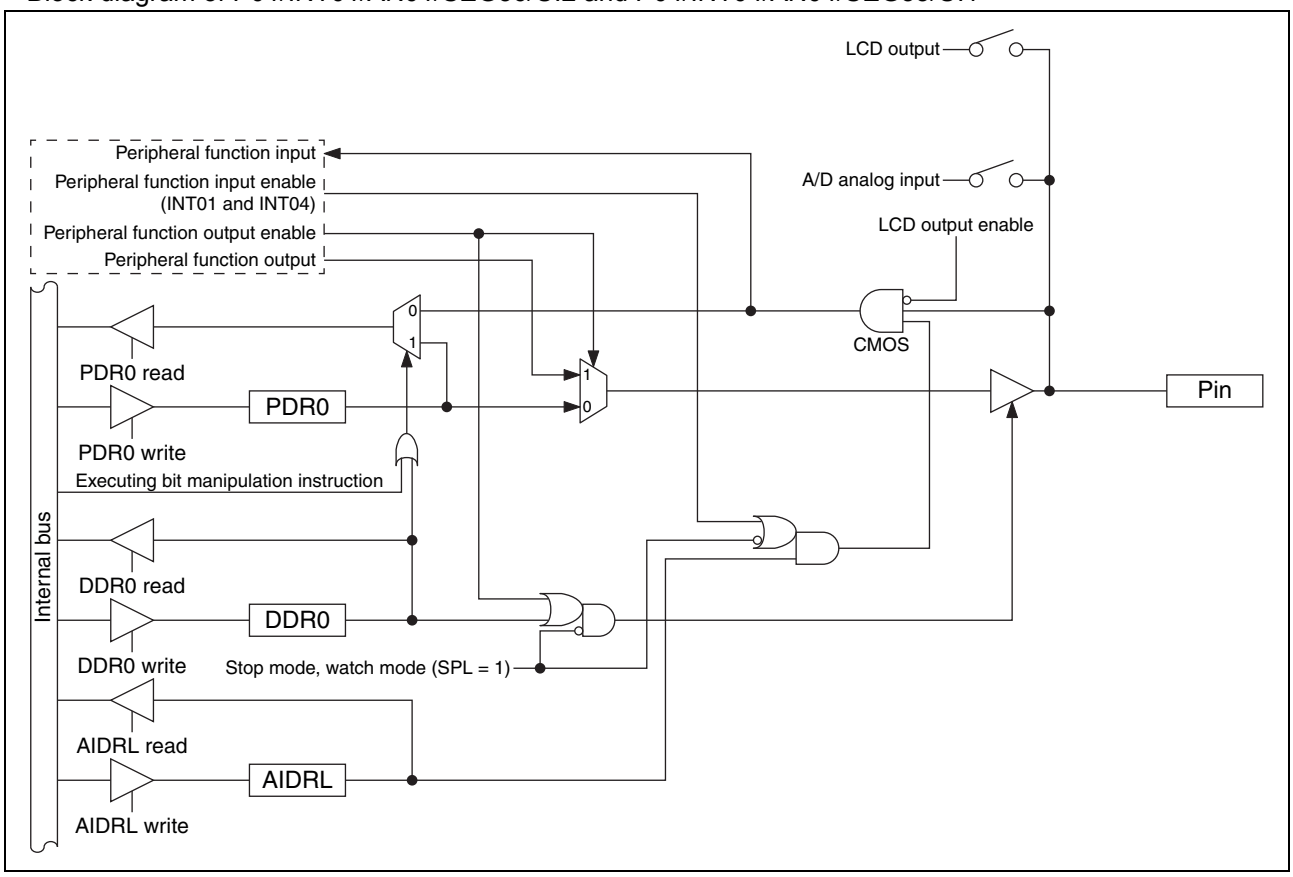
- Block diagram of P00/INT00/AN00/UO2, P02/INT02/AN02/SEG35/UCK2, P03/INT03/AN03/SEG34/UO1, P05/INT05/AN05/SEG32/UCK1, P06/INT06/AN06/SEG31 and P07/INT07/AN07/SEG30



- P01/INT01/AN01/SEG36/UI2 pin
  This pin has the following peripheral functions:
  - External interrupt input pin (INT01)
  - 8/12-bit A/D converter analog input pin (AN01)
  - LCDC SEG36 output pin (SEG36)
  - UART/SIO ch. 2 data input pin (UI2)

- P04/INT04/AN04/SEG33/UI1 pin
  This pin has the following peripheral functions:
  - External interrupt input pin (INT04)
  - 8/12-bit A/D converter analog input pin (AN04)
  - LCDC SEG33 output pin (SEG33)
  - UART/SIO ch. 1 data input pin (UI1)

• Block diagram of P01/INT01/AN01/SEG36/UI2 and P04/INT04/AN04/SEG33/UI1



18.1.3 Port 0 registers

• Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

• Correspondence between registers and pins for port 0

	Correspondence between related register bits and pins							
Pin name	P07	P06	P05	P04	P03	P02	P01	P00
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
AIDRL								

18.1.4 Port 0 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
  - If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR0 register returns the PDR0 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) or in the LCDC enable register 7 (LCDCE7:SEG[36:32]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When using an analog input shared pin as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to “1”.
  - If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) or in the LCDC enable register 7 (LCDCE7:SEG[36:32]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
  - When using the analog input shared pin as another peripheral function input pin, configure it as an input port, which is the same as the operation as an input port.
  - Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR0 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) or in the LCDC enable register 7 (LCDCE7:SEG[36:32]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset

  If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with analog input, its port input is disabled because the AIDRL register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT00 to INT07), the input is enabled and not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an analog input pin
  - Set the bit in the DDR0 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.

- Operation as an external interrupt input pin
  - Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

18.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.2.1 Port 1 configuration

Port 1 is made up of the following elements.

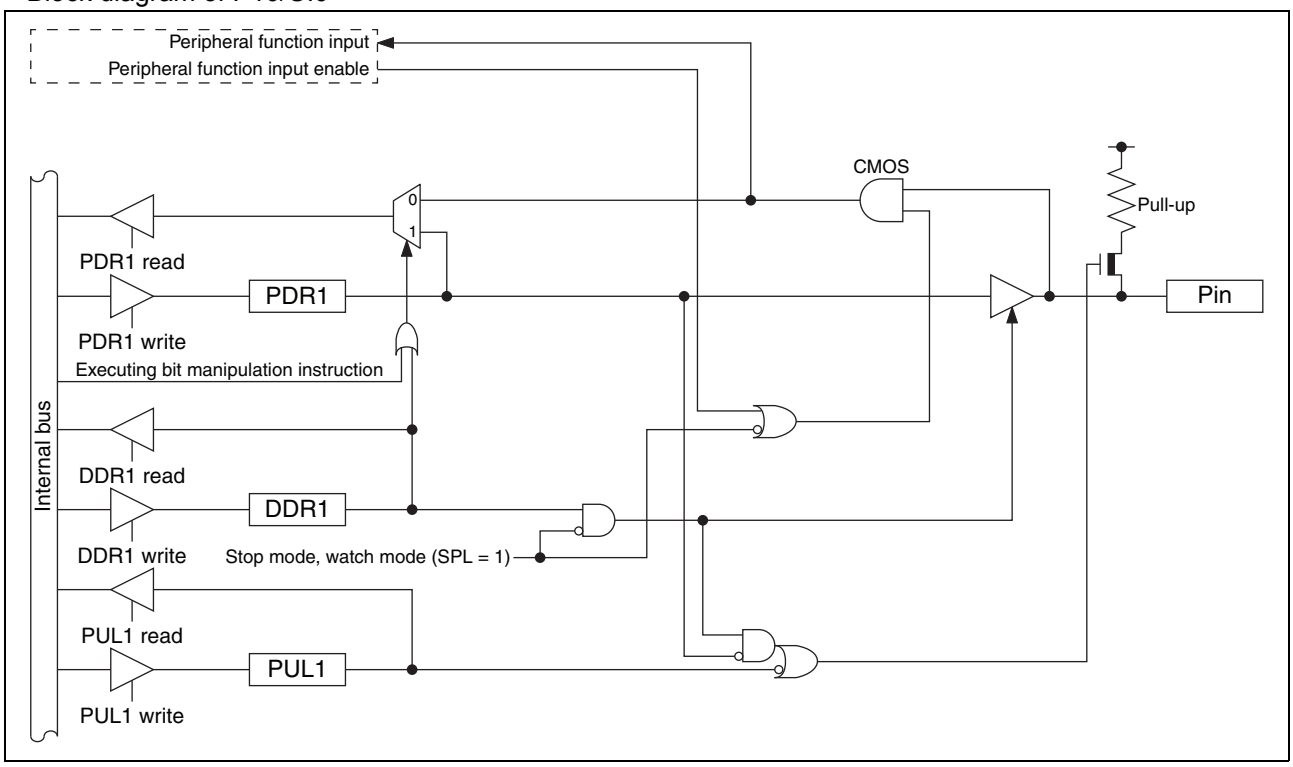
- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

18.2.2 Block diagrams of port 1

- P10/UI0 pin

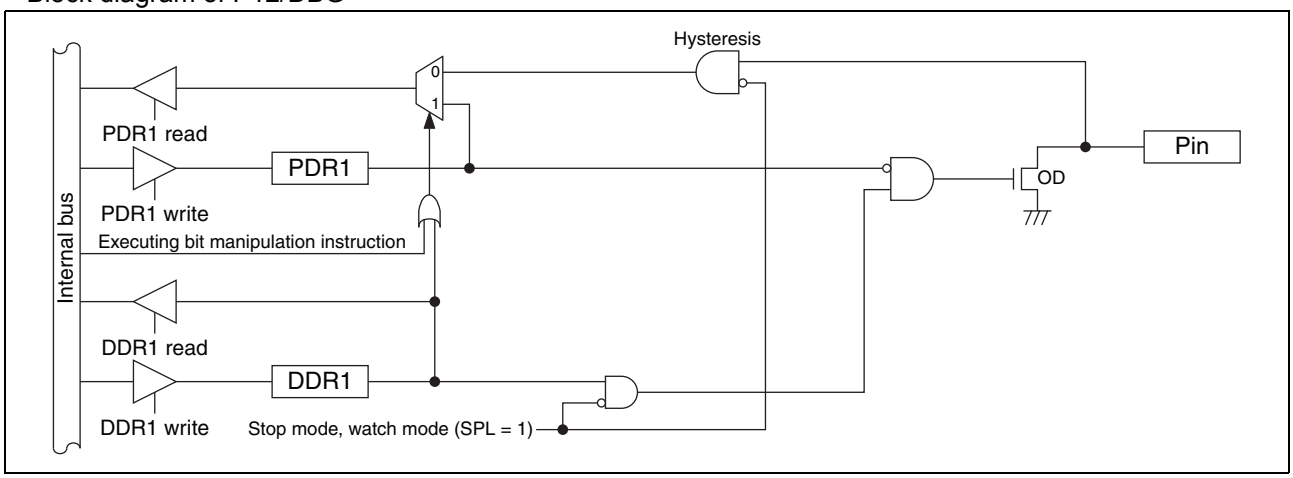
  This pin has the following peripheral function:
  - UART/SIO ch. 0 data input pin (UI0)

- Block diagram of P10/UI0



- P12/DBG pin
  This pin has the following peripheral function:
  - DBG input pin (DBG)

- Block diagram of P12/DBG



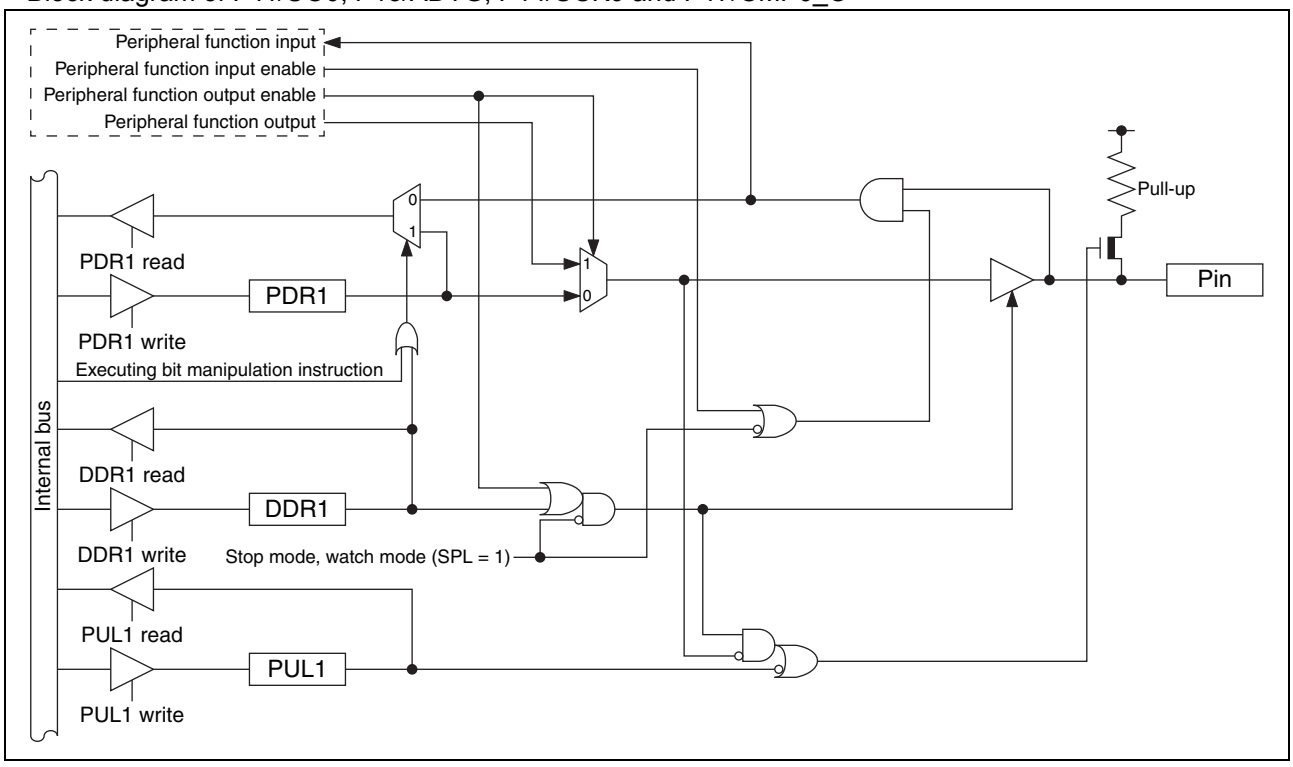
- P11/UO0 pin
  This pin has the following peripheral function:
  - UART/SIO ch. 0 data output pin (UO0)

- P13/ADTG pin
  This pin has the following peripheral function:
  - 8/12-bit A/D converter trigger input pin (ADTG)

- P14/UCK0 pin
  This pin has the following peripheral function:
  - UART/SIO ch. 0 clock I/O pin (UCK0)

- P17/CMP0_O pin
  This pin has the following peripheral function:
  - Comparator ch. 0 digital output pin (CMP0_O)

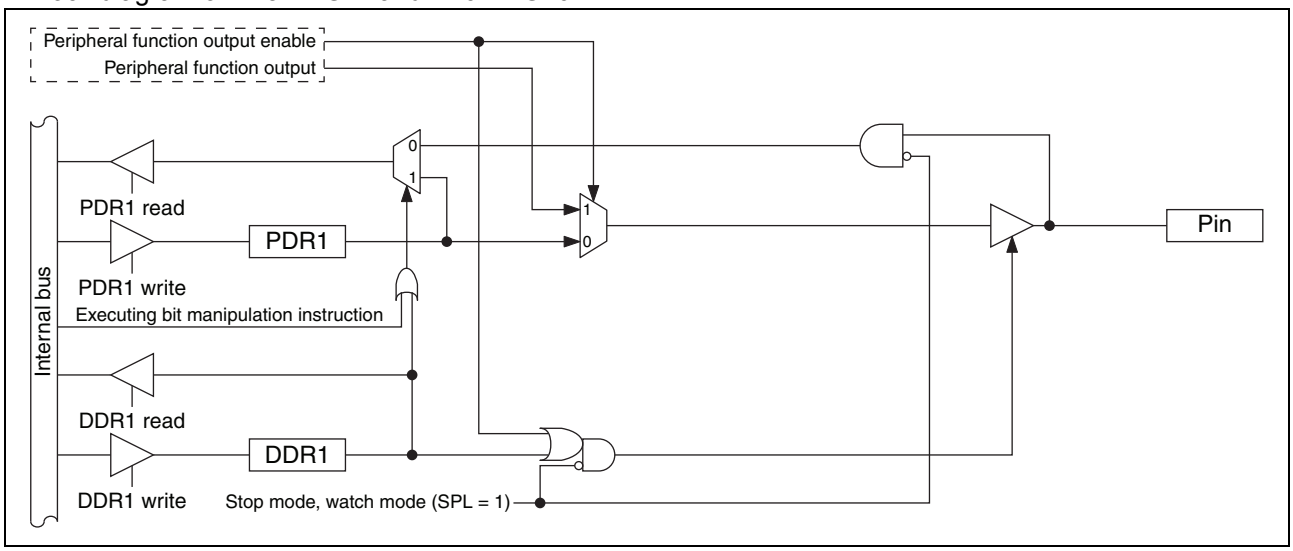
- Block diagram of P11/UO0, P13/ADTG, P14/UCK0 and P17/CMP0_O



- P15/PPG11 pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG11)

- P16/PPG10 pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG10)

- Block diagram of P15/PPG11 and P16/PPG10



18.2.3 Port 1 registers

- Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10
PDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR1								
PUL1		-	-			-		

18.2.4 Port 1 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
  - If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR1 register returns the PDR1 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P10/UI0 and P14/UCK0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

18.3 Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.3.1 Port 2 configuration

Port 2 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

18.3.2 Block diagrams of port 2

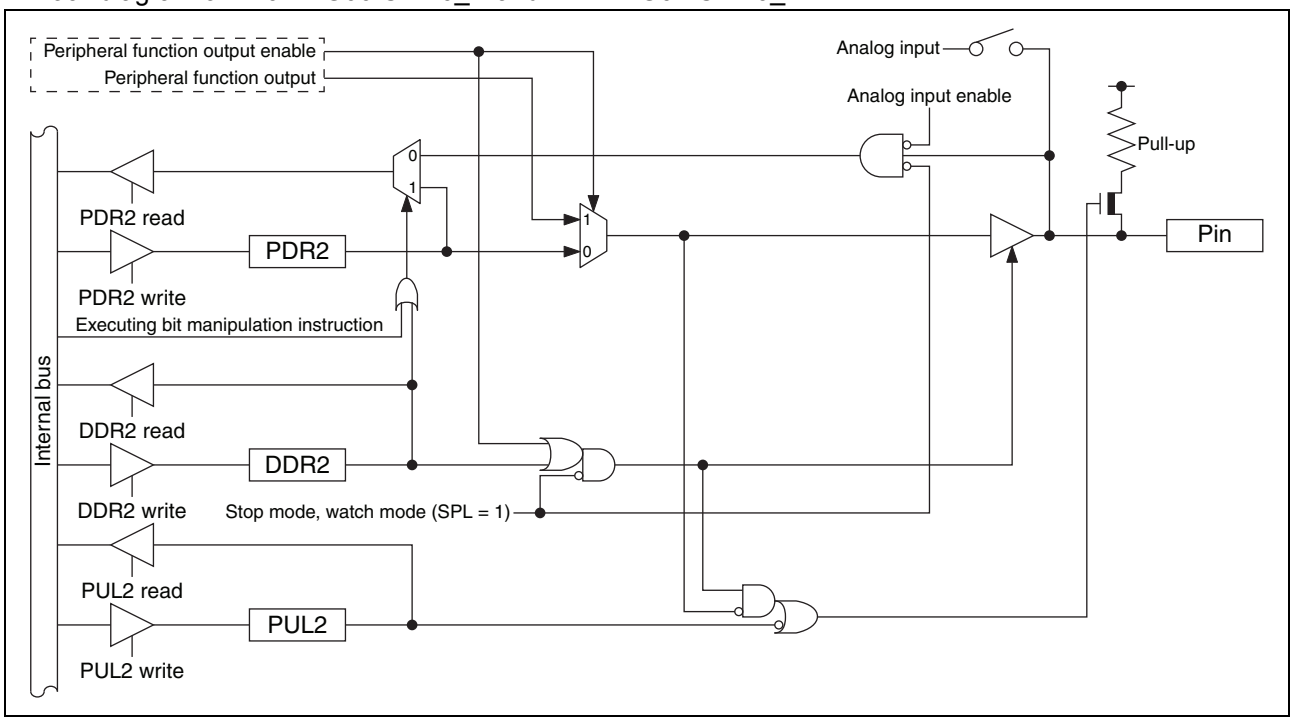
- P20/PPG00/CMP0_N pin

  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG00)
  - Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

- P21/PPG01/CMP0_P pin

  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG01)
  - Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)

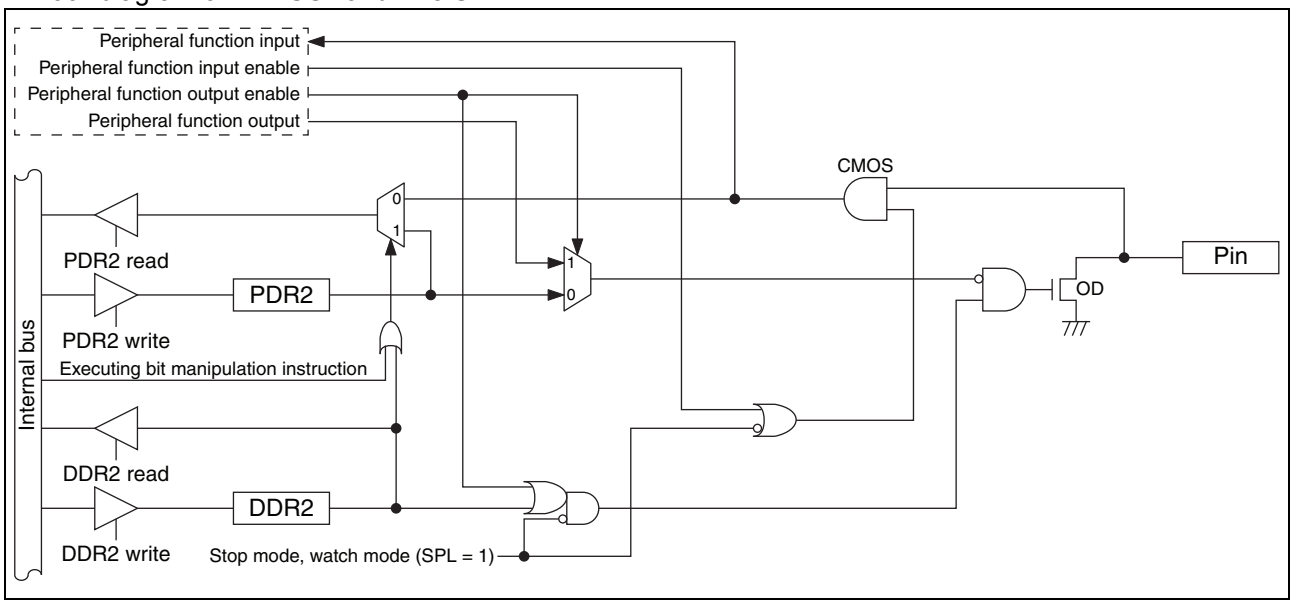
- Block diagram of P20/PPG00/CMP0_N and P21/PPG01/CMP0_P



- P22/SCL pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 clock I/O pin (SCL)

- P23/SDA pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 data I/O pin (SDA)

- Block diagram of P22/SCL and P23/SDA



18.3.3 Port 2 registers

- Port 2 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR2	0	Pin state is “L” level.	PDR2 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR2 value is “1”.	As output port, outputs “H” level.*
DDR2	0	Port input enabled		
	1	Port output enabled		
PUL2	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 2

	Correspondence between related register bits and pins							
Pin name	-	-	-	-	P23	P22	P21	P20
PDR2	-	-	-	-	bit3	bit2	bit1	bit0
DDR2								
PUL2					-	-		

18.3.4 Port 2 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR2 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR2 register to external pins.
  - If data is written to the PDR2 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR2 register returns the PDR2 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR2 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR2 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR2 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR2 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR2 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR2 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR2 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR2 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR2 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL2 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL2 register.

- Operation as a comparator input pin
  - Regardless of the value of the PDR2 register and that of the DDR2 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit to “1”.
  - For details of the comparator, refer to “CHAPTER 29 COMPARATOR” in “New 8FX MB95710M/770M Series Hardware Manual”.

18.4 Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.4.1 Port 4 configuration

Port 4 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 4 data register (PDR4)
- Port 4 direction register (DDR4)

18.4.2 Block diagrams of port 4

- P40/SEG21 pin

  This pin has the following peripheral function:
  - LCDC SEG21 output pin (SEG21)

- P41/SEG20 pin

  This pin has the following peripheral function:
  - LCDC SEG20 output pin (SEG20)

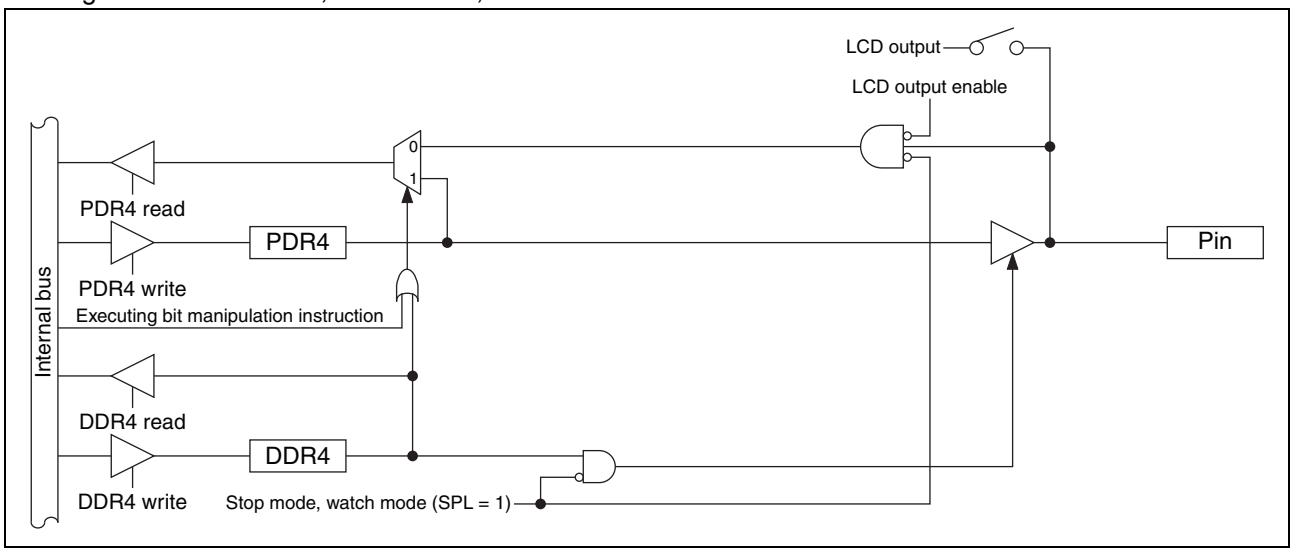
- P42/SEG19 pin

  This pin has the following peripheral function:
  - LCDC SEG19 output pin (SEG19)

- P43/SEG18 pin

  This pin has the following peripheral function:
  - LCDC SEG18 output pin (SEG18)

- Block diagram of P40/SEG21, P41/SEG20, P42/SEG19 and P43/SEG18



18.4.3 Port 4 registers

- Port 4 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR4	0	Pin state is “L” level.	PDR4 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR4 value is “1”.	As output port, outputs “H” level.
DDR4	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port 4

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**P43**	**P42**	**P41**	**P40**
PDR4	-	-	-	-	bit3	bit2	bit1	bit0
DDR4								

18.4.4 Port 4 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
  - If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR4 register returns the PDR4 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[21:18]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[21:18]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR4 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[21:18]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.5 Port 5

Port 5 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.5.1 Port 5 configuration

Port 5 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 5 data register (PDR5)
- Port 5 direction register (DDR5)
- Port 5 pull-up register (PUL5)

18.5.2 Block diagrams of port 5

- P50/TO01 pin

  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 output pin (TO01)

- P51/EC0 pin

  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 clock input pin (EC0)

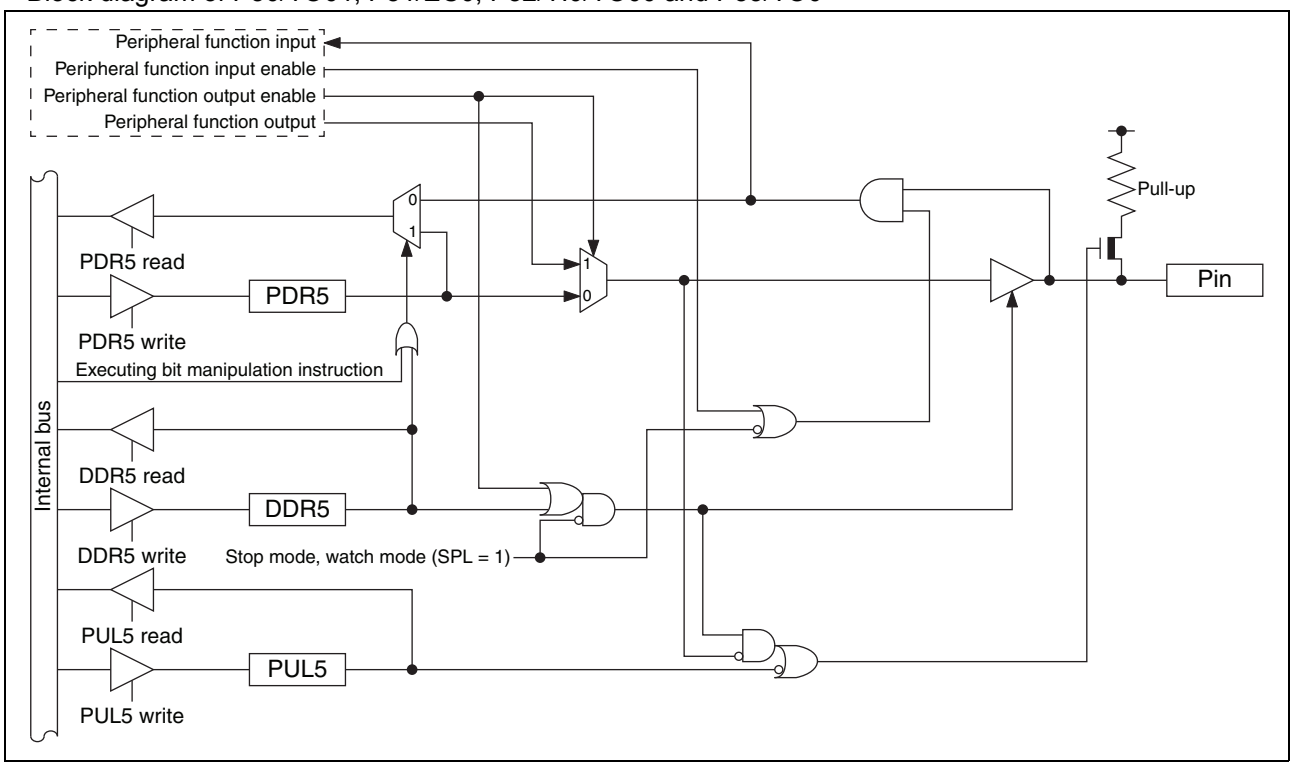
- P52/TI0/TO00 pin

  This pin has the following peripheral functions:
  - 16-bit reload timer ch. 0 input pin (TI0)
  - 8/16-bit composite timer ch. 0 output pin (TO00)

- P53/TO0 pin

  This pin has the following peripheral function:
  - 16-bit reload timer ch. 0 output pin (TO0)

• Block diagram of P50/TO01, P51/EC0, P52/TI0/TO00 and P53/TO0



18.5.3 Port 5 registers

• Port 5 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR5	0	Pin state is “L” level.	PDR5 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR5 value is “1”.	As output port, outputs “H” level.
DDR5	0	Port input enabled		
	1	Port output enabled		
PUL5	0	Pull-up disabled		
	1	Pull-up enabled		

• Correspondence between registers and pins for port 5

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**P53**	**P52**	**P51**	**P50**
PDR5	-	-	-	-	bit3	bit2	bit1	bit0
DDR5								
PUL5								

18.5.4 Port 5 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR5 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR5 register to external pins.
  - If data is written to the PDR5 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR5 register returns the PDR5 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR5 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR5 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR5 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR5 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR5 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR5 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR5 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR5 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR5 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL5 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL5 register.

18.6 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.6.1 Port 6 configuration

Port 6 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)

18.6.2 Block diagrams of port 6

- P60/SEG10 pin
  This pin has the following peripheral function:
  - LCDC SEG10 output pin (SEG10)

- P61/SEG11 pin
  This pin has the following peripheral function:
  - LCDC SEG11 output pin (SEG11)

- P62/SEG12 pin
  This pin has the following peripheral function:
  - LCDC SEG12 output pin (SEG12)

- P63/SEG13 pin
  This pin has the following peripheral function:
  - LCDC SEG13 output pin (SEG13)

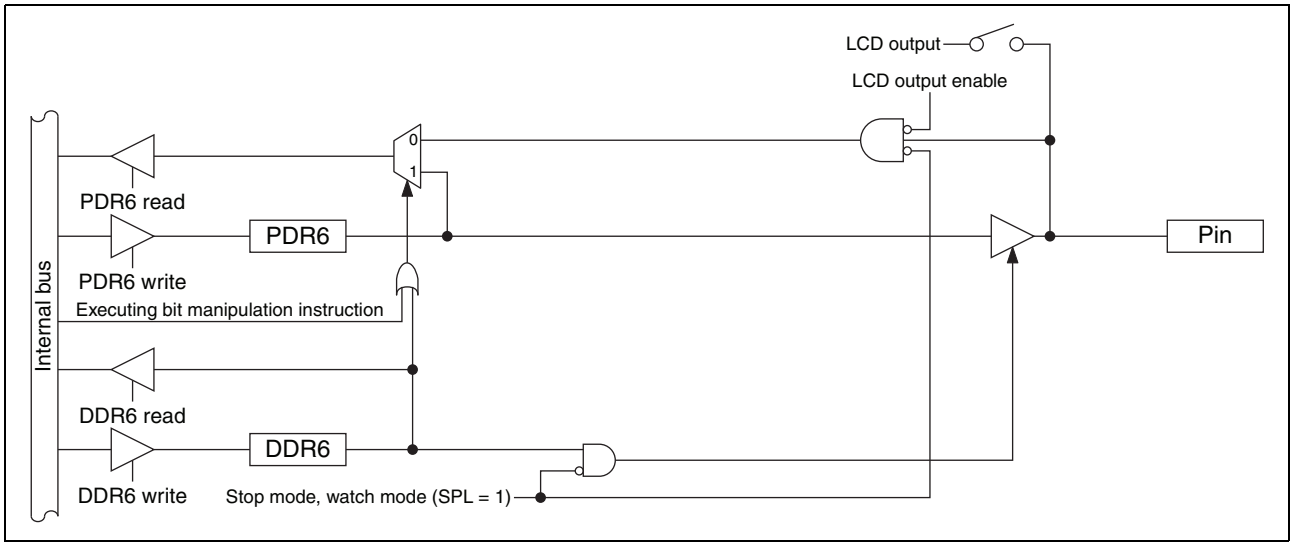
- P64/SEG14 pin
  This pin has the following peripheral function:
  - LCDC SEG14 output pin (SEG14)

- P65/SEG15 pin
  This pin has the following peripheral function:
  - LCDC SEG15 output pin (SEG15)

- P66/SEG16 pin
  This pin has the following peripheral function:
  - LCDC SEG16 output pin (SEG16)

- P67/SEG17 pin
  This pin has the following peripheral function:
  - LCDC SEG17 output pin (SEG17)

- Block diagram of P60/SEG10, P61/SEG11, P62/SEG12, P63/SEG13, P64/SEG14, P65/SEG15, P66/SEG16 and P67/SEG17



18.6.3 Port 6 registers

- Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.
DDR6	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port 6

	Correspondence between related register bits and pins							
Pin name	**P67**	**P66**	**P65**	**P64**	**P63**	**P62**	**P61**	**P60**
PDR6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR6								

18.6.4 Port 6 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
  - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR6 register returns the PDR6 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:10]) or in the LCDC enable register 5 (LCDCE5:SEG[17:16]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:10]) or in the LCDC enable register 5 (LCDCE5:SEG[17:16]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR6 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:10]) or in the LCDC enable register 5 (LCDCE5:SEG[17:16]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.7 Port 9

Port 9 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.7.1 Port 9 configuration

Port 9 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 9 data register (PDR9)
- Port 9 direction register (DDR9)

18.7.2 Block diagrams of port 9

- P90/V4 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V4)

- P91/V3 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V3)

- P92/V2 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V2)

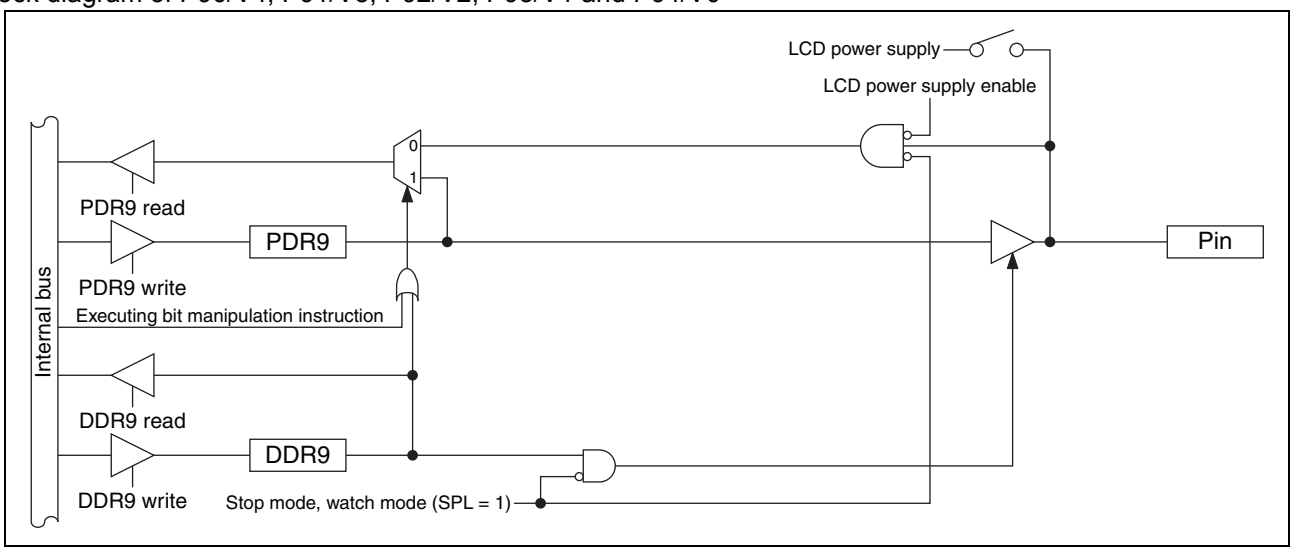
- P93/V1 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V1)

- P94/V0 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V0)

- Block diagram of P90/V4, P91/V3, P92/V2, P93/V1 and P94/V0



18.7.3 Port 9 registers

- Port 9 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR9	0	Pin state is “L” level.	PDR9 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR9 value is “1”.	As output port, outputs “H” level.
DDR9	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port 9

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**P94**	**P93**	**P92**	**P91**	**P90**
PDR9	-	-	-	bit4	bit3	bit2	bit1	bit0
DDR9								

18.7.4 Port 9 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR9 register corresponding to that pin is set to “1”.
  - When a pin is used as an output port, it outputs the value of the PDR9 register to external pins.
  - If data is written to the PDR9 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR9 register returns the PDR9 register value.
  - To use a pin shared with the LCDC as an output port, set the bit corresponding to that pin in the VE[4:0] bits in the LCDC enable register 1 (LCDCE1) to “0” to select the general-purpose I/O port function.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR9 register corresponding to that pin is set to “0”.
  - If data is written to the PDR9 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR9 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR9 register, the PDR9 register value is returned.
  - To use a pin shared with the LCDC as an input port, set the bit corresponding to that pin in the VE[4:0] bits in the LCDCE1 register to “0” to select the general-purpose I/O port function.

- Operation at reset
  If the CPU is reset, all bits in the DDR9 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR9 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an LCD drive power supply pin
  - Set the bit in the DDR9 register corresponding to an LCD drive power supply pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCD drive power supply pin, set the bit corresponding to that pin in the VE[4:0] bits in the LCDCE1 register to “1” to select the LCD drive power supply function.

18.8 Port A

Port A is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.8.1 Port A configuration

Port A is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port A data register (PDRA)
- Port A direction register (DDRA)

18.8.2 Block diagrams of port A

- PA0/COM0 pin
  This pin has the following peripheral function:
  - LCDC COM0 output pin (COM0)

- PA1/COM1 pin
  This pin has the following peripheral function:
  - LCDC COM1 output pin (COM1)

- PA2/COM2 pin
  This pin has the following peripheral function:
  - LCDC COM2 output pin (COM2)

- PA3/COM3 pin
  This pin has the following peripheral function:
  - LCDC COM3 output pin (COM3)

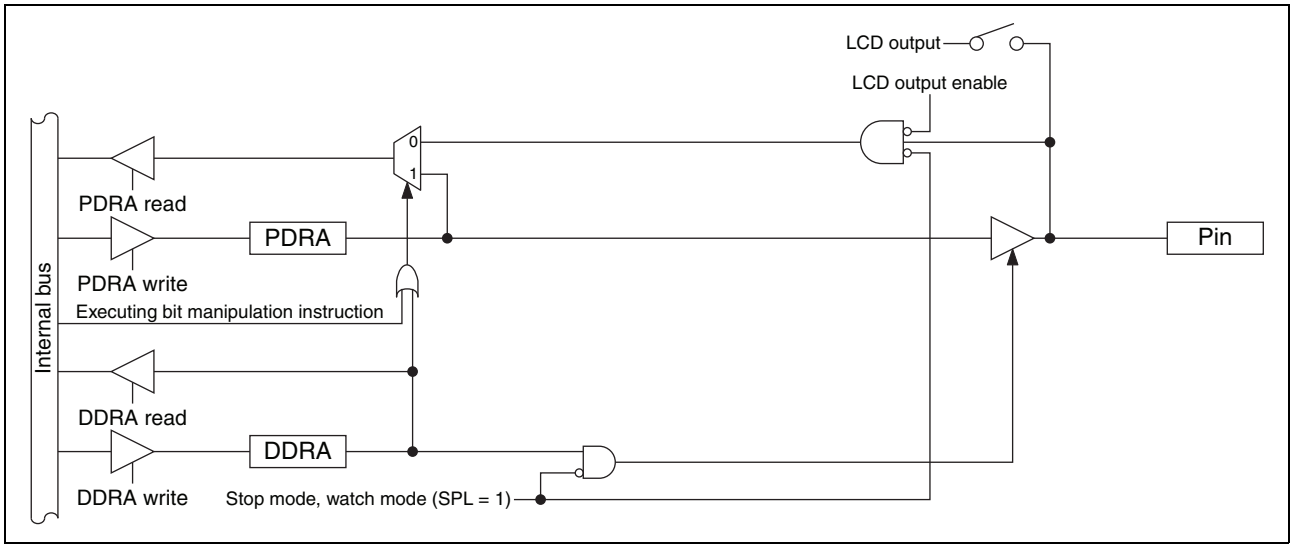
- PA4/COM4 pin
  This pin has the following peripheral function:
  - LCDC COM4 output pin (COM4)

- PA5/COM5 pin
  This pin has the following peripheral function:
  - LCDC COM5 output pin (COM5)

- PA6/COM6 pin
  This pin has the following peripheral function:
  - LCDC COM6 output pin (COM6)

- PA7/COM7 pin
  This pin has the following peripheral function:
  - LCDC COM7 output pin (COM7)

- Block diagram of PA0/COM0, PA1/COM1, PA2/COM2, PA3/COM3, PA4/COM4, PA5/COM5, PA6/COM6 and PA7/COM7



18.8.3 Port A registers

- Port A register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRA	0	Pin state is “L” level.	PDRA value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRA value is “1”.	As output port, outputs “H” level.
DDRA	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port A

	Correspondence between related register bits and pins							
Pin name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PDRA	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRA								

18.8.4 Port A operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRA register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRA register to external pins.
  - If data is written to the PDRA register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRA register returns the PDRA register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRA register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRA register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRA register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRA register, the PDRA register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC common output pin
  - Set the bit in the DDRA register corresponding to an LCDC common output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC common output pin, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “1” to select the LCDC common output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRA register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRA register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.9 Port B

Port B is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.9.1 Port B configuration

Port B is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port B data register (PDRB)
- Port B direction register (DDRB)

18.9.2 Block diagrams of port B

- PB0/SEG00 pin

  This pin has the following peripheral function:
  - LCDC SEG00 output pin (SEG00)

- PB1/SEG01 pin

  This pin has the following peripheral function:
  - LCDC SEG01 output pin (SEG01)

- PB2/SEG37 pin

  This pin has the following peripheral function:
  - LCDC SEG37 output pin (SEG37)

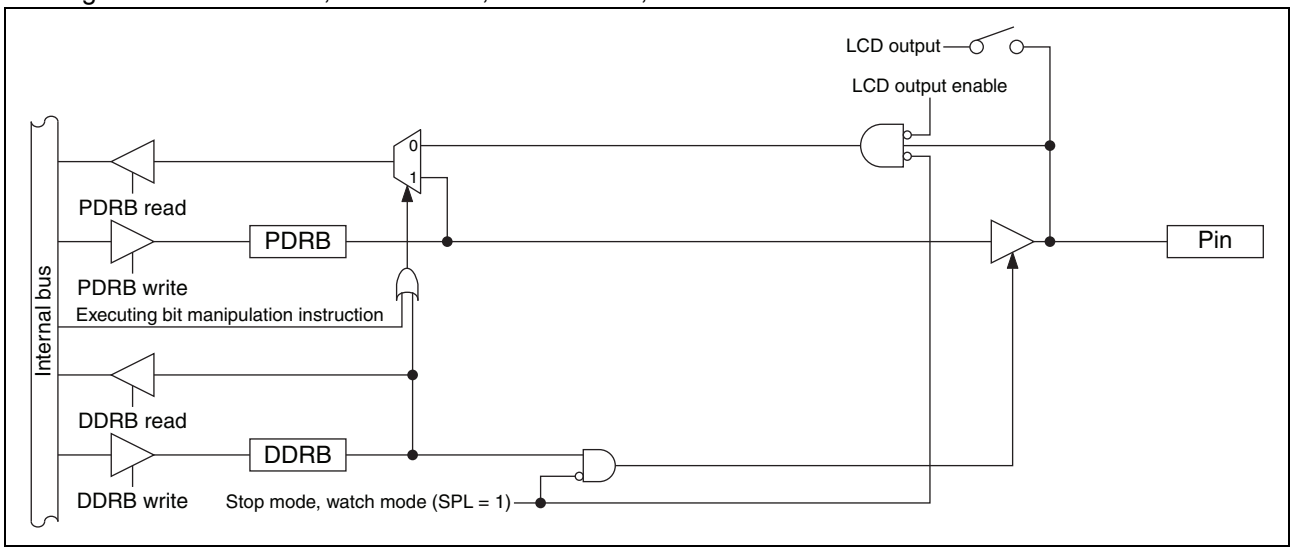
- PB3/SEG38 pin

  This pin has the following peripheral function:
  - LCDC SEG38 output pin (SEG38)

- PB4/SEG39 pin

  This pin has the following peripheral function:
  - LCDC SEG39 output pin (SEG39)

- Block diagram of PB0/SEG00, PB1/SEG01, PB2/SEG37, PB3/SEG38 and PB4/SEG39



18.9.3 Port B registers

- Port B register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRB	0	Pin state is “L” level.	PDRB value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRB value is “1”.	As output port, outputs “H” level.
DDRB	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port B

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**PB4**	**PB3**	**PB2**	**PB1**	**PB0**
PDRB	-	-	-	bit4	bit3	bit2	bit1	bit0
DDRB								

18.9.4 Port B operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRB register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRB register to external pins.
  - If data is written to the PDRB register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRB register returns the PDRB register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) or in the LCDC enable register 7 (LCDCE7:SEG[39:37]) to “0” to select the general-purpose I/O port function, and then set the port input control bit (PICTL) in the LCDC enable register 1 (LCDCE1) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRB register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRB register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRB register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRB register, the PDRB register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) or in the LCDC enable register 7 (LCDCE7:SEG[39:37]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRB register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) or in the LCDC enable register 7 (LCDCE7:SEG[39:37]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRB register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRB register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.10 Port C

Port C is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.10.1 Port C configuration

Port C is made up of the following elements.
- General-purpose I/O pins/peripheral function I/O pins
- Port C data register (PDRC)
- Port C direction register (DDRC)

18.10.2 Block diagrams of port C

- PC0/SEG02 pin
  This pin has the following peripheral function:
  - LCDC SEG02 output pin (SEG02)

- PC1/SEG03 pin
  This pin has the following peripheral function:
  - LCDC SEG03 output pin (SEG03)

- PC2/SEG04 pin
  This pin has the following peripheral function:
  - LCDC SEG04 output pin (SEG04)

- PC3/SEG05 pin
  This pin has the following peripheral function:
  - LCDC SEG05 output pin (SEG05)

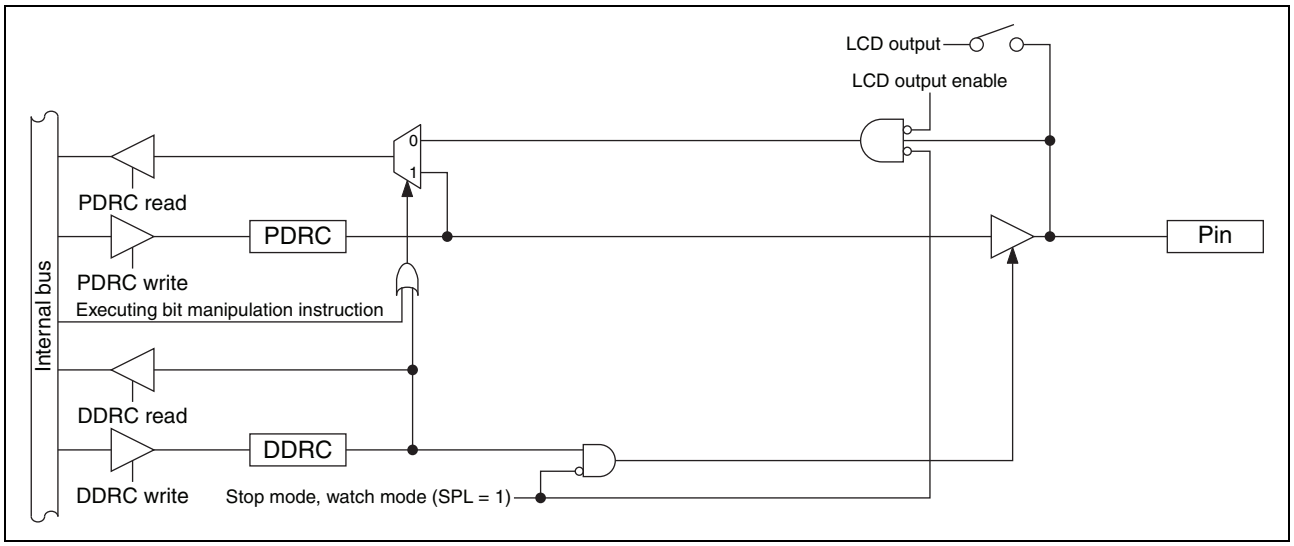
- PC4/SEG06 pin
  This pin has the following peripheral function:
  - LCDC SEG06 output pin (SEG06)

- PC5/SEG07 pin
  This pin has the following peripheral function:
  - LCDC SEG07 output pin (SEG07)

- PC6/SEG08 pin
  This pin has the following peripheral function:
  - LCDC SEG08 output pin (SEG08)

- PC7/SEG09 pin
  This pin has the following peripheral function:
  - LCDC SEG09 output pin (SEG09)

- Block diagram of PC0/SEG02, PC1/SEG03, PC2/SEG04, PC3/SEG05, PC4/SEG06, PC5/SEG07, PC6/SEG08 and PC7/SEG09



18.10.3 Port C registers

- Port C register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRC	0	Pin state is “L” level.	PDRC value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRC value is “1”.	As output port, outputs “H” level.
DDRC	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port C

	Correspondence between related register bits and pins							
Pin name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
PDRC	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRC								

18.10.4 Port C operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRC register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRC register to external pins.
  - If data is written to the PDRC register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRC register returns the PDRC register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRC register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRC register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRC register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRC register, the PDRC register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRC register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRC register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRC register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.11 Port E

Port E is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.11.1 Port E configuration

Port E is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port E data register (PDRE)
- Port E direction register (DDRE)

18.11.2 Block diagrams of port E

- PE0/SEG22 pin

  This pin has the following peripheral function:
  - LCDC SEG22 output pin (SEG22)

- PE1/SEG23 pin

  This pin has the following peripheral function:
  - LCDC SEG23 output pin (SEG23)

- PE2/SEG24 pin

  This pin has the following peripheral function:
  - LCDC SEG24 output pin (SEG24)

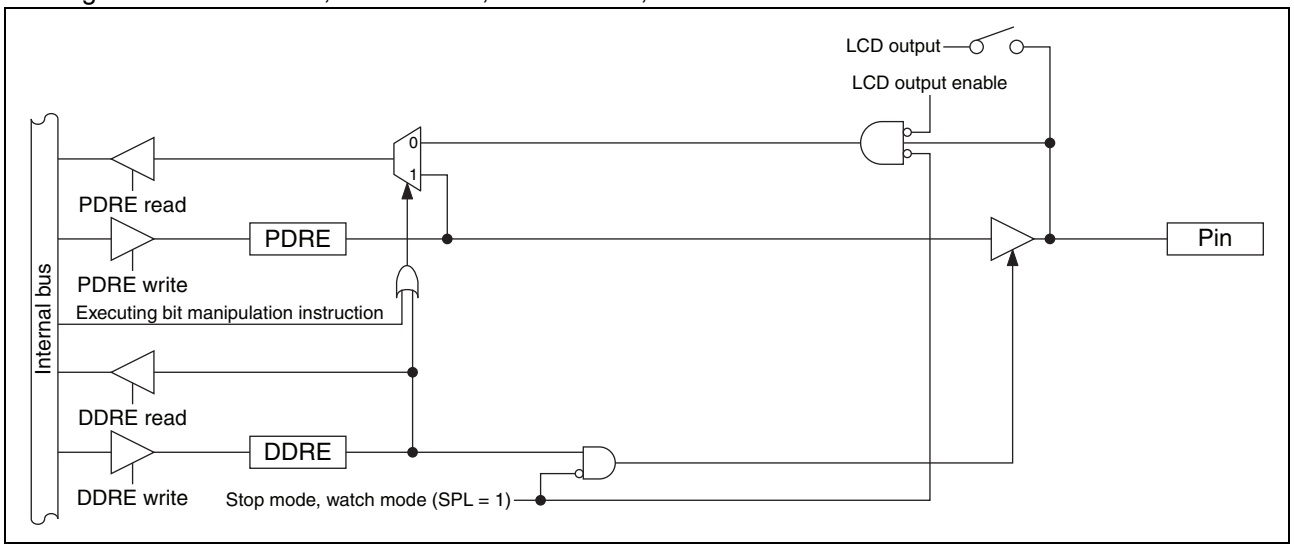
- PE3/SEG25 pin

  This pin has the following peripheral function:
  - LCDC SEG25 output pin (SEG25)

- PE4/SEG26 pin

  This pin has the following peripheral function:
  - LCDC SEG26 output pin (SEG26)

- Block diagram of PE0/SEG22, PE1/SEG23, PE2/SEG24, PE3/SEG25 and PE4/SEG26

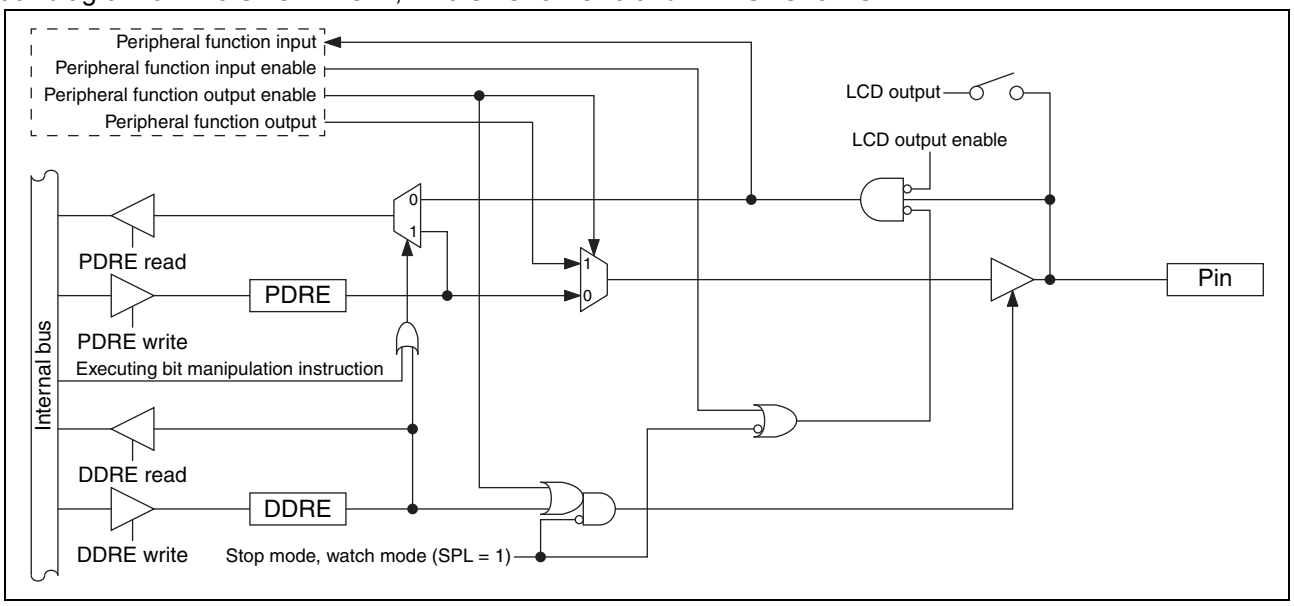


- PE5/SEG27/TO11 pin
  This pin has the following peripheral functions:
  - LCDC SEG27 output pin (SEG27)
  - 8/16-bit composite timer ch. 1 output pin (TO11)

- PE6/SEG28/TO10 pin
  This pin has the following peripheral functions:
  - LCDC SEG28 output pin (SEG28)
  - 8/16-bit composite timer ch. 1 output pin (TO10)

- PE7/SEG29/EC1 pin
  This pin has the following peripheral functions:
  - LCDC SEG29 output pin (SEG29)
  - 8/16-bit composite timer ch. 1 clock input pin (EC1)

- Block diagram of PE5/SEG27/TO11, PE6/SEG28/TO10 and PE7/SEG29/EC1



18.11.3 Port E registers

- Port E register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRE	0	Pin state is “L” level.	PDRE value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRE value is “1”.	As output port, outputs “H” level.
DDRE	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port E

	Correspondence between related register bits and pins							
Pin name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
PDRE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRE								

18.11.4 Port E operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRE register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRE register to external pins.
  - If data is written to the PDRE register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRE register returns the PDRE register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRE register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRE register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRE register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDRE register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDRE register. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDRE register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDRE register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRE register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRE register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRE register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.

- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.12 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.12.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

18.12.2 Block diagrams of port F

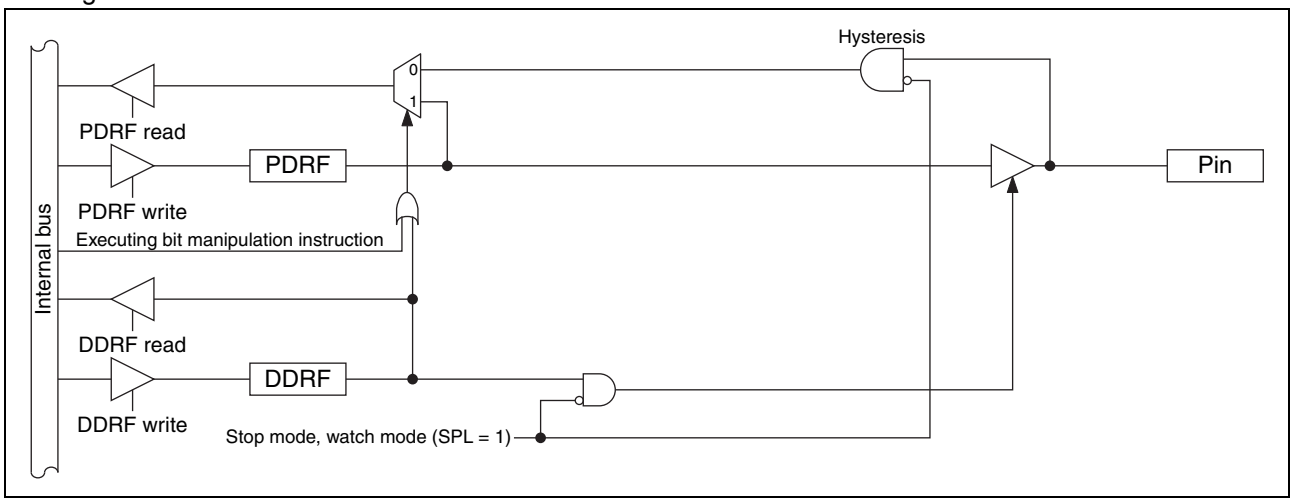
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

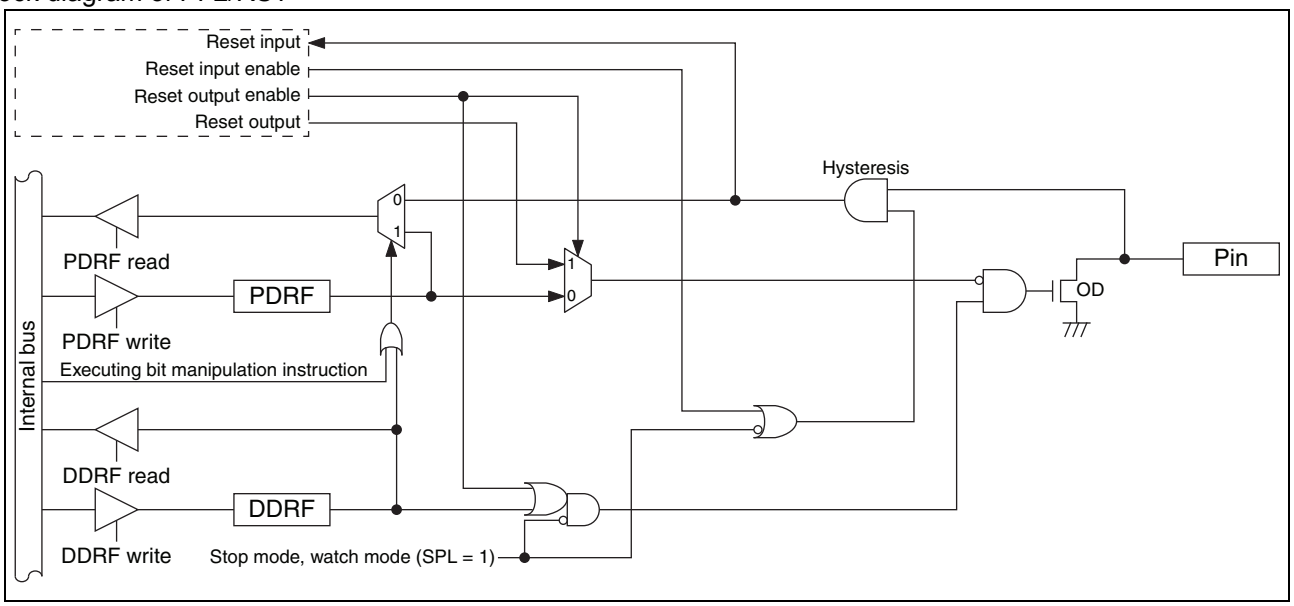
  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

- Block diagram of PF0/X0 and PF1/X1



- PF2/$\overline{\text{RST}}$ pin
  This pin has the following peripheral function:
  - Reset pin ($\overline{\text{RST}}$)

- Block diagram of PF2/$\overline{\text{RST}}$



18.12.3 Port F registers

- Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port F

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PF2***	**PF1**	**PF0**
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

*: PF2/$\overline{\text{RST}}$ is the dedicated reset pin on MB95F714M/F716M/F718M.

18.12.4 Port F operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
  - If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRF register returns the PDRF register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.13 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.13.1 Port G configuration

Port G is made up of the following elements.

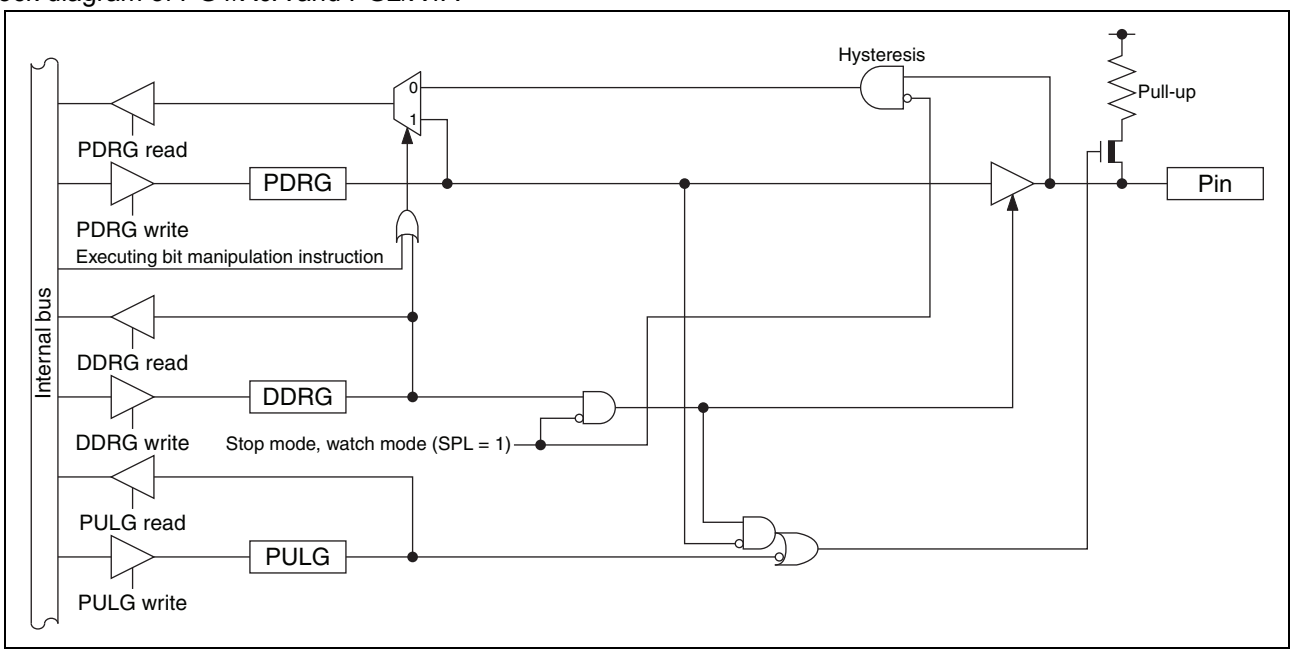
- General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up register (PULG)

18.13.2 Block diagram of port G

- PG1/X0A pin
  This pin has the following peripheral function:
  - Subclock input oscillation pin (X0A)

- PG2/X1A pin
  This pin has the following peripheral function:
  - Subclock I/O oscillation pin (X1A)

- Block diagram of PG1/X0A and PG2/X1A



18.13.3 Port G registers

- Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

- Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

18.13.4 Port G operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
  - If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRG register returns the PDRG register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

19. I/O Ports (MB95770M Series)

- List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 2 data register	PDR2	R, RM/W	0b00000000
Port 2 direction register	DDR2	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 9 data register	PDR9	R, RM/W	0b00000000
Port 9 direction register	DDR9	R/W	0b00000000
Port A data register	PDRA	R, RM/W	0b00000000
Port A direction register	DDRA	R/W	0b00000000
Port B data register	PDRB	R, RM/W	0b00000000
Port B direction register	DDRB	R/W	0b00000000
Port C data register	PDRC	R, RM/W	0b00000000
Port C direction register	DDRC	R/W	0b00000000
Port E data register	PDRE	R, RM/W	0b00000000
Port E direction register	DDRE	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 1 pull-up register	PUL1	R/W	0b00000000
Port 2 pull-up register	PUL2	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

19.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- A/D input disable register (lower) (AIDRL)

19.1.2 Block diagrams of port 0

- P00/INT00/AN00/SEG29/UO2 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT00)
  - 8/12-bit A/D converter analog input pin (AN00)
  - LCDC SEG29 output pin (SEG29)
  - UART/SIO ch. 2 data output pin (UO2)

- P02/INT02/AN02/SEG27/UCK2 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT02)
  - 8/12-bit A/D converter analog input pin (AN02)
  - LCDC SEG27 output pin (SEG27)
  - UART/SIO ch. 2 clock I/O pin (UCK2)

- P03/INT03/AN03/SEG26/UO1 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT03)
  - 8/12-bit A/D converter analog input pin (AN03)
  - LCDC SEG26 output pin (SEG26)
  - UART/SIO ch. 1 data output pin (UO1)

- P05/INT05/AN05/SEG24/UCK1 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT05)
  - 8/12-bit A/D converter analog input pin (AN05)
  - LCDC SEG24 output pin (SEG24)
  - UART/SIO ch. 1 clock I/O pin (UCK1)

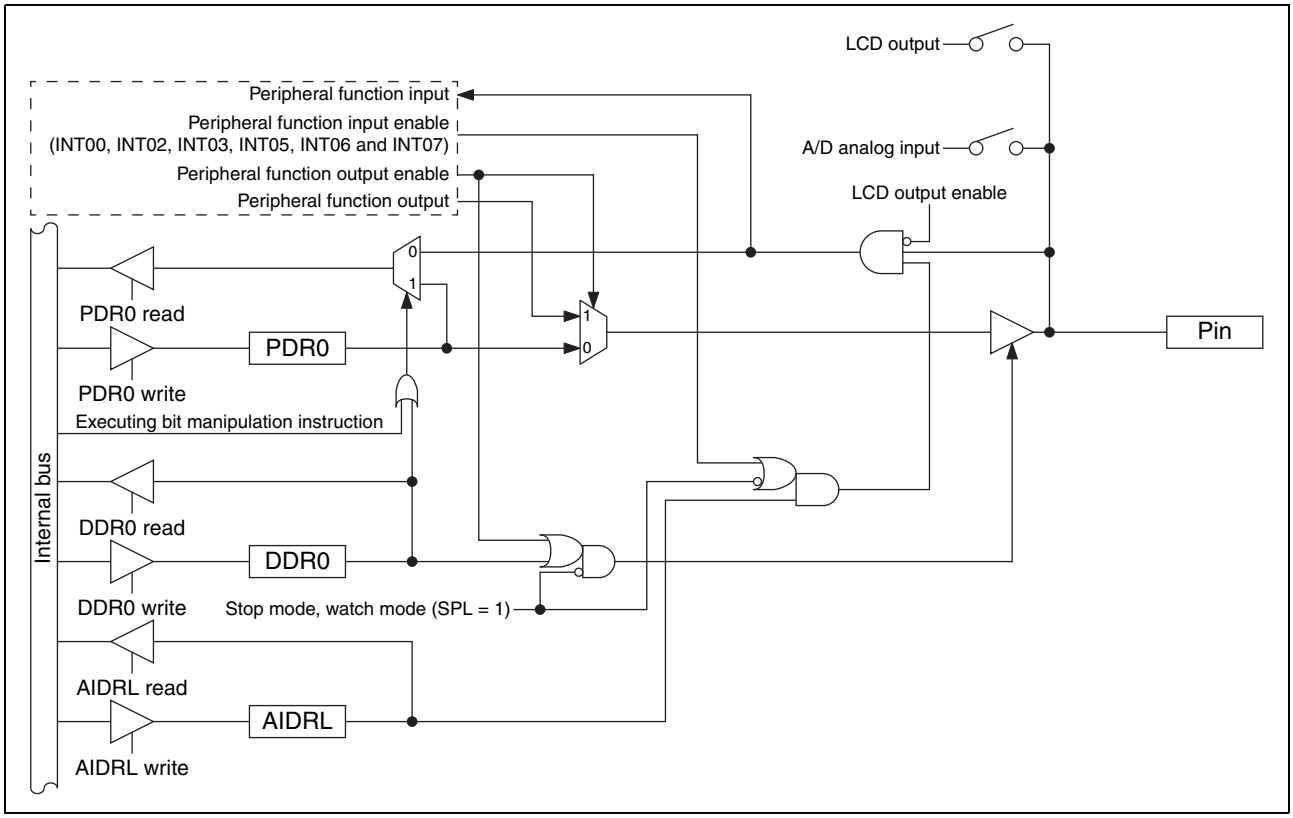
- P06/INT06/AN06/SEG23 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT06)
  - 8/12-bit A/D converter analog input pin (AN06)
  - LCDC SEG23 output pin (SEG23)

- P07/INT07/AN07/SEG22 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT07)
  - 8/12-bit A/D converter analog input pin (AN07)
  - LCDC SEG22 output pin (SEG22)

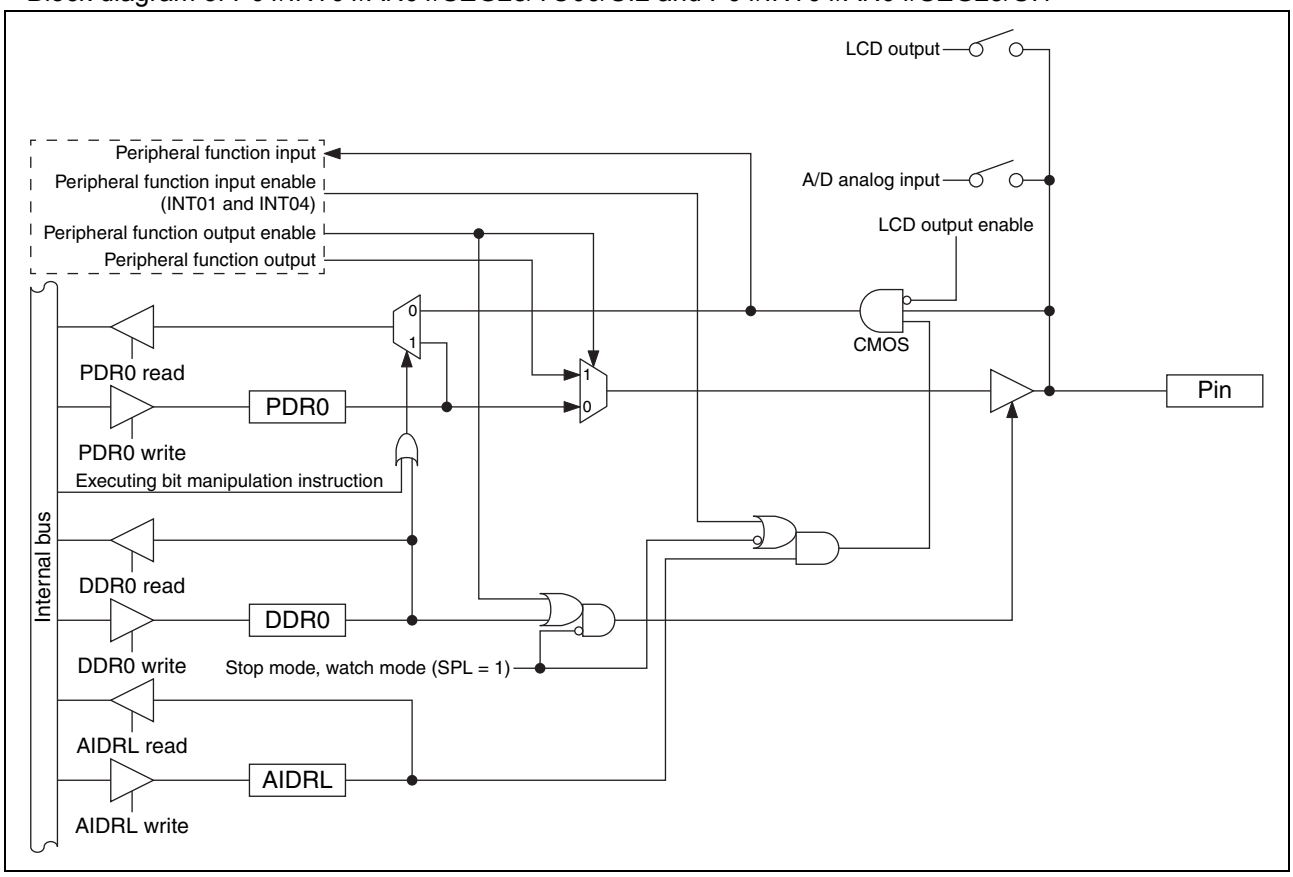
- Block diagram of P00/INT00/AN00/SEG29/UO2, P02/INT02/AN02/SEG27/UCK2, P03/INT03/AN03/SEG26/UO1, P05/INT05/AN05/SEG24/UCK1, P06/INT06/AN06/SEG23 and P07/INT07/AN07/SEG22



- P01/INT01/AN01/SEG28/TO00/UI2 pin
  This pin has the following peripheral functions:
  - External interrupt input pin (INT01)
  - 8/12-bit A/D converter analog input pin (AN01)
  - LCDC SEG28 output pin (SEG28)
  - 8/16-bit composite timer ch. 0 output pin (TO00)
  - UART/SIO ch. 2 data input pin (UI2)

- P04/INT04/AN04/SEG25/UI1 pin
  This pin has the following peripheral functions:
  - External interrupt input pin (INT04)
  - 8/12-bit A/D converter analog input pin (AN04)
  - LCDC SEG25 output pin (SEG25)
  - UART/SIO ch. 1 data input pin (UI1)

• Block diagram of P01/INT01/AN01/SEG28/TO00/UI2 and P04/INT04/AN04/SEG25/UI1



19.1.3 Port 0 registers

• Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

• Correspondence between registers and pins for port 0

	Correspondence between related register bits and pins							
Pin name	P07	P06	P05	P04	P03	P02	P01	P00
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
AIDRL								

19.1.4 Port 0 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
  - If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR0 register returns the PDR0 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When using an analog input shared pin as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to “1”.
  - If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
  - When using the analog input shared pin as another peripheral function input pin, configure it as an input port, which is the same as the operation as an input port.
  - Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR0 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset

  If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with analog input, its port input is disabled because the AIDRL register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT00 to INT07), the input is enabled and not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an analog input pin
  - Set the bit in the DDR0 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.

- Operation as an external interrupt input pin
  - Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

19.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.2.1 Port 1 configuration

Port 1 is made up of the following elements.

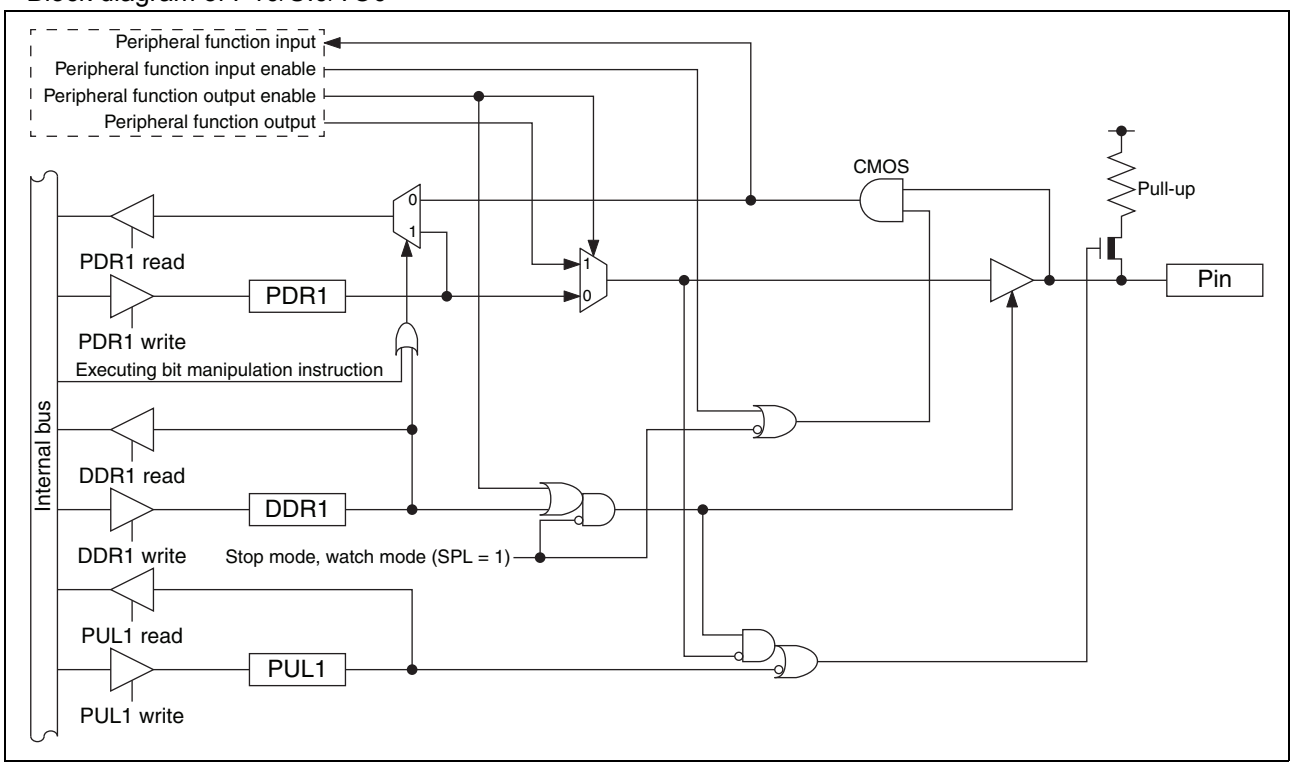
- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

19.2.2 Block diagrams of port 1

- P10/UI0/TO0 pin

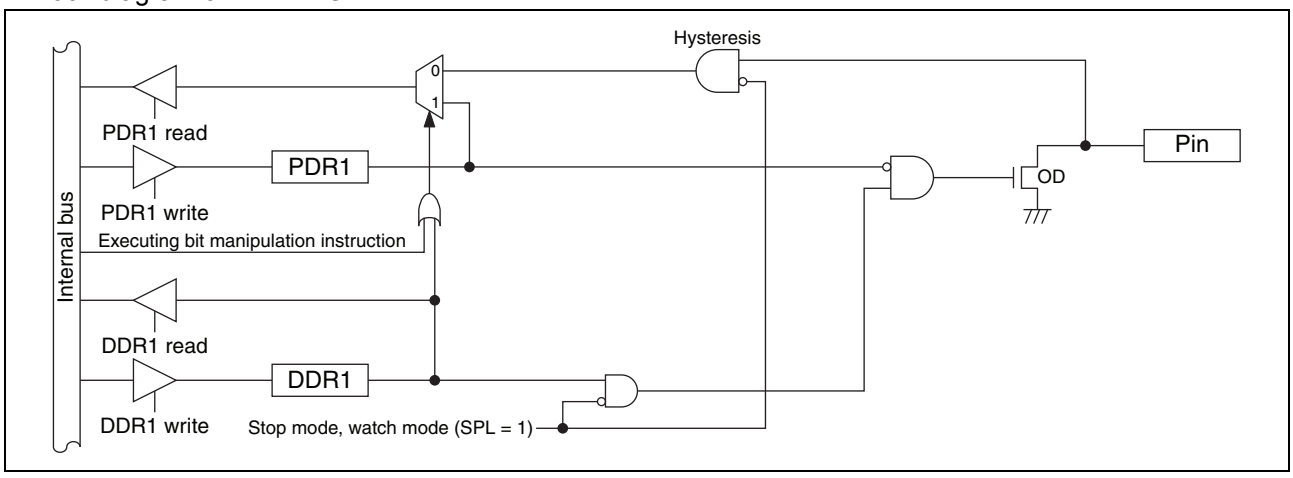
  This pin has the following peripheral functions:
  - UART/SIO ch. 0 data input pin (UI0)
  - 16-bit reload timer ch. 0 output pin (TO0)

- Block diagram of P10/UI0/TO0



- P12/DBG pin
  This pin has the following peripheral function:
  - DBG input pin (DBG)

- Block diagram of P12/DBG



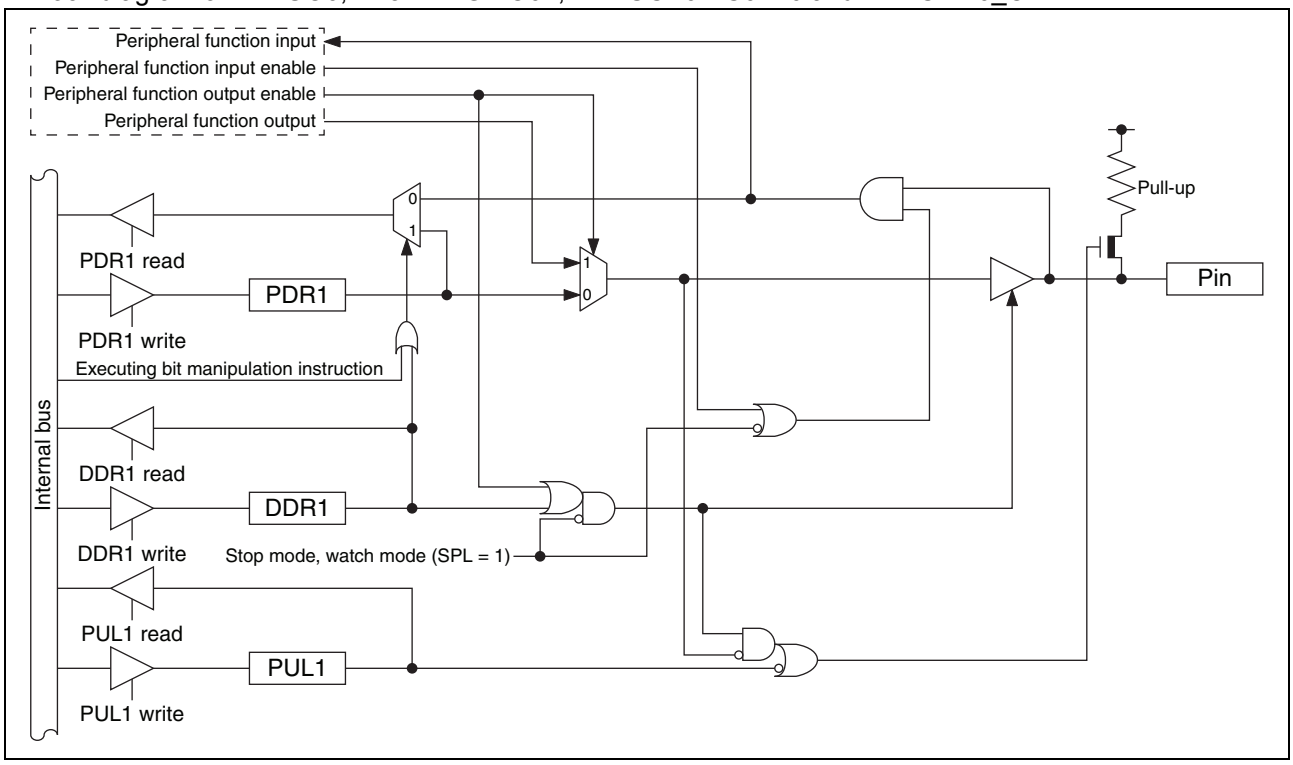
- P11/UO0 pin
  This pin has the following peripheral function:
  - UART/SIO ch. 0 data output pin (UO0)

- P13/ADTG/TO01 pin
  This pin has the following peripheral functions:
  - 8/12-bit A/D converter trigger input pin (ADTG)
  - 8/16-bit composite timer ch. 0 output pin (TO01)

- P14/UCK0/EC0/TI0 pin
  This pin has the following peripheral functions:
  - UART/SIO ch. 0 clock I/O pin (UCK0)
  - 8/16-bit composite timer ch. 0 clock input pin (EC0)
  - 16-bit reload timer ch. 0 input pin (TI0)

- P17/CMP0_O pin
  This pin has the following peripheral function:
  - Comparator ch. 0 digital output pin (CMP0_O)

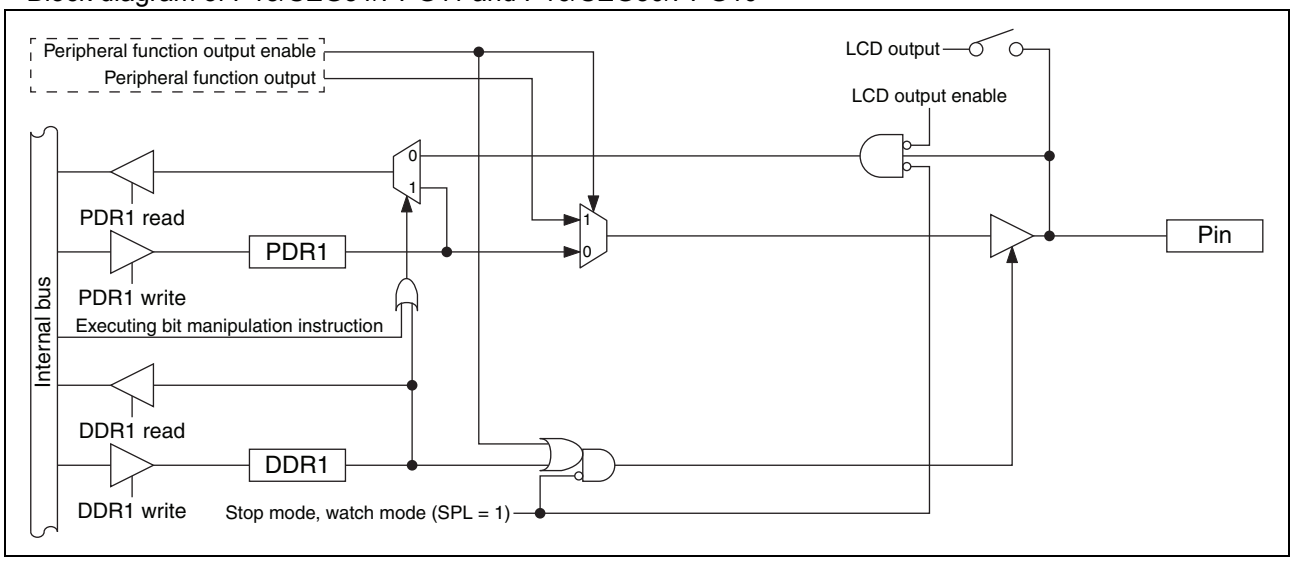
- Block diagram of P11/UO0, P13/ADTG/TO01, P14/UCK0/EC0/TI0 and P17/CMP0_O



- P15/SEG31/PPG11 pin
  This pin has the following peripheral functions:
  - LCDC SEG31 output pin (SEG31)
  - 8/16-bit PPG ch. 1 output pin (PPG11)

- P16/SEG30/PPG10 pin
  This pin has the following peripheral functions:
  - LCDC SEG30 output pin (SEG30)
  - 8/16-bit PPG ch. 1 output pin (PPG10)

- Block diagram of P15/SEG31/PPG11 and P16/SEG30/PPG10



19.2.3 Port 1 registers

- Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10
PDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR1								
PUL1		-	-			-		

19.2.4 Port 1 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
  - If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR1 register returns the PDR1 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR1 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P10/UI0/TO0 and P14/UCK0/EC0/TI0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

19.3 Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.3.1 Port 2 configuration

Port 2 is made up of the following elements.

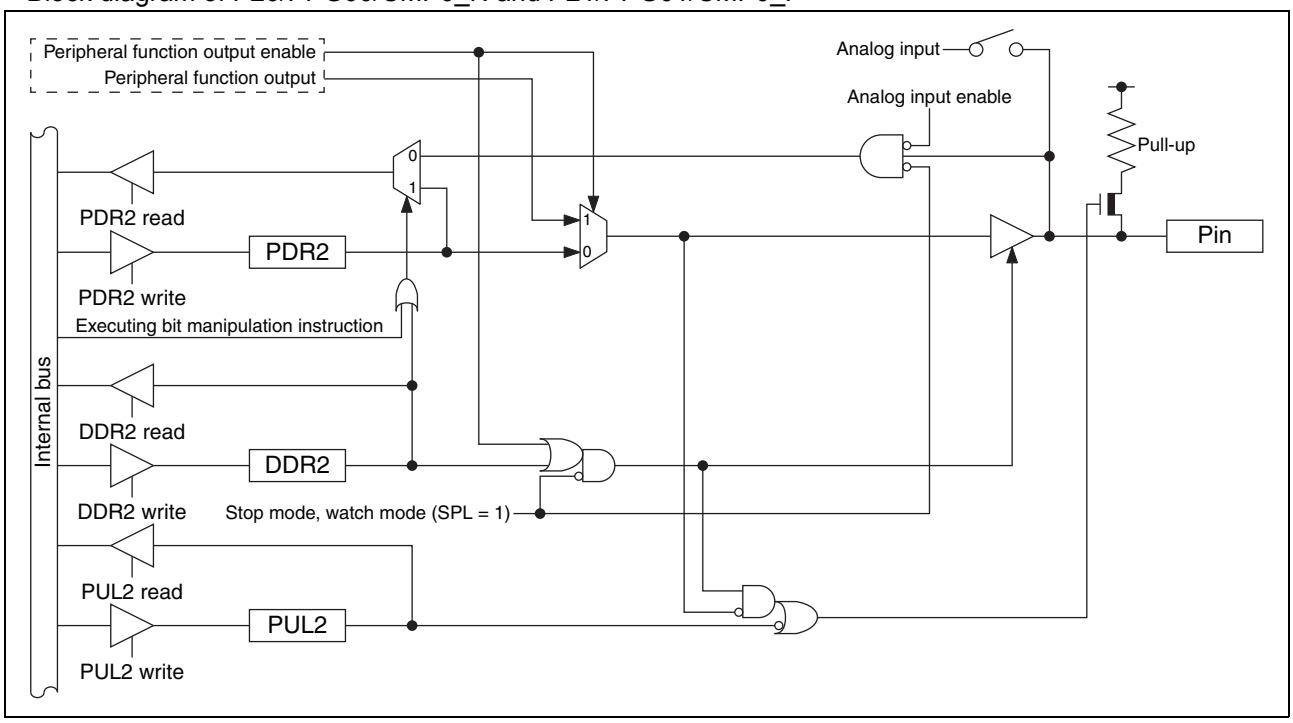
- General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

19.3.2 Block diagrams of port 2

- P20/PPG00/CMP0_N pin
  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG00)
  - Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

- P21/PPG01/CMP0_P pin
  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG01)
  - Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)

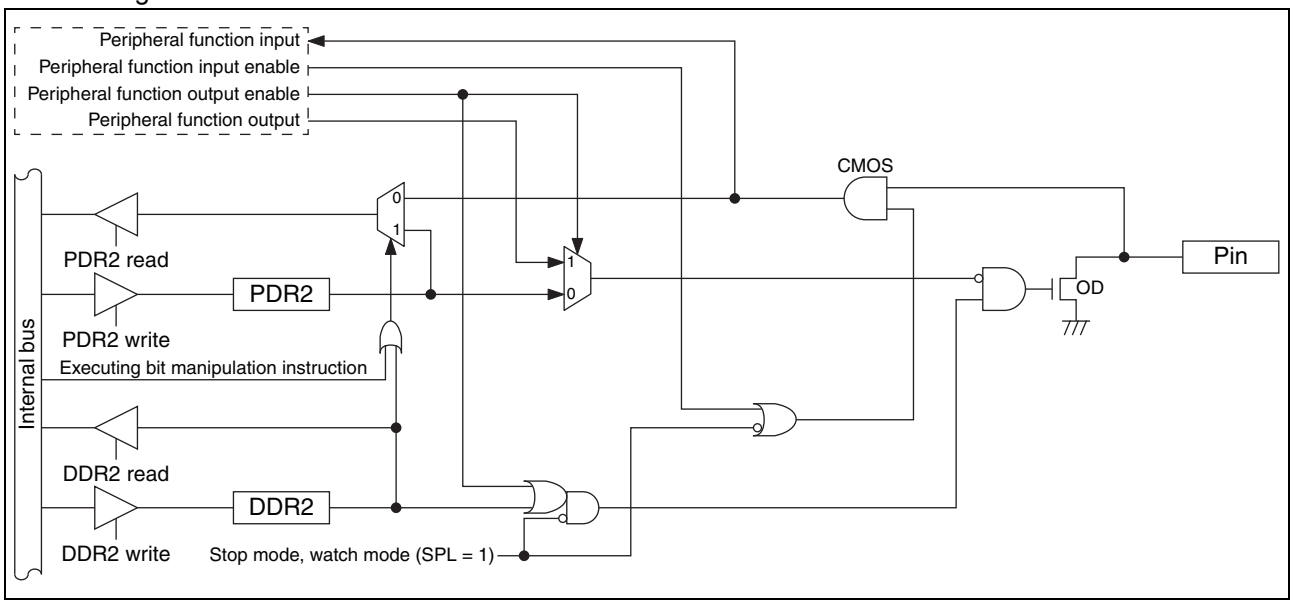
- Block diagram of P20/PPG00/CMP0_N and P21/PPG01/CMP0_P



- P22/SCL pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 clock I/O pin (SCL)

- P23/SDA pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 data I/O pin (SDA)

- Block diagram of P22/SCL and P23/SDA



19.3.3 Port 2 registers

- Port 2 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR2	0	Pin state is “L” level.	PDR2 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR2 value is “1”.	As output port, outputs “H” level.*
DDR2	0	Port input enabled		
	1	Port output enabled		
PUL2	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 2

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**P23**	**P22**	**P21**	**P20**
PDR2	-	-	-	-	bit3	bit2	bit1	bit0
DDR2								
PUL2					-	-		

19.3.4 Port 2 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR2 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR2 register to external pins.
  - If data is written to the PDR2 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR2 register returns the PDR2 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR2 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR2 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR2 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR2 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR2 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR2 register corresponding to the input pin of a peripheral function to “0”.

- Reading the PDR2 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR2 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR2 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL2 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL2 register.

- Operation as a comparator input pin
  - Regardless of the value of the PDR2 register and that of the DDR2 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit to “1”.
  - For details of the comparator, refer to “CHAPTER 29 COMPARATOR” in “New 8FX MB95710M/770M Series Hardware Manual”.

19.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.4.1 Port 6 configuration

Port 6 is made up of the following elements.
- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)

19.4.2 Block diagrams of port 6

- P60/SEG06 pin
  This pin has the following peripheral function:
  - LCDC SEG06 output pin (SEG06)

- P61/SEG07 pin
  This pin has the following peripheral function:
  - LCDC SEG07 output pin (SEG07)

- P62/SEG08 pin
  This pin has the following peripheral function:
  - LCDC SEG08 output pin (SEG08)

- P63/SEG09 pin
  This pin has the following peripheral function:
  - LCDC SEG09 output pin (SEG09)

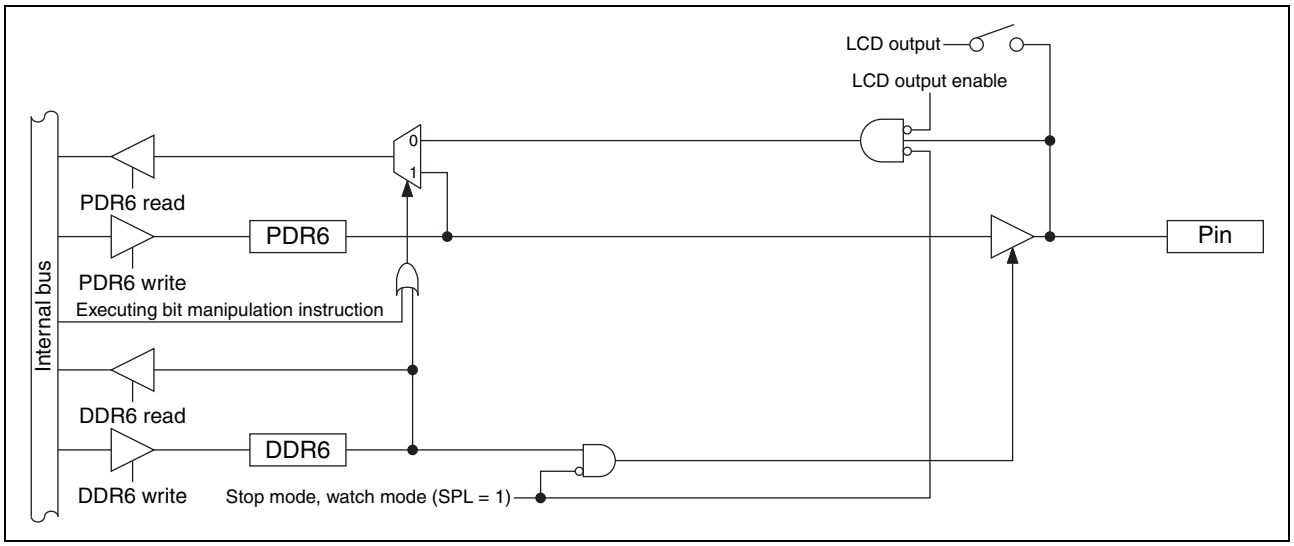
- P64/SEG10 pin
  This pin has the following peripheral function:
  - LCDC SEG10 output pin (SEG10)

- P65/SEG11 pin
  This pin has the following peripheral function:
  - LCDC SEG11 output pin (SEG11)

- P66/SEG12 pin
  This pin has the following peripheral function:
  - LCDC SEG12 output pin (SEG12)

- P67/SEG13 pin
  This pin has the following peripheral function:
  - LCDC SEG13 output pin (SEG13)

- Block diagram of P60/SEG06, P61/SEG07, P62/SEG08, P63/SEG09, P64/SEG10, P65/SEG11, P66/SEG12 and P67/SEG13



19.4.3 Port 6 registers

- Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.
DDR6	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port 6

	Correspondence between related register bits and pins							
Pin name	P67	P66	P65	P64	P63	P62	P61	P60
PDR6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR6								

19.4.4 Port 6 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
  - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR6 register returns the PDR6 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR6 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.5 Port 9

Port 9 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.5.1 Port 9 configuration

Port 9 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 9 data register (PDR9)
- Port 9 direction register (DDR9)

19.5.2 Block diagrams of port 9

- P90/V4 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V4)

- P91/V3 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V3)

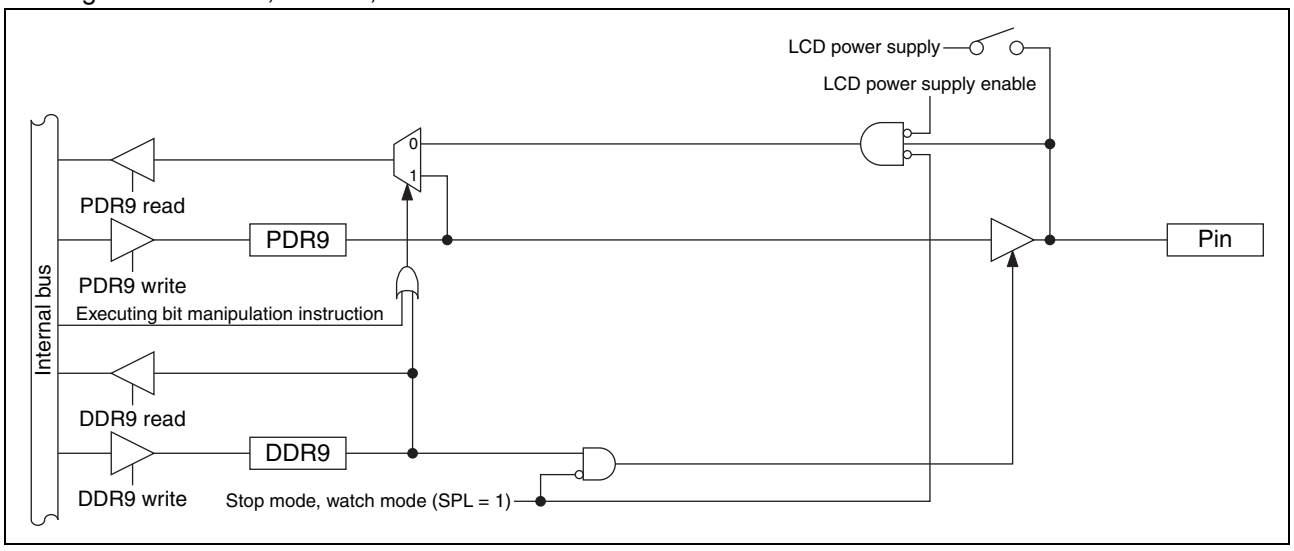
- P92/V2 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V2)

- P93/V1 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V1)

- Block diagram of P90/V4, P91/V3, P92/V2 and P93/V1



19.5.3 Port 9 registers

- Port 9 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR9	0	Pin state is “L” level.	PDR9 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR9 value is “1”.	As output port, outputs “H” level.
DDR9	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port 9

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**P93**	**P92**	**P91**	**P90**
PDR9	-	-	-	-	bit3	bit2	bit1	bit0
DDR9								

19.5.4 Port 9 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR9 register corresponding to that pin is set to “1”.
  - When a pin is used as an output port, it outputs the value of the PDR9 register to external pins.
  - If data is written to the PDR9 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR9 register returns the PDR9 register value.
  - To use a pin shared with the LCDC as an output port, set the bit corresponding to that pin in the VE[4:1] bits in the LCDC enable register 1 (LCDCE1) to “0” to select the general-purpose I/O port function.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR9 register corresponding to that pin is set to “0”.
  - If data is written to the PDR9 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR9 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR9 register, the PDR9 register value is returned.
  - To use a pin shared with the LCDC as an input port, set the bit corresponding to that pin in the VE[4:1] bits in the LCDCE1 register to “0” to select the general-purpose I/O port function.

- Operation at reset
  If the CPU is reset, all bits in the DDR9 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR9 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an LCD drive power supply pin
  - Set the bit in the DDR9 register corresponding to an LCD drive power supply pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCD drive power supply pin, set the bit corresponding to that pin in the VE[4:1] bits in the LCDCE1 register to “1” to select the LCD drive power supply function.

19.6 Port A

Port A is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.6.1 Port A configuration

Port A is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port A data register (PDRA)
- Port A direction register (DDRA)

19.6.2 Block diagrams of port A

- PA0/COM0 pin
  This pin has the following peripheral function:
  - LCDC COM0 output pin (COM0)

- PA1/COM1 pin
  This pin has the following peripheral function:
  - LCDC COM1 output pin (COM1)

- PA2/COM2 pin
  This pin has the following peripheral function:
  - LCDC COM2 output pin (COM2)

- PA3/COM3 pin
  This pin has the following peripheral function:
  - LCDC COM3 output pin (COM3)

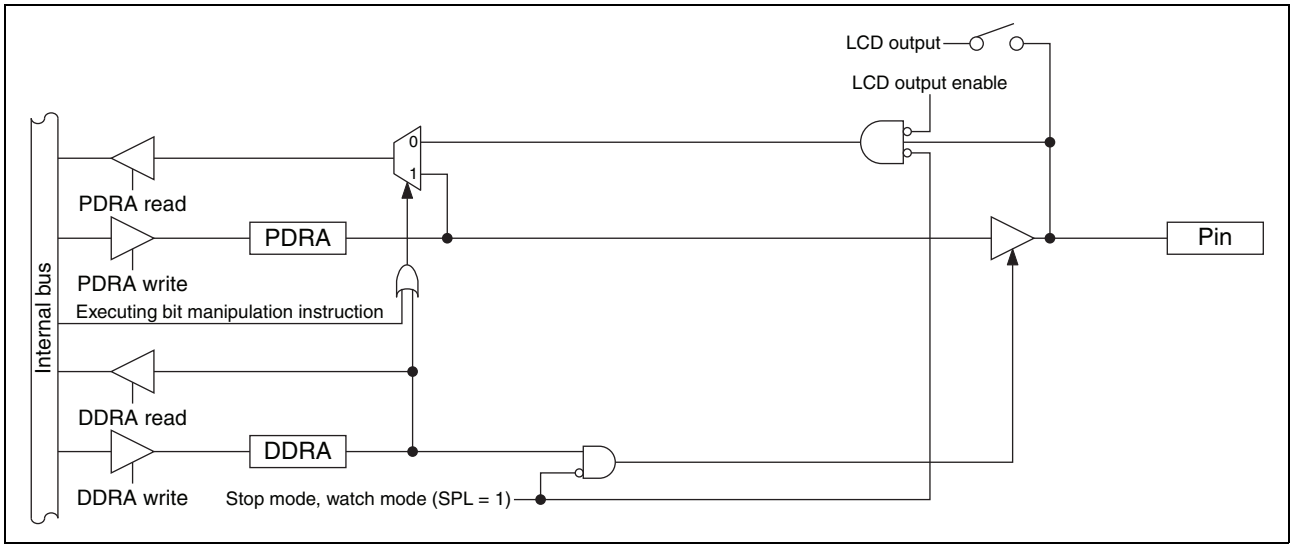
- PA4/COM4 pin
  This pin has the following peripheral function:
  - LCDC COM4 output pin (COM4)

- PA5/COM5 pin
  This pin has the following peripheral function:
  - LCDC COM5 output pin (COM5)

- PA6/COM6 pin
  This pin has the following peripheral function:
  - LCDC COM6 output pin (COM6)

- PA7/COM7 pin
  This pin has the following peripheral function:
  - LCDC COM7 output pin (COM7)

- Block diagram of PA0/COM0, PA1/COM1, PA2/COM2, PA3/COM3, PA4/COM4, PA5/COM5, PA6/COM6 and PA7/COM7



19.6.3 Port A registers

- Port A register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRA	0	Pin state is “L” level.	PDRA value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRA value is “1”.	As output port, outputs “H” level.
DDRA	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port A

	Correspondence between related register bits and pins							
Pin name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PDRA	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRA								

19.6.4 Port A operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRA register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRA register to external pins.
  - If data is written to the PDRA register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRA register returns the PDRA register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRA register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRA register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRA register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRA register, the PDRA register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC common output pin
  - Set the bit in the DDRA register corresponding to an LCDC common output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC common output pin, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “1” to select the LCDC common output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRA register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRA register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.7 Port B

Port B is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.7.1 Port B configuration

Port B is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port B data register (PDRB)
- Port B direction register (DDRB)

19.7.2 Block diagrams of port B

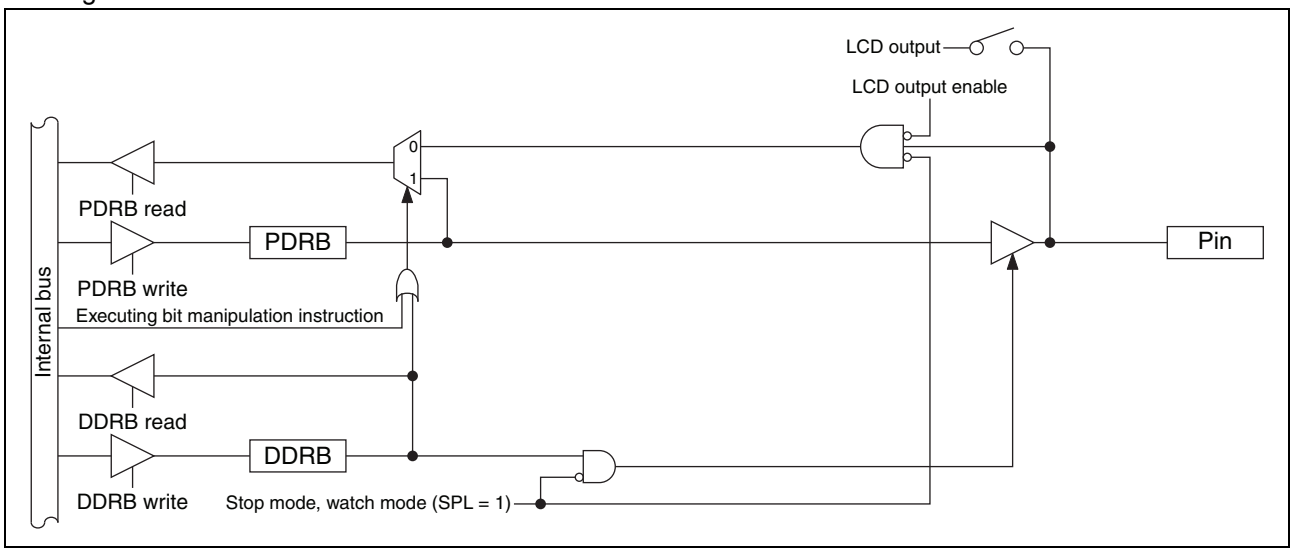
- PB0/SEG00 pin

  This pin has the following peripheral function:
  - LCDC SEG00 output pin (SEG00)

- PB1/SEG01 pin

  This pin has the following peripheral function:
  - LCDC SEG01 output pin (SEG01)

- Block diagram of PB0/SEG00 and PB1/SEG01



19.7.3 Port B registers

- Port B register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRB	0	Pin state is “L” level.	PDRB value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRB value is “1”.	As output port, outputs “H” level.
DDRB	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port B

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**-**	**PB1**	**PB0**
PDRB	-	-	-	-	-	-	bit1	bit0
DDRB								

19.7.4 Port B operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRB register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRB register to external pins.
  - If data is written to the PDRB register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRB register returns the PDRB register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRB register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRB register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRB register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRB register, the PDRB register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRB register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRB register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRB register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.8 Port C

Port C is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.8.1 Port C configuration

Port C is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port C data register (PDRC)
- Port C direction register (DDRC)

19.8.2 Block diagrams of port C

- PC0/SEG02 pin

  This pin has the following peripheral function:
  - LCDC SEG02 output pin (SEG02)

- PC1/SEG03 pin

  This pin has the following peripheral function:
  - LCDC SEG03 output pin (SEG03)

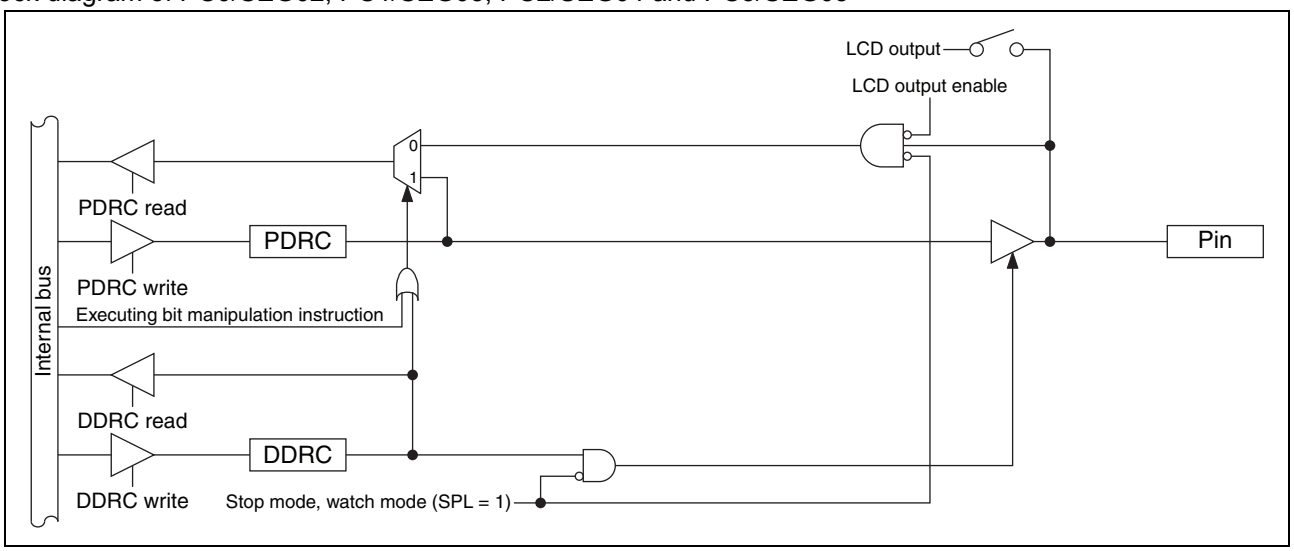
- PC2/SEG04 pin

  This pin has the following peripheral function:
  - LCDC SEG04 output pin (SEG04)

- PC3/SEG05 pin

  This pin has the following peripheral function:
  - LCDC SEG05 output pin (SEG05)

- Block diagram of PC0/SEG02, PC1/SEG03, PC2/SEG04 and PC3/SEG05



19.8.3 Port C registers

- Port C register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRC	0	Pin state is “L” level.	PDRC value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRC value is “1”.	As output port, outputs “H” level.
DDRC	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port C

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**PC3**	**PC2**	**PC1**	**PC0**
PDRC	-	-	-	-	bit3	bit2	bit1	bit0
DDRC								

19.8.4 Port C operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRC register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRC register to external pins.
  - If data is written to the PDRC register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRC register returns the PDRC register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRC register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRC register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRC register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRC register, the PDRC register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRC register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRC register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRC register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.9 Port E

Port E is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.9.1 Port E configuration

Port E is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port E data register (PDRE)
- Port E direction register (DDRE)

19.9.2 Block diagrams of port E

- PE0/SEG14 pin

  This pin has the following peripheral function:
  - LCDC SEG14 output pin (SEG14)

- PE1/SEG15 pin

  This pin has the following peripheral function:
  - LCDC SEG15 output pin (SEG15)

- PE2/SEG16 pin

  This pin has the following peripheral function:
  - LCDC SEG16 output pin (SEG16)

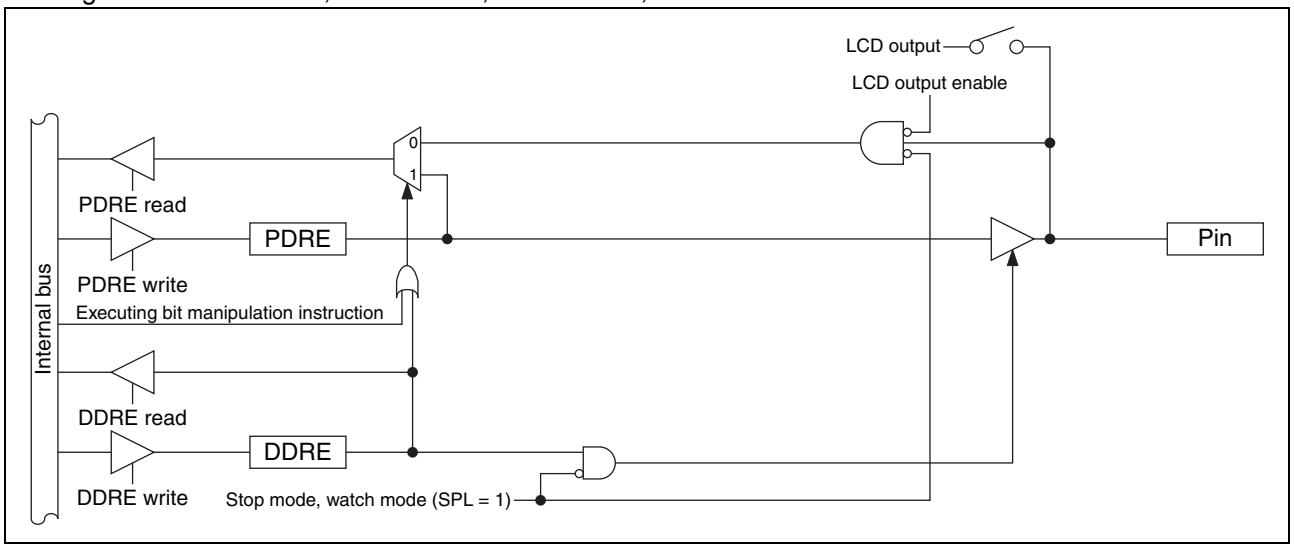
- PE3/SEG17 pin

  This pin has the following peripheral function:
  - LCDC SEG17 output pin (SEG17)

- PE4/SEG18 pin

  This pin has the following peripheral function:
  - LCDC SEG18 output pin (SEG18)

- Block diagram of PE0/SEG14, PE1/SEG15, PE2/SEG16, PE3/SEG17 and PE4/SEG18

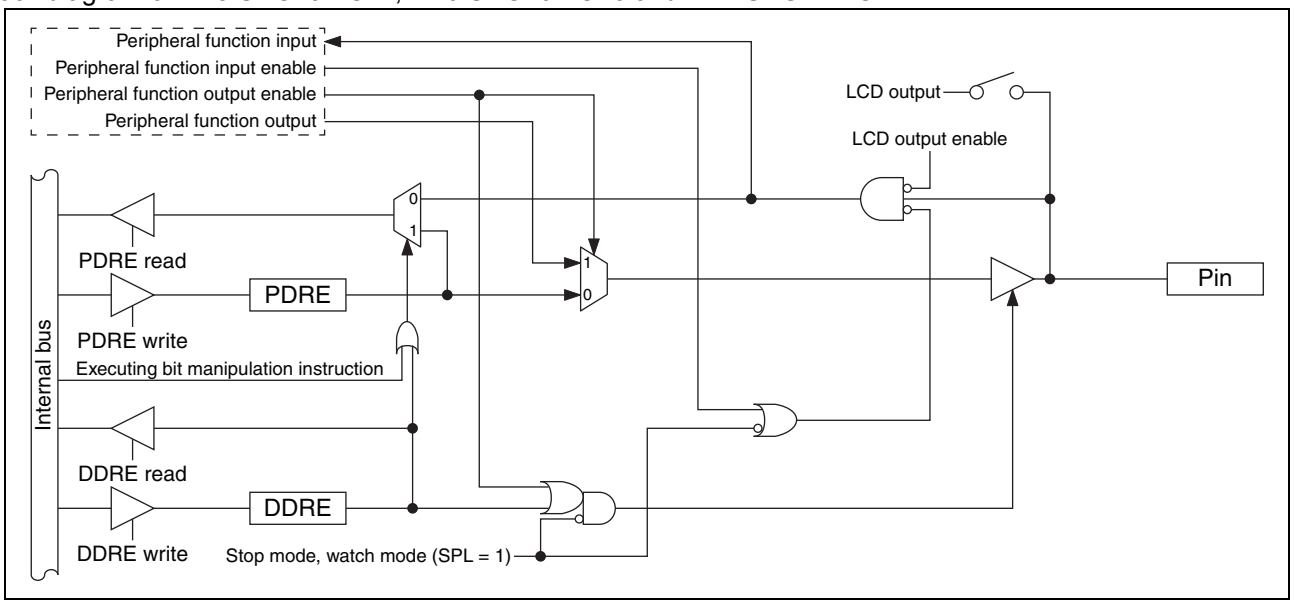


- PE5/SEG19/TO11 pin
  This pin has the following peripheral functions:
  - LCDC SEG19 output pin (SEG19)
  - 8/16-bit composite timer ch. 1 output pin (TO11)

- PE6/SEG20/TO10 pin
  This pin has the following peripheral functions:
  - LCDC SEG20 output pin (SEG20)
  - 8/16-bit composite timer ch. 1 output pin (TO10)

- PE7/SEG21/EC1 pin
  This pin has the following peripheral functions:
  - LCDC SEG21 output pin (SEG21)
  - 8/16-bit composite timer ch. 1 clock input pin (EC1)

- Block diagram of PE5/SEG19/TO11, PE6/SEG20/TO10 and PE7/SEG21/EC1



19.9.3 Port E registers

- Port E register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRE	0	Pin state is “L” level.	PDRE value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRE value is “1”.	As output port, outputs “H” level.
DDRE	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port E

	Correspondence between related register bits and pins							
Pin name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
PDRE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRE								

19.9.4 Port E operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRE register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRE register to external pins.
  - If data is written to the PDRE register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRE register returns the PDRE register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:14]) or in the LCDC enable register 5 (LCDCE5:SEG[21:16]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRE register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRE register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRE register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:14]) or in the LCDC enable register 5 (LCDCE5:SEG[21:16]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDRE register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDRE register. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDRE register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDRE register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRE register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:14]) or in the LCDC enable register 5 (LCDCE5:SEG[21:16]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRE register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRE register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.

- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.10 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.10.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

19.10.2 Block diagrams of port F

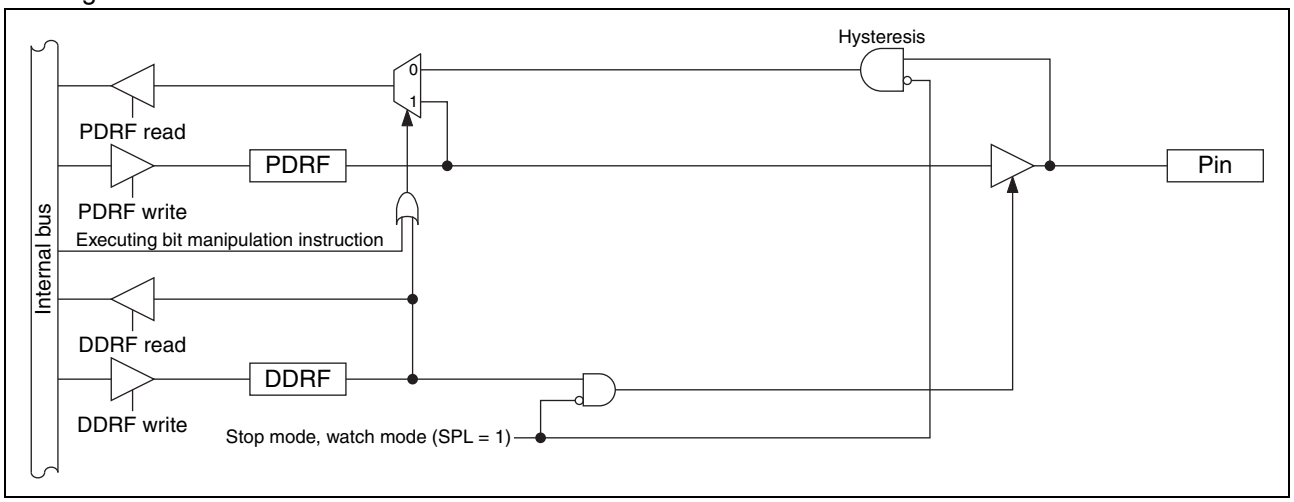
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

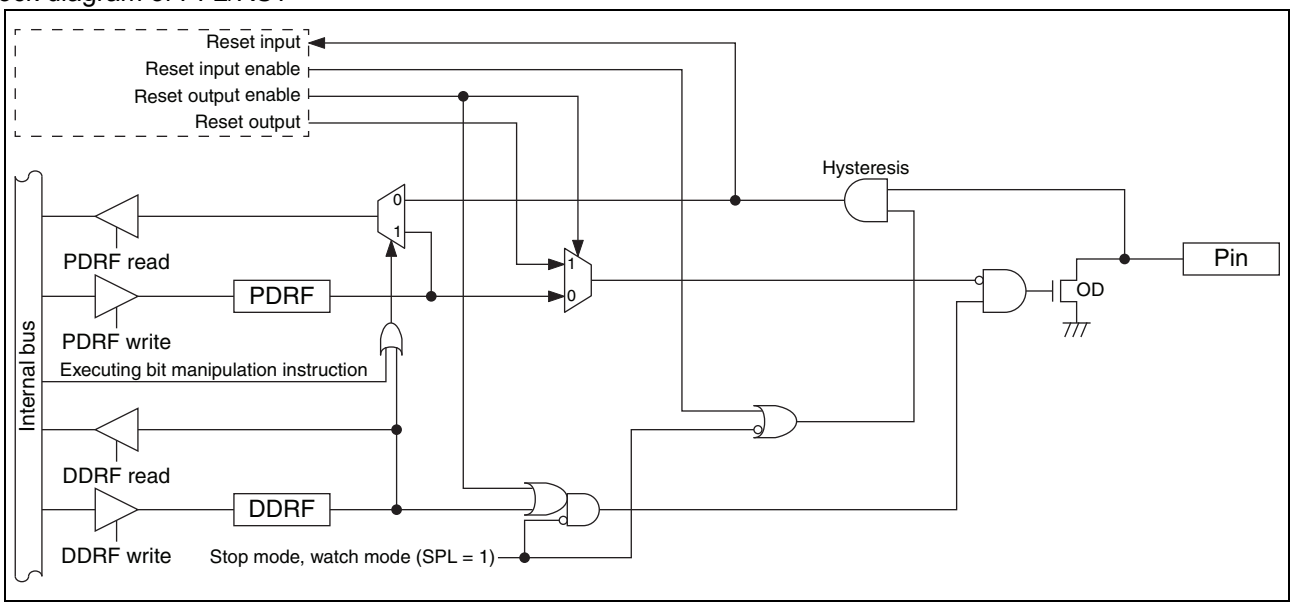
  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

- Block diagram of PF0/X0 and PF1/X1



- PF2/$\overline{\text{RST}}$ pin
  This pin has the following peripheral function:
  - Reset pin ($\overline{\text{RST}}$)

- Block diagram of PF2/$\overline{\text{RST}}$



19.10.3 Port F registers

- Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port F

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PF2***	**PF1**	**PF0**
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

*: PF2/$\overline{\text{RST}}$ is the dedicated reset pin on MB95F774M/F776M/F778M.

19.10.4 Port F operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
  - If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRF register returns the PDRF register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.11 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.11.1 Port G configuration

Port G is made up of the following elements.

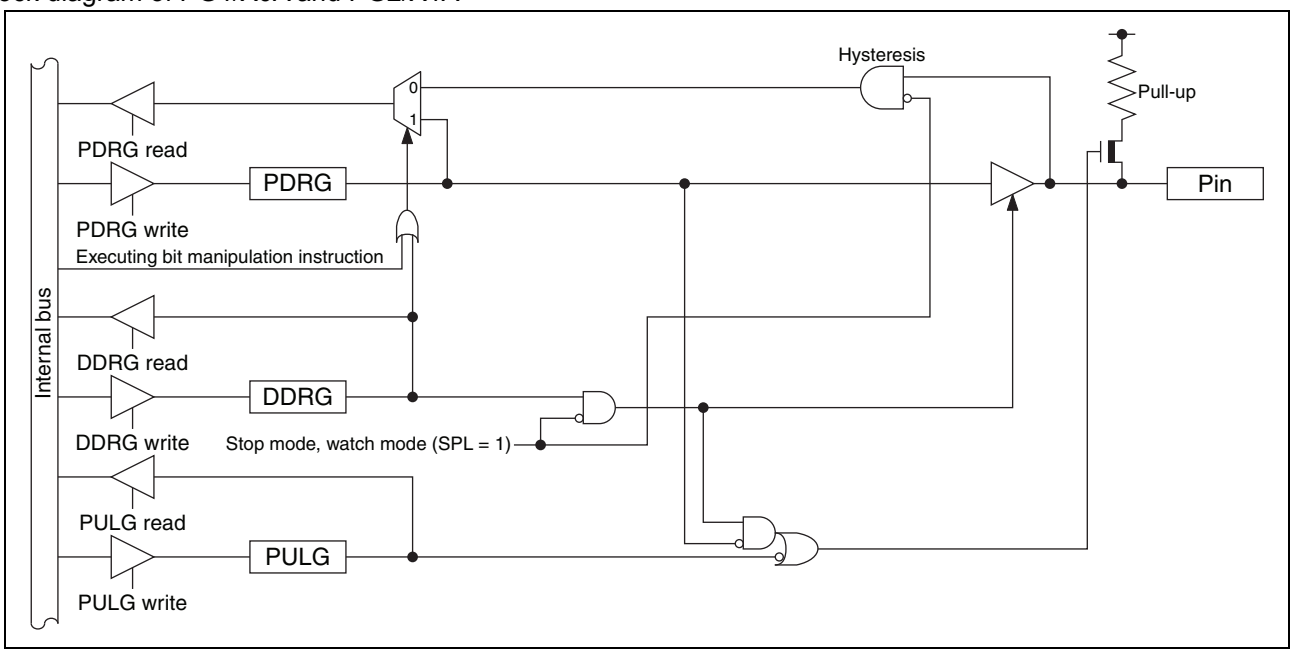
- General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up register (PULG)

19.11.2 Block diagram of port G

- PG1/X0A pin
  This pin has the following peripheral function:
  - Subclock input oscillation pin (X0A)

- PG2/X1A pin
  This pin has the following peripheral function:
  - Subclock I/O oscillation pin (X1A)

- Block diagram of PG1/X0A and PG2/X1A



19.11.3 Port G registers

- Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

- Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

19.11.4 Port G operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
  - If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRG register returns the PDRG register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

20. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High
External interrupt ch. 4						
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5						
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
Low-voltage detection circuit						
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
UART/SIO ch. 2	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
LCDC	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
UART/SIO ch. 1						
8/16-bit PPG ch. 1 (upper)	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
16-bit reload timer ch. 0	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
Comparator ch. 0	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/12-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
Watch counter						
—	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	Low

21. Pin States In Each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*1
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*1
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*5
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PG1/X0A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*6
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PG2/X1A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*6
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
P00/INT00/ AN00/ SEG29*8/ UO2 P01/INT01/ AN01/ SEG28*8/ SEG36*8/ TO00*9/UI2 P02/INT02/ AN02/ SEG27*8/ SEG35*8/ UCK2 P03/INT03/ AN03/ SEG26*8/ SEG34*8/ UO1	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Hi-Z - Input blocked*3

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P04/INT04/ AN04/ SEG25*8/ SEG33*8/ UI1 P05/INT05/ AN05/ SEG24*8/ SEG32*8/ UCK1 P06/INT06/ AN06/ SEG23*8/ SEG31*8 P07/INT07/ AN07/ SEG22*8/ SEG30*8	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Hi-Z - Input blocked*3
P10/UI0/ TO0*9 P11/UO0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Hi-Z - Input enabled*4 (However, it does not function.)
P12/DBG	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	“H”	- Previous state kept - Input blocked*3	“H”	“H”
P13/ADTG/ TO01*9 P14/UCK0/ EC0*9/TI0*9	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Hi-Z - Input enabled*4 (However, it does not function.)
P15/ SEG31*8/ PPG11 P16/ SEG30*8/ PPG10	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
P17/ CMP0_O	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept*11 - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Previous state kept*11 - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Hi-Z - Input enabled*4 (However, it does not function.)
P20/ PPG00/ CMP0_N P21/ PPG01/ CMP0_P	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*3, *12	- Hi-Z*7 - Input blocked*3, *12	- Previous state kept - Input blocked*3, *12	- Hi-Z*7 - Input blocked*3, *12	- Hi-Z - Input enabled*4
P22/SCL P23/SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3, *13	- Hi-Z - Input blocked*3, *13	- Previous state kept - Input blocked*3, *13	- Hi-Z - Input blocked*3, *13	- Hi-Z - Input enabled*4

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P40/ SEG21*14	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
P41/ SEG20*14							
P42/ SEG19*14							
P43/ SEG18*14							
P50/ TO01*14	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Hi-Z - Input enabled*4 (However, it does not function.)
P51/EC0*14							
P52/TI0/ TO00*14							
P53/TO0*14							
P60/ SEG06*8/ SEG10*8	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
P61/ SEG07*8/ SEG11*8							
P62/ SEG08*8/ SEG12*8							
P63/ SEG09*8/ SEG13*8							
P64/ SEG10*8/ SEG14*8							
P65/ SEG11*8/ SEG15*8							
P66/ SEG12*8/ SEG16*8							
P67/ SEG13*8/ SEG17*8							
P90/V4	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
P91/V3							
P92/V2							
P93/V1							
P94/V0*14							

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PA0/COM0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
PA1/COM1							
PA2/COM2							
PA3/COM3							
PA4/COM4							
PA5/COM5							
PA6/COM6							
PA7/COM7							
PB0/SEG00	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
PB1/SEG01							
PB2/ SEG37*14							
PB3/ SEG38*14							
PB4/ SEG39*14							
PC0/ SEG02	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
PC1/ SEG03							
PC2/ SEG04							
PC3/ SEG05							
PC4/ SEG06*14							
PC5/ SEG07*14							
PC6/ SEG08*14							
PC7/ SEG09*14							

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PE0/ SEG14*8/ SEG22*8	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
PE1/ SEG15*8/ SEG23*8							
PE2/ SEG16*8/ SEG24*8							
PE3/ SEG17*8/ SEG25*8							
PE4/ SEG18*8/ SEG26*8							
PE5/ SEG19*8/ SEG27*8/ TO11							
PE6/ SEG20*8/ SEG28*8/ TO10							
PE7/ SEG21*8/ SEG29*8/ EC1							

SPL: Pin state setting bit in the standby control register (STBC:SPL)
Hi-Z: High impedance
*1: PF0/X0 and PF1/X1 transit to this state on a reset when configured as a main clock oscillation pins.
*2: The pin stays at the state shown when configured as a general-purpose I/O port.
*3: “Input blocked” means direct input gate operation from the pin is disabled.
*4: “Input enabled” means that the input function is enabled. While the input function is enabled, execute a pull-up operation or a pull-down operation to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.
*5: The PF2/$\overline{\text{RST}}$ pin stays at the state shown when configured as a reset pin.
*6: PG1/X0A and PG2/X1A transit to this state on a reset when configured as subclock oscillation pins.
*7: The pull-up control setting is still effective.
*8: The MB95710M Series and the MB95770M Series have different SEG output assignment as shown below.

SEG output	Pin on MB95710M Series	Pin on MB95770M Series
SEG06	PC4	P60
SEG07	PC5	P61
SEG08	PC6	P62
SEG09	PC7	P63
SEG10	P60	P64
SEG11	P61	P65
SEG12	P62	P66
SEG13	P63	P67
SEG14	P64	PE0
SEG15	P65	PE1
SEG16	P66	PE2

SEG output	Pin on MB95710M Series	Pin on MB95770M Series
SEG17	P67	PE3
SEG18	P43	PE4
SEG19	P42	PE5
SEG20	P41	PE6
SEG21	P40	PE7
SEG22	PE0	P07
SEG23	PE1	P06
SEG24	PE2	P05
SEG25	PE3	P04
SEG26	PE4	P03
SEG27	PE5	P02
SEG28	PE6	P01
SEG29	PE7	P00
SEG30	P07	P16
SEG31	P06	P15
SEG32	P05	—
SEG33	P04	—
SEG34	P03	—
SEG35	P02	—
SEG36	P01	—

*9: On the MB95770M Series, TO00 is assigned to P01, TO0 to P10, TO01 to P13, and EC0 and TI0 to P14.

*10: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.

*11: The output function of the comparator is still in operation in stop mode and watch mode.

*12: Though input is blocked, an analog signal can also be input to generate a comparator interrupt when the comparator interrupt is enabled.

*13: The I^2C bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wakeup function is enabled. For details of the MCU standby mode wakeup function, refer to “CHAPTER 23 I^2C BUS INTERFACE” in “New 8FX MB95710M/770M Series Hardware Manual”.

*14: P40/SEG21, P41/SEG20, P42/SEG19, P43/SEG18, P50/TO01, P51/EC0, P52/TI0/TO00, P53/TO0, P94/V0, PB2/SEG37, PB3/SEG38, PB4/SEG39, PC4/SEG06, PC5/SEG07, PC6/SEG08 and PC7/SEG09 are only available on the MB95710M Series.

22. Electrical Characteristics

22.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average current	I_{OLAV}	—	4	mA	Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average current	I_{OHAV}	—	–4	mA	Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

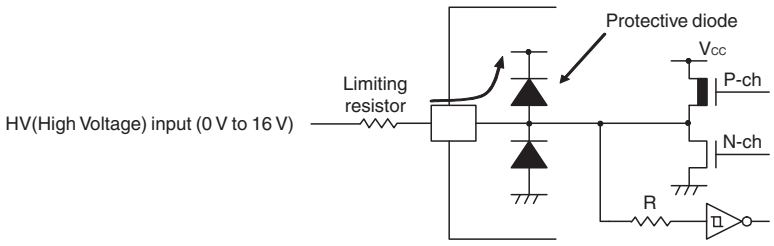
*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Specific pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P94, PA0 to PA7, PB0 to PB4, PC0 to PC7, PE0 to PE7, PF0, PF1, PG1, PG2 (P40 to P43, P50 to P53, P94, PB2 to PB4 and PC4 to PC7 are only available on the MB95710M Series.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.

- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:
  - Input/Output equivalent circuit



WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

22.2 Recommended Operating Conditions

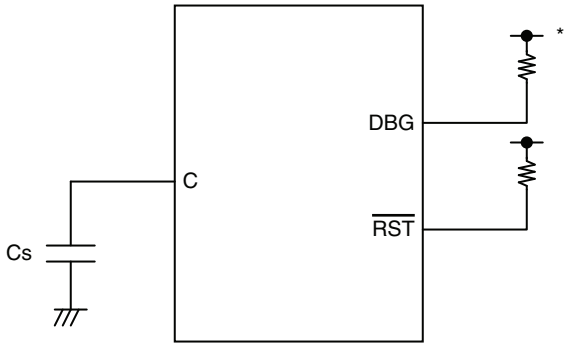
(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	1.8*1	5.5	V	In normal operation
Decoupling capacitor	C_S	0.2	10	µF	A capacitor of about 1.0 µF is recommended. *2
Operating temperature	T_A	–40	+85	°C	Other than on-chip debug mode
		+5	+35		On-chip debug mode

*1: The minimum power supply voltage becomes 2.18 V when a product with the low-voltage detection reset is used or when the on-chip debug mode is used.

*2: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

22.3 DC Characteristics

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P01, P04, P10, P22, P23	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P01, P04, P10, P22, P23	*1	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P22, P23, PF2	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH}	Output pins other than P12, P22, P23, PF2	I_{OH} = –4 mA*3	V_{CC} – 0.5	—	—	V	

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL}	All output pins	I_{OL} = 4 mA*4	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P10, P11, P13, P14, P17, P20, P21, P50 to P53*2, PG1, PG2	V_I = 0 V	75	100	150	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*5		
Power supply current*6	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	4.7	7.3	mA	Except during Flash memory programming and erasing
				—	9.8	15.8	mA	During Flash memory programming and erasing
	I_{CCS}		F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	2.1	3.4	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25 °C	—	35	60	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25 °C	—	2	7	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25 °C	—	1.2	6.2	µA	
	I_{CCMPLL}	V_{CC}	F_{MPLL} = 16 MHz F_{MP} = 16 MHz Main PLL clock mode (multiplied by 4)	—	5.3	8.5	mA	
	$I_{CCMCRPLL}$		F_{MCRPLL} = 16 MHz F_{MP} = 16 MHz Main CR PLL clock mode (multiplied by 4)	—	4.9	8.3	mA	
	I_{CCMCR}		F_{CRH} = 4 MHz F_{MP} = 4 MHz Main CR clock mode	—	1.7	3.4	mA	
	I_{CCSCR}		Sub-CR clock mode T_A = +25 °C	—	54	100	µA	

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*5		
Power supply current*6	I_{CCTS}	V_{CC} (External clock operation)	F_{CH} = 32 MHz Time-base timer mode T_A = +25 °C	—	450	500	µA	
	I_{CCH}		Substop mode T_A = +25 °C	—	0.7	5	µA	
	I_A	AV_{CC}	F_{CH} = 16 MHz Current consumption of the A/D converter	—	1.8	3.2	mA	
	I_{AH}		F_{CH} = 16 MHz Current consumption with the A/D converter halted	—	0.1	1.7	µA	
	I_V		F_{CH} = 16 MHz Current consumption of the comparator	—	160	700	µA	
	I_{PLVD}	V_{CC}	Current consumption of the low-voltage detection reset circuit in operation	—	6	26	µA	
	I_{ILVD}		Current consumption of the low-voltage detection interrupt circuit operating in normal mode	—	6	14	µA	
	I_{ILVDL}		Current consumption of the low-voltage detection interrupt circuit operating in low power consumption mode	—	3	10	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	270	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	5	20	µA	
	I_{SOSC}		Current consumption of the suboscillator	—	0.8	7	µA	

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*5		
LCD internal division resistance	R_{LCD}	—	Between V4 and V_{SS}	—	400	—	kΩ	
				—	40	—	kΩ	
COM0 to COM7 output impedance	R_{VCOM}	COM0 to COM7	V1 to V4 = 4.1 V	—	—	5	kΩ	
SEG00 to SEG39*7 output impedance	R_{VSEG}	SEG00 to SEG39*7		—	—	7	kΩ	
LCD leakage current	I_{LCDL}	V0*8 to V4, COM0 to COM7, SEG00 to SEG39*7	—	–1	—	+1	µA	

*1: V_{CC} = 3.0 V, T_A = +25 °C
*2: P40 to P43, P50 to P53, P94, PB2 to PB4 are only available on the MB95710M Series.
*3: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = –2 mA.
*4: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OL} = 2 mA.
*5: V_{CC} = 3.3 V, T_A = +85 °C (unless otherwise specified)
*6:
- The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit (I_{PLVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection reset circuit (I_{PLVD}), the current consumption of the CR oscillator (I_{CRH} or I_{CRL}) and one of the values from I_{CC} to I_{CCH}. In on-chip debug mode, the main CR oscillator (I_{CRH}) and the low-voltage detection reset circuit are always in operation, and current consumption therefore increases accordingly.
- See “4. AC Characteristics Clock Timing” for F_{CH}, F_{CL}, F_{CRH}, F_{MCRPLL} and F_{MPLL}.
- See “4. AC Characteristics Source Clock/Machine Clock” for F_{MP} and F_{MPL}.
- The power supply current in subclock mode is determined by the external clock. In subclock mode, current consumption in using the crystal oscillator is higher than that in using the external clock. When the crystal oscillator is used, the power supply current is the sum of adding I_{SOSC} (current consumption of the suboscillator) to the power supply current in using the external clock. For details of controlling the subclock, refer to “CHAPTER 3 CLOCK CONTROLLER” and “CHAPTER 30 SYSTEM CONFIGURATION REGISTER” in “New 8FX MB95710M/770M Series Hardware Manual”.

*7: SEG32 to SEG39 are only available on the MB95710M Series.
*8: V0 is only available on the MB95710M Series.

22.4 AC Characteristics

22.4.1 Clock Timing

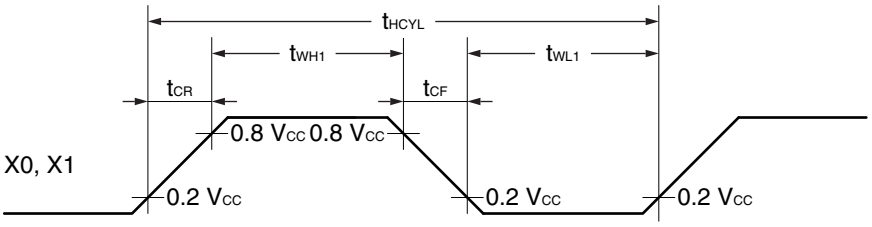
(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency		X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	—	1	—	32.5	MHz	When the main external clock is used
	F_{CH}	X0, X1	—	4	—	8.13	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 2
				4	—	6.5	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 2.5
				4	—	5.41	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 3
				4	—	4.06	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 4
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0 °C ≤ T_A ≤ +70 °C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T_A ≤ +70 °C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0 °C ≤ T_A ≤ +70 °C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T_A ≤ +70 °C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

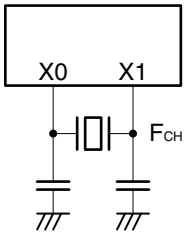
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{MCRPLL}	—	—	15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0 °C ≤ T_A ≤ +70 °C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MPLL}	—	—	8	—	16	MHz	When the main PLL clock is used
	F_{CL}	X0A, X1A	——	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	—	30.8	—	1000	ns	When an external clock is used
		X0, X1	—	—	250	—	ns	When the main PLL clock is used
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1}, t_{WL1}	X0	—	12.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	—	—	125	—	ns	When the main PLL clock is used
	t_{WH2}, t_{WL2}	X0A	—	—	15.2	—	µs	When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock rising time and falling time	t_{CR}, t_{CF}	X0, X0A	—	—	—	5	ns	When an external clock is used
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	µs	When the sub-CR clock is used
PLL oscillation start time	$t_{MCRPLLWK}$	—	—	—	—	100	µs	When the main CR PLL clock is used

- Input waveform generated when an external clock (main clock) is used

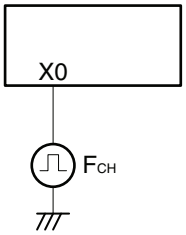


- Figure of main clock input port external connection

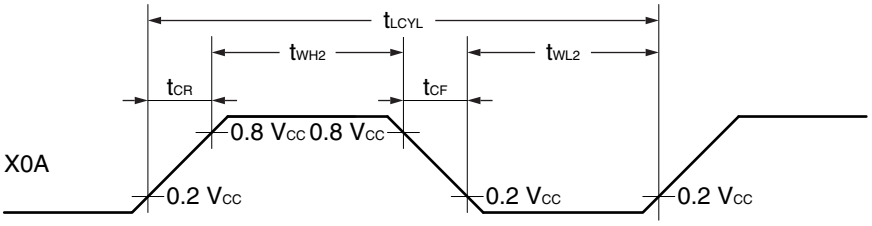
When a crystal oscillator or a ceramic oscillator is used



When an external clock is used

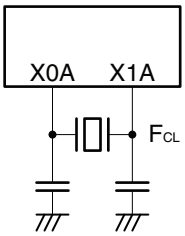


- Input waveform generated when an external clock (subclock) is used

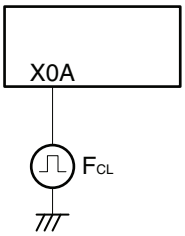


- Figure of subclock input port external connection

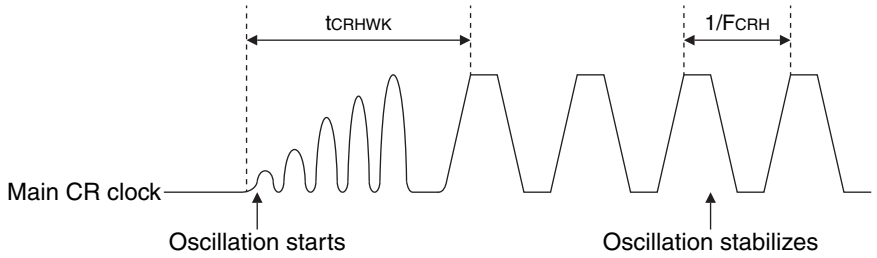
When a crystal oscillator or a ceramic oscillator is used



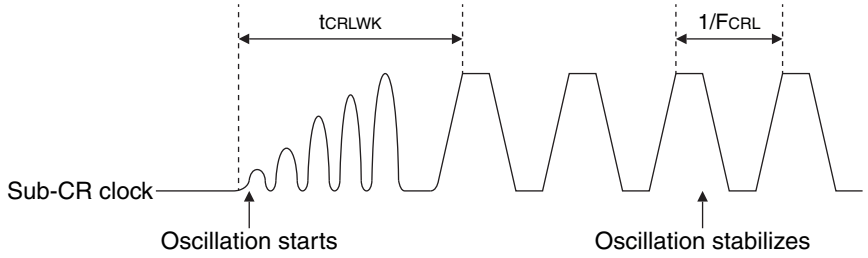
When an external clock is used



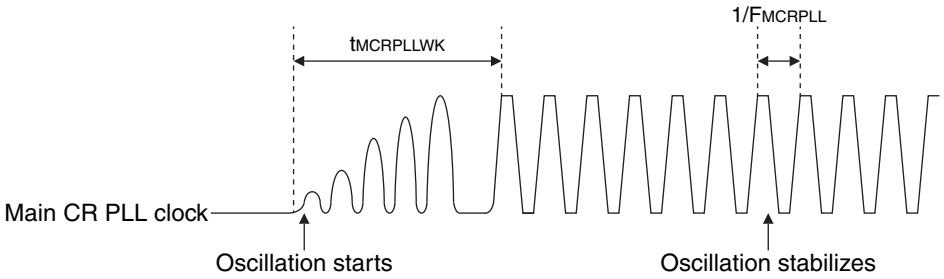
- Input waveform generated when an internal clock (main CR clock) is used



- Input waveform generated when an internal clock (sub-CR clock) is used



- Input waveform generated when an internal clock (main CR PLL clock) is used



22.4.2 Source Clock/Machine Clock

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			—	250	—	ns	When the main CR clock is used
			62.5	—	250	ns	When the main PLL clock is used Min: F_{CH} = 4 MHz, multiplied by 4 Max: F_{CH} = 4 MHz, no division
			62.5	—	250	ns	When the main CR PLL clock is used Min: F_{CRH} = 4 MHz, multiplied by 4 Max: F_{CRH} = 4 MHz, no division
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			—	4	—	MHz	When the main CR clock is used
			8	—	16	MHz	When the main PLL clock is used
			8	—	16	MHz	When the main CR PLL clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			250	—	4000	ns	When the main CR clock is used Min: F_{SP} = 4 MHz, no division Max: F_{SP} = 4 MHz, divided by 16
			62.5	—	2000	ns	When the main PLL clock is used Min: F_{SP} = 4 MHz, multiplied by 4 Max: F_{SP} = 4 MHz, divided by 16
			62.5	—	2000	ns	When the main CR PLL clock is used Min: F_{SP} = 4 MHz, multiplied by 4 Max: F_{SP} = 4 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	4	MHz	When the main CR clock is used
			0.5	—	16	MHz	When the main PLL clock is used
			0.5	—	16	MHz	When the main CR PLL clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

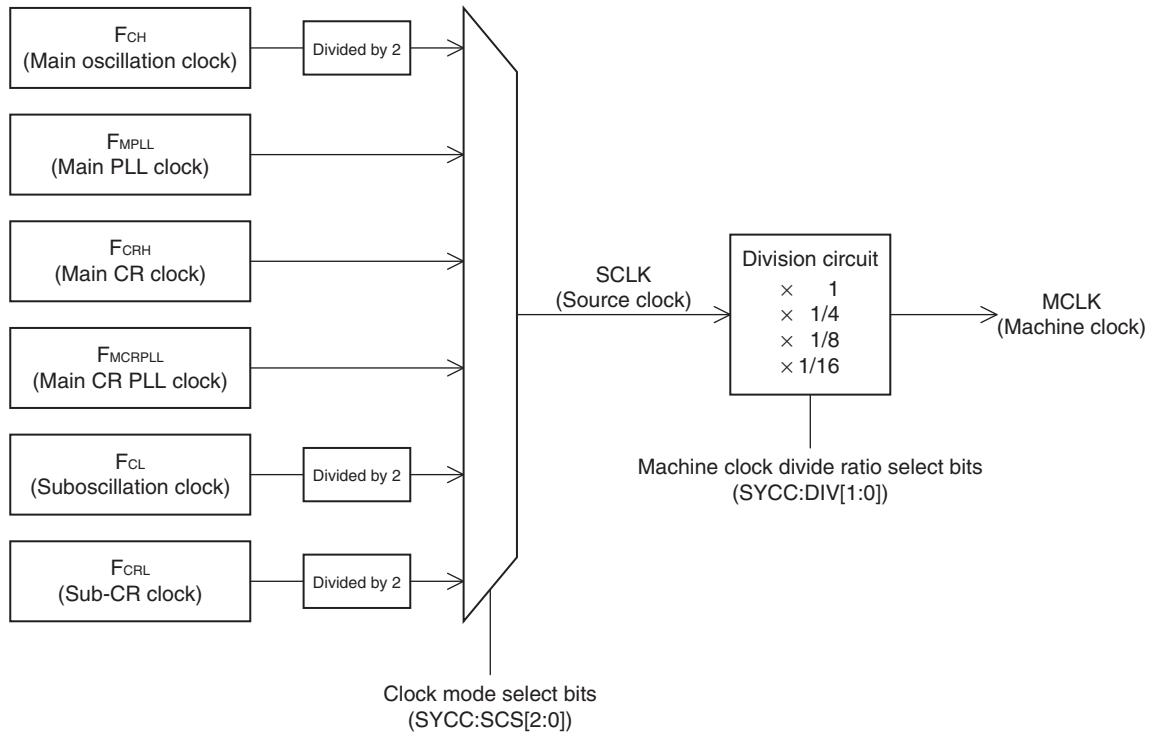
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- PLL multiplication of main clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

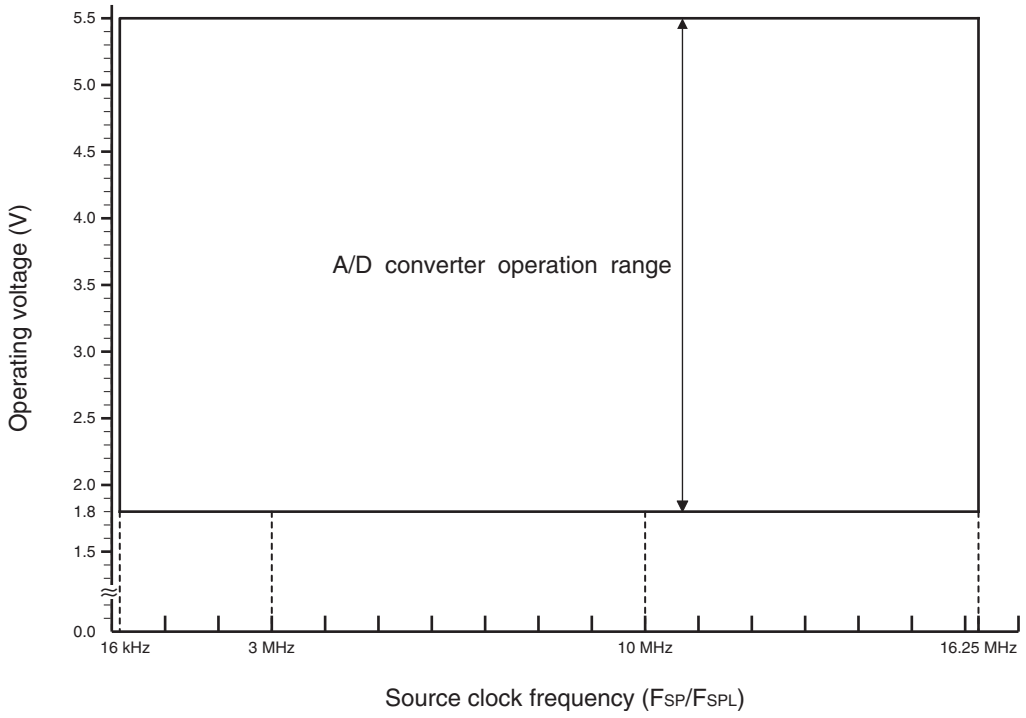
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (T_A = –40 °C to +85 °C)

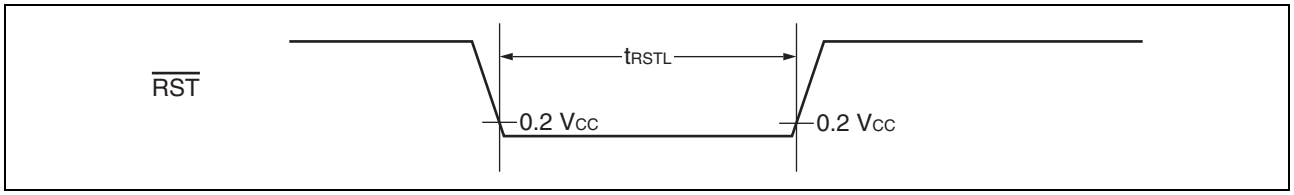


22.4.3 External Reset

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

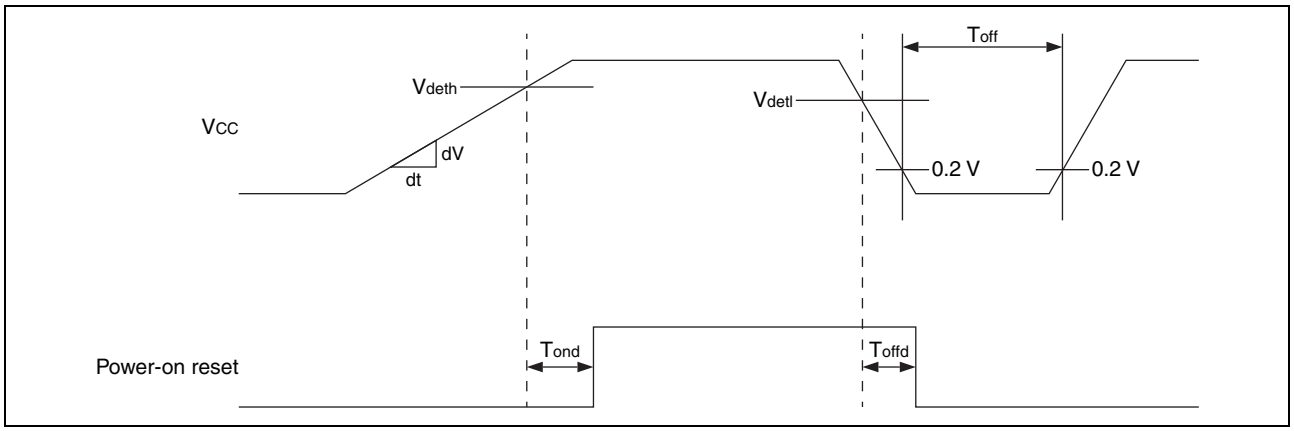
*: See "Source Clock/Machine Clock" for t_{MCLK}.



22.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	V_{CC}	0.1	—	—	V/ms	
Power supply cutoff time	T_{off}		1	—	—	ms	
Reset release voltage	V_{deth}		1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	V_{detl}		1.39	1.55	1.71	V	At voltage fall
Reset release delay time	T_{ond}		—	—	10	ms	dV/dt ≥ 0.1 mV/µs
Reset detection delay time	T_{offd}		—	—	0.4	ms	dV/dt ≥ –0.04 mV/µs

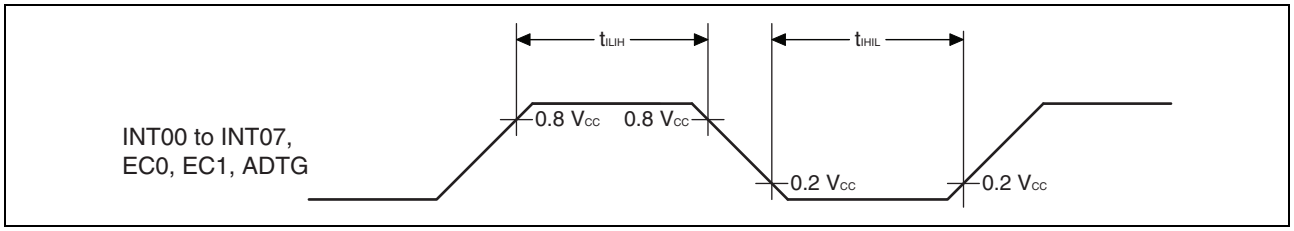


22.4.5 Peripheral Input Timing

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



22.4.6 Low-voltage Detection

• Normal mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

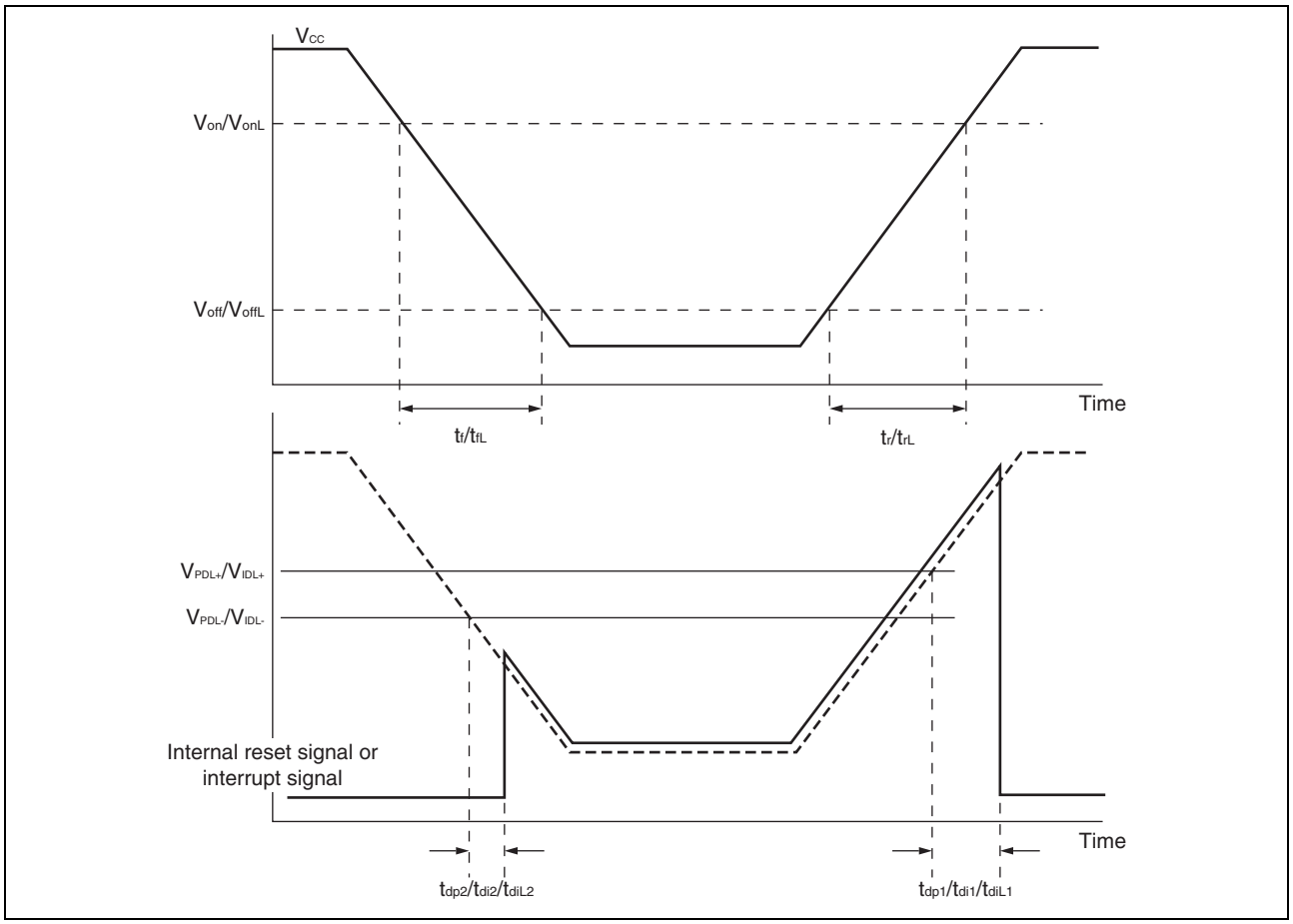
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Reset release voltage	V_{PDL+}	1.88	2.03	2.18	V	At power supply rise
Reset detection voltage	$V_{PDL–}$	1.8	1.93	2.06	V	At power supply fall
Interrupt release voltage 0	V_{IDL0+}	2.13	2.3	2.47	V	At power supply rise
Interrupt detection voltage 0	$V_{IDL0–}$	2.05	2.2	2.35	V	At power supply fall
Interrupt release voltage 1	V_{IDL1+}	2.41	2.6	2.79	V	At power supply rise
Interrupt detection voltage 1	$V_{IDL1–}$	2.33	2.5	2.67	V	At power supply fall
Interrupt release voltage 2	V_{IDL2+}	2.69	2.9	3.11	V	At power supply rise
Interrupt detection voltage 2	$V_{IDL2–}$	2.61	2.8	2.99	V	At power supply fall
Interrupt release voltage 3	V_{IDL3+}	3.06	3.3	3.54	V	At power supply rise
Interrupt detection voltage 3	$V_{IDL3–}$	2.98	3.2	3.42	V	At power supply fall
Interrupt release voltage 4	V_{IDL4+}	3.43	3.7	3.97	V	At power supply rise
Interrupt detection voltage 4	$V_{IDL4–}$	3.35	3.6	3.85	V	At power supply fall
Interrupt release voltage 5	V_{IDL5+}	3.81	4.1	4.39	V	At power supply rise
Interrupt detection voltage 5	$V_{IDL5–}$	3.73	4	4.27	V	At power supply fall
Power supply start voltage	V_{off}	—	—	1.6	V	
Power supply end voltage	V_{on}	4.39	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+})
Power supply voltage change time (at power supply fall)	t_f	697.5	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{PDL-}/V_{IDL-})
Reset release delay time	t_{dp1}	—	—	30	µs	
Reset detection delay time	t_{dp2}	—	—	30	µs	
Interrupt release delay time	t_{di1}	—	—	30	µs	
Interrupt detection delay time	t_{di2}	—	—	30	µs	
Interrupt threshold voltage transition stabilization time	t_{stb}	—	—	30	µs	

- Low power consumption mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Interrupt release voltage 0	V_{IDLL0+}	2.06	2.3	2.54	V	At power supply rise
Interrupt detection voltage 0	V_{IDLL0-}	1.98	2.2	2.42	V	At power supply fall
Interrupt release voltage 1	V_{IDLL1+}	2.33	2.6	2.87	V	At power supply rise
Interrupt detection voltage 1	V_{IDLL1-}	2.25	2.5	2.75	V	At power supply fall
Interrupt release voltage 2	V_{IDLL2+}	2.6	2.9	3.2	V	At power supply rise
Interrupt detection voltage 2	V_{IDLL2-}	2.52	2.8	3.08	V	At power supply fall
Interrupt release voltage 3	V_{IDLL3+}	2.96	3.3	3.64	V	At power supply rise
Interrupt detection voltage 3	V_{IDLL3-}	2.88	3.2	3.52	V	At power supply fall
Interrupt release voltage 4	V_{IDLL4+}	3.32	3.7	4.08	V	At power supply rise
Interrupt detection voltage 4	V_{IDLL4-}	3.24	3.6	3.96	V	At power supply fall
Interrupt release voltage 5	V_{IDLL5+}	3.68	4.1	4.52	V	At power supply rise
Interrupt detection voltage 5	V_{IDLL5-}	3.6	4	4.4	V	At power supply fall
Power supply start voltage	V_{offL}	—	—	1.6	V	
Power supply end voltage	V_{onL}	4.52	—	—	V	
Power supply voltage change time (at power supply rise)	t_{rL}	7300	—	—	µs	Slope of power supply that the interrupt release signal generates within the rating (V_{IDLL+})
Power supply voltage change time (at power supply fall)	t_{fL}	7300	—	—	µs	Slope of power supply that the interrupt detection signal generates within the rating (V_{IDLL-})
Interrupt release delay time	t_{diL1}	—	—	400	µs	
Interrupt detection delay time	t_{diL2}	—	—	400	µs	
Interrupt threshold voltage transition stabilization time	t_{stbL}	—	—	400	µs	
Interrupt low-voltage detection mode switch time	t_{mdsw}	—	—	400	µs	Normal mode ⇔ Low power consumption mode

Note: When being used for interrupt, the low-voltage detection circuit can be switched between normal mode and low power consumption mode. Compared with normal mode, in low power consumption mode, while the detection voltage and release voltage are less accurate, and the detection delay time and the release delay time become longer, there is less power consumption. For the difference in power consumption between normal mode and low power consumption mode, see “22.3 DC Characteristics”. For the method of switching between normal mode and low power consumption mode, refer to “CHAPTER 16 LOW-VOLTAGE DETECTION CIRCUIT” in “New 8FX MB95710M/770M Series Hardware Manual”.

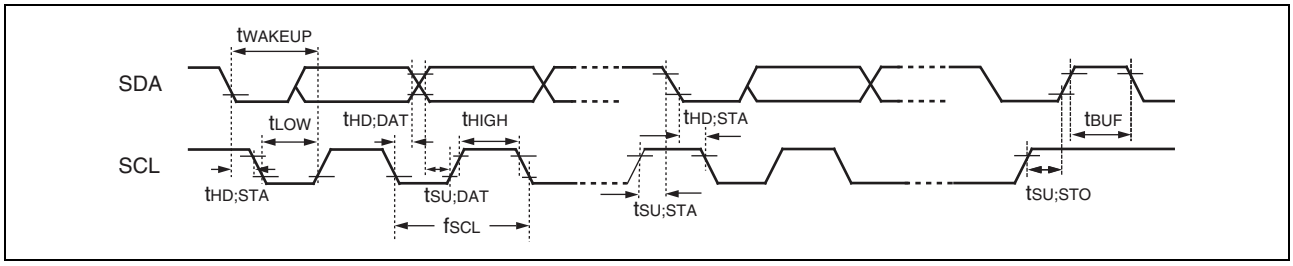

Vcc
Von/VonL
Voff/VoffL
Time
tf/tfL
tr/trL
VPDL+/VIDL+
VPDL-/VIDL-
Internal reset signal or
interrupt signal
Time
tdp2/tdi2/tdiL2
tdp1/tdi1/tdiL1

22.4.7 I²C Bus Interface Timing

(V_{CC} = 3.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.
*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.
*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT}$ ≥ 250 ns is fulfilled.



(V_{CC} = 3.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} – 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm/2)t_{MCLK} – 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm/2)t_{MCLK} – 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} – 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} – 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		$(2 nm + 4)t_{MCLK} – 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3 t_{MCLK} – 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm/2)t_{MCLK} – 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode It is assumed that “L” of SCL is not extended. The minimum value is applied to the first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)t_{MCLK} – 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	The minimum value is applied to the interrupt at the ninth SCL↓. The maximum value is applied to the interrupt at the eighth SCL↓.
SCL clock “L” width	t_{LOW}	SCL		$4 t_{MCLK} – 20$	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		$4 t_{MCLK} – 20$	—	ns	At reception

(V_{CC} = 3.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
START condition detection	$t_{HD;STA}$	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} – 20	—	ns	No START condition is detected when 1 t_{MCLK} is used at reception.
STOP condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	No STOP condition is detected when 1 t_{MCLK} is used at reception.
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	No RESTART condition is detected when 1 t_{MCLK} is used at reception.
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} – 20	—	ns	At reception
SDA↓ → SCL↑ (with wakeup function in use)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t_{MCLK} – 20	—	ns	

*1: R represents the pull-up resistance of the SCL and SDA lines, and C the load capacitance of the SCL and SDA lines.

*2: • See “Source Clock/Machine Clock” for t_{MCLK}.

- m represents the CS[4:3] bits in the I²C clock control register ch.0 (ICCR0).
- n represents the CS[2:0] bits in the I²C clock control register ch.0 (ICCR0).
- The actual timing of the I²C bus interface is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS[4:0] bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

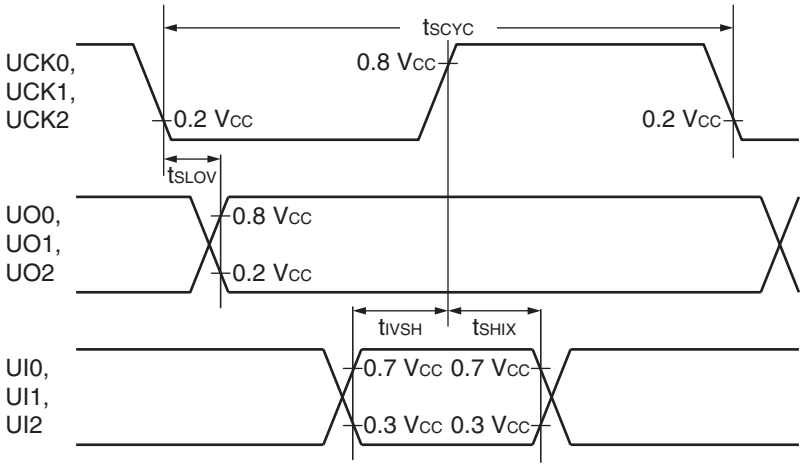
22.4.8 UART/SIO, Serial I/O Timing

(V_{CC} = 3.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

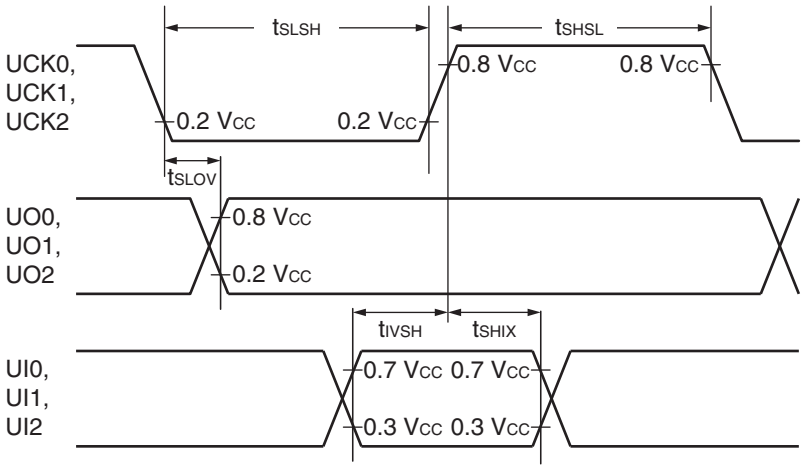
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0, UCK1, UCK2	Internal clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UCK1, UCK2, UO0, UO1, UO2		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0, UCK1, UCK2	External clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0, UCK1, UCK2		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UCK1, UCK2, UO0, UO1, UO2		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



22.4.9 Comparator Timing

(AV_{CC} = 1.8 V to 5.5 V, AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Voltage range	CMP0_P, CMP0_N	0	—	AV_{CC}	V	
Offset voltage	CMP0_P, CMP0_N	–20	—	+20	mV	
Delay time	CMP0_O	—	600	1200	ns	Overdrive 5 mV
		—	120	420	ns	Overdrive 50 mV
Power down delay	CMP0_O	—	—	1200	ns	Power down recovery PD: 1 → 0
		0	—	150	ns	Power down PD: 0 → 1
Power up stabilization time	CMP0_O	—	—	1200	ns	Output stabilization time at power up
Bandgap reference voltage	—	1.15	1.21	1.27	V	

22.5 A/D Converter

22.5.1 A/D Converter Electrical Characteristics

(AV_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	12	bit	
Total error		–6	—	+6	LSB	$V_{CC} \geq 2.7$ V
		–10	—	+10	LSB	$V_{CC} < 2.7$ V
Linearity error		–3	—	+3	LSB	$V_{CC} \geq 2.7$ V
		–5	—	+5	LSB	$V_{CC} < 2.7$ V
Differential linearity error		–1.9	—	+1.9	LSB	$V_{CC} \geq 2.7$ V
		–2.9	—	+2.9	LSB	$V_{CC} < 2.7$ V
Zero transition voltage	V_{0T}	V_{SS} – 6 LSB	—	V_{SS} + 8.2 LSB	V	
Full-scale transition voltage	V_{FST}	AV_{CC} – 6.2 LSB	—	AV_{CC} + 9.2 LSB	V	
Sampling time	T_S	*	—	10	µs	
Compare time	T_{cck}	0.861	—	14	µs	$V_{CC} \geq 2.7$ V
		2.8	—	14	µs	$V_{CC} < 2.7$ V
Time for transiting to operation enabled state	T_{stt}	1	—	—	µs	
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	AV_{CC}	V	

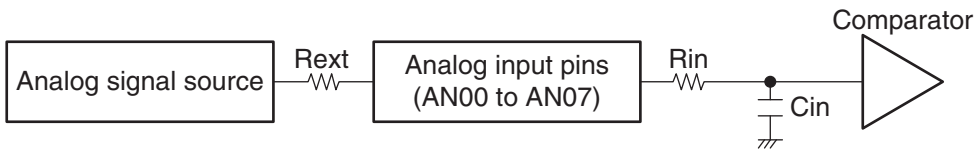
*: See “Notes on Using A/D Converter” for details of the minimum sampling time.

22.5.2 Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter of the MB95710M/770M Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit



V_{CC}	Rin	Cin
4.5 V ≤ V_{CC} ≤ 5.5 V	0.9 kΩ (max)	13 pF (max)
2.7 V ≤ V_{CC} < 4.5 V	1.6 kΩ (max)	13 pF (max)
1.8 V ≤ V_{CC} < 2.7 V	4.0 kΩ (max)	13 pF (max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

  The necessary sampling time varies according to external impedance. Ensure that the following conditions are fulfilled when setting the sampling time.

$$Ts \geq (Rin + Rext) \times Cin \times 9$$

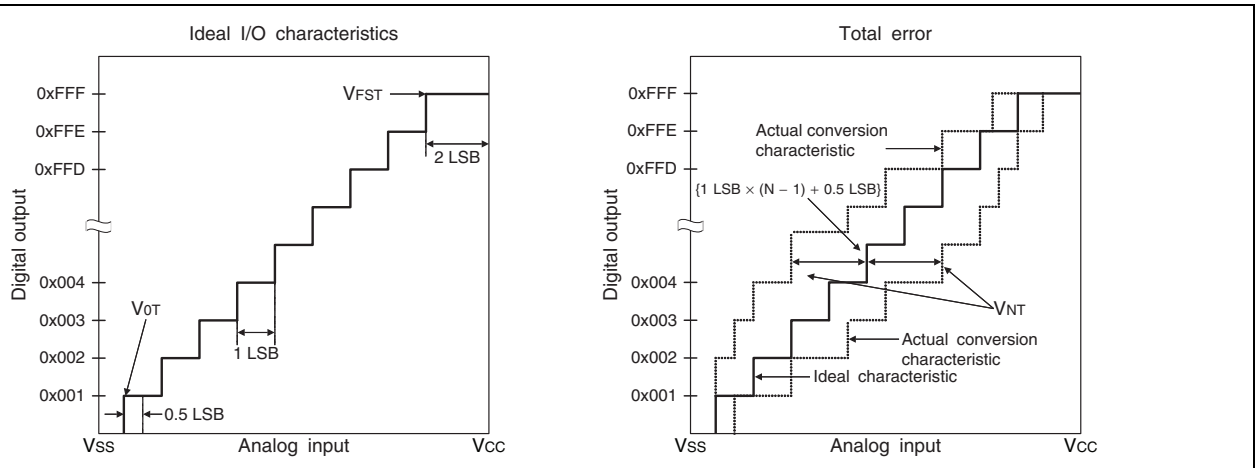
  T_s : Sampling time
  Rin : Input resistance of A/D converter
  Cin : Input capacitance of A/D converter
  Rext : Output impedance of external circuit

- A/D conversion error

  As $|V_{CC} - V_{SS}|$ decreases, the A/D conversion error increases proportionately.

22.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 12, analog voltage can be divided into 2^{12} = 4096.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“000000000000” ← → “000000000001”) of a device to the full-scale transition point (“111111111111” ← → “111111111110”) of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



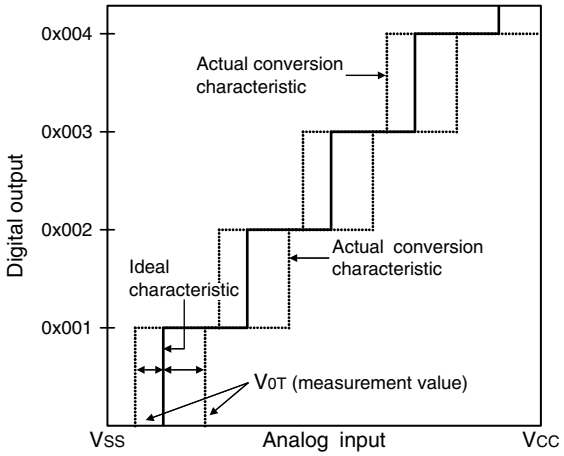
$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{4096}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

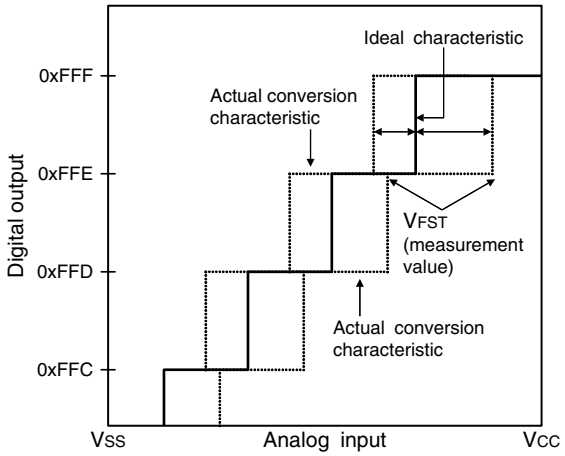
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

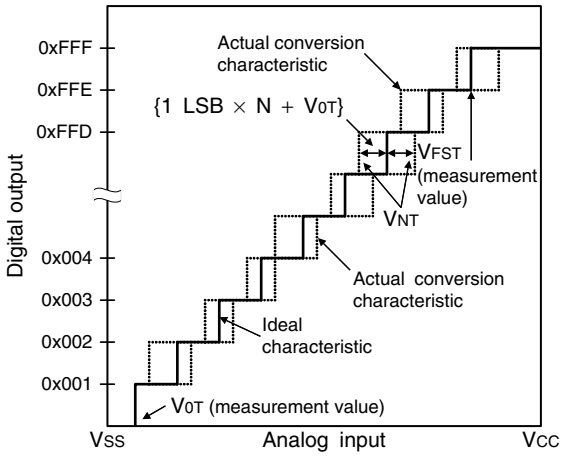
Zero transition error



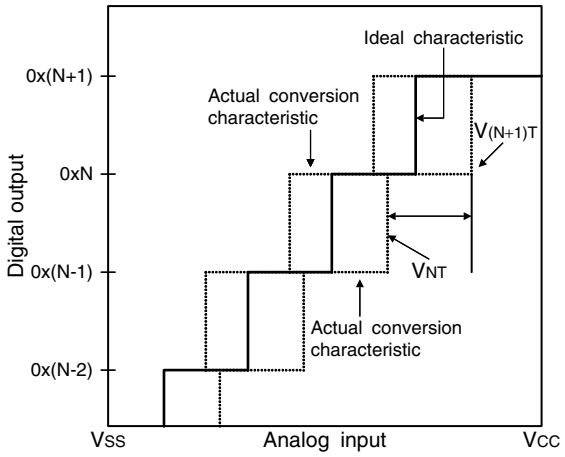
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} – 2 LSB [V]

22.6 Flash Memory Program/Erase Characteristics

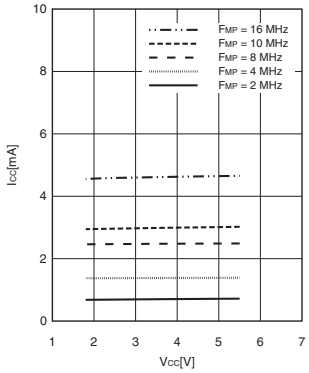
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (24 Kbyte sector and 32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	1.8	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 10001 or above

*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle
*2: V_{CC} = 1.8 V, T_A = +85 °C, 100000 cycles
*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

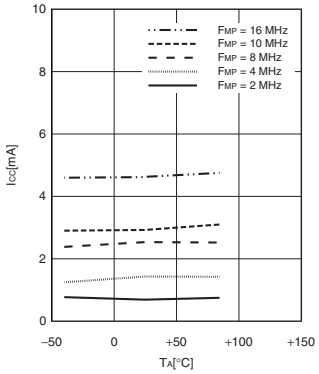
23. Sample Characteristics

- Power supply current temperature characteristics

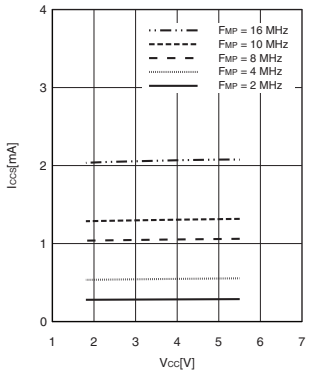
I_{CC} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



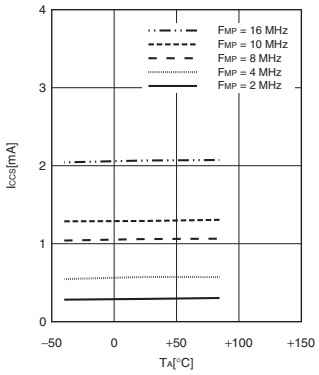
I_{CC} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



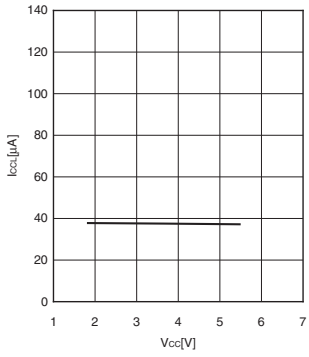
I_{CCS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



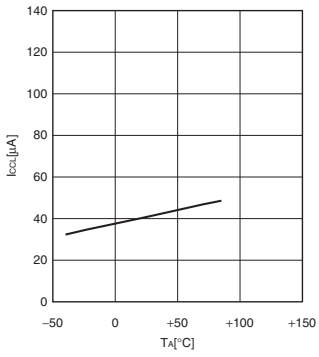
I_{CCS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



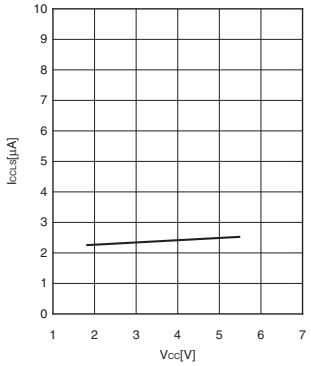
I_{CCL} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



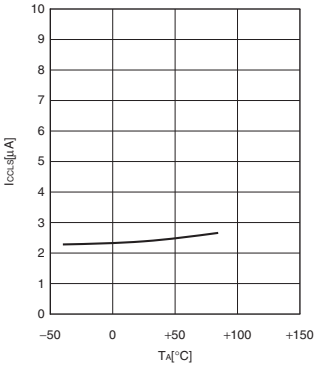
I_{CCL} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



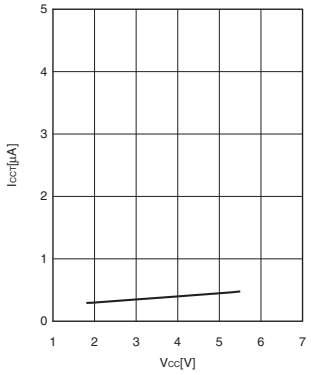
I_{CCLS} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



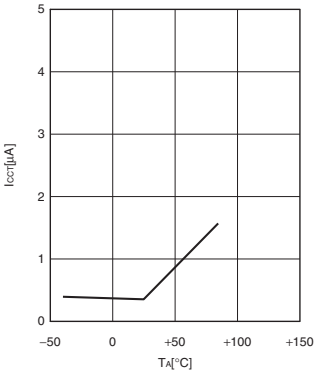
I_{CCLS} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



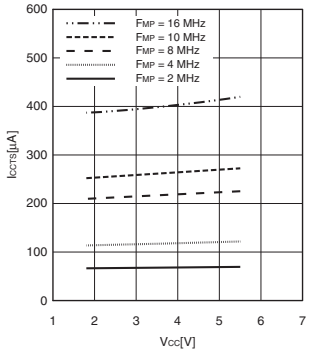
I_{CCT} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



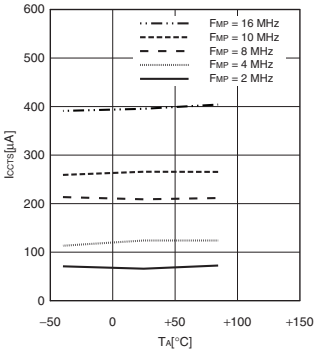
I_{CCT} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



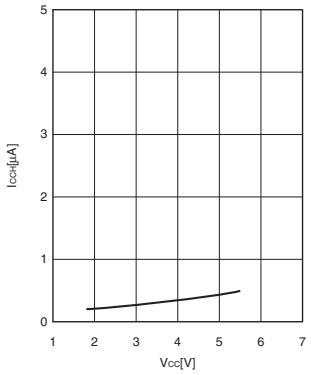
I_{CCTS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



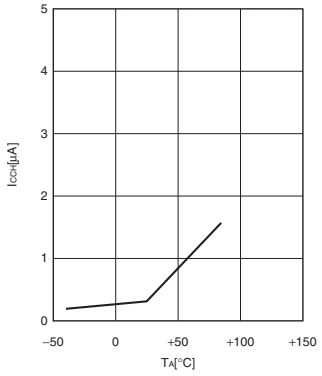
I_{CCTS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



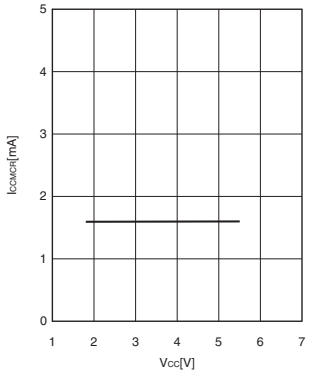
I_{CCH} – V_{CC}
T_A = +25 °C, F_{MPL} = (stop)
Substop mode with the external clock stopping



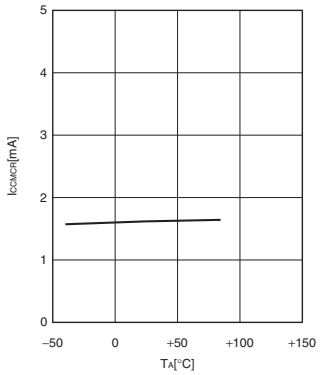
I_{CCH} – T_A
V_{CC} = 3.3 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



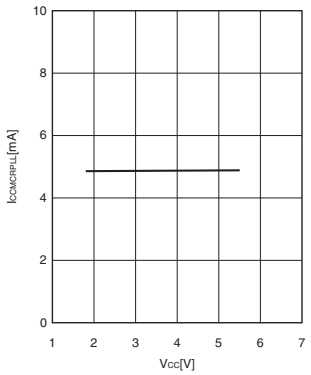
I_{CCMCR} – V_{CC}
T_A = +25 °C, F_{MP} = 4 MHz (no division)
Main CR clock mode



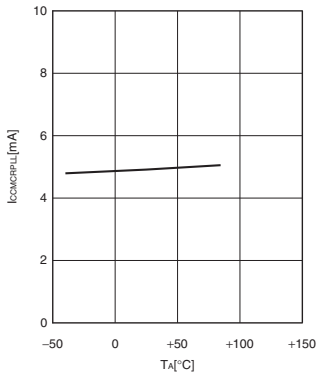
I_{CCMCR} – T_A
V_{CC} = 3.3 V, F_{MP} = 4 MHz (no division)
Main CR clock mode



$I_{CCMCRPLL}$ – V_{CC}
T_A = +25 °C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode

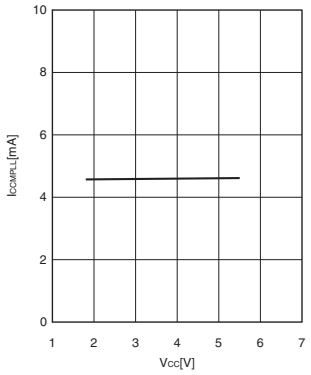


$I_{CCMCRPLL}$ – T_A
V_{CC} = 3.3 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode

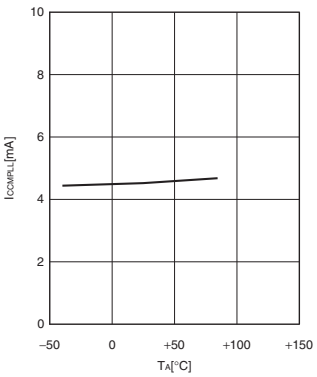


(Continued)

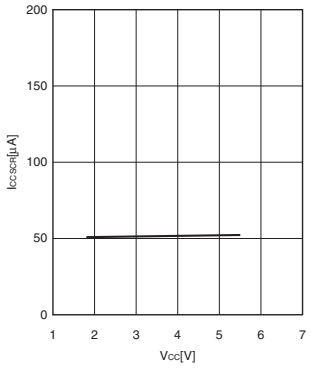
I_{CCMPLL} – V_{CC}
T_A = +25 °C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main PLL clock mode



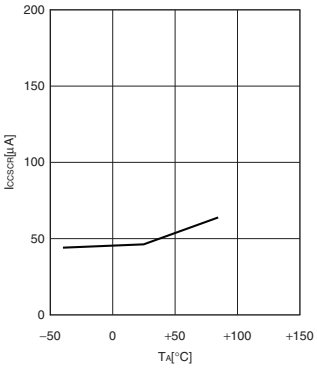
I_{CCMPLL} – T_A
V_{CC} = 3.3 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main PLL clock mode



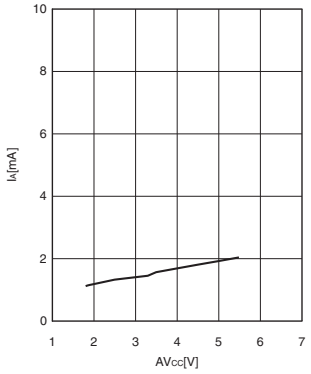
I_{CCSCR} – V_{CC}
T_A = +25 °C, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode



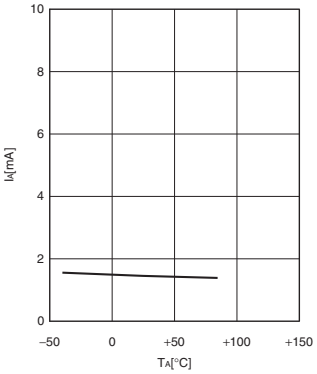
I_{CCSCR} – T_A
V_{CC} = 3.3 V, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode



I_A – AV_{CC}
T_A = +25 °C, F_{MP} = 16 MHz (divided by 2)
Main clock mode with the external clock operating

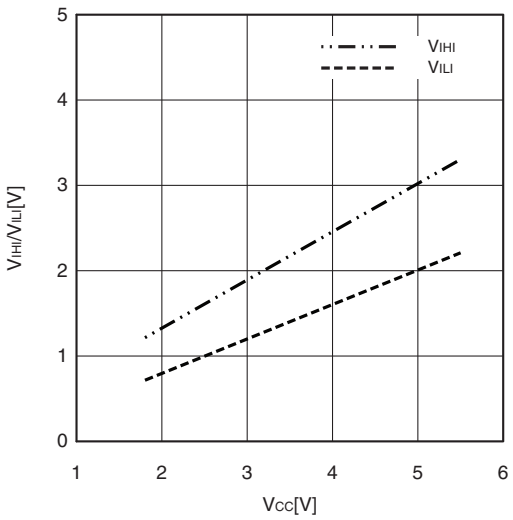


I_A – T_A
V_{CC} = 3.3 V, F_{MP} = 16 MHz (divided by 2)
Main clock mode with the external clock operating

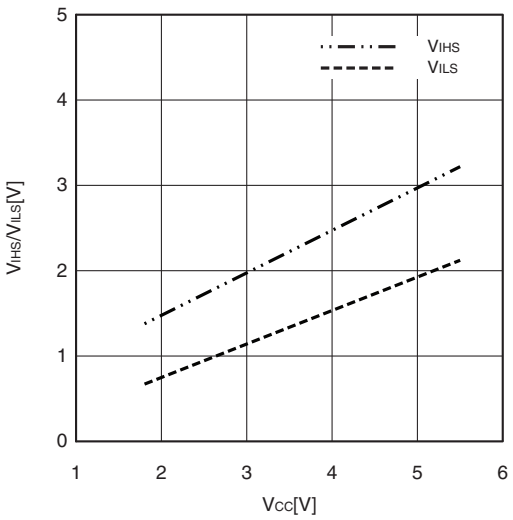


- Input voltage characteristics

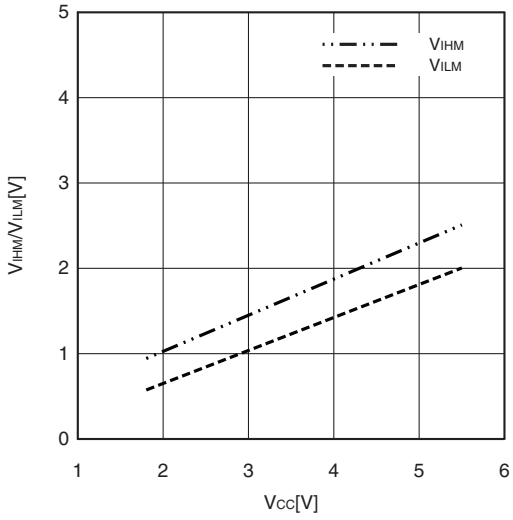
V_{IHI} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25 °C



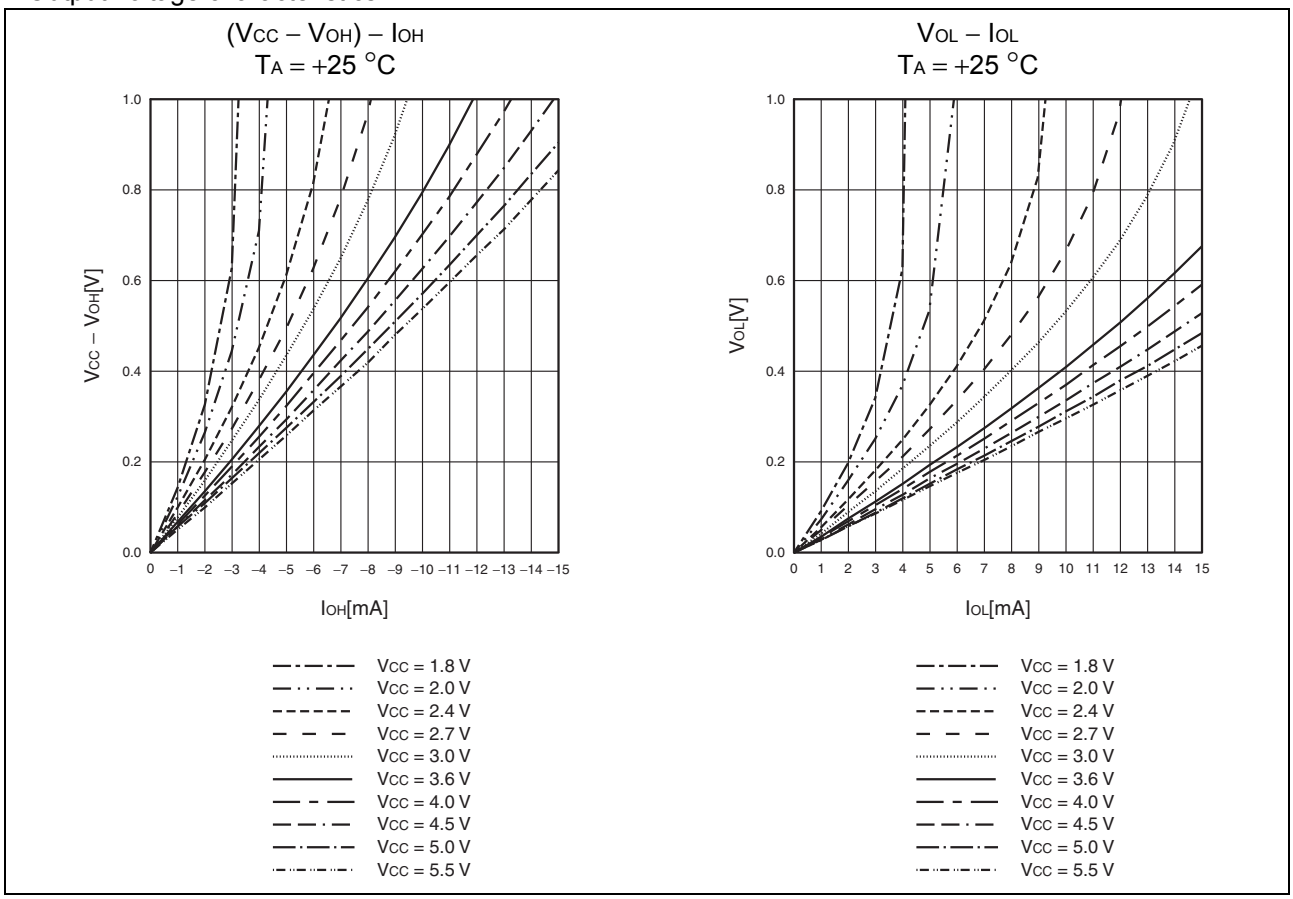
V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25 °C



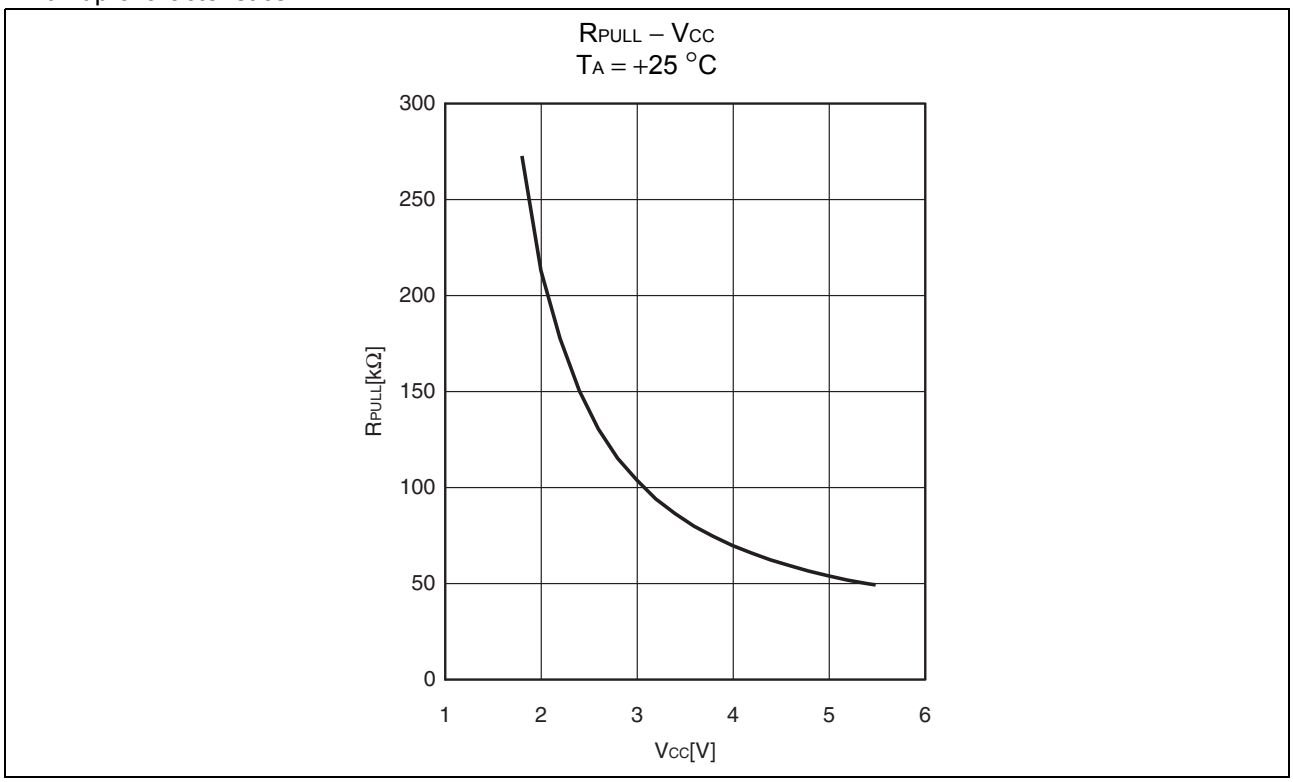
V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25 °C



- Output voltage characteristics



• Pull-up characteristics



24. Mask Options

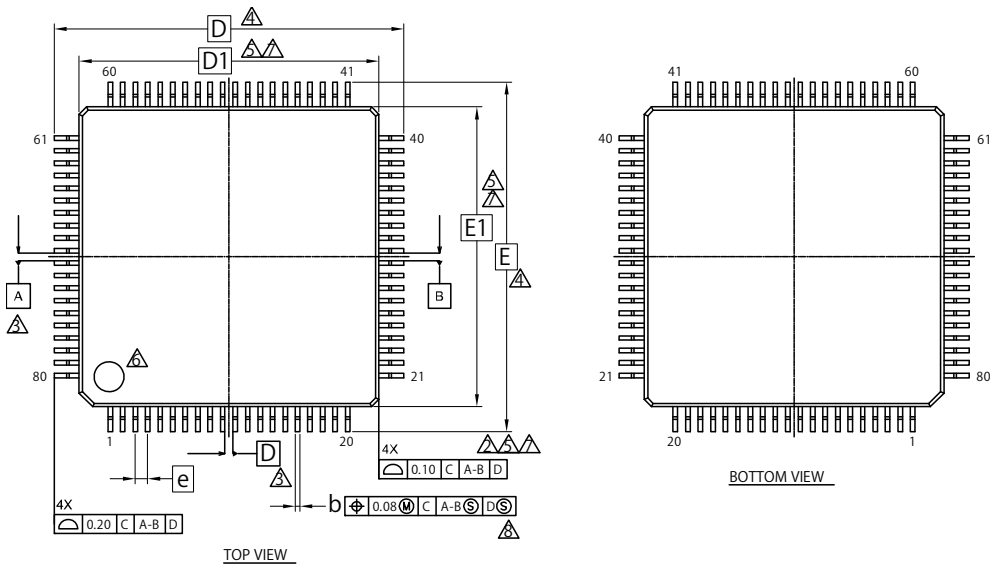
No.	Part number	MB95F714J MB95F716J MB95F718J MB95F774J MB95F776J MB95F778J	MB95F714M MB95F716M MB95F718M MB95F774M MB95F776M MB95F778M
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	With low-voltage detection reset	Without low-voltage detection reset
2	Reset	Without dedicated reset input	With dedicated reset input

25. Ordering Information

Part number	Package
MB95F714JPMC-G-SNE2 MB95F714MPMC-G-SNE2 MB95F716JPMC-G-SNE2 MB95F716MPMC-G-SNE2 MB95F718JPMC-G-UNE2 MB95F718MPMC-G-SNE2	80-pin plastic LQFP (LQH080)
MB95F774JPMC1-G-SNE2 MB95F774MPMC1-G-SNE2 MB95F776JPMC1-G-SNE2 MB95F776MPMC1-G-SNE2 MB95F778JPMC1-G-SNE2 MB95F778MPMC1-G-SNE2	64-pin plastic LQFP (LQD064)
MB95F774JPMC2-G-SNE2 MB95F774MPMC2-G-SNE2 MB95F776JPMC2-G-SNE2 MB95F776MPMC2-G-SNE2 MB95F778JPMC2-G-UNE2 MB95F778MPMC2-G-SNE2	64-pin plastic LQFP (LQG064)

26. Package Dimension

Package Type	Package Code
LQFP 80	LQH 080



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

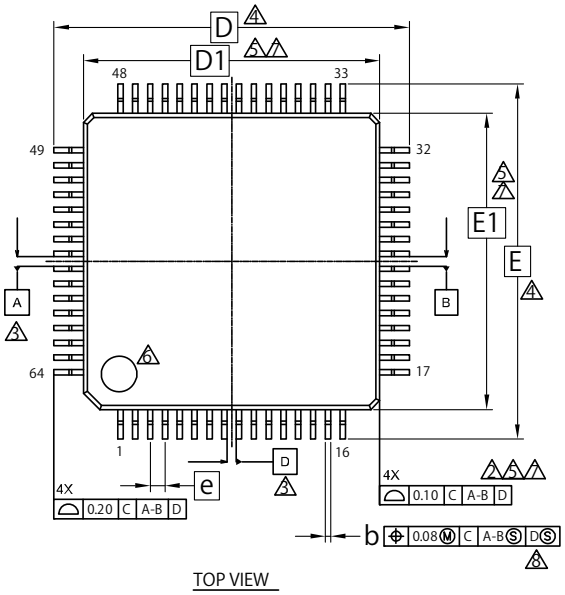
NOTES

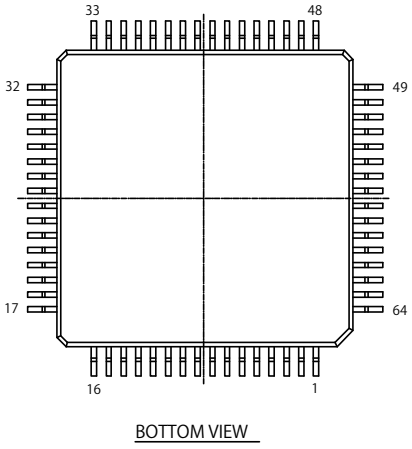
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

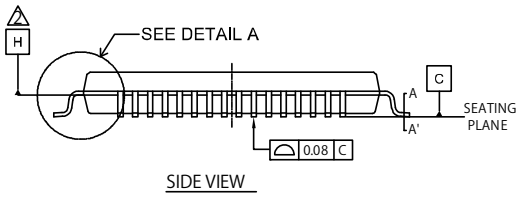
002-11501 **

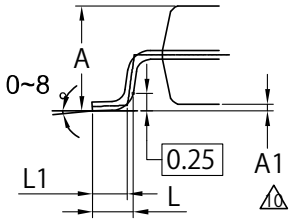
PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **

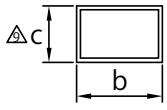
Package Type	Package Code
LQFP 64	LQD 064











SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

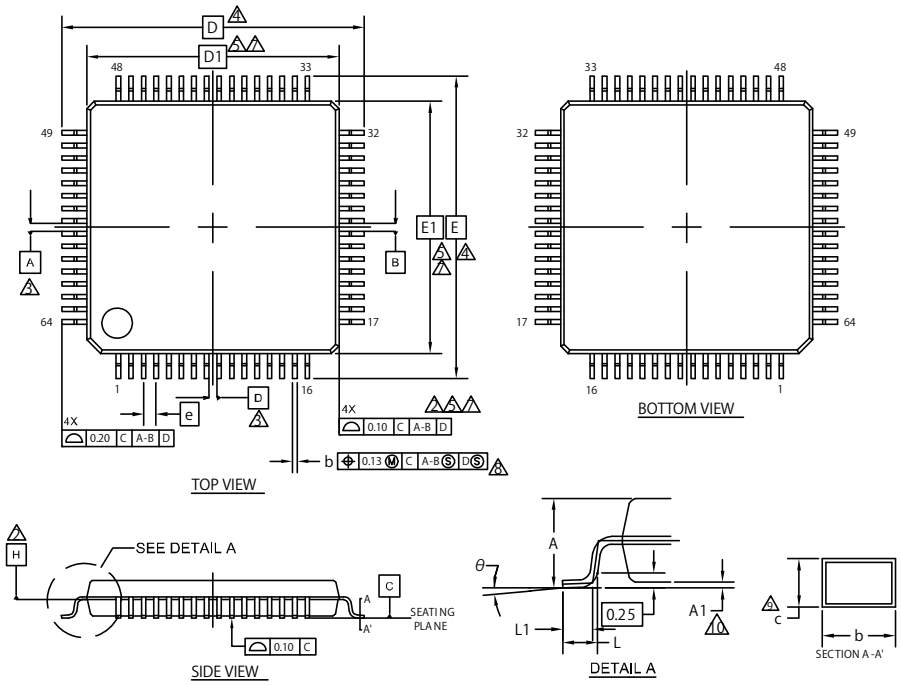
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

Package Type	Package Code
LQFP 64	LQG 064



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.27	0.32	0.37
c	0.09	——	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	——	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

Document History Page

Document Title: MB95710M Series, MB95770M Series, New 8FX 8-bit Microcontrollers Document Number: 002-09307				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	YSKA	07/31/2013	Migrated Spansion DS702-00019-1v0-E to Cypress and assigned document number 002-09307. No change to document contents or format.
*A	5511943	YSKA	11/08/2016	Updated to Cypress template
*B	5633448	HTER	03/07/2017	Changed the package codes as the following from “FPT-80P-M37” to “LQH080” from “FPT-64P-M38” to “LQD064” from “FPT-64P-M39” to “LQG064” in chapter: 1.Product Line-up (Page 6, 9) 2.Packages And Corresponding Products (Page 9) 4.Pin Assignment (Page 11 to 12) 25.Ordering Information (Page 167) 26.Package Dimensions (Page 168 to 170). Changed the Part numbers from “MB95F778JPMC2-G-SNE2” to “MB95F778JPMC2-G-UNE2” in chapter 25.Ordering Information (Page 167).
*C	5772061	YSAT	06/15/2017	Adapted new Cypress logo
*D	5900838	HUAL	09/29/2017	Modified from “MB95F718JPMC-G-SNE2” to “MB95F718JPMC-G-UNE2” in 25.Ordering Information (Page 167).

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