

## DATASHEET

# UF3C120040K4S



## 1200V-35mΩ SiC Cascode

Rev. A, January 2019

### Description

United Silicon Carbide's cascode products co-package its high-performance F3 SiC fast JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits very fast switching using a 4-terminal TO-247-package and the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.

### Features

- ◆ Typical on-resistance  $R_{DS(on),typ}$  of 35mΩ
- ◆ Maximum operating temperature of 175°C
- ◆ Excellent reverse recovery
- ◆ Low gate charge
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2
- ◆ TO-247-4L package for faster switching, clean gate waveforms

### Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating

Part Number	Package	Marking
UF3C120040K4S	TO-247-4L	UF3C120040K4S



## Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		1200	V
Gate-source voltage	$V_{GS}$	DC	-25 to +25	V
Continuous drain current <sup>1</sup>	$I_D$	$T_C = 25^\circ\text{C}$	65	A
		$T_C = 100^\circ\text{C}$	47	A
Pulsed drain current <sup>2</sup>	$I_{DM}$	$T_C = 25^\circ\text{C}$	175	A
Single pulsed avalanche energy <sup>3</sup>	$E_{AS}$	$L=15\text{mH}, I_{AS}=4.2\text{A}$	132.3	mJ
Power dissipation	$P_{tot}$	$T_C = 25^\circ\text{C}$	429	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	$T_J, T_{STG}$		-55 to 175	$^\circ\text{C}$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	$T_L$		250	$^\circ\text{C}$

1. Limited by  $T_{J,max}$

2. Pulse width  $t_p$  limited by  $T_{J,max}$

3. Starting  $T_J = 25^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.27	0.35	$^\circ\text{C}/\text{W}$

## Electrical Characteristics ( $T_J = +25^\circ\text{C}$ unless otherwise specified)

### Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	$BV_{DS}$	$V_{GS}=0V, I_D=1mA$	1200			V
Total drain leakage current	$I_{DSS}$	$V_{DS}=1200V,$ $V_{GS}=0V, T_J=25^\circ\text{C}$		8	150	$\mu\text{A}$
		$V_{DS}=1200V,$ $V_{GS}=0V, T_J=175^\circ\text{C}$		35		
Total gate leakage current	$I_{GSS}$	$V_{DS}=0V, T_J=25^\circ\text{C},$ $V_{GS}=-20V / +20V$		6	$\pm 20$	$\mu\text{A}$
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=40A,$ $T_J=25^\circ\text{C}$		35	45	$\text{m}\Omega$
		$V_{GS}=12V, I_D=40A,$ $T_J=175^\circ\text{C}$		73		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	5	6	V
Gate resistance	$R_G$	$f=1\text{MHz}, \text{open drain}$		4.5		$\Omega$

### Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current <sup>1</sup>	$I_S$	$T_C=25^\circ\text{C}$			65	A
Diode pulse current <sup>2</sup>	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			175	A
Forward voltage	$V_{FSD}$	$V_{GS}=0V, I_F=20A,$ $T_J=25^\circ\text{C}$		1.5	2	V
		$V_{GS}=0V, I_F=20A,$ $T_J=175^\circ\text{C}$		1.95		
Reverse recovery charge	$Q_{rr}$	$V_R=800V, I_F=40A,$ $V_{GS}=-5V, R_{G,EXT}=10\Omega$ $di/dt=2400A/\mu\text{s},$ $T_J=25^\circ\text{C}$		358		nC
Reverse recovery time	$t_{rr}$	$T_J=25^\circ\text{C}$		25		ns
Reverse recovery charge	$Q_{rr}$	$V_R=800V, I_F=40A,$ $V_{GS}=-5V, R_{G,EXT}=10\Omega$ $di/dt=2400A/\mu\text{s},$ $T_J=150^\circ\text{C}$		259		nC
Reverse recovery time	$t_{rr}$	$T_J=150^\circ\text{C}$		22		ns

## Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	$C_{iss}$	$V_{DS}=100V, V_{GS}=0V$ $f=100kHz$		1500		pF
Output capacitance	$C_{oss}$			210		
Reverse transfer capacitance	$C_{rss}$			1.7		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		112		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		280		pF
$C_{oss}$ stored energy	$E_{oss}$	$V_{DS}=800V, V_{GS}=0V$		35.6		$\mu J$
Total gate charge	$Q_G$	$V_{DS}=800V, I_D=40A,$ $V_{GS} = -5V$ to 12V		43		nC
Gate-drain charge	$Q_{GD}$			11		
Gate-source charge	$Q_{GS}$			19		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=800V, I_D=40A,$ Gate Driver = -5V to +12V, Turn-on $R_{G,EXT}=8.5\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load,		24		ns
Rise time	$t_r$			27		
Turn-off delay time	$t_{d(off)}$			50		
Fall time	$t_f$			10		
Turn-on energy	$E_{ON}$	FWD: same device with $V_{GS} = -5V, R_G = 10\Omega,$ $T_J=25^\circ C$		780		$\mu J$
Turn-off energy	$E_{OFF}$			195		
Total switching energy	$E_{TOTAL}$			975		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=800V, I_D=40A,$ Gate Driver = -5V to +12V, Turn-on $R_{G,EXT}=8.5\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load,		23		ns
Rise time	$t_r$			24		
Turn-off delay time	$t_{d(off)}$			50		
Fall time	$t_f$			9		
Turn-on energy	$E_{ON}$	FWD: same device with $V_{GS} = -5V, R_G = 10\Omega,$ $T_J=150^\circ C$		668		$\mu J$
Turn-off energy	$E_{OFF}$			134		
Total switching energy	$E_{TOTAL}$			802		

## Typical Performance Diagrams

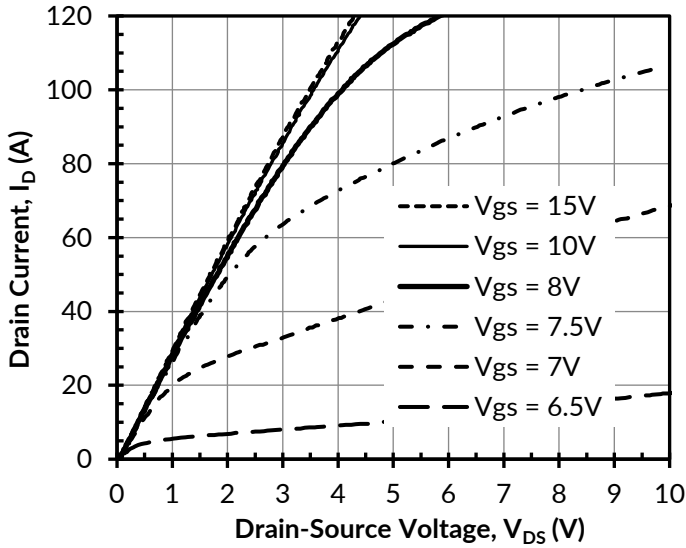


Figure 1. Typical output characteristics at  $T_J = -55^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

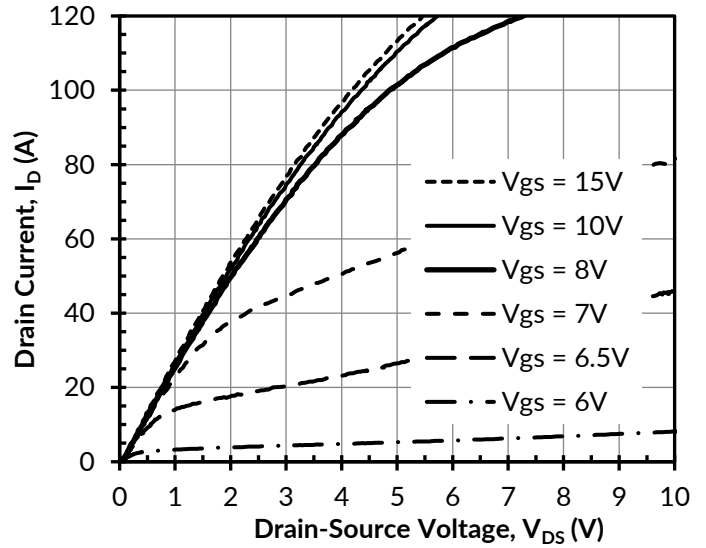


Figure 2. Typical output characteristics at  $T_J = 25^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

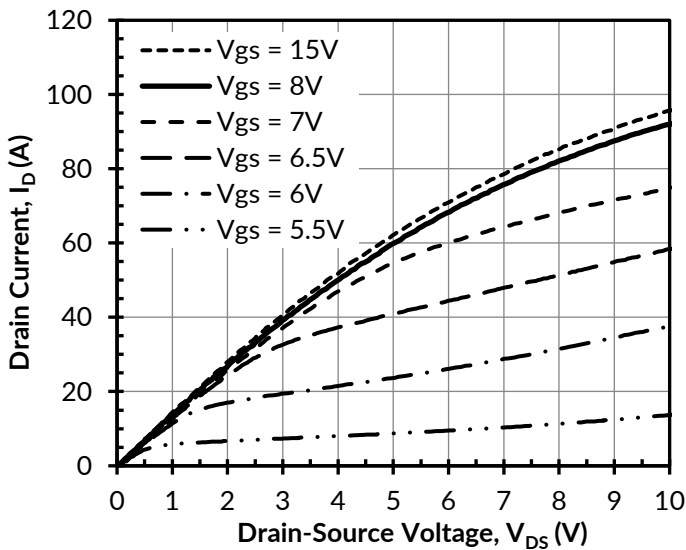


Figure 3. Typical output characteristics at  $T_J = 175^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

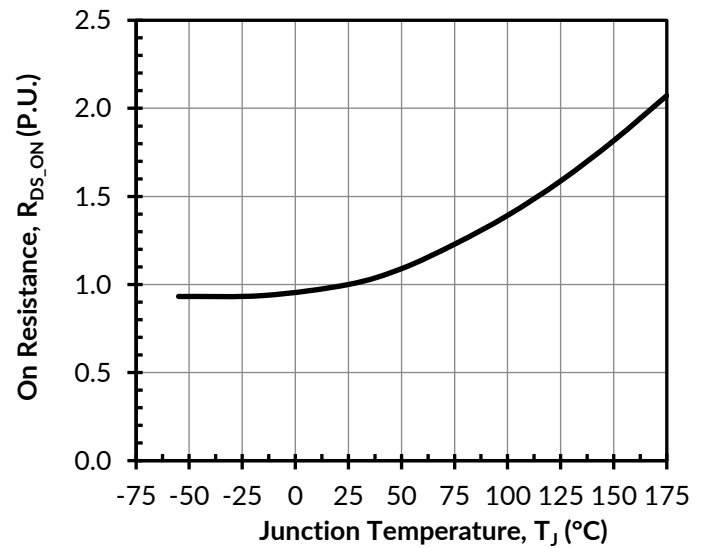


Figure 4. Normalized on-resistance vs. temperature at  $V_{GS} = 12\text{V}$  and  $I_D = 40\text{A}$

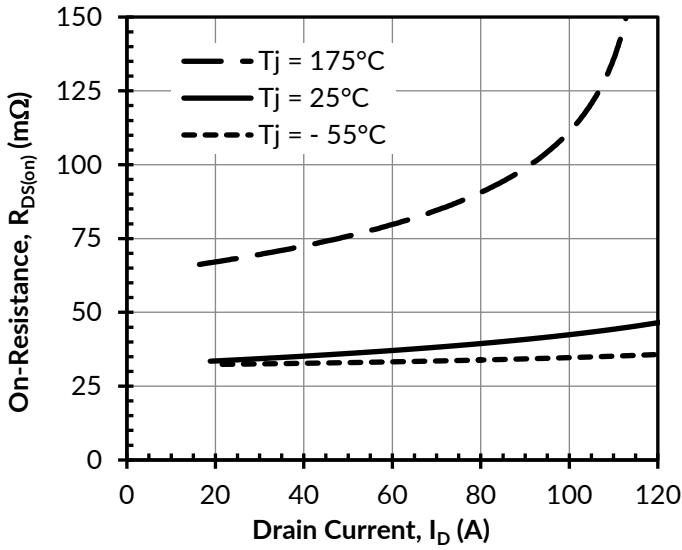


Figure 5. Typical drain-source on-resistances at  $V_{GS} = 12\text{V}$

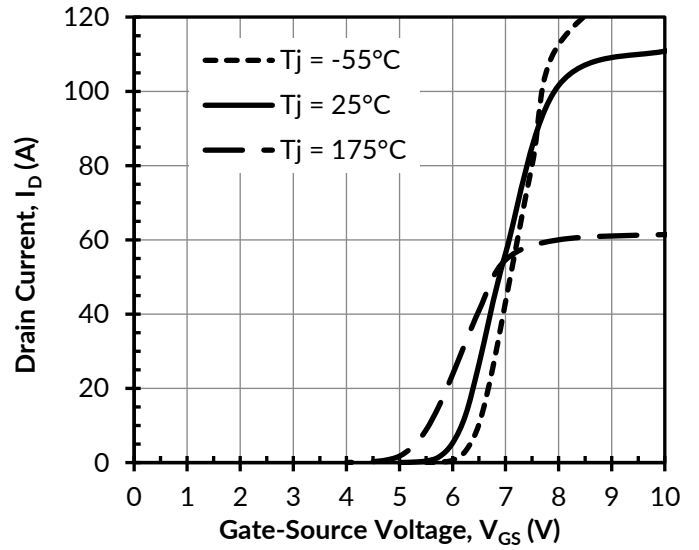


Figure 6. Typical transfer characteristics at  $V_{DS} = 5\text{V}$

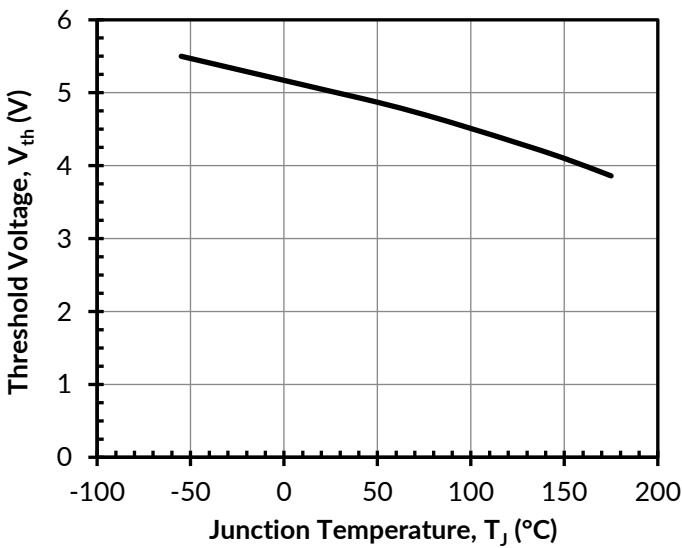


Figure 7. Threshold voltage vs. junction temperature at  $V_{DS} = 5\text{V}$  and  $I_D = 10\text{mA}$

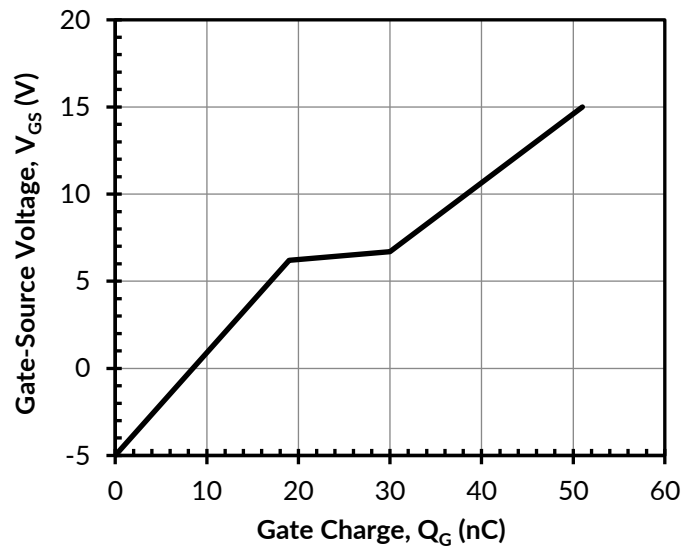


Figure 8. Typical gate charge at  $V_{DS} = 800\text{V}$  and  $I_D = 40\text{A}$

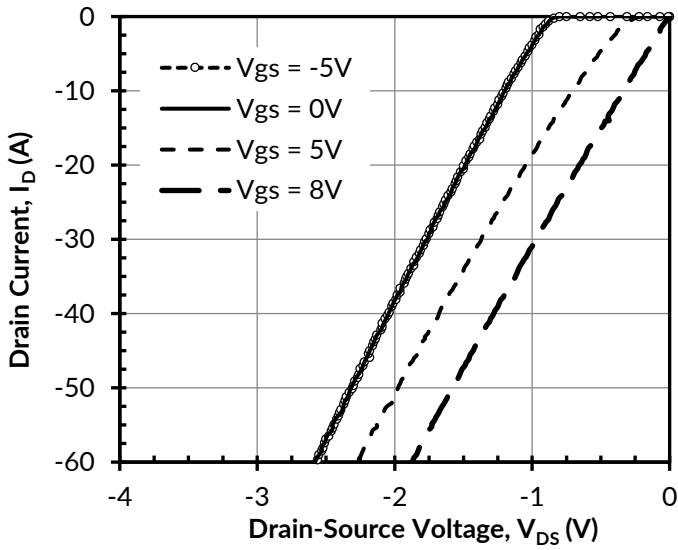


Figure 9. 3rd quadrant characteristics at  $T_j = -55^\circ\text{C}$

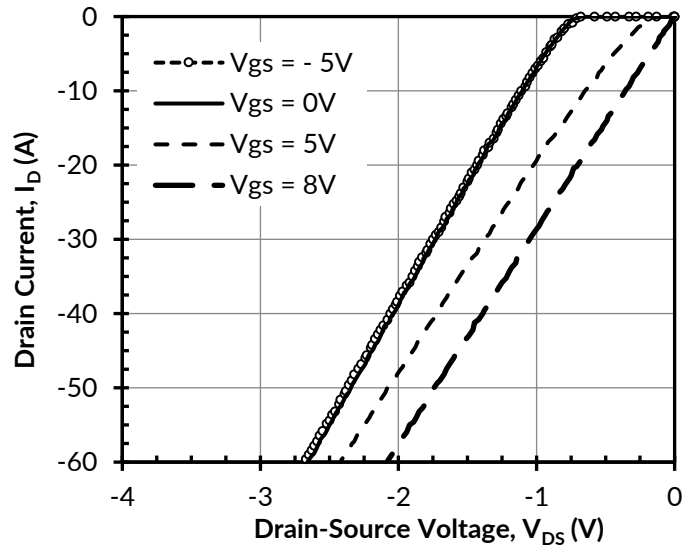


Figure 10. 3rd quadrant characteristics at  $T_j = 25^\circ\text{C}$

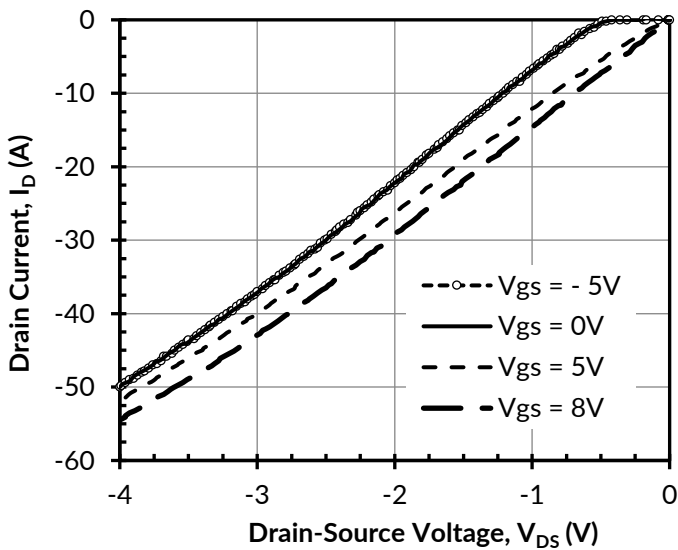


Figure 11. 3rd quadrant characteristics at  $T_j = 175^\circ\text{C}$

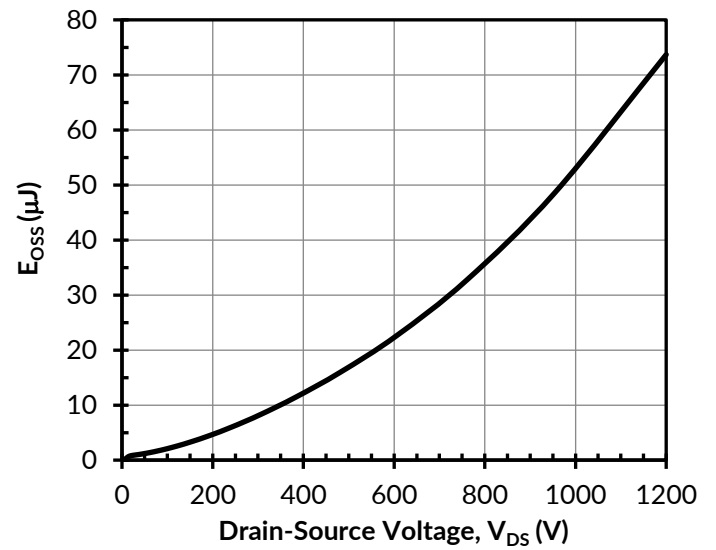


Figure 12. Typical stored energy in  $C_{OSS}$  at  $V_{GS} = 0\text{V}$

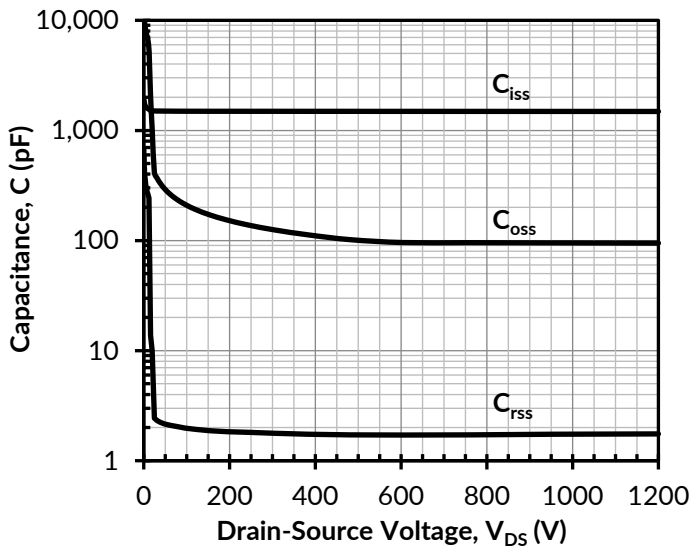


Figure 13. Typical capacitances at  $f = 100\text{kHz}$  and  $V_{GS} = 0\text{V}$

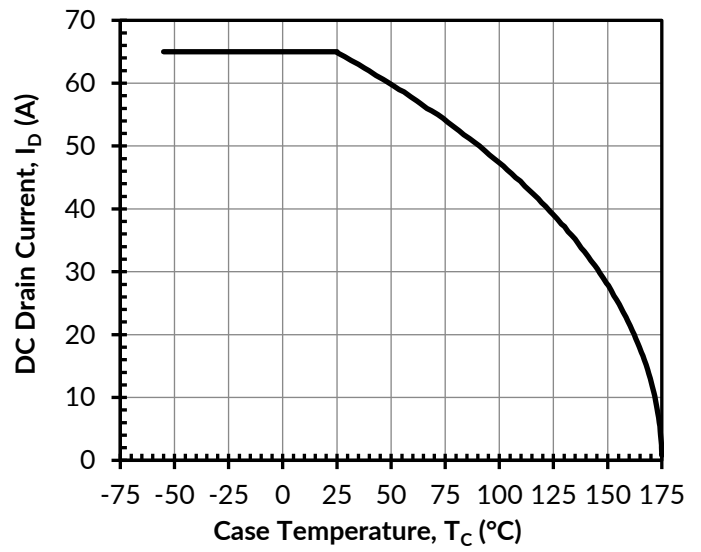


Figure 14. DC drain current derating

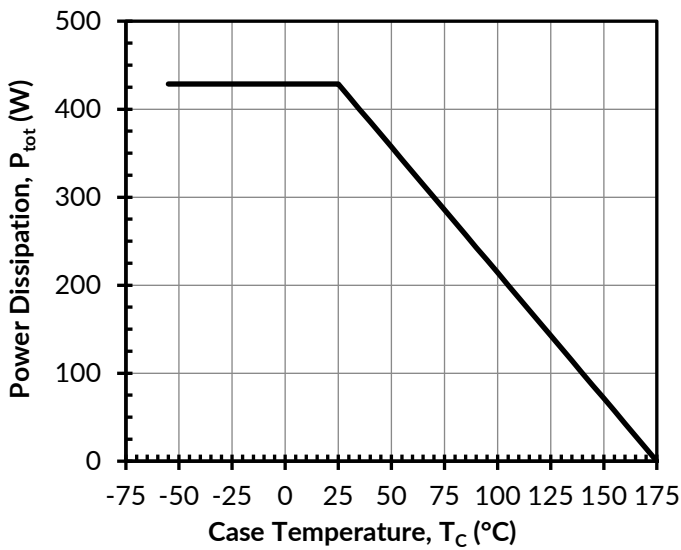


Figure 15. Total power dissipation

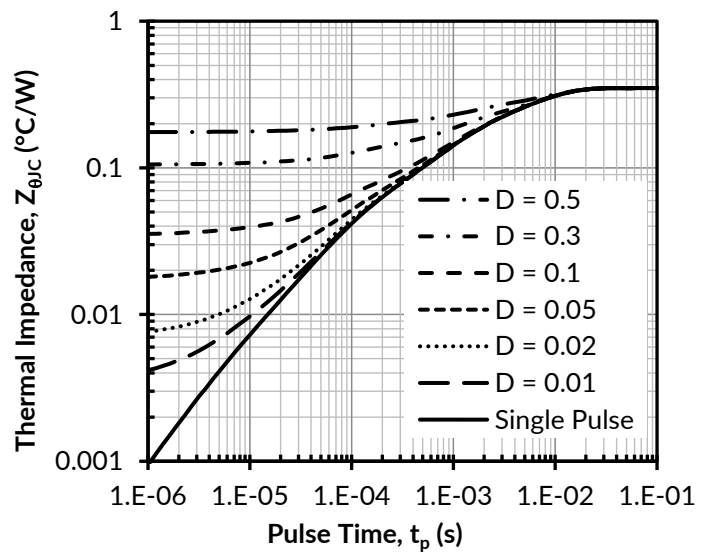


Figure 16. Maximum transient thermal impedance



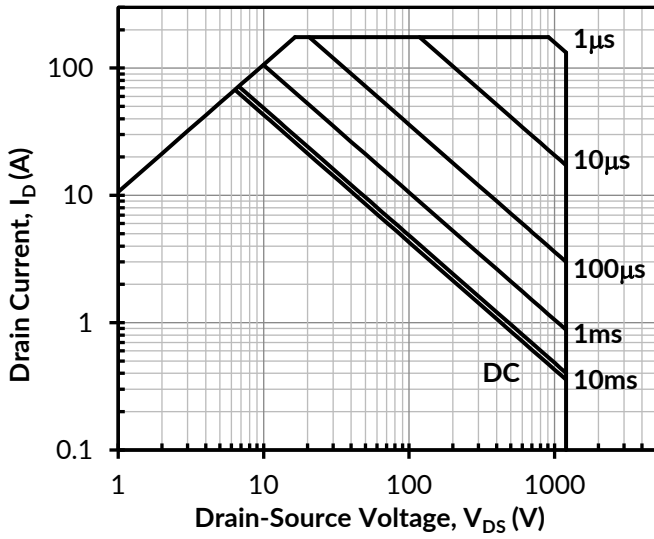


Figure 17. Safe operation area at  $T_C = 25^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$

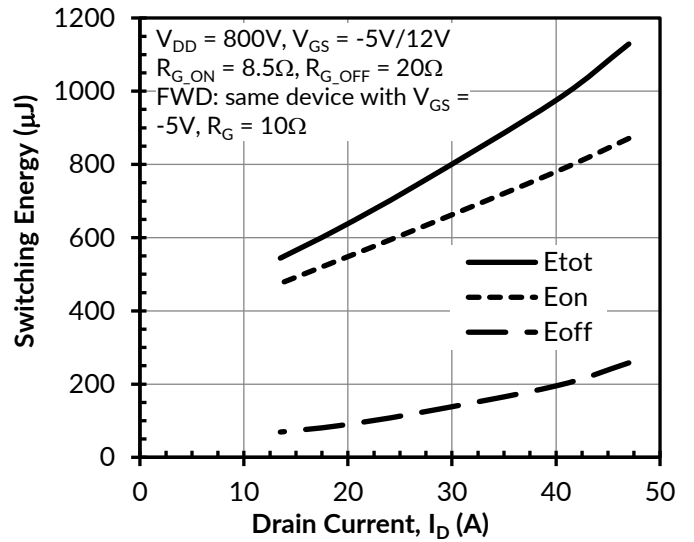


Figure 18. Clamped inductive switching energy vs. drain current at  $T_J = 25^\circ\text{C}$

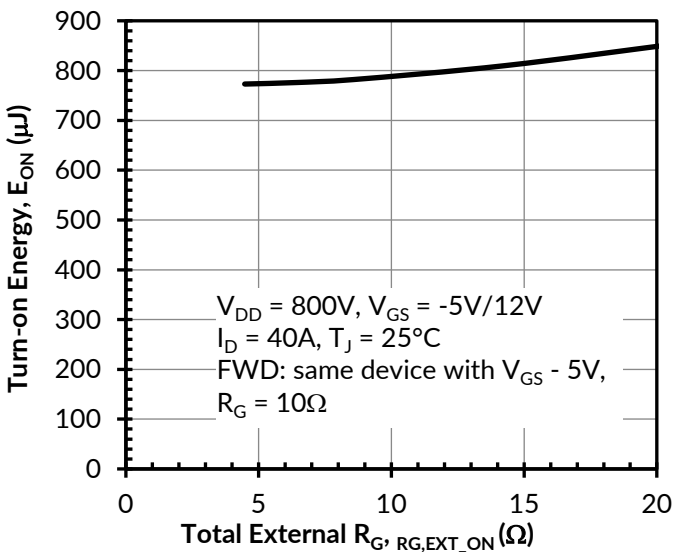


Figure 19. Clamped inductive switching turn-on energy vs.  $R_{G,EXT,ON}$

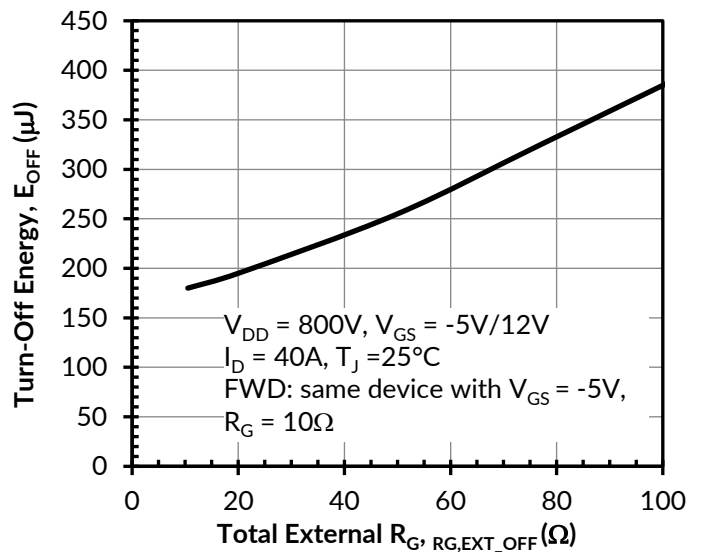


Figure 20. Clamped inductive switching turn-off energy vs.  $R_{G,EXT,OFF}$

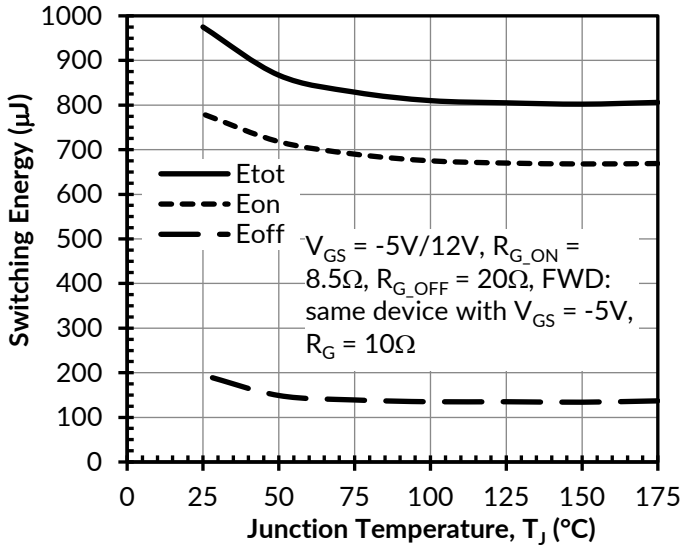


Figure 21. Clamped inductive switching energy vs. junction temperature at  $V_{DS} = 800V$  and  $I_D = 40A$

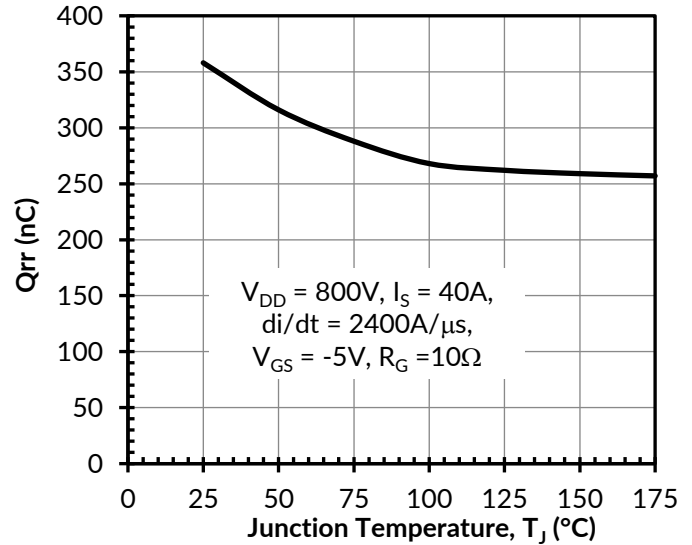


Figure 22. Reverse recovery charge  $Q_{rr}$  vs. junction temperature

## Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see [www.unitedsic.com](http://www.unitedsic.com).

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