#### **MAX9768**

# 10W Mono Class D Speaker Amplifier with Volume Control

## **General Description**

The MAX9768 mono 10W Class D speaker amplifier provides high-quality, efficient audio power with an integrated volume control function.

The MAX9768 features a 64-step dual-mode (analog or digitally programmable) volume control and mute function. The audio amplifier operates from a 4.5V to 14V single supply and can deliver up to 10W into an  $8\Omega$  speaker with a 14V supply.

A selectable spread-spectrum mode reduces EMIradiated emissions, allowing the device to pass EMC testing with ferrite bead filters and cable lengths up to 1m. The MAX9768 can be synchronized to an external clock, allowing synchronization of multiple Class D amplifiers.

The MAX9768 features high 77dB PSRR, low 0.08% THD+N, and SNR up to 97dB. Robust short-circuit and thermal-overload protection prevent device damage during a fault condition. The MAX9768 is available in a 24-pin thin QFN-EP (4mm x 4mm x 0.8mm) package and is specified over the extended -40°C to +85°C temperature range.

## **Applications**

- Notebook Computers
- Flat-Panel Displays
- Multimedia Monitors
- GPS Navigation Systems
- Security/Personal Mobile Radio

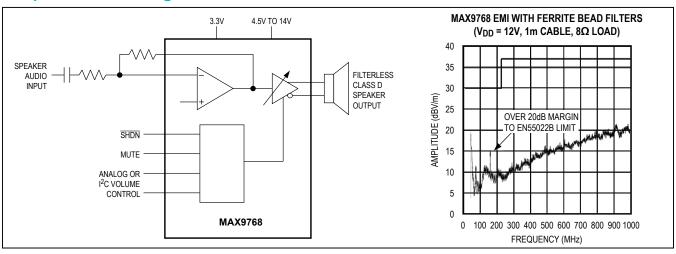
#### **Features**

- 10W Output (8Ω, PV<sub>DD</sub> = 14V, THD+N = 10%)
- Spread-Spectrum Modulation
- Meets EN55022B EMC with Ferrite Bead Filters
- Amplifier Operation from 4.5V to 14V Supply
- 64-Step Integrated Volume Control (I<sup>2</sup>C or Analog)
- Low 0.08% THD+N ( $R_L = 8\Omega$ ,  $P_{OUT} = 6W$ )
- High 77dB PSRR
- Two t<sub>ON</sub> Times Offered
  - MAX9768—220ms
  - MAX9768B—15ms
- Low-Power Shutdown Mode (0.5µA)
- Short-Circuit and Thermal-Overload Protection

<u>Pin Configuration</u> located toward end of data sheet.

Ordering Information located at end of data sheet.

# **Simplified Block Diagram**





# 10W Mono Class D Speaker Amplifier with Volume Control

# **Absolute Maximum Ratings**

PV <sub>DD</sub> to PGND0.3\	√ to +16V	Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )
V <sub>DD</sub> to GND0.3	3V to +4V	Single-Layer Board:
SCLK, SDA/VOL to GND0.3	3V to +4V	24-Pin Thin QFN 4mm x 4mm,
FB, SYNCOUT0.3V to (V <sub>DI</sub>	D + 0.3V)	(derate 20.8mW/°C above +70°C)1.67W
BOOT_ to OUT0.3	3V to +4V	Multilayer Board:
OUT_ to GND0.3V to (PV <sub>DI</sub>	D + 0.3V)	24-Pin Thin QFN 4mm x 4mm,
PGND to GND0.3V	to +0.3V	(derate 27.8mW/°C above +70°C)2.22W
Any Other Pin to GND0.3	3V to +4V	θ <sub>JA</sub> , Single-Layer Board48°C/W
OUT_ Short-Circuit Duration	ontinuous	θ <sub>JA</sub> , Multilayer Board36°C/W
Continuous Current (PV <sub>DD</sub> , PGND, OUT_)	2.2A	Operating Temperature Range40°C to +85°C
Continuous Input Current (Any Other Pin)	±20mA	Storage Temperature Range65°C to +150°C
Continuous Input Current (FB_)	±60mA	Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **Electrical Characteristics**

 $(PV_{DD}$  = 12V,  $V_{DD}$  = 3.3V,  $V_{GND}$  =  $V_{PGND}$  = 0,  $V_{\overline{SHDN}}$  =  $V_{DD}$ ,  $V_{MUTE}$  = 0; Max volume setting; speaker load resistor connected between OUT+ and OUT-,  $R_L$  = ∞, unless otherwise noted.  $C_{BIAS}$  = 2.2μF, C1 = C2 = 0.1μF,  $C_{IN}$  = 0.47μF,  $R_{IN}$  = 20kΩ,  $R_F$  = 30kΩ, SSM mode. Filterless modulation mode (see the *Functional Diagram/Typical Application Circuit*).  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Speaker Supply Voltage Range	PV <sub>DD</sub>	Inferred from P	SRR test	4.5		14.0	V
Supply Voltage Range	V <sub>DD</sub>	Inferred from P	SRR and UVLO test	2.7		3.6	V
	I <sub>VDD</sub>				7	14.2	
Quiescent Current	l	Filterless modu	llation		4	7.6	mA
	I <sub>PVDD</sub>	Classic PWM n	nodulation		4	7.6	
Shutdown Current	I <sub>SHDN</sub>	I <sub>SHDN</sub> = I <sub>PVDD</sub>	+ $I_{DD}$ , $\overline{SHDN}$ = GND, $T_A$ = +25°C		0.5	50	μΑ
Output Offact	\/	Filterless modulation, V <sub>MUTE</sub> = V <sub>DD</sub> , T <sub>A</sub> = +25°C			±2	±12.5	mV
Output Offset	Vos	Filterless modu	llation, V <sub>MUTE</sub> = 0V, T <sub>A</sub> = +25°C		±2	±14	IIIV
Turn-On Time t <sub>ON</sub>		MAX9768			220		ma
		MAX9768B			15		ms
Common-Mode Bias Voltage	V <sub>BIAS</sub>				1.5		V
Input Amplifier Output- Voltage Swing High	V <sub>OH</sub>	Specified as V <sub>DD</sub> - V <sub>OH</sub>	$R_L$ = 2kΩ connect to 1.5V		3.6	100	mV
Input Amplifier Output- Voltage Swing Low	V <sub>OL</sub>	Specified as V <sub>OL</sub> - GND	$R_L$ = 2kΩ connect to 1.5V		6	50	mV
Input Amplifier Output Short-Circuit Current Limit					±60		mA
Input Amplifier Gain- Bandwidth Product	GBW				1.8		MHz
SPEAKER AMPLIFIERS							
Internal Gain	A <sub>VMAX</sub>	Max volume setting; from FB to amplifier outputs  (OUT+) - (OUT-) ; excludes external gain resistors		29.27	30.1	31.00	dB

 $((PV_{DD}=12V,V_{DD}=3.3V,V_{GND}=V_{PGND}=0,V_{\overline{SHDN}}=V_{DD},V_{MUTE}=0;$  Max volume setting; speaker load resistor connected between OUT+ and OUT-,  $R_L=\infty$ , unless otherwise noted.  $C_{BIAS}=2.2\mu F$ , C1 = C2 = 0.1μF,  $C_{IN}=0.47\mu F$ ,  $R_{IN}=20k\Omega$ ,  $R_F=30k\Omega$ , SSM mode. Filterless modulation mode (see the *Functional Diagram/Typical Application Circuit*).  $T_A=T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A=+25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Efficiency (Note 2)	n	P <sub>OUT</sub> = 8W, f <sub>IN</sub> =	Filterless mo	dulation		87		0/
Efficiency (Note 2)	η	1kHz, $R_L = 8\Omega$	Classic PWM	I modulation		85		%
		D\/ - 5\/		$R_L = 8\Omega$ , THD+N = 1%, filterless modulation		1.3		
		PV <sub>DD</sub> = 5V	R <sub>L</sub> = 8Ω, THI filterless mod			1.7		
Output Dawer (Note 2)		DV - 40V	$R_L = 8\Omega$ , THI classic PWM			9		
Output Power (Note 2)	Роит	PV <sub>DD</sub> = 12V	$R_L = 8\Omega$ , THI filterless mod			9		W
		DV = 14V	$R_L = 8\Omega$ , THI classic PWM			10		
		PV <sub>DD</sub> = 14V	$R_L = 8\Omega$ , THD+N = 10%, filterless modulation			10		
Soft Output Current Limit	I <sub>LIM</sub>				1.75	2		Α
Hard Output Current Limit	I <sub>SC</sub>					2.5		Α
Total Harmonic Distortion	THD+N	$f = 1kHz, R_L = 8\Omega,$	Filterless modulation		0.09		%	
Plus Noise (Note 2)	111211	P <sub>OUT</sub> = 5W	Classic PWM	l modulation	0.08			
	SNR	0dB = 8W, R <sub>L</sub> = 8Ω, BW = 22Hz to 22kHz, filterless modulation mode	Unweighted	FFM		94		- dB
				SSM		93		
			A-weighted	FFM		97		
Signal-to-Noise Ratio				SSM		97		
(Note 2)		0dB = 8W, R <sub>L</sub> = 8Ω, BW = 22Hz	Unweighted A-weighted	FFM		93		
				SSM		89		
		to 22kHz, classic PWM modulation		FFM		97		
		Pyvivi modulation	SSM			91		
MUTE Attenuation (Note 3)		0dB = 8W, f = 1kHz				115		dB
		V <sub>DD</sub> = 2.7V to 3.6V, filterless modulation, T <sub>A</sub> = +25°C			52	68		
Power-Supply Rejection Ratio	PSRR	PV <sub>DD</sub> = 4.5V to 14V T <sub>A</sub> = +25°C	/, filterless mod	dulation,	67	84		dB
		f = 1kHz, V <sub>RIPPLE</sub> =	= 200mV <sub>P-P</sub> or	PV <sub>DD</sub>		77		
		f = 1kHz, V <sub>RIPPLE</sub> = 100mV <sub>P-P</sub> on V <sub>DD</sub>			60			
		SYNC = GND			1060	1200	1320	- kHz
Oscillator Frequency	focas	SYNC = unconnect	ed		1296	1440	1584	
Oscillator Frequency	focs	SYNC = V <sub>DD</sub> (spreamode)	read-spectrum modulation			1200 ±30		, Kriz

 $((PV_{DD}=12V,V_{DD}=3.3V,V_{GND}=V_{PGND}=0,V_{\overline{SHDN}}=V_{DD},V_{MUTE}=0;$  Max volume setting; speaker load resistor connected between OUT+ and OUT-,  $R_L=\infty$ , unless otherwise noted.  $C_{BIAS}=2.2\mu F$ , C1 = C2 = 0.1μF,  $C_{IN}=0.47\mu F$ ,  $R_{IN}=20k\Omega$ ,  $R_F=30k\Omega$ , SSM mode. Filterless modulation mode (see the *Functional Diagram/Typical Application Circuit*).  $T_A=T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A=+25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			TYP	MAX	UNITS	
		SYNC = GND		265	300	330		
Class D Switching Frequency		SYNC = unconnected	324	360	396	kHz		
olass 2 sillisillig i requelle,		SYNC = V <sub>DD</sub> (spread-spectrum modulation			300			
		mode)			±7.5			
SYNC Frequency Lock Range				1000		1600	kHz	
Minimum SYNC Frequency Lock Duty Cycle					40		%	
Maximum SYNC Frequency Lock Duty Cycle					60		%	
Gain Matching		Full volume (ideal matching fo	r R <sub>IN</sub> and R <sub>F</sub> )		2		%	
		Peak voltage, 32 samples	Into shutdown		52.6			
	14	per second, A-weighted, R <sub>IN</sub> x C <sub>IN</sub> ≤ 10ms to guarantee clickless/popless operation	Out of shutdown		48		dBV	
Click-and-Pop Level (Note 2)	K <sub>CP</sub>		Into mute		67			
			Out of mute		57			
Input Impedance		DC volume control mode (SDA/VOL)			100		ΜΩ	
Input Hysteresis		DC volume control mode (SDA	A/VOL)		11		mV	
9.5dB Gain Voltage		DC volume control mode (SDA	VVOL)	0.1 x V <sub>DD</sub>			V	
Full Mute Voltage		DC volume control mode (SDA	A/VOL)	0.9 x V <sub>DD</sub>		V		
DIGITAL INPUTS (SHDN, MU	TE, ADDR1,	ADDR2, SYNC)						
lament Valtage I ligh		SYNC		2.33			V	
Input-Voltage High	V <sub>IH</sub>	All other pins		0.7 x V <sub>D</sub>	)D		V	
		SYNC			-	8.0	V	
Input-Voltage Low	V <sub>IL</sub>	All other pins			0.	3 x V <sub>DD</sub>	V	
	I <sub>SYNC</sub>	T <sub>A</sub> = +25°C			±7.5	±13		
Input Leakage Current	I <sub>LK</sub>	All other digital inputs, $T_A = +2$	25°C			±1	μA	
DIGITAL OUTPUT (SYNCOU	Τ)							
Output-Voltage High		Load = 1mA		V <sub>DD</sub> - 0.	3		V	
Output-Voltage Low		Load = 1mA				0.3	V	
Rise/Fall Time		C <sub>L</sub> = 10pF			5		ns	
		•		-				

 $((PV_{DD}=12V,V_{DD}=3.3V,V_{GND}=V_{PGND}=0,V_{\overline{SHDN}}=V_{DD},V_{MUTE}=0;$  Max volume setting; speaker load resistor connected between OUT+ and OUT-,  $R_L=\infty$ , unless otherwise noted.  $C_{BIAS}=2.2\mu F$ , C1 = C2 = 0.1μF,  $C_{IN}=0.47\mu F$ ,  $R_{IN}=20k\Omega$ ,  $R_F=30k\Omega$ , SSM mode. Filterless modulation mode (see the *Functional Diagram/Typical Application Circuit*).  $T_A=T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A=+25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP MAX	UNITS
THERMAL PROTECTION	•			
Thermal Shutdown Threshold			150	°C
Thermal Shutdown Hysteresis			15	°C
DIGITAL INPUTS (SCLK, SD.	A/VOL)			
Input-Voltage High	V <sub>IH</sub>		0.7 x V <sub>DD</sub>	V
Input-Voltage Low	V <sub>IL</sub>		0.3 x V <sub>DD</sub>	V
Input High Leakage Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub> , T <sub>A</sub> = +25°C	±1	μΑ
Input Low Leakage Current	I <sub>IL</sub>	V <sub>IN</sub> = GND, T <sub>A</sub> = +25°C	±1	μΑ
Input Hysteresis			0.1 x V <sub>DD</sub>	V
Input Capacitance	C <sub>IN</sub>		5	pF
DIGITAL OUTPUTS (SDA/VO	L)			
Output High Current	Гон	V <sub>OH</sub> = V <sub>DD</sub>	1	μΑ
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3mA	0.4	V
I <sup>2</sup> C TIMING CHARACTERIST	ICS (Figure	3)		
Serial Clock	f <sub>SCL</sub>		400	kHz
Bus Free Time Between a STOP and START Condition	t <sub>BUF</sub>		1.3	μs
Hold Time (Repeated) START Condition	t <sub>HD,STA</sub>		0.6	μs
Repeated START Condition Setup Time	t <sub>SU,STA</sub>		0.6	μs
STOP Condition Setup Time	t <sub>SU,STO</sub>		0.6	μs
Data Hold Time	t <sub>HD,DAT</sub>		0 0.9	μs
Data Setup Time	t <sub>SU,DAT</sub>		100	ns
SCL Clock Low Period	t <sub>LOW</sub>		1.3	μs
SCL Clock High Period	tHIGH		0.6	μs
Rise Time of SDA and SCL, Receiving	t <sub>R</sub>	(Note 4)	20 + 0.1Cb 300	ns
Fall Time of SDA and SCL, Receiving	t <sub>F</sub>	(Note 4)	20 + 0.1Cb 300	ns

((PV<sub>DD</sub> = 12V, V<sub>DD</sub> = 3.3V, V<sub>GND</sub> = V<sub>PGND</sub> = 0, V<sub>SHDN</sub> = V<sub>DD</sub>, V<sub>MUTE</sub> = 0; Max volume setting; speaker load resistor connected between OUT+ and OUT-, R<sub>L</sub> = ∞, unless otherwise noted. C<sub>BIAS</sub> = 2.2μF, C1 = C2 = 0.1μF, C<sub>IN</sub> = 0.47μF, R<sub>IN</sub> = 20kΩ, R<sub>F</sub> = 30kΩ, SSM mode. Filterless modulation mode (see the *Functional Diagram/Typical Application Circuit*). T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time of SDA, Transmitting	t <sub>F</sub>	(Note 4)	20 + 0.1Cb		250	ns
Pulse Width of Spike Suppressed	t <sub>SP</sub>		0		50	ns
Capacitive Load for Each Bus Line	C <sub>b</sub>				400	pF

Note 1: All devices are 100% production tested at  $T_A = +25$ °C. All temperature limits are guaranteed by design.

Note 2: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For  $R_L = 8\Omega$ ,  $L = 68\mu H$ .

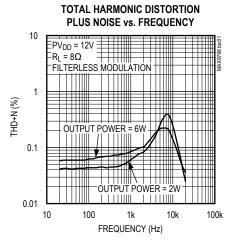
Note 3: Device muted by either asserting MUTE or minimum V<sub>OL</sub> setting.

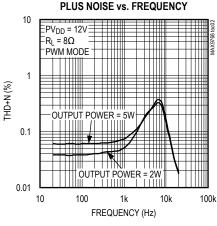
**Note 4:**  $C_b$  = total capacitance of one bus line in pF.

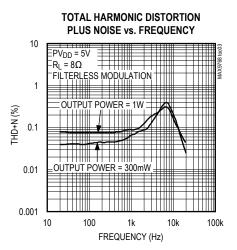
# **Typical Operating Characteristics**

((PV<sub>DD</sub> = 12V, V<sub>DD</sub> = 3.3V, V<sub>GND</sub> = V<sub>PGND</sub> = 0, V<sub>MUTE</sub> = 0; 0dB volume setting; all speaker load resistors connected between OUT+ and OUT-, R<sub>L</sub> = 8Ω, unless otherwise noted.  $C_{BIAS}$  = 2.2μF, C1 = C2 = 0.1μF,  $C_{IN}$  = 0.47μF,  $R_{IN}$  = 20kΩ,  $R_{FB}$  = 30kΩ, spread-spectrum modulation mode.)

TOTAL HARMONIC DISTORTION

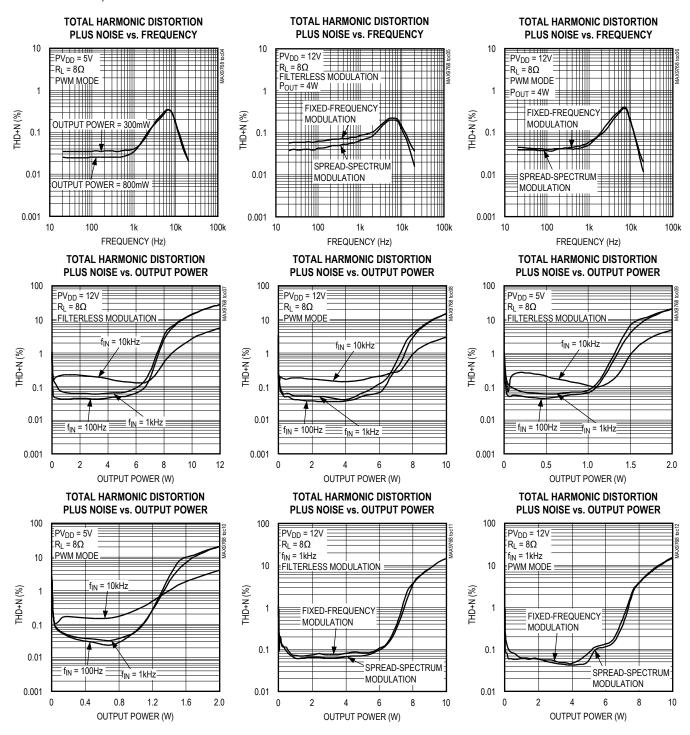






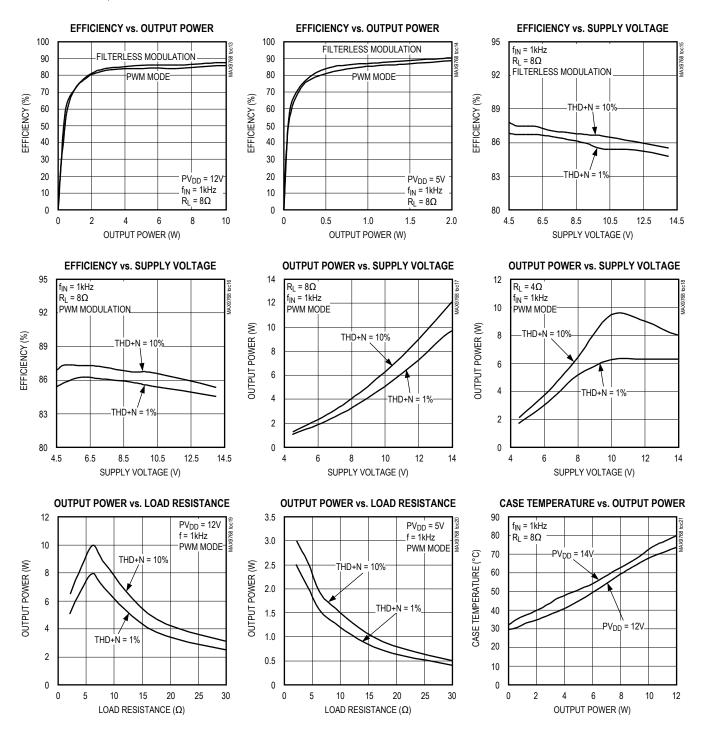
## **Typical Operating Characteristics (continued)**

((PV<sub>DD</sub> = 12V, V<sub>DD</sub> = 3.3V, V<sub>GND</sub> = V<sub>PGND</sub> = 0, V<sub>MUTE</sub> = 0; 0dB volume setting; all speaker load resistors connected between OUT+ and OUT-, R<sub>L</sub> = 8Ω, unless otherwise noted.  $C_{BIAS}$  = 2.2μF, C1 = C2 = 0.1μF,  $C_{IN}$  = 0.47μF,  $R_{IN}$  = 20kΩ,  $R_{FB}$  = 30kΩ, spread-spectrum modulation mode.)



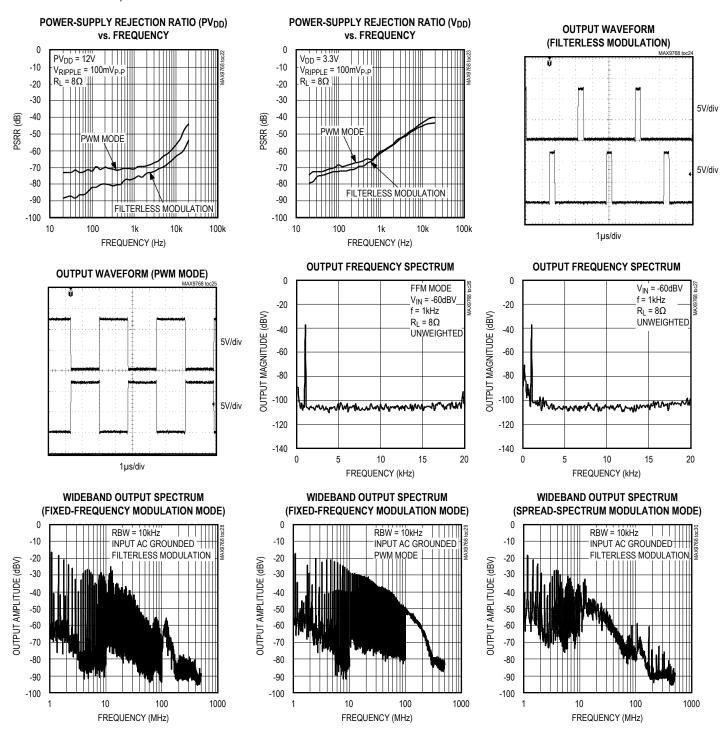
# **Typical Operating Characteristics (continued)**

((PV<sub>DD</sub> = 12V, V<sub>DD</sub> = 3.3V, V<sub>GND</sub> = V<sub>PGND</sub> = 0, V<sub>MUTE</sub> = 0; 0dB volume setting; all speaker load resistors connected between OUT+ and OUT-, R<sub>L</sub> = 8Ω, unless otherwise noted.  $C_{BIAS}$  = 2.2μF, C1 = C2 = 0.1μF,  $C_{IN}$  = 0.47μF,  $R_{IN}$  = 20kΩ,  $R_{FB}$  = 30kΩ, spread-spectrum modulation mode.)



## **Typical Operating Characteristics (continued)**

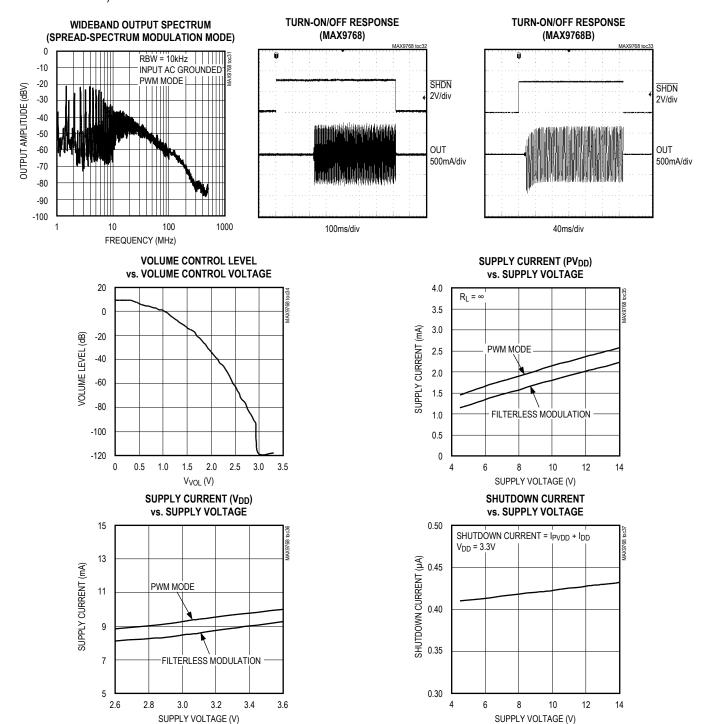
((PV<sub>DD</sub> = 12V, V<sub>DD</sub> = 3.3V, V<sub>GND</sub> = V<sub>PGND</sub> = 0, V<sub>MUTE</sub> = 0; 0dB volume setting; all speaker load resistors connected between OUT+ and OUT-, R<sub>L</sub> = 8Ω, unless otherwise noted.  $C_{BIAS}$  = 2.2μF, C1 = C2 = 0.1μF,  $C_{IN}$  = 0.47μF,  $R_{IN}$  = 20kΩ,  $R_{FB}$  = 30kΩ, spread-spectrum modulation mode.)



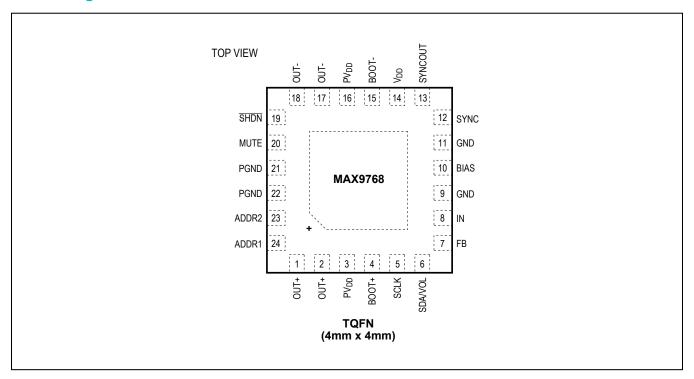
# 10W Mono Class D Speaker Amplifier with Volume Control

# **Typical Operating Characteristics (continued)**

((PV<sub>DD</sub> = 12V, V<sub>DD</sub> = 3.3V, V<sub>GND</sub> = V<sub>PGND</sub> = 0, V<sub>MUTE</sub> = 0; 0dB volume setting; all speaker load resistors connected between OUT+ and OUT-, R<sub>L</sub> = 8Ω, unless otherwise noted.  $C_{BIAS}$  = 2.2μF, C1 = C2 = 0.1μF,  $C_{IN}$  = 0.47μF,  $R_{IN}$  = 20kΩ,  $R_{FB}$  = 30kΩ, spread-spectrum modulation mode.)



# **Pin Configuration**



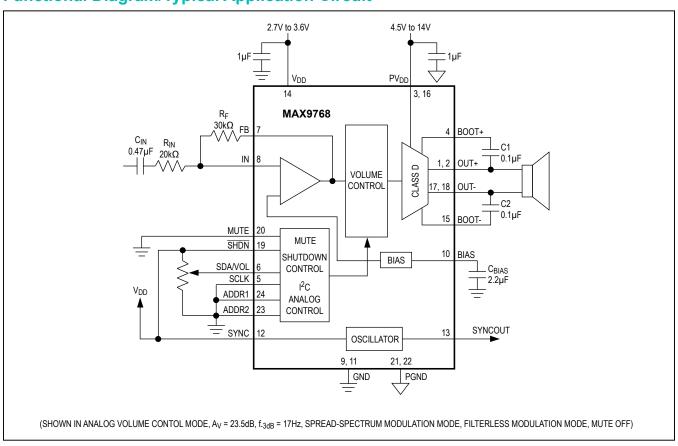
# **Pin Description**

PIN	NAME	FUNCTION	
1, 2	OUT+	Positive Speaker Output	
3, 16	PV <sub>DD</sub>	Speaker Amplifier Power-Supply Input. Bypass with a 1µF capacitor to ground.	
4	BOOT+	Positive Speaker Output Boost Flying-Capacitor Connection. Connect a 0.1µF ceramic capacitor between BOOT+ and OUT+.	
5	SCLK	I <sup>2</sup> C Serial-Clock Input and Modulation Scheme Select. In I <sup>2</sup> C mode (ADDR1 and ADDR2 $\neq$ GND) acts as I <sup>2</sup> C serial-clock input. Connect SCLK to V <sub>DD</sub> for classic PWM modulation, or connect SCLK to ground for filterless modulation.	
6	SDA/VOL	I <sup>2</sup> C Serial Data I/O and Analog Volume Control Input	
7	FB	Feedback. Connect feedback resistor between FB and IN to set amplifier gain. See the <u>Adjustable Gain</u> section.	
8	IN	Audio Input	
9, 11	GND	Ground	
10	BIAS	Common-Mode Bias Voltage. Bypass with a 2.2µF capacitor to GND.	
12	SYNC	Frequency Select and External Clock Input. SYNC = GND: Fixed-frequency mode with $f_S = 300 \text{kHz}$ . SYNC = Unconnected: Fixed-frequency mode with $f_S = 360 \text{kHz}$ . SYNC = V <sub>DD</sub> : Spread-spectrum mode with $f_S = 300 \text{kHz} \pm 7.5 \text{kHz}$ . SYNC = Clocked: Fixed-frequency mode with $f_S = 800 \text{kHz} \pm 7.5 \text{kHz}$ .	

# **Pin Configuration (continued)**

13	SYNCOUT	Clock Signal Output
14	V <sub>DD</sub>	Power-Supply Input. Bypass with a 1µF capacitor to GND.
15	воот-	Negative Speaker Output Boost Flying-Capacitor Connection. Connect a 0.1µF ceramic capacitor between BOOTL- and OUTL
17, 18	OUT-	Negative Speaker Output
19	SHDN	Shutdown Input. Drive $\overline{\text{SHDN}}$ low to disable the audio amplifiers. Connect $\overline{\text{SHDN}}$ to $V_{DD}$ for normal operation
20	MUTE	Mute Input. Drive MUTE high to mute the speaker outputs. Connect Mute to GND for normal operation.
21, 22	PGND	Power Ground
23	ADDR2	Address Select Input 2. I <sup>2</sup> C address option, also selects volume control mode.
24	ADDR1	Address Select Input 1. I <sup>2</sup> C address option, also selects volume control mode.
_	EP	Exposed Pad. Connect the exposed thermal pad to GND, and use multiple vias to a solid copper area on the bottom of the PCB.

# **Functional Diagram/Typical Application Circuit**



## **Detailed Description**

The MAX9768 10W, Class D audio power amplifier with spread-spectrum modulation provides a significant step forward in switch-mode amplifier technology. The MAX9768 offers Class AB performance with Class D efficiency and a minimal board space solution. This device features a wide supply voltage operation (4.5V to 14V), analog or digitally adjusted volume control, externally set input gain, shutdown mode, SYNC input and output, speaker mute, and industry-leading click-and-pop suppression.

The MAX9768 features a 64-step, dual-mode (analog or I<sup>2</sup>C programmed) volume control and mute function. In analog volume control mode, voltage applied to SDA/VOL sets the volume level. Two address inputs (ADDR1, ADDR2) set the volume control function between analog and I<sup>2</sup>C and set the slave address. In I<sup>2</sup>C mode there are three selectable slave addresses allowing for multiple devices on a single bus.

Spread-spectrum modulation and synchronizable switching frequency significantly reduce EMI emissions. The outputs use Maxim's low-EMI modulation scheme with minimum pulse outputs when the audio inputs are at the zero crossing. As the input voltage increases or decreases, the duration of the pulse at one output increases while the other output pulse duration remains the same. This causes the net voltage across the speaker (V<sub>OUT+</sub> - V<sub>OUT-</sub>) to change. The minimum-width pulse topology reduces EMI and increases efficiency.

### **Operating Modes**

### **Fixed-Frequency Mode**

The MAX9768 features two fixed-frequency modes: 300kHz and 360kHz. Connect SYNC to GND to select 300kHz switching frequency; leave SYNC unconnected to select 360kHz switching frequency. The frequency spectrum of the MAX9768 consists of the fundamental switching frequency and its associated harmonics (see the Wideband Output Spectrum graphs in the *Typical Operating Characteristics*). For applications where exact

spectrum placement of the switching fundamental is important, program the switching frequency so the harmonics do not fall within a sensitive frequency band (Table 1). Audio reproduction is not affected by changing the switching frequency.

### **Spread-Spectrum Mode**

The MAX9768 features a unique spread-spectrum mode that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables. This mode is enabled by setting SYNC =  $V_{DD}$  (Table 1). In SSM mode, the switching frequency varies randomly by  $\pm 7.5$ kHz around the center frequency (300kHz). The modulation scheme remains the same, but the period of the triangle waveform changes from cycle to cycle. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequen-

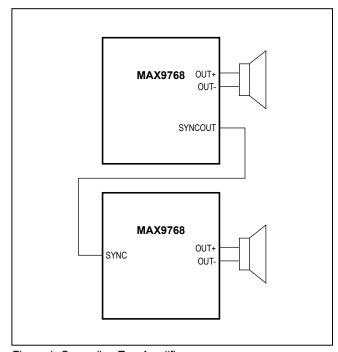


Figure 1. Cascading Two Amplifiers

## **Table 1. Operating Modes**

SYNC	OSCILLATOR FREQUENCY (kHZ)	CLASS D FREQUENCY (kHZ)
GND	Fixed-frequency modulation with f <sub>OSC</sub> = 1200	Fixed-frequency modulation with f <sub>OSC</sub> = 300
Unconnected	Fixed-frequency modulation with f <sub>OSC</sub> = 1440	Fixed-frequency modulation with f <sub>OSC</sub> = 360
V <sub>DD</sub>	Spread-spectrum modulation with f <sub>OSC</sub> = 1200 ±30	Spread-spectrum modulation with f <sub>OSC</sub> = 300 ±7.5
Clocked	Fixed-frequency modulation with f <sub>OSC</sub> = external clock frequency	Fixed-frequency modulation with f <sub>OSC</sub> = external clock frequency/4

cy. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes. A proprietary amplifier topology ensures this does not corrupt the noise floor in the audio bandwidth.

#### **External Clock Mode**

The SYNC input allows the MAX9768 to be synchronized to an external clock, or another Maxim Class D amplifier, creating a fully synchronous system, minimizing clock intermodulation, and allocating spectral components of the switching harmonics to insensitive frequency bands. Applying a clock signal between 1MHz and 1.6MHz to SYNC synchronizes the MAX9768. The Class D switching frequency is equal to one-fourth the SYNC input frequency.

SYNCOUT is equal to the SYNC input frequency and allows several Maxim amplifiers to be cascaded. The synchronized output minimizes interference due to clock intermodulation caused by the switching spread between single devices. The modulation scheme remains the same when using SYNCOUT, and audio reproduction is not affected (Figure 1). Current flowing between SYNCOUT of a master device and SYNC of a slave device is low as the SYNC input is high impedance (typically  $200k\Omega$ ).

#### Filterless Modulation/PWM Modulation

The MAX9768 features two output modulation schemes: filterless modulation or classic PWM, selectable through SCLK when the device is in analog mode (ADDR2 and ADDR1 = GND, <u>Table 2</u>) or through the I<sup>2</sup>C interface (<u>Table 7</u>). Maxim's unique, filterless modulation scheme eliminates the LC filter required by traditional Class D amplifiers, reducing component count, conserving board space and system cost. Although the MAX9768 meets FCC and other EMI limits with a low-cost ferrite bead filter, many applications still may want to use a full LC-filtered output. If using a full LC filter, the performance is best with the MAX9768 configured for classic PWM output.

Switching between schemes while in normal operating mode with the  $I^2C$  interface, the output is not click-and-pop protected. To have click-and-pop protection when switching between output schemes, the device must enter shutdown mode and be configured to the new output scheme before the startup sequence is terminated.

The startup time for the MAX9768 is typically 220ms. The startup time for the MAX9768B is typically 15ms.

### **Efficiency**

Efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current-steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I<sup>2</sup>R loss of the MOSFET on-resistance, and quiescent-current overhead.

The theoretical best efficiency of a linear amplifier is 78%, however, that efficiency is only exhibited at peak output power. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the MAX9768 still exhibits > 80% efficiencies under the same conditions (Figure 2).

### **Soft Current Limit**

When the output current exceeds the soft current limit, 2A (typ), the MAX9768 enters a cycle-by-cycle current-limit mode. In soft current-limit mode, the output is clipped at 2A. When the output decreases so the output current falls below 2A, normal operation resumes. The effect of soft current limiting is a slight increase in distortion. Most

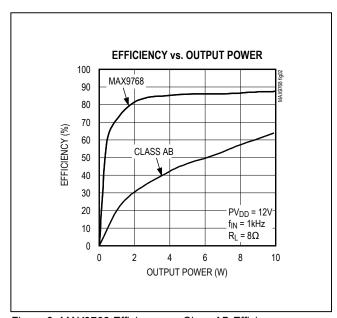


Figure 2. MAX9768 Efficiency vs. Class AB Efficiency

**Table 2. Modulation Scheme Selection In Analog Mode** 

ADDR2	ADDR1	SDA/VOL	SCLK	FUNCTION	
0	0	Analog Volume Control	0	Filterless Modulation	
0	0	Analog Volume Control	1	Classic PWM (50% Duty Cycle)	

# 10W Mono Class D Speaker Amplifier with Volume Control

applications will not enter soft current-limit mode unless the speaker or filter creates impedance nulls below  $8\Omega$ .

#### **Hard Current Limit**

When the output current exceeds the hard current limit, 2.5A (typ), the MAX9768 disables the outputs and initiates a startup sequence. This startup sequence takes 220ms for the MAX9768 and 15ms for the MAX9768B. The shutdown and startup sequence is repeated until the output fault is removed. When in hard current limit, the output may make a soft clicking sound. The average supply current is relatively low, as the duty cycle of the output short is brief. Most applications will not enter hard current-limit mode unless the output is short circuited or incorrectly connected.

#### **Thermal Shutdown**

When the die temperature exceeds the thermal shutdown threshold, +150°C (typ), the MAX9768 outputs are disabled. When the die temperature decreases below +135°C (typ), normal operation resumes. The effect of thermal shutdown is an output signal turning off for approximately 3s in most applications, depending on the thermal time constant of the audio system. Most applications should never enter thermal shutdown. Some of the possible causes of thermal shutdown are too low of a load impedance, high ambient temperature, poor PCB layout and assembly, or excessive output overdrive.

#### Shutdown

The MAX9768 features a shutdown mode that reduces power consumption and extends battery life. Driving  $\overline{SHDN}$  low places the device in low-power (0.5µA) shutdown mode. Connect  $\overline{SHDN}$  to digital high for normal operation. In shutdown mode, the outputs are high impedance, SYNCOUT is pulled high, the BIAS voltage decays to zero, and the common-mode input voltage decays to zero. The I²C register retains its contents during shutdown.

#### Undervoltage Lockout (UVLO)

The MAX9768 features an undervoltage lockout protection that shuts down the device if either of the supplies are too low. The device will go into shutdown if  $V_{DD}$  is less than 2.5V ( $V_{DD}$  UVLO = 2.5V) or if  $PV_{DD}$  is less than 4V ( $PV_{DD}$  UVLO = 4V).

### **Mute Function**

The MAX9768 features a clickless/popless mute mode. When the device is muted, the outputs do not stop switching, only the volume level is muted to the speaker. To mute the MAX9768, drive MUTE to logic-high. MUTE should be held high during system power-up and power-down to ensure optimum click-and-pop performance.

#### **Volume Control**

The volume control operates from either an analog voltage input or through the I<sup>2</sup>C interface. The volume control has 64 levels, with the lowest setting equal to mute.

To set the device to analog mode, connect ADDR1 and ADDR2 to GND. In analog mode, SDA/VOL is an analog input for volume control, see the *Functional Diagram/Typical Application Circuit*. The analog input range is ratiometric between 0.9 x  $V_{DD}$  and 0.1 x  $V_{DD}$ , where 0.9 x  $V_{DD}$  = full mute and 0.1 x  $V_{DD}$  = full volume (Table 6).

In I<sup>2</sup>C mode, volume control for the speaker is controlled separately by the command register (see <u>Table 4</u>, <u>Table 5</u>, and <u>Table 6</u>). See the <u>Write Data Format</u> section for more information regarding formatting data and tables to set volume levels.

#### I<sup>2</sup>C Interface

The MAX9768 features an I<sup>2</sup>C 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX9768 and the master at clock rates up to 400kHz. When the MAX9768 is used on an I<sup>2</sup>C bus with multiple devices, the V<sub>DD</sub> supply must stay powered on to ensure proper I<sup>2</sup>C bus operation. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 3 shows the 2-wire interface timing diagram.

A master device communicates to the MAX9768 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (S $_r$ ) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9768 SDA line operates as both an input and an open-drain output. A pullup resistor, greater than  $500\Omega$ , is required on the SDA bus. The MAX9768 SCL line operates as an input only. A pullup resistor, greater than  $500\Omega$ , is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

### **Bit Transfer**

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the <u>START and STOP Conditions</u> section). SDA and SCL idle high when the I<sup>2</sup>C bus is not busy.

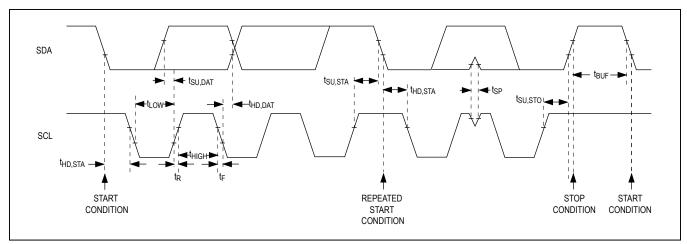


Figure 3. 2-Wire Serial-Interface Timing Diagram

#### **START and STOP Conditions**

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START (S) condition from the master signals the beginning of a transmission to the MAX9768. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

#### **Early STOP Conditions**

The MAX9768 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

#### Slave Address

The slave address of the MAX9768 is 8 bits and consist-

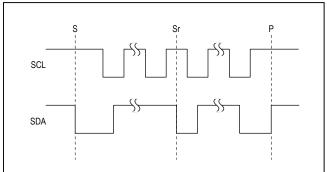


Figure 4. START, STOP, and REPEATED START Conditions

ing of 3 fields: the first field is 5 bits wide and is fixed

(10010). The second is a 2-bit field, which is set through ADDR2 and ADDR1 (externally connected as logic-high or low). Third field is a  $R/\overline{W}$  flag bit. Set  $R/\overline{W}$  = 0 to write to the slave. A representation of the slave address is shown in Table 3.

When ADDR1 and ADDR2 are connected to GND, serial interface communication is disabled. <u>Table 4</u> summarizes the slave address of the device as a function of ADDR1 and ADDR2.

#### **Acknowledge**

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9768 uses to handshake receipt each byte of data (Figure 5). The MAX9768 pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

#### **Write Data Format**

A write to the MAX9768 includes transmission of a START condition, the slave address with the R/ $\overline{W}$  bit set to 0 (see <u>Table 3</u>), one byte of data to the command register, and a STOP condition. <u>Figure 6</u> illustrates the proper format for one frame.

**Table 3. Slave Address Block** 

SA7 (MSB)	SA6	SA5	SA4	SA3	SA2	SA1	SA0 (LSB)
1	0	0	1	0	ADDR2	ADDR1	R/W

### **Table 4. Slave Address**

ADDR2	ADDR1	SLAVE ADDRESS
0	0	Disabled
0	1	1001001_
1	0	1001010_
1	1	1001011_

#### **Volume Control**

The command register is used to control the volume level of the speaker amplifier. The two MSBs (D7 and D6) should be set to 00 to choose the speaker register. V5–V0 is the volume control data that will be written into the addresses register to set the volume level (see <u>Table</u> 5 and Table 6).

For a write byte operation, the master sends a single byte to the slave device (MAX9768). This is done as follows:

- 1) The master sends a start condition.
- 2) The master sends the 7-bit slave ID plus a write bit (low).
- 3) The addressed slave asserts an ACK on the data
- 4) The master sends 8 data bits.
- The active slave asserts an ACK (or NACK) on the data line.
- 6) The master generates a stop condition.

# **Applications Information**

### **Filterless Class D Operation**

The MAX9768 can be operated without a filter and meet common EMC radiation limits when the speaker leads are less than approximately 10cm. Lengths beyond 10cm are possible but should be verified against the appropriate EMC standard. Select the filter-less modulation mode with spread-spectrum modulation mode for best performance.

For longer speaker wire lengths, a simple ferrite bead and capacitor-based filter can be used to meet EMC limits. See Figure 7 for the correct connections of these components. Select a ferrite bead with  $100\Omega$  to  $600\Omega$  impedance, and rated for at least 1.5A. The capacitor value will vary based on the ferrite bead chosen and the actual

**Table 5. Data Byte Format** 

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	0	V5	V4	V3	V2	V1	V0

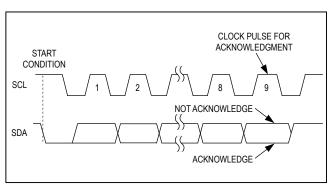


Figure 5. Acknowledge

VRITI	BYTE FORMAT	r				
S	SLAVE ADDRESS	WR	ACK	DATA	ACK	Р
	7 bits	0		8 bits		
	SLAVE ADDRESS: EQUIVALENT TO CHIP- SELECT LINE OF A 3- WIRE INTERFACE.			DATA BYTE: GIVES A C	COMMA	AND.

Figure 6. Write Data Format Example

**Table 6. Speaker Volume Levels** 

V5	V4	V3	V2	V1	V0	VOLUME POSITION	VOLUME LEVEL (dB)	STEP SIZE (dB)
1	1	1	1	1	1	63	9.5	0.7
1	1	1	1	1	0	62	8.8	0.7
1	1	1	1	0	1	61	8.2	0.6
1	1	1	1	0	0	60	7.6	0.6
1	1	1	0	1	1	59	7.0	0.6
1	1	1	0	1	0	58	6.5	0.5
1	1	1	0	0	1	57	5.9	0.5
1	1	1	0	0	0	56	5.4	0.5
1	1	0	1	1	1	55	4.9	0.5
1	1	0	1	1	0	54	4.4	0.5
1	1	0	1	0	1	53	3.9	0.6
1	1	0	1	0	0	52	3.4	0.4
1	1	0	0	1	1	51	2.9	0.5
1	1	0	0	1	0	50	2.4	0.4
1	1	0	0	0	1	49	2.0	0.4
1	1	0	0	0	0	48	1.6	0.4
1	0	1	1	1	1	47	1.2	0.7
1	0	1	1	1	0	46	0.5	1.0
1	0	1	1	0	1	45	-0.5	1.5
1	0	1	1	0	0	44	-1.9	1.5
1	0	1	0	1	1	43	-3.4	1.5
1	0	1	0	1	0	42	-5.0	1.1
1	0	1	0	0	1	41	-6.0	1.1
1	0	1	0	0	0	40*	-7.1	1.8
1	0	0	1	1	1	39	-8.9	1.0
1	0	0	1	1	0	38	-9.9	1.0
1	0	0	1	0	1	37	-10.9	1.1
1	0	0	1	0	0	36	-12.0	1.2
1	0	0	0	1	1	35	-13.1	1.3
1	0	0	0	1	0	34	-14.4	0.9
1	0	0	0	0	1	33	-15.4	1.0
1	0	0	0	0	0	32	-16.4	1.1

\*Default.

**Table 6. Speaker Volume Levels (continued)** 

V5	V4	V3	V2	V1	V0	VOLUME POSITION	VOLUME LEVEL (dB)	STEP SIZE (dB)
0	1	1	1	1	1	31	-17.5	2.2
0	1	1	1	1	0	30	-19.7	1.9
0	1	1	1	0	1	29	-21.6	1.9
0	1	1	1	0	0	28	-23.5	1.7
0	1	1	0	1	1	27	-25.2	2.0
0	1	1	0	1	0	26	-27.2	2.6
0	1	1	0	0	1	25	-29.8	1.6
0	1	1	0	0	0	24	-31.5	2.0
0	1	0	1	1	1	23	-33.4	2.5
0	1	0	1	1	0	22	-36.0	1.6
0	1	0	1	0	1	21	-37.6	2.0
0	1	0	1	0	0	20	-39.6	2.5
0	1	0	0	1	1	19	-42.1	1.6
0	1	0	0	1	0	18	-43.7	2.0
0	1	0	0	0	1	17	-45.6	2.5
0	1	0	0	0	0	16	-48.1	2.5
0	0	1	1	1	1	15	-50.6	3.5
0	0	1	1	1	0	14	-54.2	2.5
0	0	1	1	0	1	13	-56.7	3.5
0	0	1	1	0	0	12	-60.2	2.5
0	0	1	0	1	1	11	-62.7	3.5
0	0	1	0	1	0	10	-66.2	2.5
0	0	1	0	0	1	9	-68.7	3.5
0	0	1	0	0	0	8	-72.2	2.5
0	0	0	1	1	1	7	-74.7	3.5
0	0	0	1	1	0	6	-78.3	2.5
0	0	0	1	0	1	5	-80.8	3.5
0	0	0	1	0	0	4	-84.3	2.5
0	0	0	0	1	1	3	-86.8	3.5
0	0	0	0	1	0	2	-90.3	2.5
0	0	0	0	0	1	1	-92.8	_
0	0	0	0	0	0	0 (MUTE)	-161.5	_

\*Default.

speaker lead length. Select the capacitor value based on EMC performance.

When doing bench evaluation without a filter or a ferrite bead filter, include a series inductor ( $68\mu H$  for  $8\Omega$  load) to model the actual loudspeaker's behavior. If this inductance is omitted, the MAX9768 will have reduced efficiency and output power, as well as worse THD+N performance.

#### **Inductor-Based Output Filters**

Some applications will use the MAX9768 with a full inductor-/capacitor-based (LC) output filter. This is common for longer speaker lead lengths, and to gain increased margin to EMC limits. Select the PWM output mode and use fixed-frequency modulation mode for best audio performance. See <a href="Figure 8">Figure 8</a> for the correct connections of these components.

The component selection is based on the load impedance of the speaker. <u>Table 8</u> lists suggested values for a variety of load impedances.

Inductors L3 and L4, and capacitor C15 form the primary output filter. In addition to these primary filter components, other components in the filter improve its functionality. Capacitors C13 and C14, plus resistors R6 and R7, form a Zobel at the output. A Zobel corrects the output load-

ing to compensate for the rising impedance of the loudspeaker. Without a Zobel, the filter will have a peak in its response near the cutoff frequency. Capacitors C11 and C12 provide additional high-frequency bypass to reduce radiated emissions.

### Adjustable Gain

### **Gain-Setting Resistors**

External feedback resistors set the gain of the MAX9768. The output stage has an internal 20dB gain in addition to the externally set gain. Set the maximum gain by using resistors  $R_F$  and  $R_{IN}$  (Figure 9) as follows:

$$A_V = -10 \left( \frac{R_F}{R_{IN}} \right) V / V$$

Choose  $R_F$  between  $10k\Omega$  and  $50k\Omega.$  Please note that the actual gain of the amplifier is dependent on the volume level setting. For example, with the volume control set to +9.5dB, the amplifier gain would be 9.5dB + 20dB, assuming  $R_F$  =  $R_{\rm IN}$ .

The input amplifier can be configured into a variety of circuits. The FB terminal is an actual operational amplifier output, allowing the MAX9768 to be configured as a summing amplifier, a filter, or an equalizer, for example.

**Table 7. Setting Class D Output Modulation Scheme** 

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	FUNCTION
1	1	0	1	0	1	0	1	Classic PWM
1	1	0	1	0	1	1	0	FILTERLESS MODULATION*

<sup>\*</sup>Power-on default.

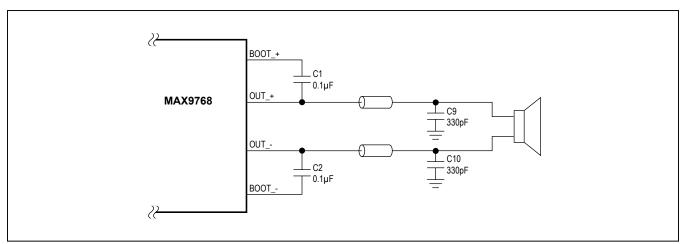


Figure 7. Ferrite Bead Filter

### **Power Supplies**

The MAX9768 has different supplies for each portion of the device, allowing for the optimum combination of headroom power dissipation and noise immunity. The speaker amplifiers are powered from PVDD and can range from 4.5V to 14V. The remainder of the device is powered by VDD. Power supplies are independent of each other so sequencing is not necessary. Power may be supplied by separate sources or derived from a single higher source using a linear regulator to reduce the voltage, as shown in Figure 10.

### **Component Selection**

#### **Input Filter**

An input capacitor,  $C_{IN}$ , in conjunction with the input resistor of the MAX9768 forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f - 3dB = \frac{1}{2\pi R_{IN}C_{IN}}$$

Choose  $C_{IN}$  so  $f_{-3dB}$  is well below the lowest frequency of interest. Use capacitors whose dielectrics have lowvoltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Other considerations when designing the input filter include the constraints of the overall system and the actual frequency band of interest. Although high-fidelity audio calls for a flat-gain response between 20Hz and 20kHz, portable voice-reproduction devices such as cellular phones and two-way radios need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 300Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

#### **BIAS Capacitor**

BIAS is the output of the internally generated DC bias voltage. The BIAS bypass capacitor,  $C_{BIAS}$ , improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node. Bypass BIAS with a  $2.2\mu F$  capacitor to GND.

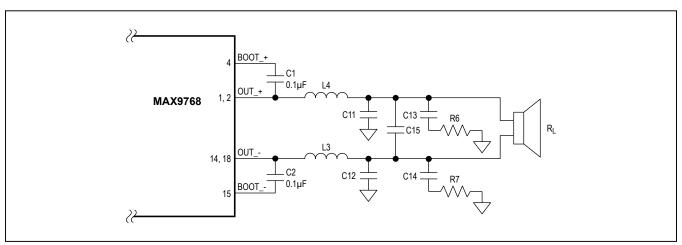


Figure 8. Output Filter for PWM Mode

Table 8. Suggested Values for LC filter

R <sub>L</sub> (Ω)	L3, L4 (µH)	C15 (µF)	C11, C12 (µF)	R6, R7 (Ω)	C13, C14 (µF)
6	15	0.33	0.01	7.5	0.68
8	22	0.22	0.01	10	0.47
12	33	0.1	0.01	15	0.33

# 10W Mono Class D Speaker Amplifier with Volume Control

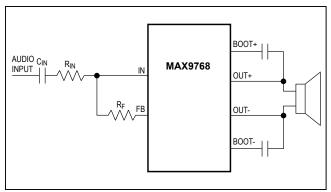


Figure 9. Setting Gain

## Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect PGND and GND together at a single point on the PCB. Route all traces that carry switching transients away from GND and the traces/components in the audio signal path.

# **Ordering Information**

PART	PIN-PACKAGE	t <sub>ON</sub> (ms)
MAX9768ETG+	24 TQFN-EP*	220
MAX9768BETG+	24 TQFN-EP*	15
MAX9768BETG/V+	24 TQFN-EP*	15

**Note:** All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package. /V Denotes an automotive-qualified part,

\*EP = Exposed pad.

# **Chip Information**

PROCESS: BICMOS

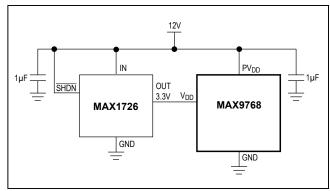


Figure 10. Using a Linear Regulator to Produce 3.3V from a 12V Power Supply

Bypass  $V_{DD}$  and  $PV_{DD}$  with a 1µF capacitor to PGND. Place the bypass capacitors as close to the MAX9768 as possible. Place a bulk capacitor between  $PV_{DD}$  and PGND, if needed.

Use large, low-resistance output traces. Current drawn from the outputs increase as load impedance decreases. High output trace resistance decreases the power delivered to the load. Large output, supply, and GND traces allow more heat to move from the MAX9768 to the air, decreasing the thermal impedance of the circuit if possible.

## **Package Information**

For the latest package outline information and land patterns (footprints), go to <a href="www.maximintegrated.com/packages">www.maximintegrated.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	DOCUMENT
TYPE	CODE	NO.
24 TQFN-EP	T2444+4	<u>21-0139</u>

## MAX9768

# 10W Mono Class D Speaker **Amplifier with Volume Control**

# **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/07	Initial release	_
1	3/08	Updated package outline	24, 25
2	11/08	Corrected various items	2, 4, 5, 11
3	12/17	Converted data sheet to new template; updated globals in <i>Electrical Characteristics</i> and <i>Typical Operating Characteristics</i> , and added new variant (MAX9768BETG/V+) to <i>Ordering Information</i>	1–25
4	7/19	Updated Table 6	18, 19

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.



Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

### Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



**«JONHON»** (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А