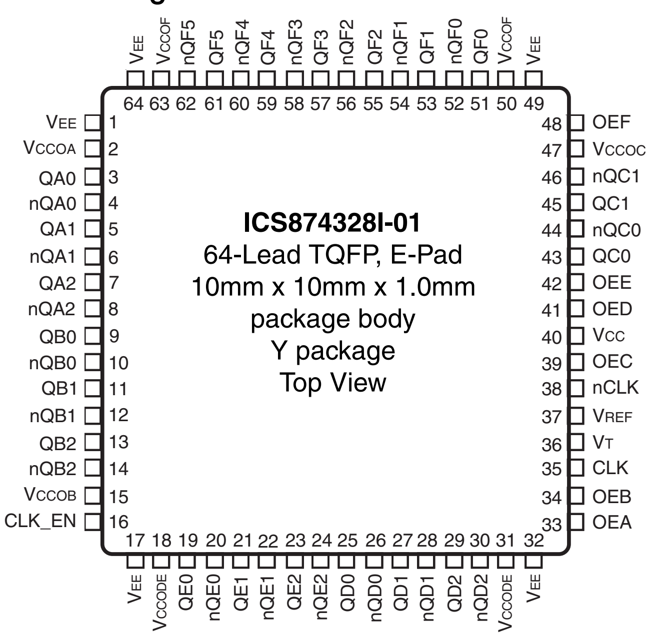
General Description

The 874328I-01 is a high-performance differential ÷1 and ÷4 clock divider and fanout buffer. The device is designed for the frequency-division and signal fanout of high-frequency, low phase-noise clock signals. The differential input signal is frequency divided by ÷1 and ÷4. Three LVPECL and three LVDS output banks are provided with a total of twenty differential outputs. The 874328I-01 is characterized to operate from a 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 874328I-01 ideal for those clock distribution applications demanding well-defined performance and repeatability.

Features

- One differential input LVPECL reference clock
- Differential pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Integrated input termination resistors
- One bank of three LVPECL outputs (÷1 frequency-divided)
- One bank of three LVPECL outputs (÷4 frequency-divided)
- One bank of two LVPECL outputs (÷4 frequency-divided)
- Two banks of three LVDS outputs (÷4 frequency-divided)
- One bank of six LVDS outputs (÷4 frequency-divided)
- Total of twenty differential clock outputs
- Maximum input frequency: 650MHz
- Maximum output frequency: 650MHz (÷1 outputs)
- Maximum output frequency: 162.5MHz (÷4 outputs)
- LVCMOS interface levels for all control inputs
- Output skew: 70ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Full 2.5V supply voltage
- Available in lead-free (RoHS 6) package
- -40°C to 85°C ambient temperature

Pin Assignment



Block Diagram

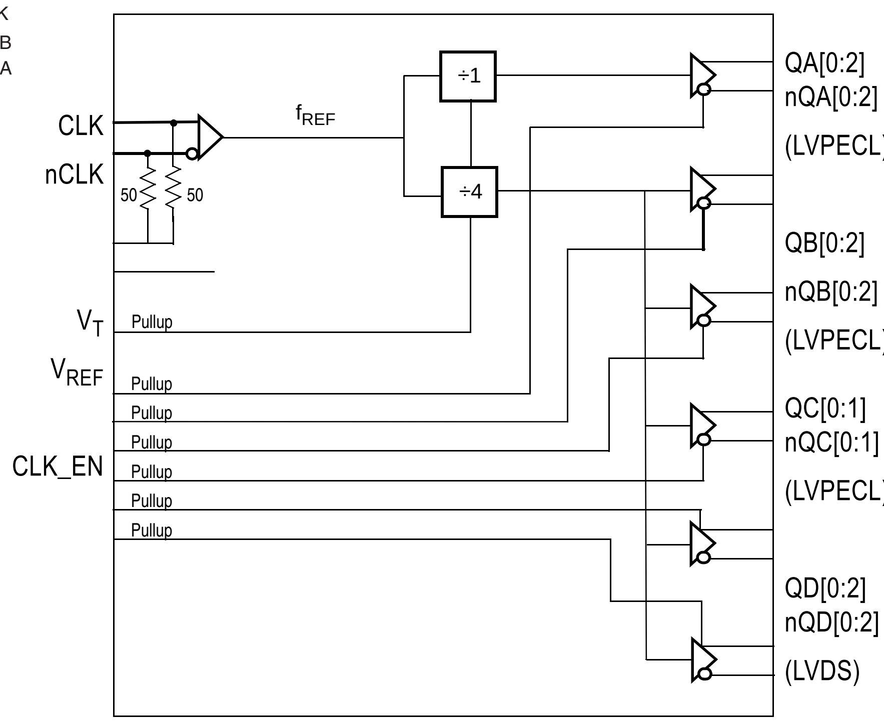


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 17, 32, 49, 64	V_{EE}	Power		Negative supply pins.
2	V_{CCOA}	Power		Output power supply for Bank A outputs.
3, 4	QA0, nQA0	Output		Differential Bank A output pair. LVPECL interface levels.
5, 6	QA1, nQA1	Output		Differential Bank A output pair. LVPECL interface levels.
7, 8	QA2, nQA2	Output		Differential Bank A output pair. LVPECL interface levels.
9, 10	QB0, nQB0	Output		Differential Bank B output pair. LVPECL interface levels.
11, 12	QB1, nQB1	Output		Differential Bank B output pair. LVPECL interface levels.
13, 14	QB2, nQB2	Output		Differential Bank B output pair. LVPECL interface levels.
15	V_{CCOB}	Power		Output power supply for Bank B outputs.
16	CLK_EN	Input	Pullup	Clock enable. See Table 3G for function. LVCMOS/LVTTL interface levels.
18, 31	V_{CCODE}	Power		Output power supply for Bank D and E outputs.
19, 20	QE0, nQE0	Output		Differential Bank E output pair. LVDS interface levels.
21, 22	QE1, nQE1	Output		Differential Bank E output pair. LVDS interface levels
23, 24	QE2, nQE2	Output		Differential Bank E output pair. LVDS interface levels
25, 26	QD0, nQD0	Output		Differential Bank D output pair. LVDS interface levels.
27, 28	QD1, nQD1	Output		Differential Bank D output pair. LVDS interface levels.
29, 30	QD2, nQD2	Output		Differential Bank D output pair. LVDS interface levels.
33	OEA	Input	Pullup	Output enable for Bank A outputs. See Table 3A for function. LVCMOS/LVTTL interface levels.
34	OEB	Input	Pullup	Output enable for Bank B outputs. See Table 3B for function. LVCMOS/LVTTL interface levels.
35	CLK	Input		Non-inverting differential LVPECL clock input.
36	V_T	Termination input		Input for termination. Both CLK and nCLK inputs are terminated to this pin. See input termination information in the applications section.
37	V_{REF}	Output		Reference voltage output. Provides a bias voltage of V_{CC} - 1.10V. Connect the V_{REF} output to V_T if the differential input pair CLK, nCLK is AC-coupled. Leave V_{REF} open if the differential input pair CLK, nCLK is DC-coupled. See input termination information in the applications section.
38	nCLK	Input		Inverting differential LVPECL clock input.
39	OEC	Input	Pullup	Output enable for Bank C outputs. See Table 3C for function. LVCMOS/LVTTL interface levels.
40	V_{CC}	Power		Power supply pin.
41	OED	Input	Pullup	Output enable for Bank D outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
42	OEE	Input	Pullup	Output enable for Bank E outputs. See Table 3E for function. LVCMOS/LVTTL interface levels.
43, 44	QC0, nQC0	Output		Differential Bank C output pairs. LVPECL interface levels.

Continued on next page.

Number	Name	Type		Description
45, 46	QC1, nQC1	Output		Differential Bank C output pair. LVPECL interface levels.
47	V_{CCOC}	Power		Output power supply for Bank C outputs.
48	OEF	Input	Pullup	Output enable for Bank F outputs. See Table 3F for function. LVCMOS/LVTTL interface levels.
50, 63	V_{CCOF}	Power		Output power supply for Bank F outputs.
51, 52	QF0, nQF0	Output		Differential Bank F output pair. LVDS interface levels.
53, 54	QF1, nQF1	Output		Differential Bank F output pair. LVDS interface levels.
55, 56	QF2, nQF2	Output		Differential Bank F output pair. LVDS interface levels.
57, 58	QF3, nQF3	Output		Differential Bank F output pair. LVDS interface levels.
59, 60	QF4, nQF4	Output		Differential Bank F output pair. LVDS interface levels.
61, 62	QF5, nQF5	Output		Differential Bank F output pair. LVDS interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. OEA Configuration Table

Input	
OEA	**Operation**
0	Outputs QAx/nQAx are in a high-impedance state.
1	Outputs are enabled. (Default)

NOTE: OEA is an asynchronous control.

Table 3B. OEB Configuration Table

Input	
OEB	**Operation**
0	Outputs QBx/nQBx are in a high-impedance state.
1	Outputs are enabled. (Default)

NOTE: OEB is an asynchronous control.

Table 3C. OEC Configuration Table

Input	
OEC	**Operation**
0	Outputs QCx/nQCx are in a high-impedance state.
1	Outputs are enabled. (Default)

NOTE: OEC is an asynchronous control.

Table 3D. OED Configuration Table

Input	
OED	**Operation**
0	Outputs QDx/nQDx are in a high-impedance state.
1	Outputs are enabled. (Default)

NOTE: OED is an asynchronous control.

Table 3E. OEE Configuration Table

Input	
OEE	**Operation**
0	Outputs QEx/nQEx are in a high-impedance state.
1	Outputs are enabled. (Default)

NOTE: OEE is an asynchronous control

Table 3F. OEF Configuration Table

Input	
OEF	**Operation**
0	Outputs QFx/nQFx are in a high-impedance state.
1	Outputs are enabled. (Default)

NOTE: OEF is an asynchronous control

Table 3G. CLK_EN Mode Configuration Table

Input	
CLK_EN	**Operation**
0	Output clock signals are disabled (logic low). Stops the output clock signals in a logic low state, and thus, eliminates potential output runt pulses.
1	Output clock signals are enabled. (Default)

NOTE: CLK_EN is synchronous to the falling edge of the input clock.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA 10mA 15mA
Input Current, CLK, nCLK	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	±2mA
Package Thermal Impedance, θ_{JA}	31.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCOA} = V_{CCOB} = V_{CCOC} = V_{CCODE} = V_{CCOF}$ = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{CCOX}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No Load		47	54	mA
I_{CCOX}	Output Supply Current	No Load		139	160	mA

V_{CCOX} denotes V_{CCOA}, V_{CCOB}, V_{CCOC}, V_{CCODE}, V_{CCOF}.
I_{CCOX} denotes I_{CCODE}, I_{CCOF}.

Table 4B. LVCMOS/LVTTL Input DC Characteristics, V_{CC} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN OEA, OEB, OEC, OED, OEE, OEF	$V_{CC} = V_{IN}$ = 2.625V			5	µA
I_{IL}	Input Low Current	CLK_EN OEA, OEB, OEC, OED, OEE, OEF	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA

Table 4D. Differential LVPECL Input DC Characteristics, V_{CC} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	CLK, nCLK	CLK-to-VT, nCLK-to-VT	40	50	60	Ω
V_{IH}	Input High Voltage	CLK, nCLK		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	CLK, nCLK		0		V_{IH} – 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_{IN_CLK}	Input Current; NOTE 2	CLK, nCLK				35	mA
V_{REF_AC}	Reference Voltage			V_{CC} – 1.4	V_{CC} – 1.0	V_{CC} – 0.80	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Guaranteed by design.

Table 4E. LVPECL DC Characteristics, V_{CC} = V_{CCOA} = V_{CCOB} = V_{CCOC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} – 1.4		V_{CCO} – 0.8	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} – 2.0		V_{CCO} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.

Table 4F. LVDS DC Characteristics, V_{CC} = V_{CCODE} = V_{CCOF} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		240	380	520	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.00	1.35	1.70	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

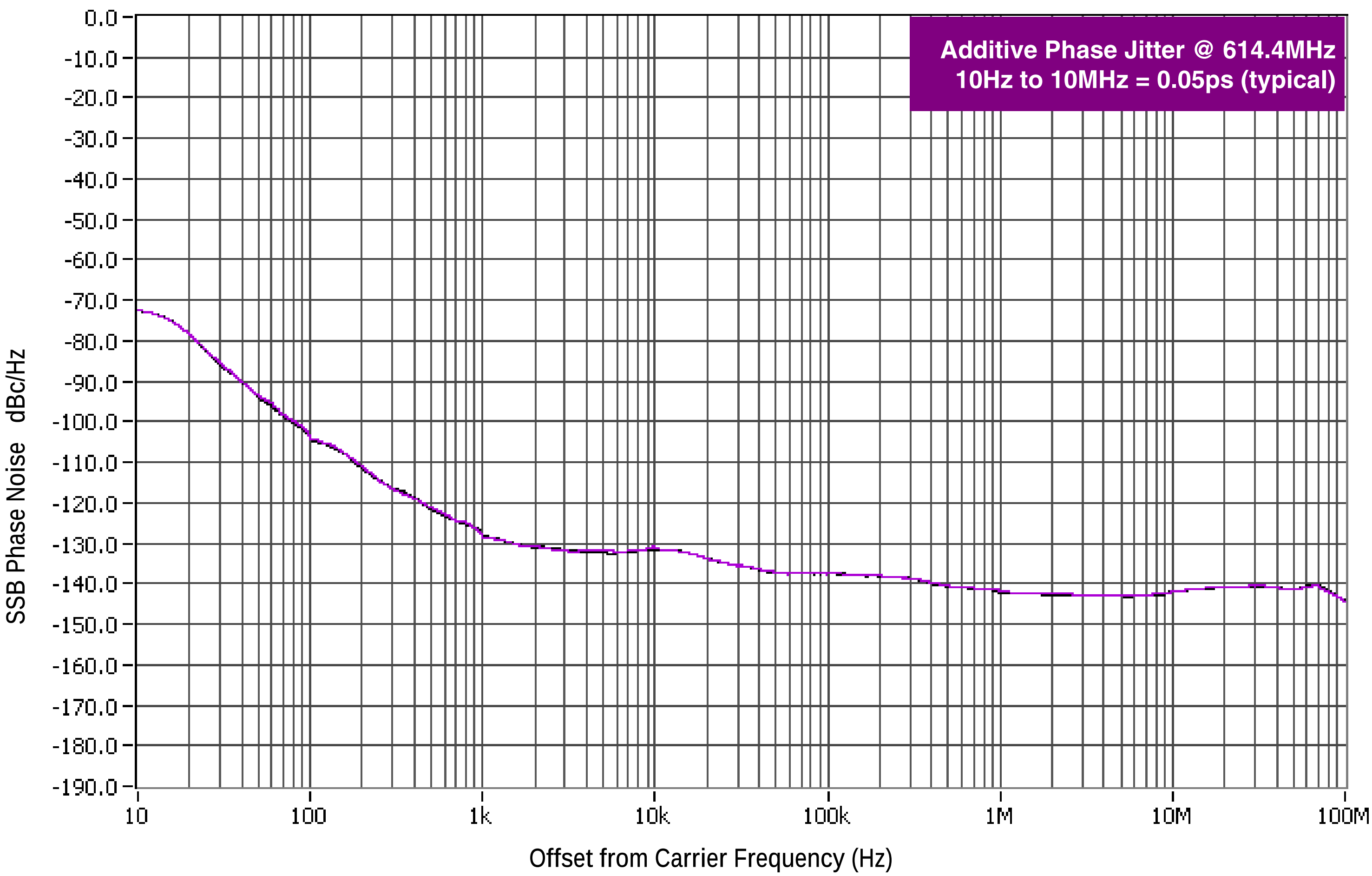
Table 5. AC Electrical Characteristics, V_{CC} = V_{CCOA} = V_{CCOB} = V_{CCOC} = = V_{CCODE} = V_{CCOF} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency				614.4	650	MHz
f_{OUT}	Output Frequency	QA[0:2]			614.4	650	MHz
		Q[Bx:Fx]			153.6	162.5	MHz
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		f_{REF} = 614.4MHz, Integration Range: 10Hz – 10MHz		0.05		ps
t_{PD}	Propagation Delay; NOTE 1		CLK to any QA, QB or QC output	1.2		4.2	ns
			CLK to any QD, QE or QF output	2.0		4.8	ns
*t*sk(b)	Bank Skew; NOTE 2, 3		Within each output Bank			65	ps
*t*sk(o)	Output Skew; NOTE 3, 4		Across output Banks QA, QB and QC			50	ps
			Across output Banks QD, QE and QF			65	ps
			Across all output Banks QA to QF			70	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5		Within each output bank			250	ps
odc	Output Duty Cycle	QA[0:2]		45		55	%
		Q[Bx:Fx]		48		52	%
t_R / t_F	Output Rise/ Fall Time	QA[0:2]	20% to 80%	200		400	ps
		Q[Bx:Fx]	20% to 80%	300		600	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the differential cross points.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

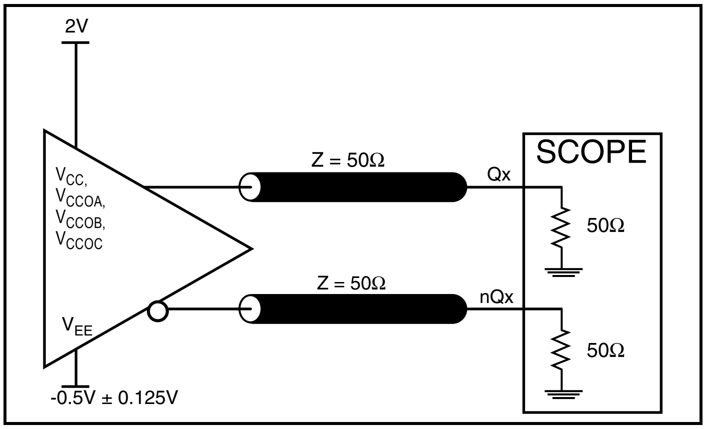
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



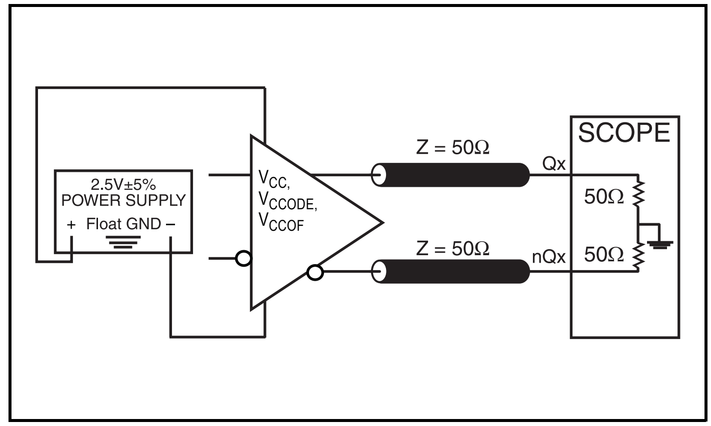
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator.

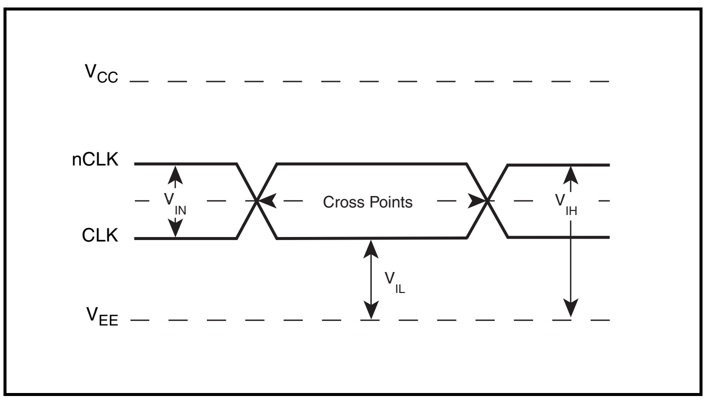
Parameter Measurement Information



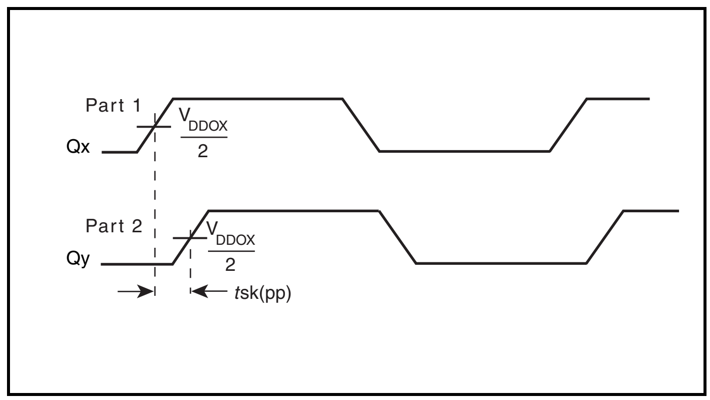
LVPECL Output Load AC Test Circuit



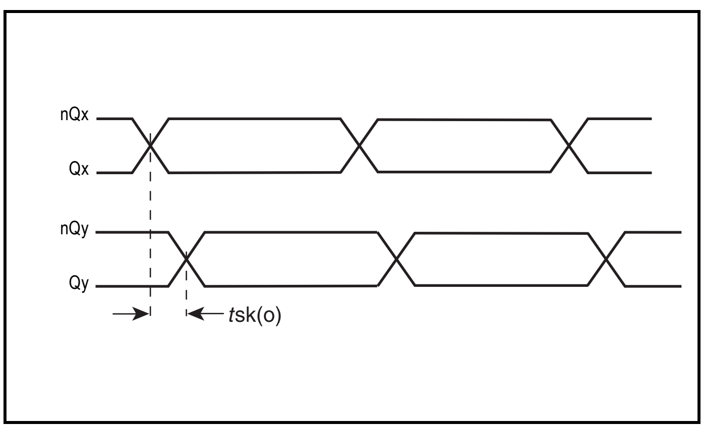
LVDS Output Load AC Test Circuit



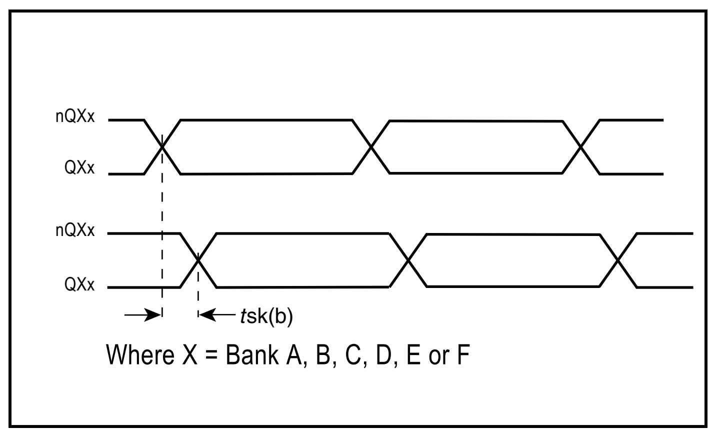
Differential Input Level



Part-to-Part Skew

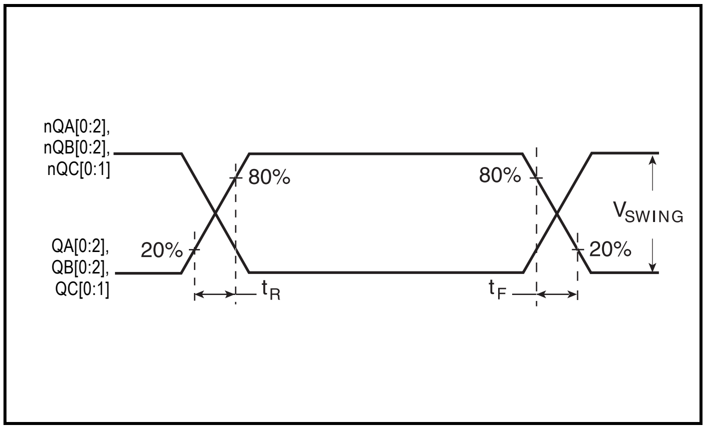


Output Skew

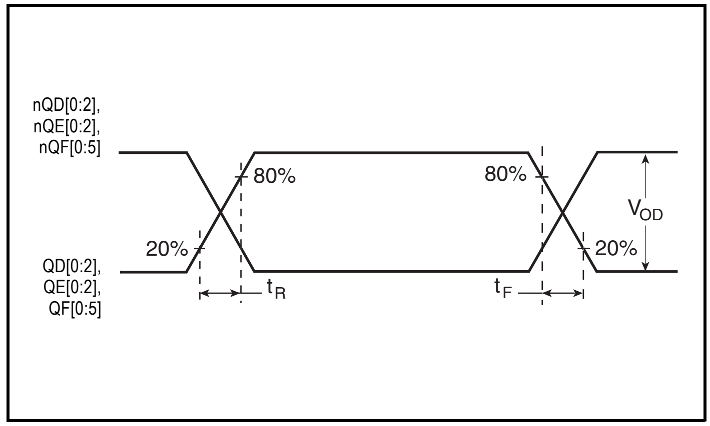


Bank Skew

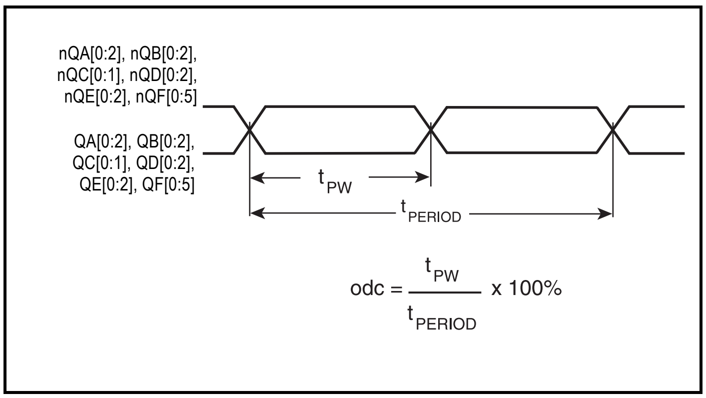
Parameter Measurement Information, continued



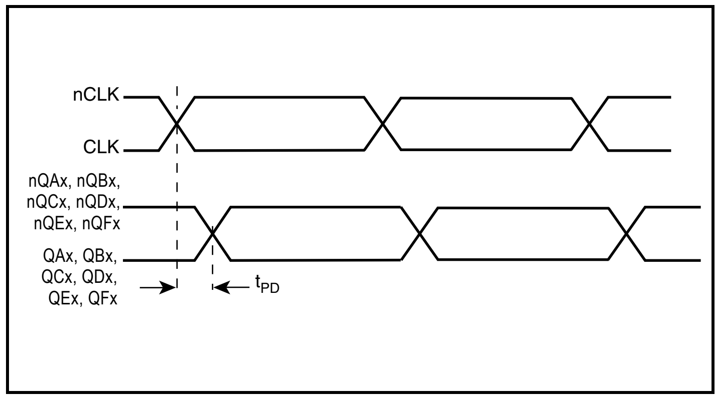
LVPECL Output Rise/Fall Time



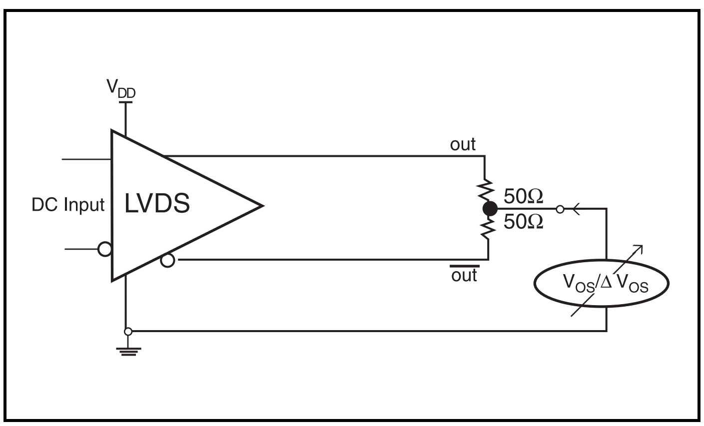
LVDS Output Rise/Fall Time



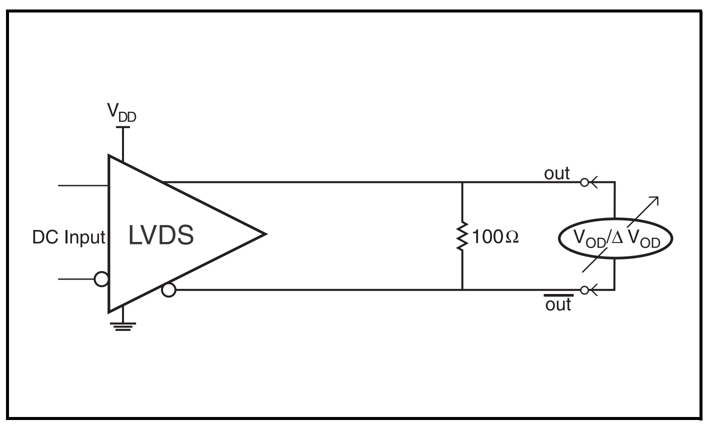
Output Duty Cycle/Pulse Width/Period



Propagation Delay



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

Differential LVPECL Clock Input Interface

The CLK/nCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

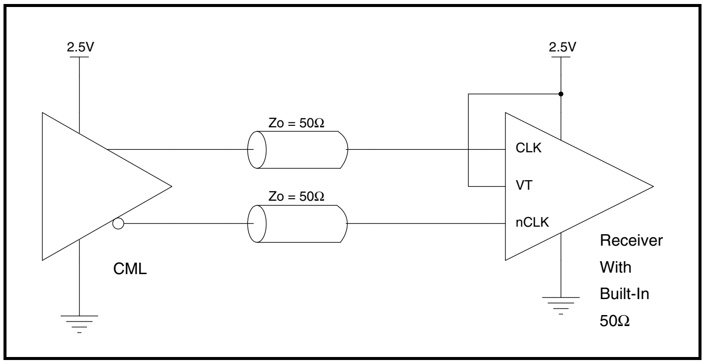


Figure 2A. CLK/nCLK Input with Built-In 50Ω Driven by a CML Driver

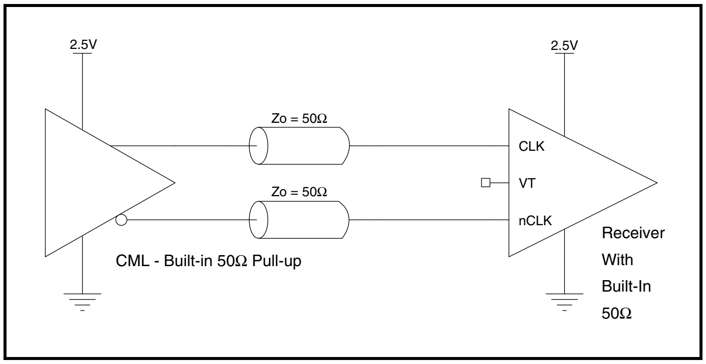


Figure 2B. CLK/nCLK Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

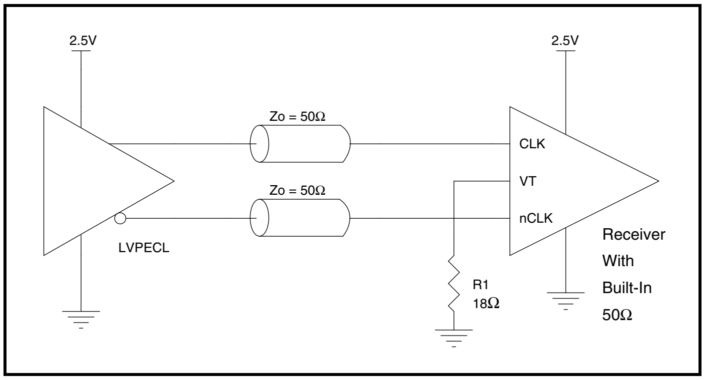


Figure 2C. CLK/nCLK Input with Built-In 50Ω Driven by an LVPECL Driver

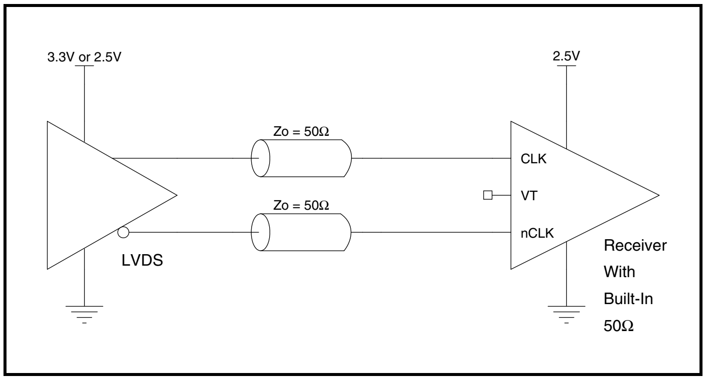


Figure 2D. CLK/nCLK Input with Built-In 50Ω Driven by an LVDS Driver

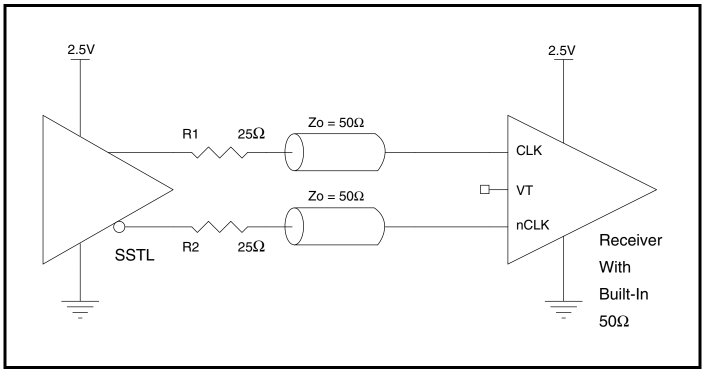


Figure 2E. CLK/nCLK Input with Built-In 50Ω Driven by an SSTL Driver

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

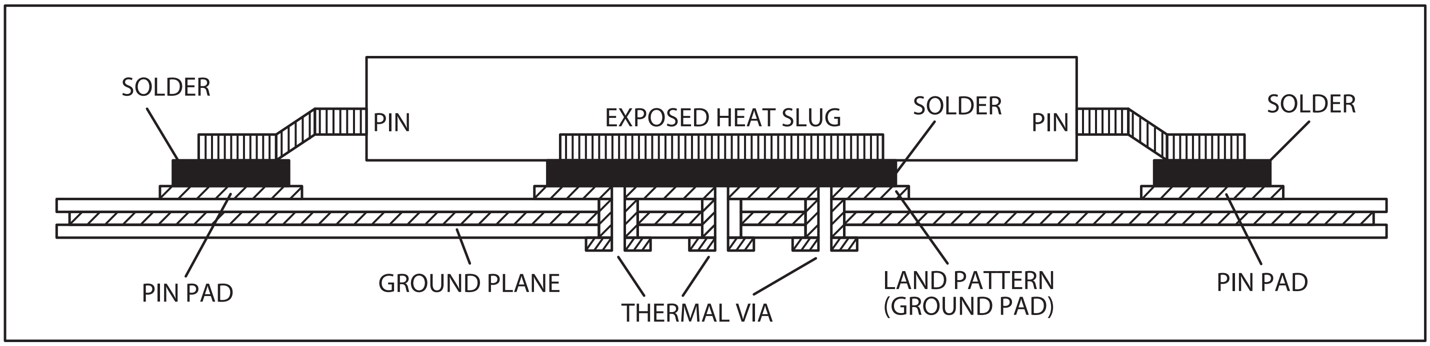


Figure 3. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

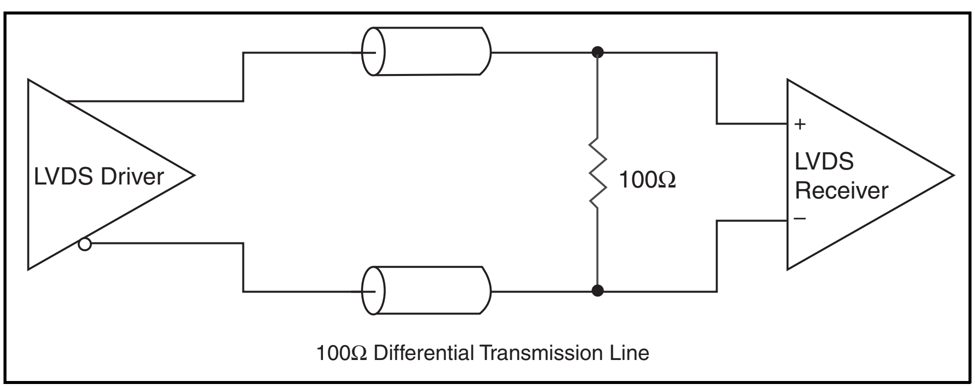


Figure 4. Typical LVDS Driver Termination

Termination for LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

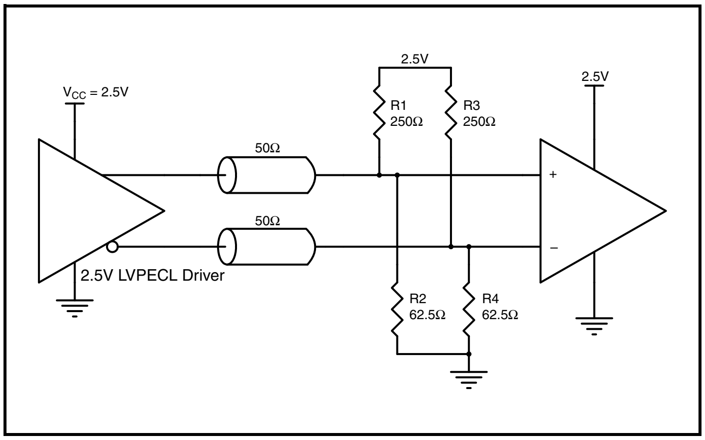


Figure 5A. 2.5V LVPECL Driver Termination Example

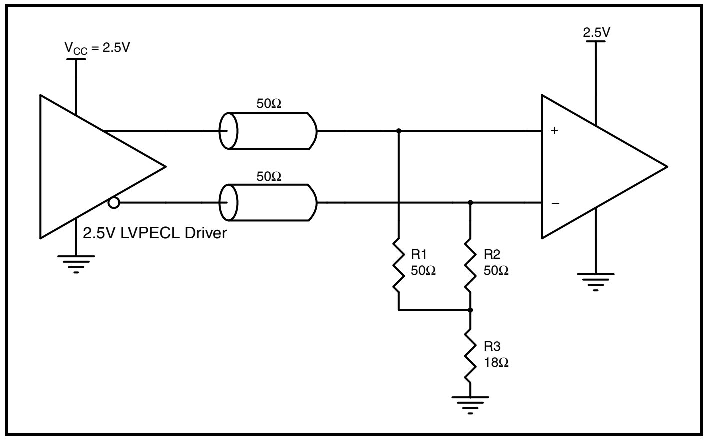


Figure 5B. 2.5V LVPECL Driver Termination Example

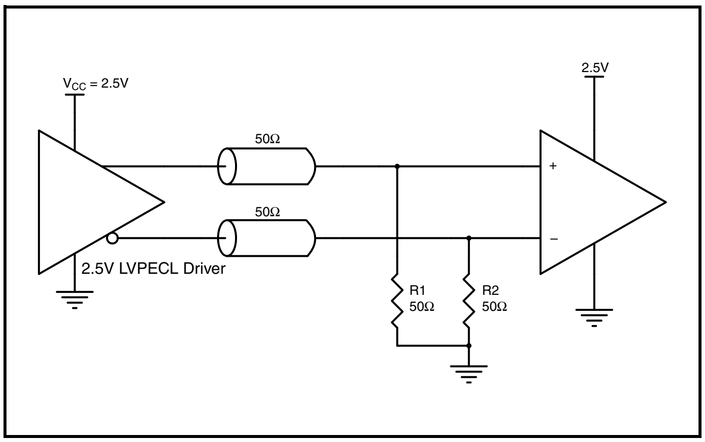


Figure 5C. 2.5V LVPECL Driver Termination Example

Power Considerations (typical)

This section provides information on power dissipation and junction temperature for the 874328I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 874328I-01 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 2.5V + 5% = 2.625V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{TYP}$ = V_{CC_TYP} * I_{CC_TYP} = 2.5V * 47mA = **117.5mW**
- $Power(LVDS)_{TYP}$ = $V_{CCO\_DEF\_TYP}$ * $I_{CCO\_DEF\_TYP}$ = 2.5V * 139mA = **347.5mW**
- Power (LVPECL) = **29.4mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 29.4mW = **235.2mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{TYP}$ = $(V_{IN\_TYP})^2$ / R_{T_TYP} = $(0.675V)^2$ / 100Ω = **4.56mW**

Total Power$_{\_TYP}$ = 117.5mW + 347.5mW + 4.56mW + 235.2mW = **704.76mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 31.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.705W * 31.8°C/W = 107°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 64 Lead TQFP, E-Pad, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 6.*

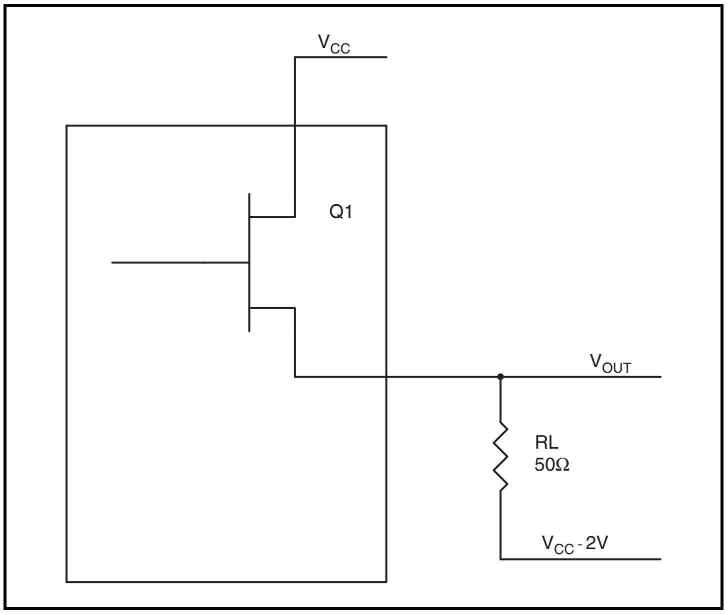


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V =$ **19.2mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **29.4mW**

Power Considerations (maximum)

This section provides information on power dissipation and junction temperature for the 874328I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 874328I-01 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 2.5V + 5% = 2.625V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX}$ = V_{CC_MAX} * I_{CC_MAX} = 2.625V * 54mA = **141.75mW**
- $Power(LVDS)_{MAX}$ = $V_{CCO\_DEF\_MAX}$ * $I_{CCO\_DEF\_MAX}$ = 2.625V * 160mA = **420mW**
- Power (LVPECL) = **29.4mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 29.4mW = **235.2mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX}$ = $(V_{IN\_MAX})^2$ / R_{T_MIN} = $(1.2V)^2$ / 80Ω = **18mW**

Total Power$_{\_MAX}$ = 141.75mW + 420mW + 235.2mW + 18mW = **814.95mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 31.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.815W * 31.8°C/W = 111°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 64 Lead TQFP, E-Pad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 7.*

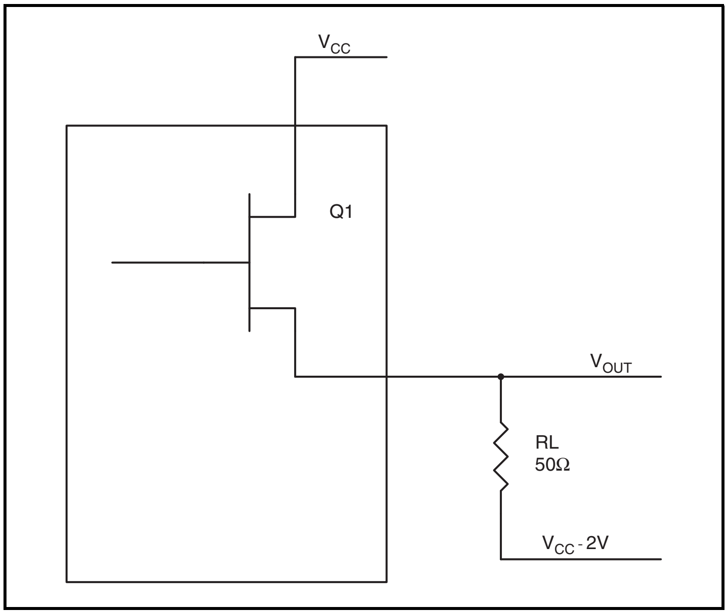


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V = \mathbf{19.2mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **29.4mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 64 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

Transistor Count

The transistor count for 874328I-01 is: 1453

Package Outline and Package Dimensions

Package Outline - Y Suffix for 64 Lead TQFP, E-Pad

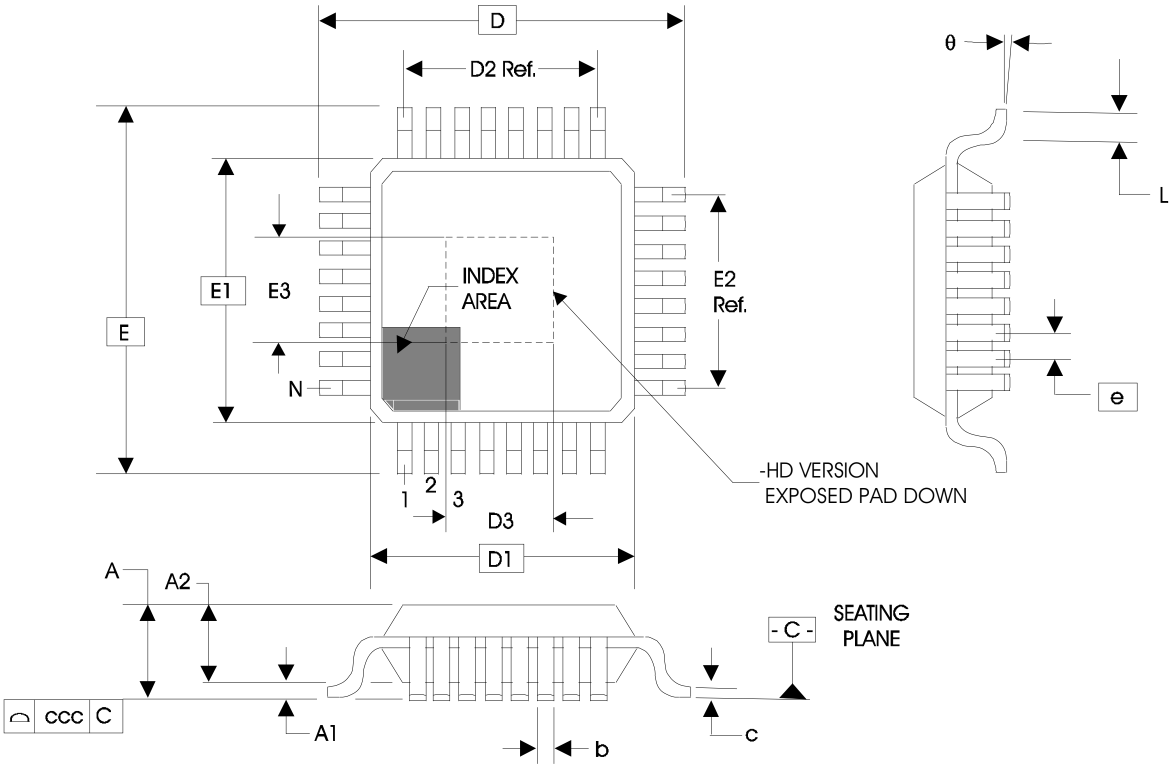


Table 9. Package Dimensions for 64 Lead TQFP, E-Pad

JEDEC Variation: ACD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		64	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E		12.00 Basic	
D1 & E1		10.00 Basic	
D2 & E2		7.50 Ref.	
D3 & E3	4.5		5.5
e		0.50 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874328BYI-01LF	ICS874328BI01L	Lead-Free, 64 Lead TQFP, E-Pad	Tray	-40°C to 85°C
874328BYI-01LFT	ICS874328BI01L	Lead-Free, 64 Lead TQFP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History

]

Revision Date	Description of Change
January 27, 2016	▪ Removed ICS from part numbers where needed. ▪ General Description - Deleted ICS chip. ▪ Ordering Information - Deleted quantity from tape and reel. Deleted LF note below table. ▪ Updated header and footer.

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