NEW PRODUCT

APR343

SECONDARY SIDE SYNCHRONOUS RECTIFICATION CONTROLLER

Description

APR343 is a secondary side MOSFET driver for synchronous rectification in DCM operation, which integrates the output voltage detection function for primary side control system.

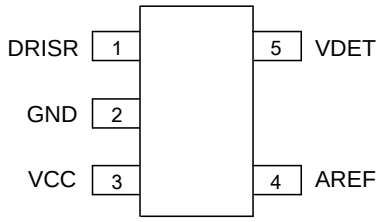
The synchronous rectification can effectively reduce the secondary side rectifier power dissipation and provide high performance solution. By sensing MOSFET drain-to-source voltage, APR343 can output ideal drive signal with less external components. It can provide high performance solution for 5V output voltage application.

Same as AP4341, APR343 detects the output voltage and provides a periodical signal when the output voltage is lower than a certain threshold. By fast response to secondary side voltage, APR343 can effectively improve the transient performance of primary side control system.

The APR343 is available in SOT25 package.

Pin Assignments

(Top View)



SOT25

Features

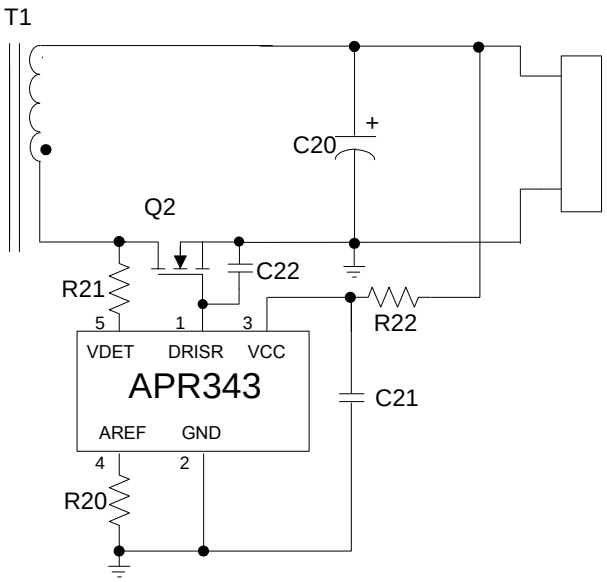
- Synchronous Rectification for DCM Operation Flyback
- Eliminate Resonant Ring Interference
- Fast Detector of Supply Voltage
- Fewest External Components
- **Totally Lead-free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Adapters/Chargers for Cell/Cordless Phones, ADSL Modems, MP3 and Other Portable Apparatus
- Standby and Auxiliary Power Supplies

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



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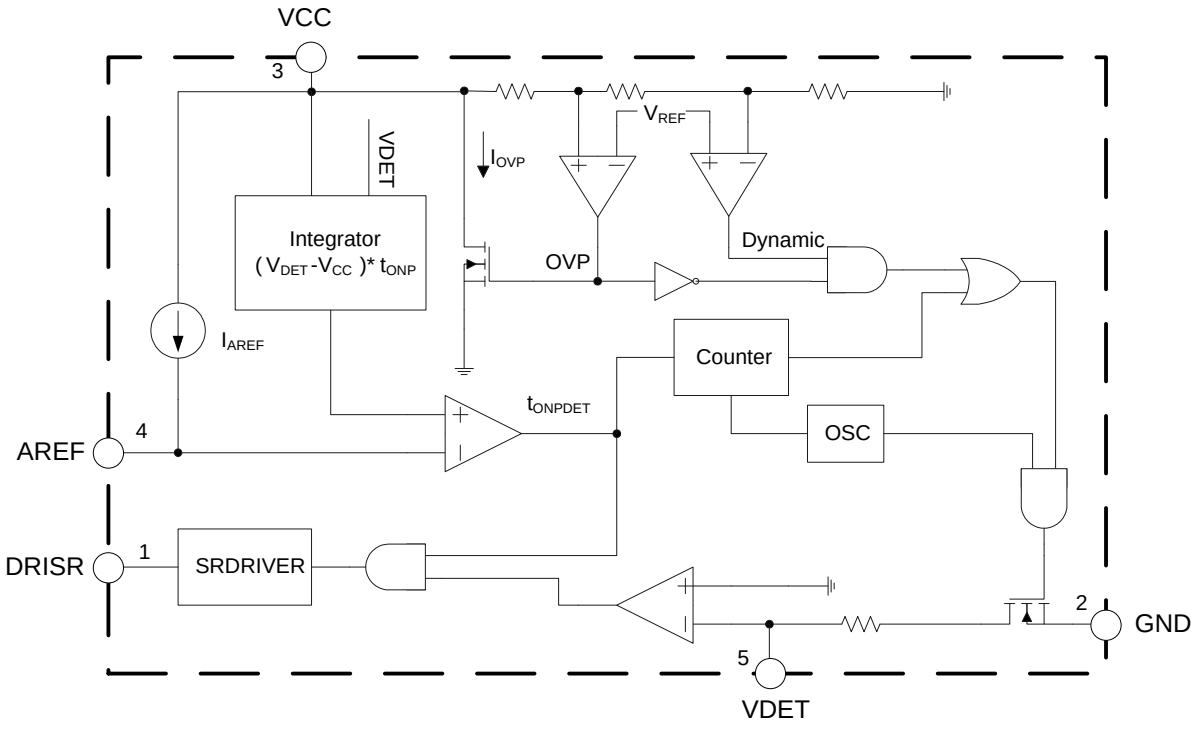
Pin Descriptions

Pin Number	Pin Name	Function
1	DRISR	Synchronous rectification MOSFET Gate drive
2	GND	Ground
3	VCC	Power supply, connected with system output
4	AREF	Program a voltage reference with a resistor from AREF to GND, to enable synchronous rectification MOSFET drive signal
5	VDET	Synchronous rectification sense input and dynamic function output, connected with secondary winding

Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to 7.5	V
V_{DET}	Voltage at VDET Pin	-2 to 50	V
V_{AREF}, V_{DRISR}	Voltage at AREF, DRISR Pin	-0.3 to 6	V
–	Output Current at VDET	Internally limited	A
P_D	Power Dissipation at T_A = +25ºC	0.6	W
T_J	Operating Junction Temperature	+150	ºC
T_{STG}	Storage Temperature	-65 to +150	ºC
–	Lead Temperature (Soldering, 10 sec)	+300	ºC
θ_{JA}	Thermal Resistance (Junction to Ambient)	197	ºC/W
θ_{JC}	Thermal Resistance (Junction to Case)	76	ºC/W

Note 4: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	0	6	V
T_A	Ambient Temperature	-40	+85	ºC

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Electrical Characteristics (@V_{CC} = 5V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
$I_{STARTUP}$	Startup Current	V_{CC} = $V_{STARTUP}$-0.1V	–	100	150	μA
I_{OP}	Operating Current	VDET pin floating V_{CC} = $V_{TRIGGER}$+20mV	40	100	150	μA
$V_{STARTUP}$	Startup Voltage	–	2.6	3.1	3.4	V
–	UVLO	–	2.3	2.8	3.1	V
Dynamic Output Section/Oscillator Section						
$V_{TRIGGER}$	Internal Trigger Voltage	–	5.25	5.3	5.35	V
–	Duty Cycle	–	4	8	12	%
t_{OSC}	Oscillation Period	V_{CC} = 5V	18	30	37.5	μs
$I_{TRIGGER}$	Internal Trigger Current	V_{CC} = $V_{TRIGGER}$, VCC/VDET pin is separately connected to a 20Ω resistor	30	–	42	mA
t_{DIS}	Minimum Period	–	18	30	37.5	ms
V_{DIS}	Discharge Voltage	–	5.28	5.44	5.52	V
I_{DIS}	Discharge Current	V_{CC} = V_{DIS}+0.1V	1.5	3	4.5	mA
V_{DIS}-$V_{TRIGGER}$	Trigger Discharger Gap	–	30	110	–	mV
V_{OVP}	Overshoot Voltage for Discharge	–	5.8	5.9	6.0	V
I_{OVP}	Overshoot Current for Discharge	V_{CC} = V_{OVP}+0.1V, VCC pin is connected to a 20Ω resistor	40	–	100	mA
Synchronous Rectification Detection and Drive						
V_{THON}	Gate Turn On Threshold	–	0	–	1	V
V_{THOFF}	Gate Turn Off Threshold	–	-20	-12.5	-5	mV
t_{DON}	Turn On Delay Time	From V_{THON} to V_{DRISR} = 1V	–	70	130	ns
t_{DOFF}	Turn Off Propagation Delay Time	From V_{THOFF} to V_{DRISR} = 3V	–	100	150	ns
t_{RG}	Turn On Rising Time	From 1V to 3V, C_L = 4.7nF	–	50	100	ns
t_{FG}	Turn Off Falling Time	From 3V to 1V, C_L = 4.7nF	–	50	100	ns
t_{LEB_S}	Minimum On Time	(V_{DET}-V_{CC})*t_{ONP} = 25Vμs	0.9	1.8	2.7	μs
t_{LEB_L}		(V_{DET}-V_{CC})*t_{ONP} = 50Vμs	–	–	6.5	
V_{DRISR_HIGH}	Drive Output Voltage	V_{CC} = 5V	3.7	–	–	V
V_{S_MIN}	Synchronous Rectification (SR) Minimum Operating Voltage (Note 5)	–	–	–	4.5	V
t_{OVP_LAST}	Added OVP Discharge Time	–	–	2.0	–	ms
Kqs	(Note 6)	(V_{DET}-V_{CC})*t_{ONP} = 25Vμs	0.325	–	0.625	mA*μs

Notes: 5. This item specifies the minimum SR operating voltage of V_{IN_DC}, $V_{IN\_DC} \geq N_{PS} * V_{S\_MIN}$.
6. This item is used to specify the value of R_{AREF}.

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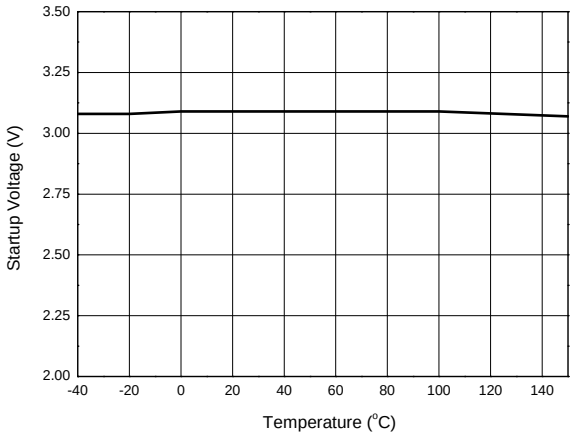
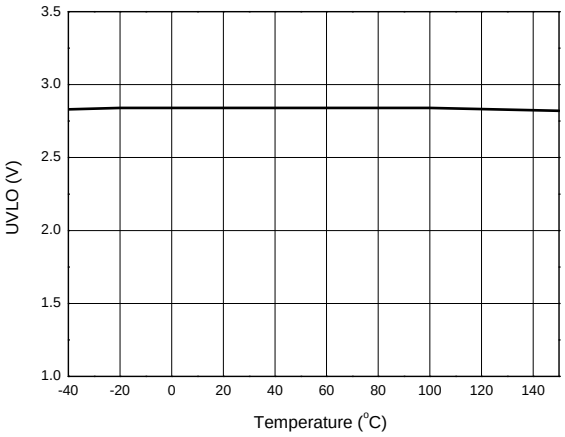
Performance Characteristics

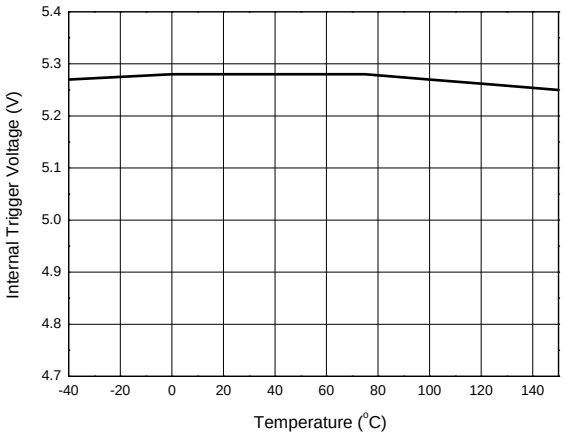
Startup Voltage vs. Temperature



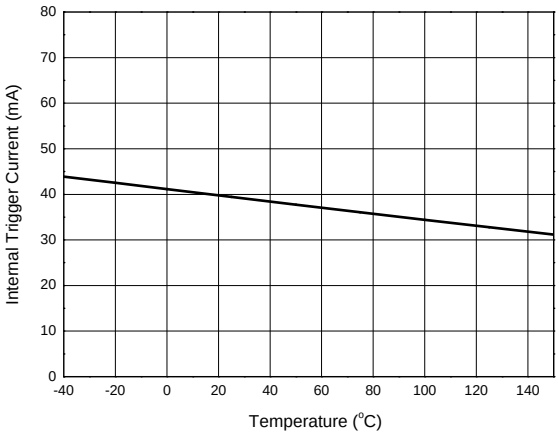
UVLO vs. Temperature



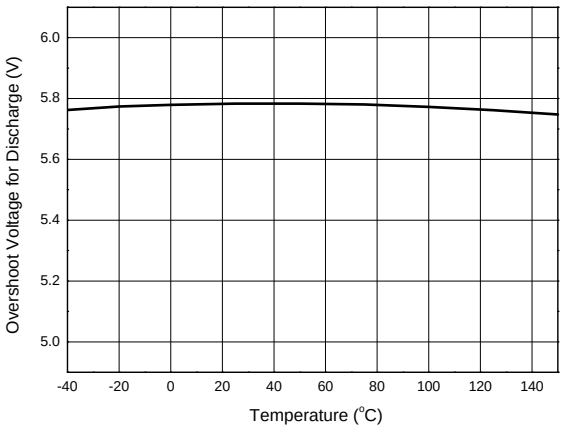
Internal Trigger Voltage vs. Temperature



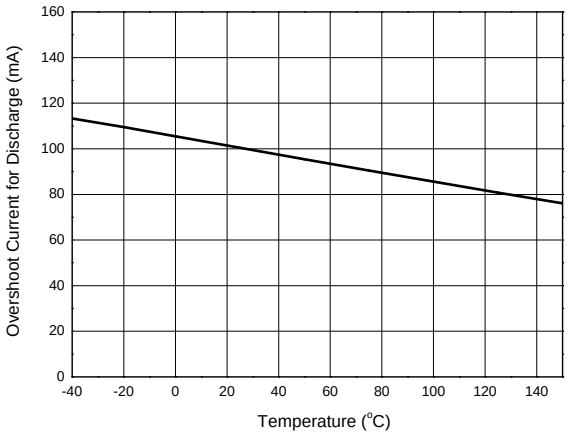
Internal Trigger Current vs. Temperature



Overshoot Voltage for Discharge vs. Temperature



Overshoot Current for Discharge vs. Temperature



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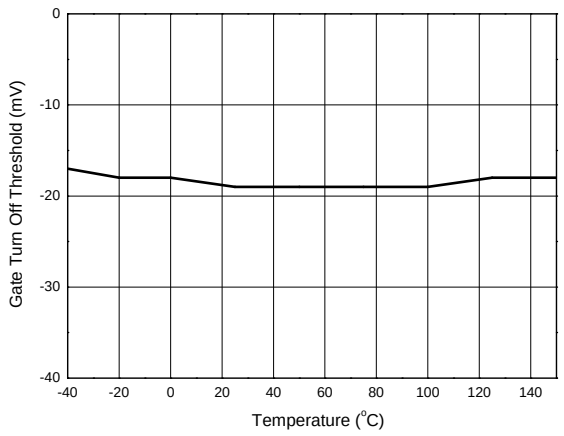
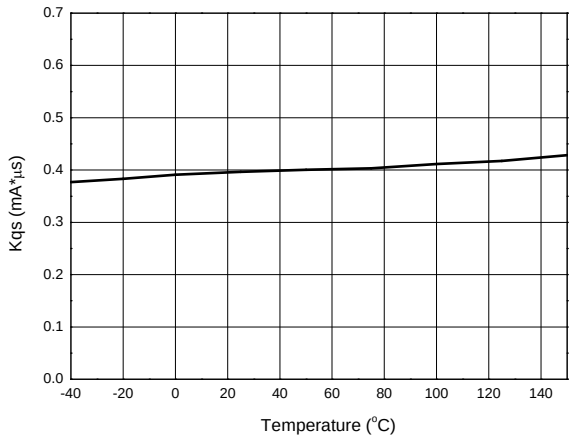
Performance Characteristics (Cont.)

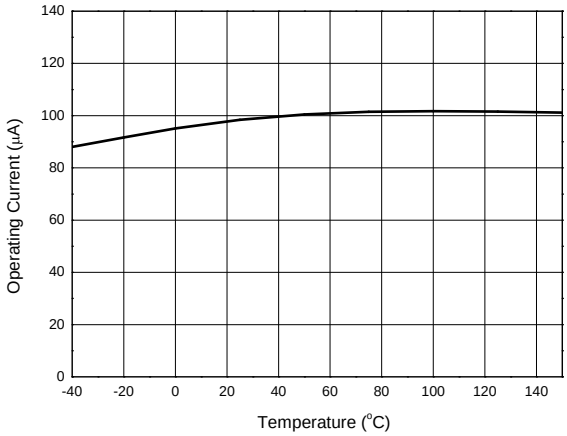
Gate Turn Off Threshold vs. Temperature



Kqs (See Note 6) vs. Temperature



Operating Current vs. Temperature



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Output Voltage Detection Function Description

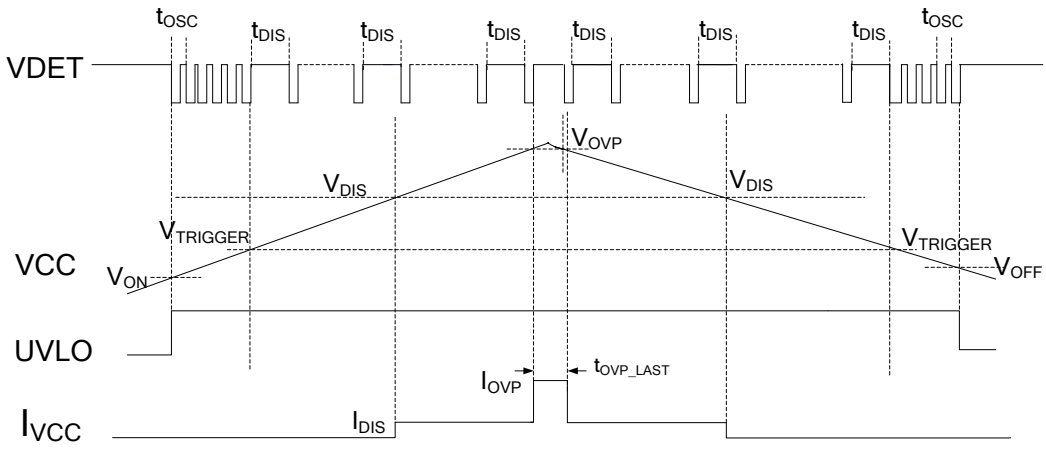

Figure 1. Typical Waveforms 1 of APR343

When V_{CC} is beyond power-on voltage (V_{ON}), the APR343 starts up. The VDET pin asserts a periodical pulse and the oscillation period is t_{OSC}. When V_{CC} is beyond the trigger voltage ($V_{TRIGGER}$), the periodical pulse at VDET pin is discontinued. When V_{CC} is beyond the discharge voltage (V_{DIS}), the discharge circuit will be enabled, and a 3mA current (I_{DIS}) will flow into VCC pin. When V_{CC} is higher than the overshoot voltage (V_{OVP}), the APR343 will enable a discharge circuit, the discharge current (I_{OVP}) will last t_{OVP_LAST} time. After the t_{OVP_LAST} time, APR343 will stop the discharge current and detect VCC voltage again. If V_{CC} is still higher than V_{OVP}, the t_{OVP_LAST} time discharge current will be enabled again. Once the OVP discharge current is asserted, the periodical pulse at VDET pin will be disabled.

When the V_{CC} is below the power-off voltage (V_{OFF}), the APR343 will be shut down.

MOSFET Driver Operation Description

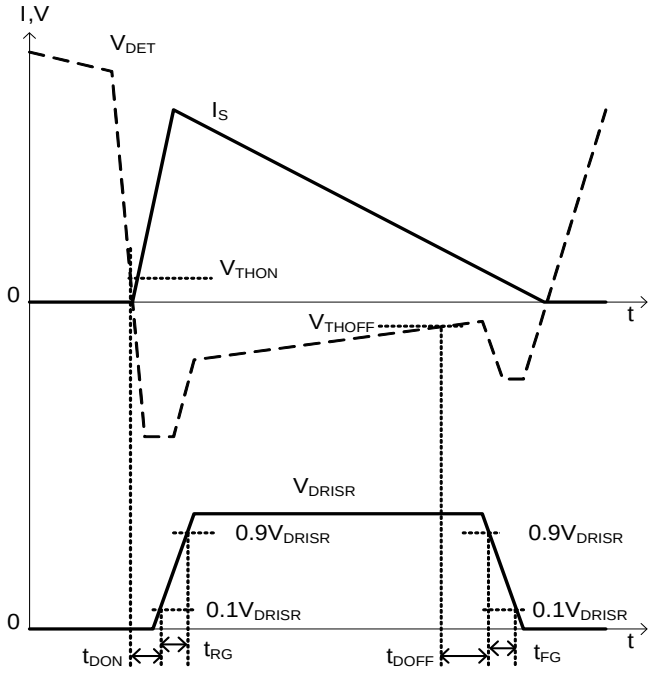

Figure 2. Typical Waveforms 2 of APR343

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MOSFET Driver Operation Description (Cont.)

The operation of the SR is described with timing diagram shown in Figure 2. APR343 monitors the MOSFET drain-source voltage. When the drain voltage is lower than the turn-on threshold voltage V_{THON}, the IC outputs a positive drive voltage after a turn-on delay time (t_{DON}). The MOSFET will turn on and the current will transfer from the body diode into the MOSFET's channel.

In the process of drain current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage V_{THOFF}, APR343 pulls the drive signal down after a turn off delay (t_{DOFF}).

Minimum On Time

When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the V_{THOFF} comparator, keeping the controlled MOSFET on for at least the minimum on time. If V_{THOFF} falls below the threshold before minimum on time expires, the MOSFET will keep on until the end of the minimum on time.

The minimum on time is in direct proportion to the $(V_{DET}-V_{CC})*t_{ONP}$. When $(V_{DET}-V_{CC})*t_{ONP}=5V*5\mu s$, the minimum on time is about 1.8µs.

The Value and Meaning of AREF Resistor

As to DCM operation Flyback converter, after secondary rectifier stops conduction the primary MOSFET Drain-to-source ringing waveform is resulted from the resonant of primary inductance and equivalent switch device output capacitance. This ringing waveform probably leads to Synchronous Rectifier error conduction. To avoid this fault happening, APR343 has a special function design by means of volt-second product detecting. From the sensed voltage of VDET pin to see, the volt-second product of voltage above V_{CC} at primary switch on time is much higher than the volt-second product of each cycle ringing voltage above $V_{CC.}$ Therefore, before every time Synchronous Rectifier turning on, APR343 judges if the detected volt-second product of VDET voltage above V_{CC} is higher than a threshold and then turn on synchronous Rectifier. The purpose of AREF resistor is to determine the volt-second product threshold. APR343 has a parameter, Kqs, which converts R_{AREF} value to volt-second product.

$$Area2 = R_{AREF} * Kqs$$

In general, Area1 and Area3 value depend on system design and always are fixed after system design frozen. As to BCD PSR design, the Area1 value changes with primary peak current value and Area3 value generally keeps constant at all of conditions. So the AREF resistor design should consider the worst case, the minimum primary peak current condition. Since of system design parameter distribution, Area1 and Area3 have moderate tolerance. So Area2 should be designed between the middle of Area1 and Area3 to keep enough design margin.

$$Area3 < R_{AREF} * Kqs < Area1$$

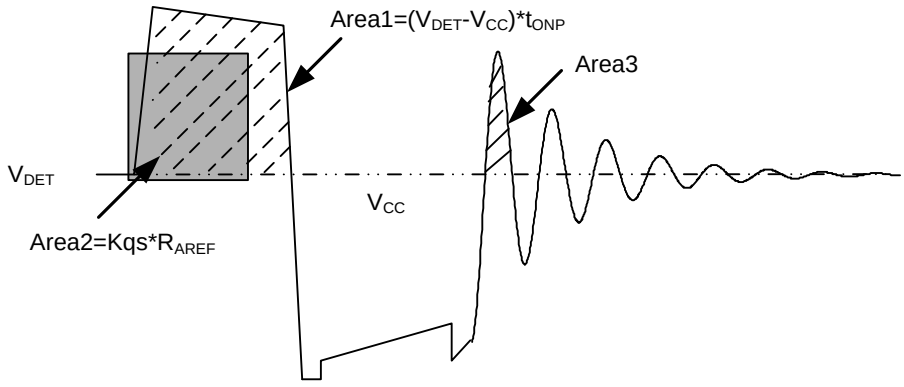


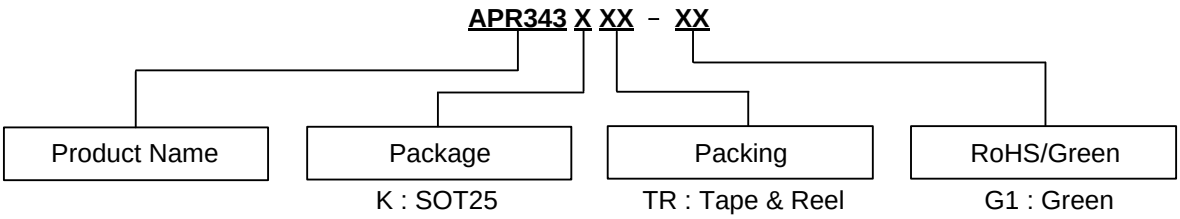
Figure 3. AREF Function

SR Minimum Operating Voltage

APR343 sets a minimum SR operating voltage by comparing the difference between V_{DET} and output voltage (V_{CC}). The value of V_{DET}–V_{CC} must be higher than its internal reference, then APR343 will begin to integrate the area of $(V_{DET}–V_{CC})*t_{ONP}$. If not, the area integrating will not begin and the SR driver will be disabled.

NEW PRODUCT

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
SOT25	-40°C to +85°C	APR343KTR-G1	GHZ	3000/Tape & Reel

Marking Information

(Top View)

: Logo
GHZ: Marking ID

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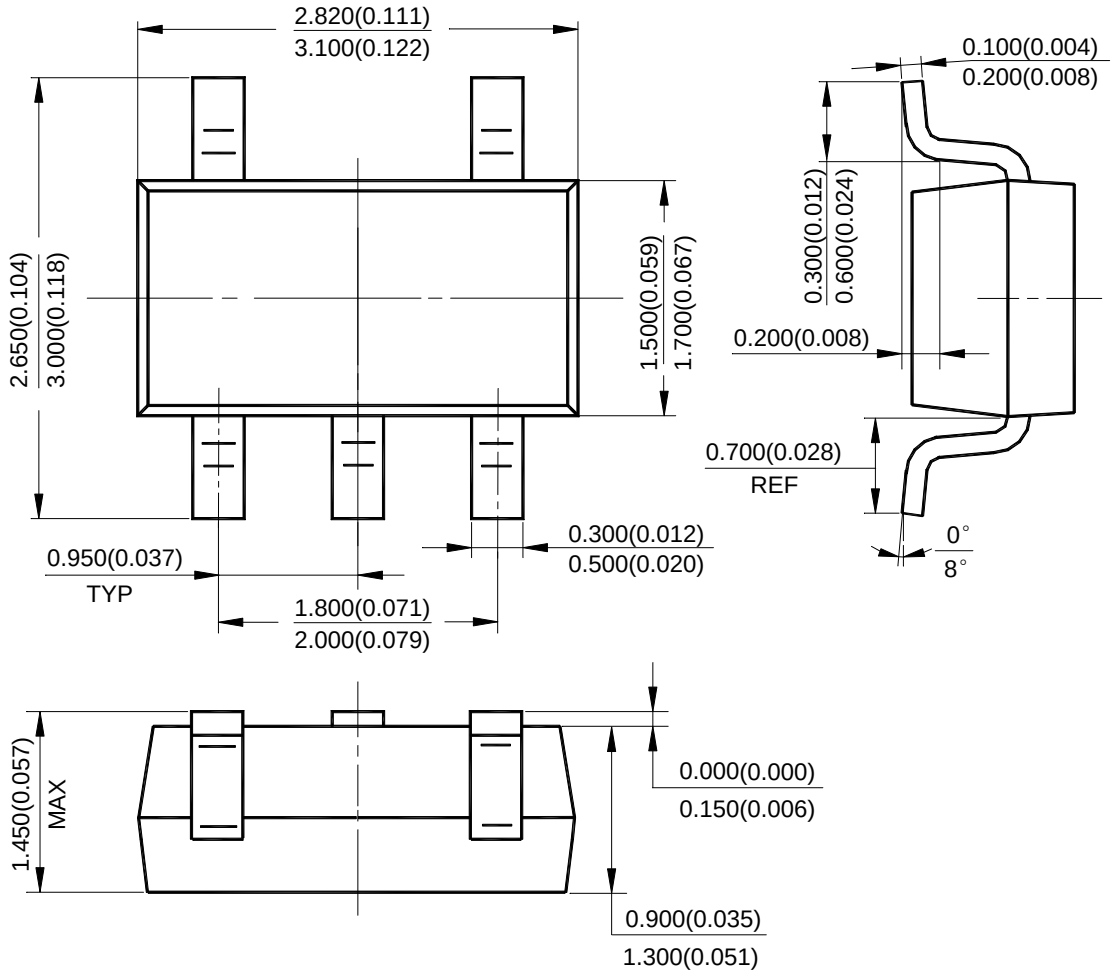
Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: SOT25



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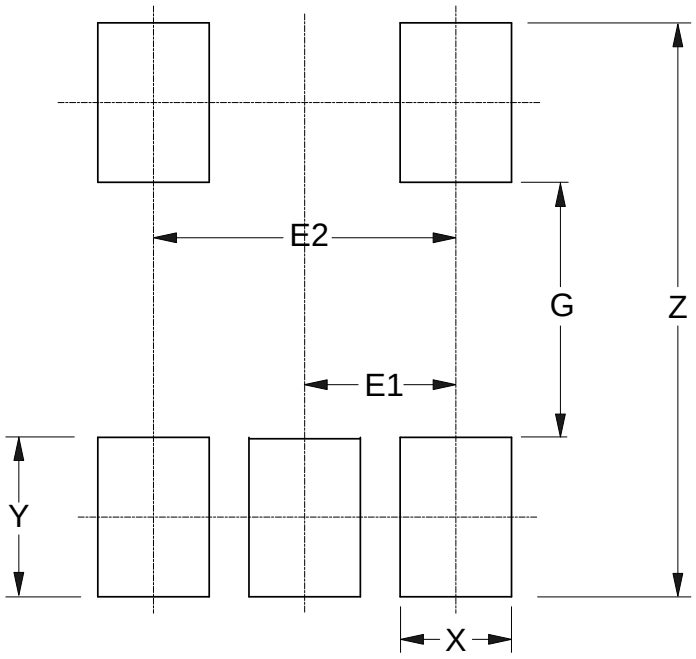
Suggested Pad Layout

(1) Package Type: SOT25



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E1 (mm)/(inch)	E2 (mm)/(inch)
Value	3.600/0.142	1.600/0.063	0.700/0.028	1.000/0.039	0.950/0.037	1.900/0.075

NEW PRODUCT

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