Si5319

ANY-FREQUENCY PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

Features

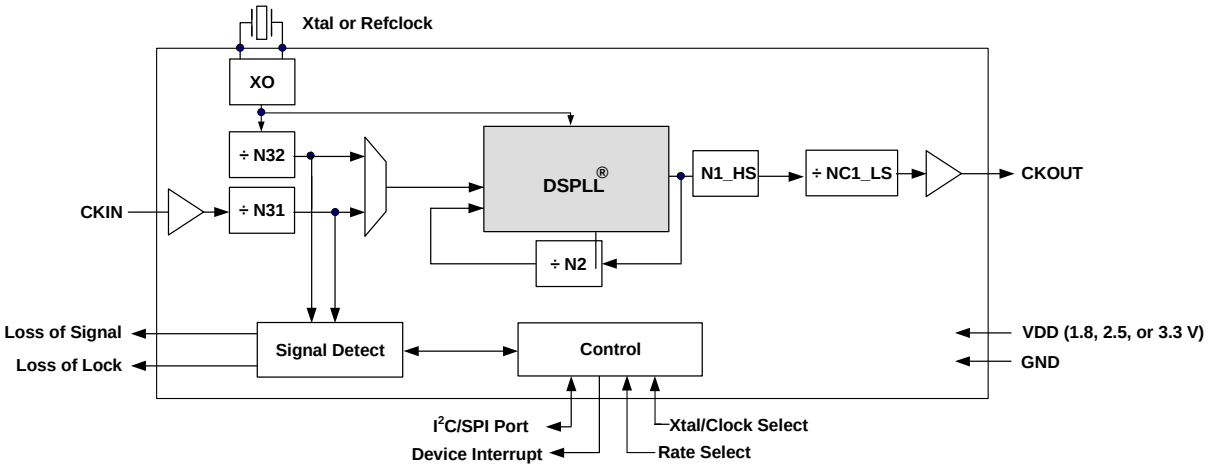
- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock output with jitter generation as low as 0.3 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Clock or crystal input with manual clock selection
- Selectable clock output signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom OTN FEC ratios (e.g. 255/238, 255/237, 255/236)
- Supports various frequency translations for Synchronous Ethernet
- LOL, LOS alarm outputs
- I^2C or SPI programmable
- On-chip voltage regulator for 1.8 V ±5%, 2.5 V ±10% or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

Applications

- 10G/40G/100G OTN line cards
- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Synchronous Ethernet
- Optical modules
- Wireless basestations
- Data converter clocking
- DSLAM/MSANs
- Test and measurement
- Broadcast video
- Discrete PLL replacement

Description

The Si5319 is a jitter-attenuating precision M/N clock multiplier for applications requiring sub 1 ps jitter performance. The Si5319 accepts one clock input ranging from 2 kHz to 710 MHz and generates one clock output ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The Si5319 can also use its crystal oscillator as a clock source for free-running clock generation. The device provides virtually any frequency translation combination across this operating range. The Si5319 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. The Si5319 is based on Silicon Laboratories' third-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5319 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		-40	25	85	°C
Supply Voltage during Normal Operation	V_{DD}	3.3 V Nominal	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 ºC unless otherwise stated.						

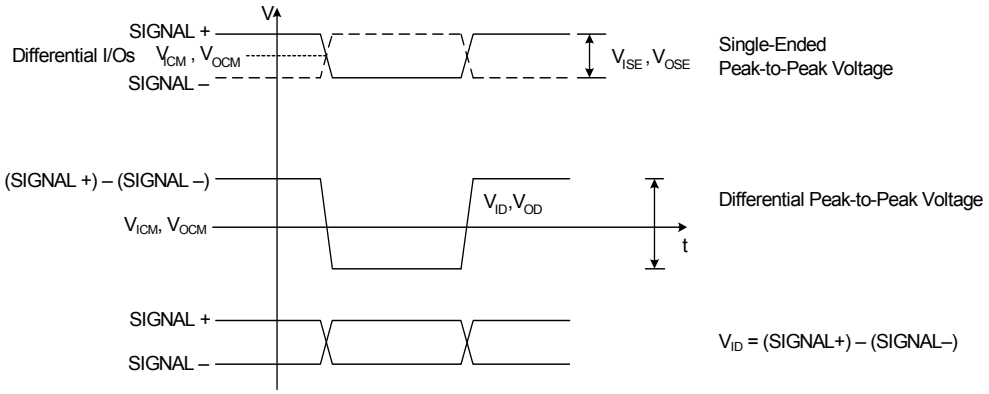

Figure 1. Differential Voltage Characteristics

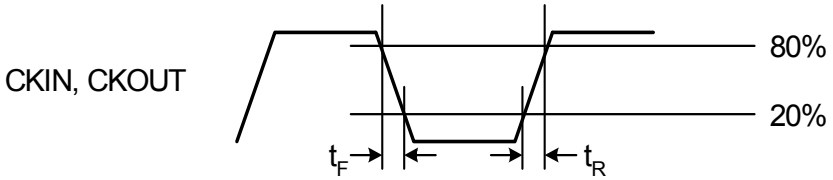

Figure 2. Rise/Fall Time Characteristics

Table 2. DC Characteristics
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1]	I_{DD}	LVPECL Format 622.08 MHz Out	—	217	243	mA
		CMOS Format 19.44 MHz Out	—	194	220	mA
		Disable Mode	—	165	—	mA
CKIN Input Pin[2]						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ± 5%	0.9	—	1.4	V
		2.5 V ± 10%	1	—	1.7	V
		3.3 V ± 10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Output Clock (CKOUT)[3]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} –1.42	—	V_{DD} –1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} ≥ 2.5 V.
4. This is the amount of leakage that the 3-level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD} – 0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V
Output Drive Current (CMOS driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO_{IO}	ICMOS[1:0] =11 V_{DD} = 1.8 V	—	7.5	—	mA
		ICMOS[1:0] =10 V_{DD} = 1.8 V	—	5.5	—	mA
		ICMOS[1:0] =01 V_{DD} = 1.8 V	—	3.5	—	mA
		ICMOS[1:0] =00 V_{DD} = 1.8 V	—	1.75	—	mA
		ICMOS[1:0] =11 V_{DD} = 3.3 V	—	32	—	mA
		ICMOS[1:0] =10 V_{DD} = 3.3 V	—	24	—	mA
		ICMOS[1:0] =01 V_{DD} = 3.3 V	—	16	—	mA
		ICMOS[1:0] =00 V_{DD} = 3.3 V	—	8	—	mA

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} ≥ 2.5 V.
4. This is the amount of leakage that the 3-level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V
3-Level Input Pins[4]						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}	See Note 4	–20	—	—	µA
Input Mid Current	I_{IMM}	See Note 4	–2	—	+2	µA
Input High Current	I_{IHH}	See Note 4	—	—	20	µA
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	IO = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
Output Voltage Low		IO = 2 mA V_{DD} = 2.97 V	—	—	0.4	V

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal $V_{DD} \geq 2.5$ V.
4. This is the amount of leakage that the 3-level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	V_{OH}	IO = –2 mA V_{DD} = 1.71 V	V_{DD} –0.4	—	—	V
Output Voltage High		IO = –2 mA V_{DD} = 2.97 V	V_{DD} –0.4	—	—	V
Disabled Leakage Current	I_{OZ}	RSTb = 0	–100	—	100	µA

Notes:
1. Current draw is independent of supply voltage.
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal V_{DD} ≥ 2.5 V.
4. This is the amount of leakage that the 3-level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 3. Microprocessor Control
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I^2C Bus Lines (SDA, SCL)						
Input Voltage Low	VIL_{I2C}		—	—	0.25 x V_{DD}	V
Input Voltage High	VIH_{I2C}		0.7 x V_{DD}	—	V_{DD}	V
Input Current	II_{I2C}	VIN = 0.1 x V_{DD} to 0.9 x V_{DD}	–10	—	10	µA
Hysteresis of Schmitt trigger inputs	$VHYS_{I2C}$	V_{DD} = 1.8V	0.1 x V_{DD}	—	—	V
		V_{DD} = 2.5 or 3.3 V	0.05 x V_{DD}	—	—	V
Output Voltage Low	VOL_{I2C}	V_{DD} = 1.8 V IO = 3 mA	—	—	0.2 x V_{DD}	V
		V_{DD} = 2.5 or 3.3 V IO = 3 mA	—	—	0.4	V
SPI Specifications						
Duty Cycle, SCLK	t_{DC}	SCLK = 10 MHz	40	—	60	%
Cycle Time, SCLK	t_c		100	—	—	ns
Rise Time, SCLK	t_r	20–80%	—	—	25	ns
Fall Time, SCLK	t_f	20–80%	—	—	25	ns

Table 3. Microprocessor Control (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Low Time, SCLK	t_{lsc}	20–20%	30	—	—	ns
High Time, SCLK	t_{hsc}	80–80%	30	—	—	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	25	ns
Delay Time, SS Rise to SDO Tri-state	t_{d3}		—	—	25	ns
Setup Time, SS to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, SS to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Slave Selects	t_{cs}		25	—	—	ns

Table 4. AC Specifications
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Reference Clock Input Pin XA (XB with cap to GND)						
Input Resistance	XA_{RIN}	RATE[1:0] = LM or MH, ac coupled	—	12	—	kΩ
Input Voltage Swing	XA_{VPP}	RATE[1:0] = LM or MH, ac coupled	0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Voltage Swing	XA/XB_{VPP}	RATE[1:0] = LM or MH	0.5	—	1.2	V_{PP}, each.
CKIN Input Pins						
Input Frequency	CKN_F		0.002	—	710	MHz

Table 4. AC Specifications (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high-frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUT Output Pins (See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F	N1 ≥ 6	0.002	—	945	MHz
		N1 = 5	970	—	1134	MHz
		N1 = 4	1.213	—	1.4	GHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 1.71 C_{LOAD} = 5 pF	—	—	8	ns
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 2.97 C_{LOAD} = 5 pF	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO_{DC}	100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	+/-40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMN}		1	—	—	µs
Reset to Microprocessor Access Ready	t_{READY}		—	—	10	ms
Input Capacitance	C_{in}		—	—	3	pF

Table 4. AC Specifications (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKINn ↑ to ↓ Internal detection of LOSn N3 ≠ 1	—	—	4.5 x N3	T_{CKIN}
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	↓LOS to ↓LOL Fold = Fnew Stable Xa/XB reference	—	10	—	ms
Device Skew						
Input to Output Phase Change Due to Temperature Variation	t_{TEMP}	Max phase changes from –40 to +85 °C	—	300	500	ps
PLL Performance **(fin=fout = 622.08 MHz; BW=120 Hz; LVPECL)**						
Lock Time	t_{LOCKMP}	Start of ICAL to ↓ of LOL	—	35	1200	ms
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise fout = 622.08 MHz	CKO_{PN}	1 kHz Offset	—	–106	–87	dBc/Hz
		10 kHz Offset	—	–121	–100	dBc/Hz
		100 kHz Offset	—	–132	–104	dBc/Hz
		1 MHz Offset	—	–132	–119	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	–88	–76	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	–93	–70	dBc

Table 5. Jitter Generation

Parameter	Symbol	Test Condition*		Min	Typ	Max	GR-253-Specification	Unit
		Measurement Filter	DSPLL BW[2]					
Jitter Gen OC-192	J_{GEN}	0.02–80 MHz	120 Hz	—	4.2	6.2	30	ps_{PP}
				—	0.27	0.42	N/A	ps_{rms}
		4–80 MHz	120 Hz	—	3.7	6.4	10	ps_{PP}
				—	0.14	0.31	N/A	ps_{rms}
		0.05–80 MHz	120 Hz	—	4.4	6.9	10	ps_{PP}
				—	0.26	0.41	1.0	ps_{rms}
Jitter Gen OC-48	J_{GEN}	0.12–20 MHz	120 Hz	—	3.5	5.4	40.2	ps_{PP}
				—	0.27	0.41	4.02	ps_{rms}

***Note:** Test conditions:
1. fIN = fOUT = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 120 Hz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6. V_{DD} = 2.5 V
7. T_A = 85 °C

Table 6. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	32	C°/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	14	C°/W

Table 7. Absolute Maximum Limits

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		–0.5	—	3.8	V
LVCMOS Input Voltage	V_{DIG}		–0.3		V_{DD}+0.3	V
CKINn Voltage Level Limits	CKN_{VIN}		0	—	V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Operating Junction Temperature	T_{JCT}		–55	—	150	ºC
Storage Temperature Range	T_{STG}		–55	—	150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–			2	—	—	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–			150	—	—	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–			750	—	—	V
ESD MM Tolerance; CKIN+/CKIN–			100	—	—	V
Latch-up Tolerance			JESD78 Compliant			

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

2. Typical Phase Noise Plots

The following typical phase noise plot was taken using a Rohde and Schwarz SML03 RF Generator as the clock input source to the Si5326. The Agilent model E5052B was used for the phase noise measurement. For this measurement, the Si5319 operates at 3.3 V with an ac coupled differential PECL output and an ac coupled differential sine wave input from the RF generator at 0 dBm. Note that, as with any PLL, the output jitter that is below the loop BW is caused by the jitter at the input clock. The loop BW was 120 Hz.

2.1. Example: SONET OC-192

Figure 3. Typical Phase Noise Plot

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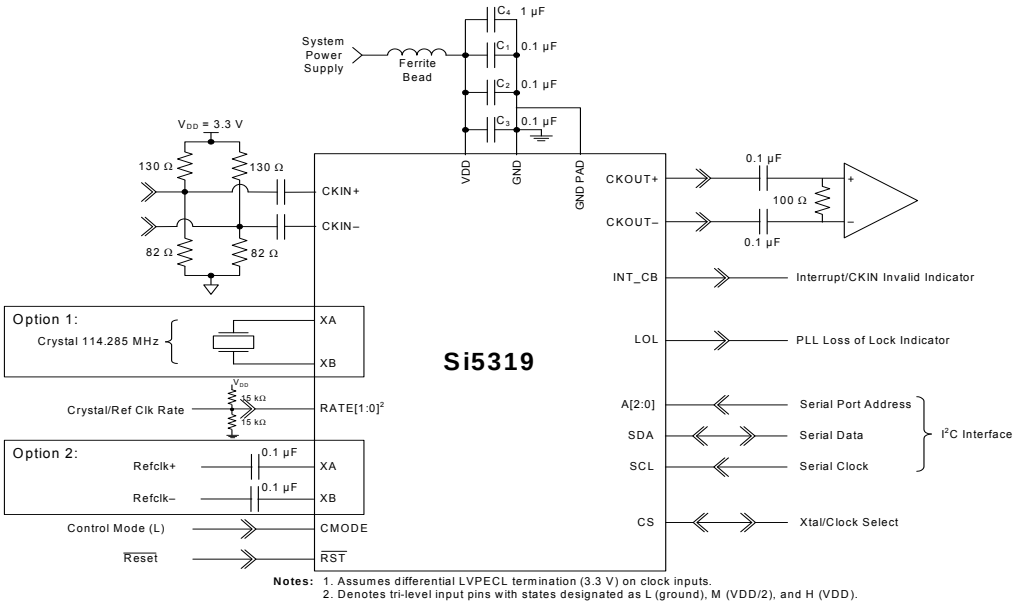
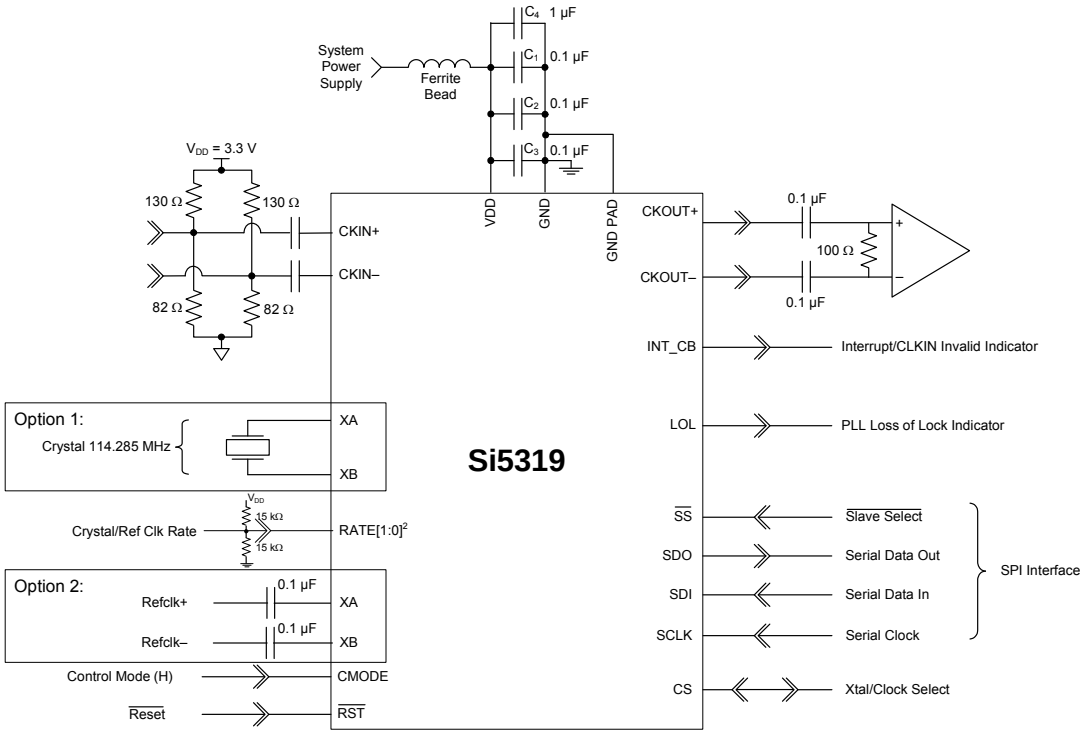
Jitter Band	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	250 fs
SONET_OC192_A, 20 kHz to 80 MHz	274 fs
SONET_OC192_B, 4 to 80 MHz	166 fs
SONET_OC192_C, 50 kHz to 80 MHz	267 fs
Brick Wall, 800 Hz to 80 MHz	274 fs



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).

Figure 4. Si5319 Typical Application Circuit (I^2C Control Mode)



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).

Figure 5. Si5319 Typical Application Circuit (SPI Control Mode)

3. Functional Description

The Si5319 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5319 accepts one clock input ranging from 2 kHz to 710 MHz and generates one clock output ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The Si5319 can also use its crystal oscillator as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. The Si5319 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing.

The Si5319 is based on Silicon Laboratories' third generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5319 PLL loop bandwidth is digitally programmable and supports a range from 60 Hz to 8.4 kHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5319 monitors the input clock for loss-of-signal and provides a LOS alarm when it detects missing pulses on the input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5319 provides a VCO freeze capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During VCO freeze, the DSPLL latches its VCO settings and uses its XO as its frequency reference.

The Si5319 has one differential clock output. The electrical format of the clock output is programmable to support LVPECL, LVDS, CML, or CMOS loads. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

3.1. External Reference

A low-cost 114.285 MHz 3rd overtone crystal or an external reference oscillator is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to operate. Silicon Laboratories recommends using a high quality crystal. Specific recommendations may be found in the Family Reference Manual. An external oscillator as well as other crystal frequencies can also be used as a reference for the device.

In VCO Freeze, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in VCO freeze will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

3.2. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5319. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing.

4. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Do not write to registers not listed in the register map, such as Register 64.

Register	D7	D6	D5	D4	D3	D2	D1	D0
0		FREE_RUN	CKOUT_ ALWAYS_ ON				BYPASS_ REG	
2	BWSEL_REG[3:0]							
3			VCO_ FREEZE	SQ_ICAL				
5	ICMOS[1:0]							
6						SFOUT1_REG[2:0]		
8			HLOG[1:0]					
10						DSBL_ REG		
11								PD_CK
19				VALTIME[1:0]		LOCK[T2:0]		
20							LOL_PIN	INT_PIN
22							LOL_POL	INT_POL
23							LOS_MSK	LOSX_MSK
24								LOL_MSK
25		N1_HS[2:0]						
31					NC1_LS[19:16]			
32	NC1_LS[15:8]							
33	NC1_LS[7:0]							
40		N2_HS[2:0]			N2_LS[19:16]			
41	N2_LS[15:8]							
42	N2_LS[7:0]							
43						N31[18:16]		
44	N31[15:8]							
45	N31[7:0]							
46						N32[18:16]		
47	N32[15:8]							
48	N32[7:0]							

Register	D7	D6	D5	D4	D3	D2	D1	D0
128								CK_ACTV_ REG
129							LOS_INT	LOSX_INT
130								LOL_INT
131							LOS_FLG	LOSX_FLG
132							LOL_FLG	
134	PARTNUM_RO[11:4]							
135	PARTNUM_RO[3:0]				REVID_RO[3:0]			
136	RST_REG	ICAL					GRADE_RO[1:0]	
138								LOS_EN [1:1]
139				LOS_EN [0:0]				
185	NVM_REVID[7:0]							

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FREE_ RUN	CKOUT_ ALWAYS_ ON				BYPASS_ REG	
Type	R	R/W	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7	Reserved	**Reserved.**
6	FREE_RUN	**Free Run.** Internal to the device, route XA/XB to CKIN2. This allows the device to lock to its XA-XB reference (either internal or external). 0: Disable 1: Enable
5	CKOUT_ ALWAYS_ON	**CKOUT Always On.** This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 9 on page 39. 0: Squelch output until part is calibrated (ICAL). 1: Device generates output clock, including during calibration. Note: The frequency may be significantly off until the part is calibrated.
4:2	Reserved	**Reserved.**
1	BYPASS_ REG	**Bypass Register.** This bit enables or disables the PLL bypass mode. Use only when the device is in VCO_FREEZE or before the first ICAL. Bypass mode is not supported for CMOS output clocks. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL.
0	Reserved	**Reserved.**

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]				Reserved			
Type	R/W				R			

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	**BWSEL_REG.** Selects nominal f3dB bandwidth for PLL. See the DSPLL*sim* for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	Reserved	**Reserved.**

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		VCO_ FREEZE	SQ_ICAL	Reserved			
Type	R		R/W	R/W	R			

Reset value = 0000 0101

Bit	Name	Function
7:6	Reserved	**Reserved.**
5	VCO_ FREEZE	**VCO_FREEZE.** Forces the part into VCO Freeze. This bit overrides all other manual and automatic clock selection controls. 0: Normal operation. 1: Force VCO Freeze mode. Overrides all other settings and ignores the quality of all of the input clocks.
4	SQ_ICAL	**SQ_ICAL.** This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 9 on page 39. 0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.
3:0	Reserved	**Reserved.**

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ICMOS [1:0]		Reserved					
Type	R/W		R					

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	**ICMOS [1:0].** When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-. 00: 8 mA/2 mA. 01: 16 mA/4 mA 10: 24 mA/6 mA 11: 32 mA/ 8mA
5:0	Reserved	**Reserved.**

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		Reserved			SFOUT_REG [2:0]		
Type	R		R			R/W		

Reset value = 0010 1101

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	SFOUT_ REG [2:0]	**SFOUT_REG [2:0].** Controls output signal format and disable for CKOUT output buffer. Bypass mode is not supported for CMOS output clocks. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS

Register 8.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		HLOG[1:0]		Reserved			
Type	R		R/W		R			

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:4		**HLOG [1:0].** 00: Normal operation. 01: Holds CKOUT output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved.
3:0	Reserved	**Reserved.**

Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					DSBL_ REG	Reserved	
Type	R					R/W	R	

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	**Reserved.**
2	DSBL_REG	**DSBL_REG.** This bit controls the powerdown of the CKOUT output buffer. If disable mode is selected, the NC_LS output divider is also powered down. 0: CKOUT enabled. 1: CKOUT disabled.
1:0	Reserved	**Reserved.**

Register 11.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved							PD_CK
Type	R							R/W

Reset value = 0100 0000

Bit	Name	Function
7:1	Reserved	**Reserved.**
0	PD_CK	**PD_CK.** This bit controls the powerdown of the CKIN input buffer. 0: CKIN enabled. 1: CKIN disabled.

Register 19.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			VALTIME [1:0]		LOCKT [2:0]		
Type	R			R/W		R/W		

Reset value = 0010 1100

Bit	Name	Function
7:5	FOS_EN	**Reserved.**
4:3	VALTIME [1:0]	**VALTIME [1:0].** Sets amount of time for input clock to be valid before the associated alarm is removed. 00: 2 ms 01: 100 ms 10: 200 ms 11: 13 seconds
2:0	LOCKT [2:0]	**LOCKT [2:0].** Sets retrigger interval for one shot monitoring phase detector output. One shot is triggered by a phase slip in the DSPLL. Refer to the Family Reference Manual for more details. 000: 106 ms 001: 53 ms 010: 26.5 ms 011: 13.3 ms 100: 6.6 ms 101: 3.3 ms 110: 1.66 ms 111: .83 ms

Register 20.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						LOL_PIN	INT_PIN
Type	R						R/W	R/W

Reset value = 0011 1110

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	LOL_PIN	**LOL_PIN.** The LOL_INT status bit can be reflected on the LOL output pin. 0: LOL output pin tristated 1: LOL_INT status reflected to output pin
0	INT_PIN	**INT_PIN.** Reflects the interrupt status on the INT_CB output pin. 0: Interrupt status not displayed on INT_CB output pin. If CK1_BAD_PIN = 0, INT_CB output pin is tristated. 1: Interrupt status reflected to output pin. Instead, the INT_CB pin indicates when CKIN is bad.

Register 22.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						LOL_POL	INT_POL
Type	R						R/W	R/W

Reset value = 1101 1111

Bit	Name	Function
7:2	Reserved	**Reserved.**
2	CK_BAD_ POL	**CK_BAD_POL.** Sets the active polarity for the INT_CB and C2B signals when reflected on output pins. 0: Active low 1: Active high
1	LOL_POL	**LOL_POL.** Sets the active polarity for the LOL status when reflected on an output pin. 0: Active low 1: Active high
0	INT_POL	**INT_POL.** Sets the active polarity for the interrupt status when reflected on the INT_CB output pin. 0: Active low 1: Active high

Register 23.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						LOS_ MSK	LOSX_ MSK
Type	R						R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	LOS_MSK	**LOS_MSK.** Determines if a LOS on CKIN (LOS_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS_FLG register. 0: LOS alarm triggers active interrupt on INT_CB output (if INT_PIN=1). 1: LOS_FLG ignored in generating interrupt output.
0	LOSX_MSK	**LOSX_MSK.** Determines if a LOS on XA/XB(LOSX_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOSX_FLG register. 0: LOSX alarm triggers active interrupt on INT_CB output (if INT_PIN=1). 1: LOSX_FLG ignored in generating interrupt output.

Register 24.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved							LOL_MSK
Type	R							R/W

Reset value = 0011 1111

Bit	Name	Function
7:2	Reserved	**Reserved.**
0	LOL_MSK	**LOL_MSK.** Determines if the LOL_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the LOL_FLG register. 0: LOL alarm triggers active interrupt on INT_CB output (if INT_PIN=1). 1: LOL_FLG ignored in generating interrupt output.

Register 25.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1_HS [2:0]			Reserved				
Type	R/W			R				

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	**N1_HS [2:0].** Sets value for N1 high speed divider which drives NC1_LS low-speed divider. 000: N1= 4 001: N1= 5 010: N1=6 011: N1= 7 100: N1= 8 101: N1= 9 110: N1= 10 111: N1= 11
4:0	Reserved	**Reserved.**

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				NC1_LS [19:16]			
Type	R				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	NC1_LS [19:16]	**NC1_LS [19:16].** Sets value for NC1_LS divider, which drives CKOUT output. The value of the register must be either odd or zero. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	**NC1_LS [15:8].** Sets value for NC1_LS, which drives CKOUT output. The value of the register must be either odd or zero. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [19:0]	**NC1_LS [7:0].** Sets value for NC1_LS, which drives CKOUT output. The value of the register must be either odd or zero. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_HS [2:0]			Reserved	N2_LS [19:16]			
Type	R/W			R	R/W			

Reset value = 1100 0000

Bit	Name	Function
7:5	N2_HS [2:0]	**N2_HS [2:0].** Sets value for N2 high speed divider which drives N2_LS low-speed divider. 000: 4 001: 5 010: 6 011: 7 100: 8 101: 9 110: 10 111: 11
4	Reserved	**Reserved.**
3:0	N2_LS [19:16]	**N2_LS [19:16].** Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^20 Valid divider values = [2, 4, 6, ..., 2^20]

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	**N2_LS [15:8].** Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^20 Valid divider values = [2, 4, 6, ..., 2^20]

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [7:0]							
Type	R/W							

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	**N2_LS [7:0].** Sets value for N2 low-speed divider, which drives phase detector. 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2^20 Valid divider values = [2, 4, 6, ..., 2^20]

Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					N31 [18:16]		
Type	R					R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	N31 [18:16]	**N31 [18:16].** Sets value for input divider for CKIN. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N31_[15:8]	**N31_[15:8].** Sets value for input divider for CKIN. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N31_[7:0	**N31_[7:0].** Sets value for input divider for CKIN. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					N32_[18:16]		
Type	R					R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	N32_[18:16]	**N32_[18:16].** Sets value for input divider for the XO clock in free-run mode. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N32_[15:8]	**N32_[15:8].** Sets value for input divider for the XO clock in free-run mode. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N32_[7:0]	**N32_[7:0].** Sets value for input divider for the XO clock in free-run mode. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved							CK_ACTV_ REG
Type	R							R

Reset value = 0010 0000

Bit	Name	Function
7:1	Reserved	**Reserved.**
0	CK_ACTV_ REG	**CK_ACTV_REG.** Indicates if CKIN is currently the active clock for the PLL input. 0: CKIN is not the active input clock. Either it is not selected or LOS_INT is 1. 1: CKIN is the active input clock.

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						LOS_INT	LOSX_INT
Type	R						R	R

Reset value = 0000 0110

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	LOS_INT	**LOS_INT.** Indicates the LOS status on CKIN. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN input.
0	LOSX_INT	**LOSX_INT.** Indicates the LOS status of the external reference on the XA/XB pins. 0: Normal operation. 1: Internal loss-of-signal alarm on XA/XB reference clock input.

Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved							LOL_INT
Type	R							R

Reset value = 0000 0001

Bit	Name	Function
7:3	Reserved	**Reserved.**
0	LOL_INT	**PLL Loss of Lock Status.** 0: PLL locked. 1: PLL unlocked.

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						LOS_FLG	LOSX_FLG
Type	R						R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	LOS_FLG	**CKIN Loss-of-Signal Flag.** 0: Normal operation 1: Held version of LOS_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS_MSK bit. Flag cleared by writing 0 to this bit.
0	LOSX_FLG	**External Reference (signal on pins XA/XB) Loss-of-Signal Flag.** 0: Normal operation 1: Held version of LOSX_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOSX_MSK bit. Flag cleared by writing 0 to this bit.

Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						LOL_FLG	Reserved
Type	R						R/W	R

Reset value = 0000 0010

Bit	Name	Function
7:2, 0	Reserved	**Reserved.**
1	LOL_FLG	**PLL Loss of Lock Flag.** 0: PLL locked 1: Held version of LOL_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOL_MSK bit. Flag cleared by writing 0 to this bit.

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [11:4]							
Type	R							

Reset value = 0000 0001

Bit	Name	Function
7:0	PARTNUM_ RO [11:0]	**Device ID (1 of 2).** 0000 0001 + 0011: Si5319

Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [3:0]				REVID_RO [3:0]			
Type	R				R			

Reset value = 1010 0010

Bit	Name	Function
7:4	PARTNUM_ RO [11:0]	**Device ID (2 of 2).** 0000 0001 + 0011: Si5319
3:0	REVID_RO [3:0]	**Indicates Revision Number of Device.** 0000: Revision A 0001: Revision B 0010: Revision C Others: Reserved

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	ICAL	Reserved				GRADE_RO [1:0]	
Type	R/W	R/W	R				R	

Reset value = 0000 0000

Bit	Name	Function
7	RST_REG	**Internal Reset (Same as Pin Reset).** **Note:** The I2C (or SPI) port may not be accessed until 10 ms after RST_REG is asserted. 0: Normal operation. 1: Reset of all internal logic. Outputs disabled or tristated during reset.
6	ICAL	**Start an Internal Calibration Sequence.** For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL. Note: Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect. 0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, LOL will go low.
5:2	Reserved	**Reserved.**
1:0	GRADE_RO [1:0]	**Indicates Maximum Clock Output Frequency of this Device.** Limits the range of the N1_HS divider. 00: N1_HS x NC1_LS > 4. Maximum clock output frequency = 1.4175 GHz. 01: N1_HS x NC1_LS > 6. Maximum clock output frequency = 808 MHz. 10: N1_HS x NC1_LS > 14. Maximum clock output frequency = 346 MHz. 11: N1_HS x NC1_LS > 20. Maximum clock output frequency = 243 MHz.

Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved							LOS_EN [1:1]
Type	R							R/W

Reset value = 0000 1111

Bit	Name	Function
7:3	Reserved	**Reserved.**
0	LOS_EN [1:0]	**Enable CKIN LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.

Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			LOS_EN [0:0]	Reserved			
Type	R			R/W	R			

Reset value = 1111 1111

Bit	Name	Function
7:5	Reserved	**Reserved.**
4	LOS_EN [1:0]	**Enable CKIN LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.
3:0	Reserved	**Reserved.**

Register 185.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NVM_REVID [7:0]							
Type	R							

Reset value = 0001 0011

Bit	Name	Function
7:0	NVM_REVID [7:0]	**NVM_REVID.**

Table 8. CKOUT_ALWAYS_ON and SQ_ICAL Truth Table

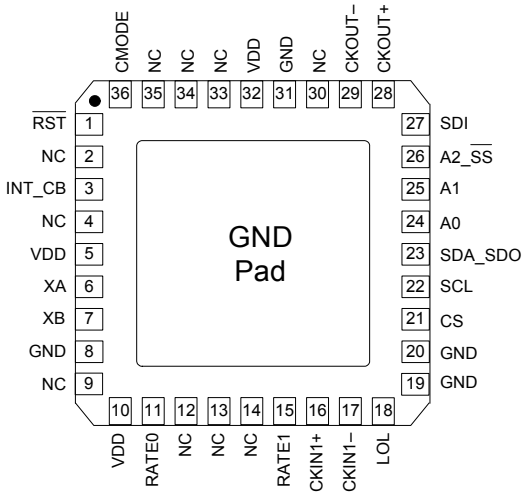
CKOUT_ALWAYS_ON	SQ_ICAL	Results
0	0	CKOUT OFF until after the first ICAL.
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low).
1	0	CKOUT always ON, including during an ICAL.
1	1	CKOUT always ON, including during an ICAL. Use these settings to preserve output-to-output skew.

Table 9 lists all of the register locations that should be followed by an ICAL after their contents are changed.

Table 9. Register Locations Requiring ICAL

Addr	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
2	BWSEL_REG
5	ICMOS
10	DSBL_REG
11	PD_CK
19	VALTIME
19	LOCKT
25	N1_HS
31	NC1_LS
40	N2_HS
40	N2_LS
43	N31

5. Pin Descriptions: Si5319



Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are disabled during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details. This pin has a weak pull-up.
2, 4, 9, 12–14, 30, 33–35	NC	—	—	**No Connection.** Leave floating. Make no external connections to this pin for normal operation.
3	INT_CB	O	LVCMOS	**Interrupt/CKIN Invalid Indicator.** This pin functions as a device interrupt output or an alarm output for CKIN. If used as an interrupt output, *INT_PIN* must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the *INT_POL* register bit. If used as an alarm output, the pin functions as a LOS alarm indicator for CKIN. Set *CK_BAD_PIN* = 1 and *INT_PIN* = 0. 0 = CKIN present. 1 = LOS on CKIN. The active polarity is controlled by *CK_BAD_POL*. If no function is selected, the pin tristates.
5, 10, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should also be placed as close to the device as is practical.
Note: Internal register names are indicated by underlined italics (e.g., *INT_PIN*. See Si5319 Register Map).				

Pin #	Pin Name	I/O	Signal Level	Description
7 6	XB XA	I	Analog	**External Crystal or Reference Clock.** External crystal should be connected to these pins to use internal oscillator based reference. Refer to the Family Reference Manual for interfacing to an external reference. The external reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pins.
8, 31 19,20	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device. Grounding these pins does not eliminate the requirement to ground the GND PAD on the bottom of the package.
11 15	RATE0 RATE1	I	3-Level	**External Crystal or Reference Clock Rate.** Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down; they default to M. The "HH" setting is not supported. **Note:** L setting corresponds to ground. M setting corresponds to $V_{DD}/2$. H setting corresponds to V_{DD}. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
16 17	CKIN+ CKIN–	I	Multi	**Clock Input.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 2 kHz to 710 MHz.
18	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator if the *LOL_PIN* register bit is set to 1. 0 = PLL locked. 1 = PLL unlocked. If *LOL_PIN* = 0, this pin will tristate. Active polarity is controlled by the *LOL_POL* bit. The PLL lock status will always be reflected in the *LOL_INT* read only register bit.
21	CS	I	LVCMOS	**Xtal/Input Clock Select.** This pin selects the active DSPLL input clock, which can be a clock input or a crystal input. See the *FREE_EN* register for free run settings. 0 = Select clock input (CKIN). 1 = Select crystal or external reference clock. This pin should not be left open.
22	SCL	I	LVCMOS	**Serial Clock/Serial Clock.** This pin functions as the serial clock input for both SPI and I^2C modes. This pin has a weak pull-down.
23	SDA_SDO	I/O	LVCMOS	**Serial Data.** In I^2C control mode (CMODE = 0), this pin functions as the bidirectional serial data port. In SPI control mode (CMODE = 1), this pin functions as the serial data output.
Note: Internal register names are indicated by underlined italics (e.g., *INT_PIN*. See Si5319 Register Map).				

Pin #	Pin Name	I/O	Signal Level	Description
25 24	A1 A0	I	LVCMOS	**Serial Port Address.** In I^2C control mode (CMODE = 0), these pins function as hardware controlled address bits. The I^2C address is 1101 [A2] [A1] [A0]. In SPI control mode (CMODE = 1), these pins are ignored. These pins have a weak pull-down.
26	A2_$\overline{SS}$	I	LVCMOS	**Serial Port Address/Slave Select.** In I^2C control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2]. In SPI control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pull-down.
27	SDI	I	LVCMOS	**Serial Data In.** In I^2C control mode (CMODE = 0), this pin is ignored. In SPI control mode (CMODE = 1), this pin functions as the serial data input. This pin has a weak pull-down.
29 28	CKOUT– CKOUT+	O	Multi	**Output Clock.** Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by *SFOUT1_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
36	CMODE	I	LVCMOS	**Control Mode.** Selects I^2C or SPI control mode for the Si5319. 0 = I^2C Control Mode 1 = SPI Control Mode
GND PAD	GND	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.
Note: Internal register names are indicated by underlined italics (e.g., *INT_PIN*. See Si5319 Register Map).				

6. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	ROHS6, Pb-Free	Temperature Range
Si5319A-C-GM	2 kHz–945 MHz 970–1134 MHz 1.213–1.417 GHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5319B-C-GM	2 kHz–808 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5319C-C-GM	2 kHz–346 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Note: Add an R at the end of the device part number to denote tape and reel ordering options.				

7. Package Outline: 36-Pin QFN

Figure 6 illustrates the package details for the Si5319. Table 10 lists the values for the dimensions shown in the illustration.

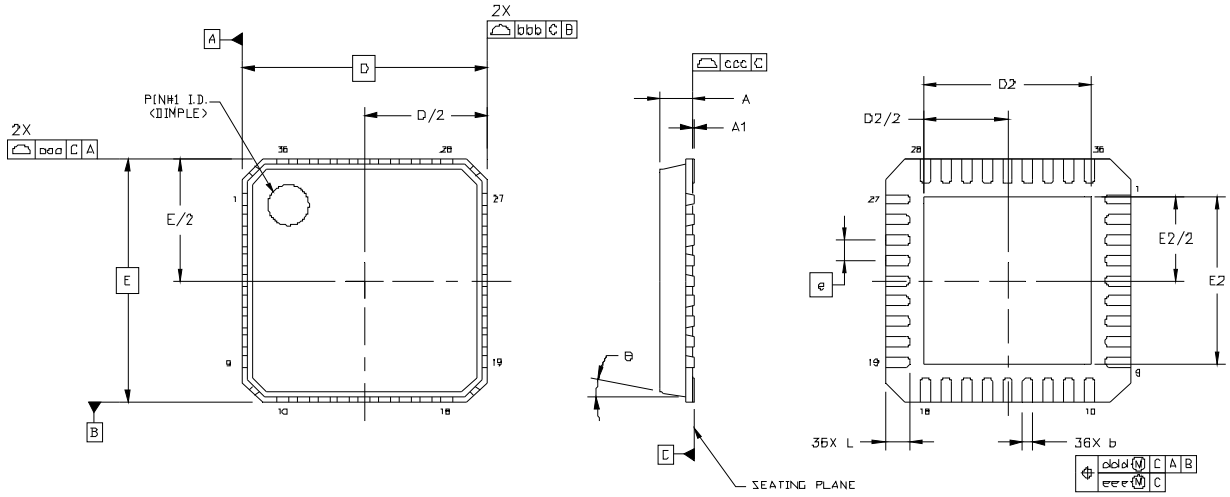


Figure 6. 36-Pin Quad Flat No-lead (QFN)

Table 10. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	6.00 BSC		
D2	3.95	4.10	4.25
e	0.50 BSC		
E	6.00 BSC		
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.70
θ	—	—	12º
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Recommended PCB Layout

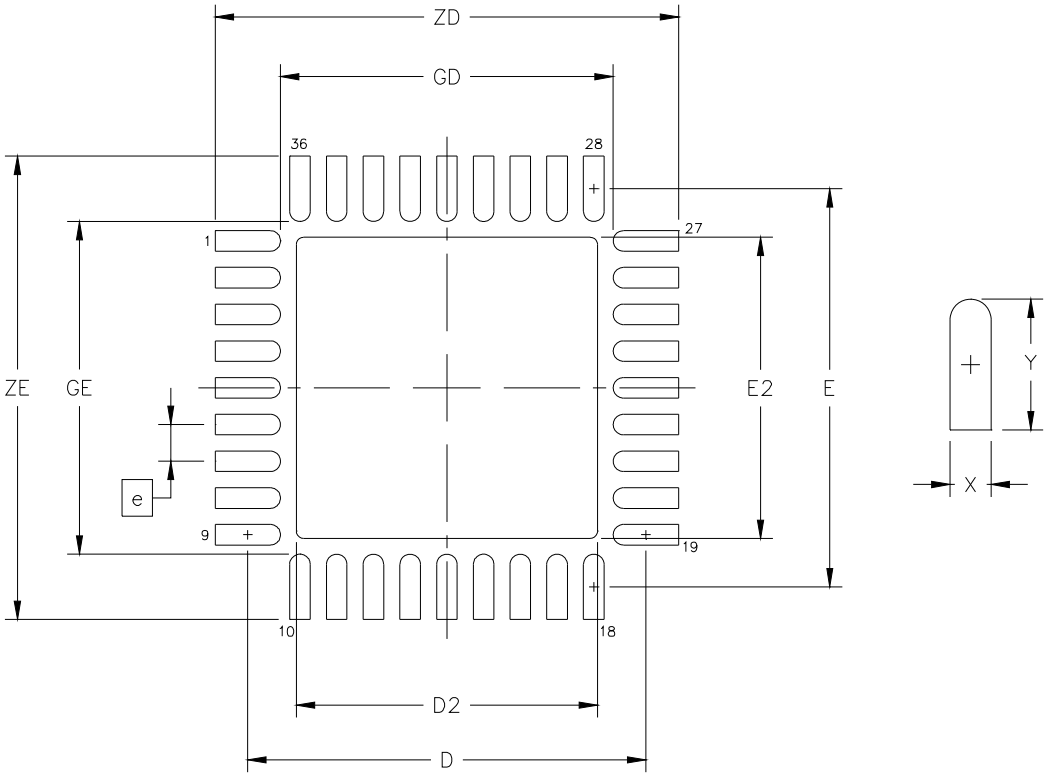


Figure 7. PCB Land Pattern Diagram

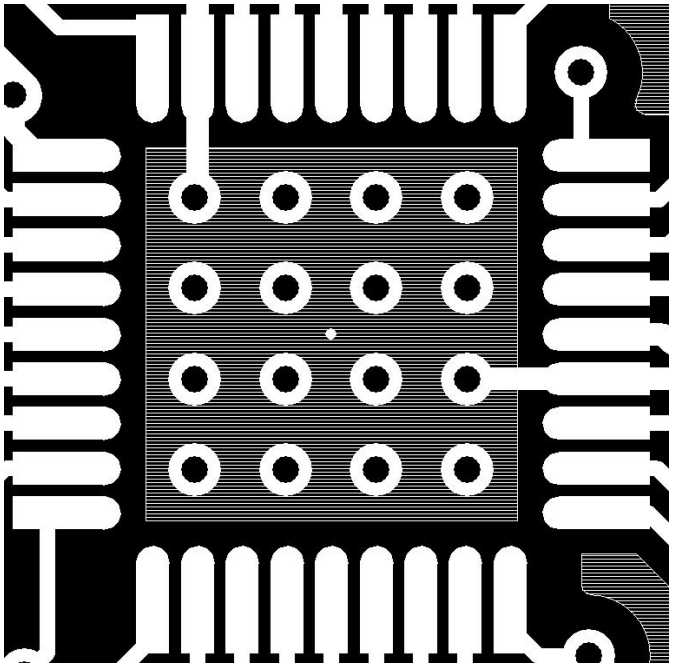


Figure 8. Ground Pad Recommended Layout

Table 11. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

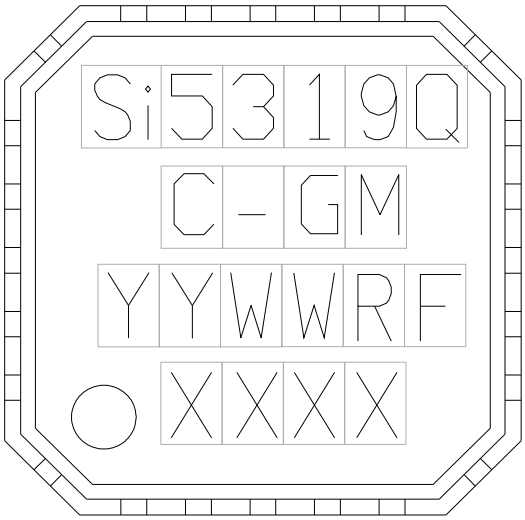
Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Si5319 Device Top Mark



Mark Method:	Laser	
Font Size:	0.80 mm Right-Justified	
Line 1 Marking:	Si5319	Customer Part Number Q = Speed Code: A, B, C See Ordering Guide for options
Line 2 Marking:	C-GM	C = Product Revision G = Temperature Range –40 to 85 °C (RoHS6) M = QFN Package
Line 3 Marking:	YYWWRF	YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 4 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	XXXX	Internal Code

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 4.
- Updated Table 2 on page 5.
- Added table under Figure 3 on page 14.
- Updated "3. Functional Description" on page 16.
- Clarified "5. Pin Descriptions: Si5319" on page 40.

Revision 0.2 to Revision 0.3

- Updated "5. Pin Descriptions: Si5319" on page 40.
  - Corrected Pins 11 and 15 description in table.

Revision 0.3 to Revision 0.4

- Updated Table 1 on page 4.
- Added "9. Si5319 Device Top Mark" on page 47.

Revision 0.4 to Revision 0.41

- Updated Table 1 on page 4.
  - Updated Thermal Resistance Junction to Ambient typical specification.
- Updated Figure 4, “Si5319 Typical Application Circuit (I^2C Control Mode),” on page 15.
- Updated Figure 5, “Si5319 Typical Application Circuit (SPI Control Mode),” on page 15.
- Updated NC pin description in "5. Pin Descriptions: Si5319" on page 40.
- Updated "7. Package Outline: 36-Pin QFN" on page 44.
- Added Figure 8, “Ground Pad Recommended Layout,” on page 45.
- Added register map documentation.
- Updated Rise/Fall Time values.

Revision 0.41 to Revision 0.42

- Changed register address labels to decimal.

Revision 0.42 to Revision 0.43

- Updated the following:
  - ESD specifications
  - phase noise values
  - absolute Vdd maximum voltage
  - typical phase noise plot
- Added specification for phase changes due to temperature variation
- Added information for the N32 register
- Added θ_{JC} specification

Revision 0.43 to Revision 1.0

- Replaced the specification tables (tables 1 and 2 from rev. 0.43) with the specification tables from the Si53x Reference Manual, rev 0.42.

NOTES:

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