

NCV7425

LIN Transceiver with Voltage Regulator and Reset Pin



ON Semiconductor®

<http://onsemi.com>

General Description

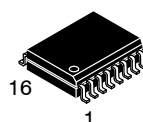
The NCV7425 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus.

The NCV7425 LIN device is a member of the in-vehicle networking (IVN) transceiver family of ON Semiconductor that integrates a LIN v2.1 physical transceiver and a low-drop voltage regulator. It is designed to work in harsh automotive environment and is submitted to the TS16949 qualification flow.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU-state machine that recognizes and translates the instructions specific to that function. The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

Features

- LIN-Bus Transceiver
 - ◆ LIN compliant to specification revision 2.1 (backward compatible to versions 2.0 and 1.3) and J2602
 - ◆ Bus Voltage ± 45 V
 - ◆ Transmission Rate up to 20 kBaud
 - ◆ Integrated Slope Control for Improved EMI Compatibility
- Package
 - ◆ SOIC-16 Wide Body Green Package with Exposed Pad
- Protection
 - ◆ Thermal Shutdown
 - ◆ Indefinite Short-Circuit Protection on Pins LIN and WAKE Towards Supply and Ground
 - ◆ Load Dump Protection (45 V)
 - ◆ Bus Pins Protected Against Transients in an Automotive Environment
 - ◆ ESD Protection Level for LIN, INH, WAKE and V_{BB} up to ± 10 kV
- Voltage Regulator
 - ◆ Two Device Versions: Output Voltage 3.3 V or 5 V For Loads up to 150 mA



SOIC-16 LEAD
WIDE BODY
EXPOSED PAD
CASE 751AG

MARKING DIAGRAM



x = 0 or 5
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

- ◆ Under-Voltage Detector with a Reset Output to the Supplied Microcontroller
- ◆ INH Output for Auxiliary Purposes (switching of an external pull-up or resistive divider towards battery, control of an external voltage regulator etc.)
- Modes
 - ◆ Normal Mode: LIN Communication in Either Low (up to 10 kBaud) or Normal Slope
 - ◆ Sleep Mode: V_{CC} is Switched “off” and No Communication on LIN Bus
 - ◆ Stand-by Mode: V_{CC} is Switched “on” but There is No Communication on LIN Bus
 - ◆ Wake-up Bringing the Component From Sleep Mode Into Standby Mode is Possible Either by LIN Command or Digital Input Signal on WAKE Pin Wake-up from LIN Bus can also be Detected and Flagged When the Chip is Already in Standby Mode
- These are Pb-Free Devices

Typical Applications

- Automotive
- Industrial Networks

Table 1. KEY TECHNICAL CHARACTERISTICS

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------------------|---|-------|-----|-----------------|------|
| 3.3 V VERSION | | | | | |
| V _{BB} | Nominal battery operating voltage | 5 | 12 | 28 | V |
| V _{BB} | Load dump protection (Note 1) | | | 45 | V |
| I _{BB_SLP} | Supply current in sleep mode | | | 20 | μA |
| V _{CC_OUT} (Note 2) | Regulated V _{CC} output in normal mode, V _{CC} load 0–100 mA | 3.234 | 3.3 | 3.366 | V |
| | Regulated V _{CC} output in normal mode, 100 mA < V _{CC} load < 150 mA | 3.201 | 3.3 | 3.399 | |
| I _{OUT_LIM} | V _{CC} regulator current limitation | 150 | 225 | 300 | mA |
| V _{WAKE} | Operating DC voltage on WAKE pin | 0 | | V _{BB} | V |
| | Maximum rating voltage on WAKE pin | –45 | | 45 | |
| V _{INH} | Operating DC voltage on INH pin | 0 | | V _{BB} | V |
| T _{J_tsd} | Junction thermal shutdown temperature | 165 | | 195 | °C |
| T _J | Operating junction temperature | –40 | | +150 | °C |

5 V VERSION

| | | | | | |
|---------------------------------|---|------|-----|-----------------|----|
| V _{BB} | Nominal battery operating voltage | 6 | 12 | 28 | V |
| V _{BB} | Load dump protection (Note 1) | | | 45 | V |
| I _{BB_SLP} | Supply current in sleep mode | | | 20 | μA |
| V _{CC_OUT} (Note 2) | Regulated V _{CC} output in normal mode, V _{CC} load 0–100 mA | 4.90 | 5 | 5.10 | V |
| | Regulated V _{CC} output in normal mode, 100 mA < V _{CC} load < 150 mA | 4.85 | 5 | 5.15 | V |
| I _{OUT_LIM} | V _{CC} regulator current limitation | 150 | 225 | 300 | mA |
| V _{WAKE} | Operating DC voltage on WAKE pin | 0 | | V _{BB} | V |
| | Maximum rating voltage on WAKE pin | –45 | | 45 | |
| V _{INH} | Operating DC voltage on INH pin | 0 | | V _{BB} | V |
| T _{J_TSD} | Junction thermal shutdown temperature | 165 | | 195 | °C |
| T _J | Operating junction temperature | –40 | | +150 | °C |

1. The applied transients shall be in accordance with ISO 7637 part 1, test pulse 5. The device complies with functional class C;. The LIN communication itself complies with functional class B. On regulator class A can be reached depending on the application and external components
2. V_{CC} voltage must be properly stabilized by external capacitors: capacitor of min. 80 nF with ESR < 10 mΩ in parallel with a capacitor of min. 8 μF, ESR < 1 Ω.

Table 2. THERMAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Value | Unit |
|-------------------------|--|------------|-------|------|
| R _{th(vj-a)_1} | Thermal resistance junction–to–ambient on JEDEC 1S0P PCB | Free Air | 138 | K/W |
| R _{th(vj-a)_2} | Thermal resistance junction–to–ambient on JEDEC 1S0P + 300 mm ² PCB | Free Air | 94 | K/W |
| R _{th(vj-a)_3} | Thermal resistance junction–to–ambient on JEDEC 2S2P PCB | Free Air | 70 | K/W |
| R _{th(vj-a)_4} | Thermal resistance junction–to–ambient on JEDEC 2S2P + 300 mm ² PCB | Free Air | 49 | K/W |

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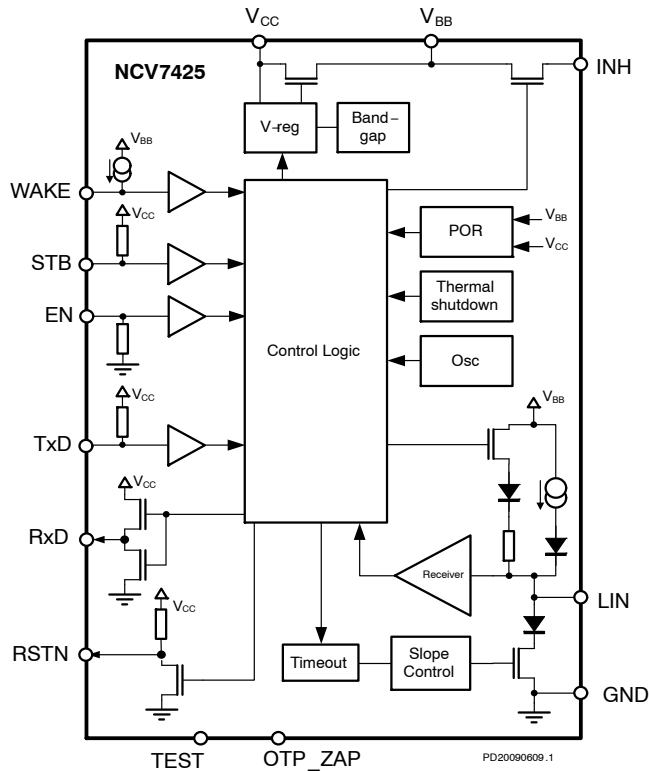


Figure 1. Block Diagram

TYPICAL APPLICATION

Application Information

The EMC immunity of the Master-mode device can be further enhanced by adding a capacitor between the LIN output and ground. The optimum value of this capacitor is determined by the length and capacitance of the LIN bus, the number and capacitance of Slave devices, the pull-up resistance of all devices (Master and Slave), and the required time constant of the system, respectively.

V_{CC} voltage must be properly stabilized by external capacitors: capacitor of min. 80 nF (ESR < 10 mΩ) in parallel with a capacitor of min. 8 μF (ESR < 1 Ω).

The 10 μF capacitor on the battery is optional and serves as reservoir capacitor to deal with battery supply micro-cuts.

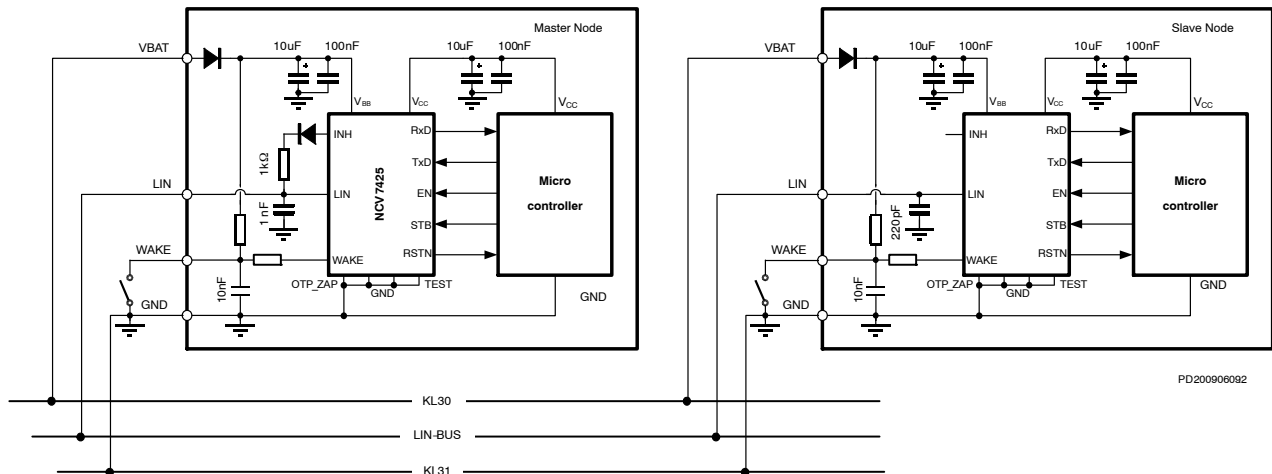


Figure 2. Application Diagram

NCV7425

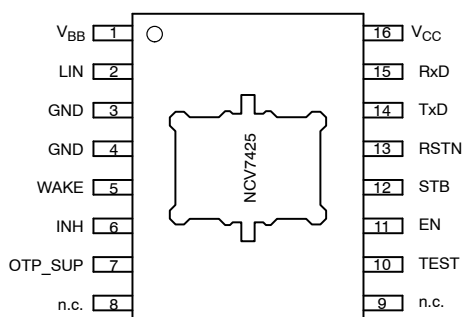


Figure 3. Pin Assignment

Table 3. PIN FUNCTION DESCRIPTION

| Pin Number | Pin Name | Description |
|------------|-----------------|---|
| 1 | V _{BB} | Battery supply input |
| 2 | LIN | LIN bus output/input |
| 3 | GND | Ground |
| 4 | GND | Ground |
| 5 | WAKE | High voltage digital input pin to switch the part from sleep- to standby mode |
| 6 | INH | Inhibit output |
| 7 | OTP_SUP | Supply for programming of trimming bits at factory testing, needs to be grounded in the application |
| 8 | n.c. | not connected |
| 9 | n.c. | not connected |
| 10 | TEST | Digital input for factory testing, needs to be grounded in the application |
| 11 | EN | Enable input for mode control |
| 12 | STB | Standby mode control input |
| 13 | RSTN | Reset output; open-drain output with an on-chip pull-up resistor |
| 14 | TxD | Transmit data input, low in dominant state |
| 15 | RxD | Receive data output; low in dominant state; push-pull output |
| 16 | V _{CC} | Voltage regulator output |

FUNCTIONAL DESCRIPTION

Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications. The domain is class-A multiplex buses with a single master node and a set of slave nodes.

NCV7425 is designed as a master or slave node for the LIN communication interface with an integrated 3.3 V or 5 V voltage regulator having a current capability up to 150 mA for supplying any external components (microcontroller, CAN node, etc.).

NCV7425 contains the LIN transmitter, LIN receiver, voltage regulator, power-on-reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for the maximum specified transmission speed of 20 kBaud

with EMC performance due to reduced slew rate of the LIN output.

The junction temperature is monitored via a thermal shutdown circuit that switches the LIN transmitter and voltage regulator off when temperature exceeds the TSD trigger level.

NCV7425 has four operating states (normal mode, low slope mode, stand-by mode, and sleep mode) that are determined by the input signals EN, WAKE, STB, and TxD.

Operating States

NCV7425 provides four operating states, two modes for normal operation with communication, one stand-by without communication and one low power mode with very low current consumption – see Figure 4 and Table 4.

Table 4. MODE SELECTION

| Mode | V _{CC} | RxD | INH | LIN Transceiver | 30 kΩ on LIN | RSTN |
|-----------------------------|-----------------|--|---|-----------------|--------------|---|
| Normal – Slope (Note 3) | ON | Low = Dominant State High = Recessive State | High if STB = High during state transition; Floating otherwise | Normal Slope | ON | High |
| Normal – Low Slope (Note 4) | ON | Low = Dominant State High = Recessive State | High if STB = High during state transition; Floating otherwise | Low Slope | ON | High |
| Stand-by (Note 5) | ON | Low after LIN wake-up, high otherwise (Note 6) | Floating | OFF | OFF | Controlled by V _{CC} under-voltage monitor |
| Sleep | OFF | Clamped to V _{CC} (Note 6) | Floating | OFF | OFF | Low |

- The normal slope mode is entered when pin EN goes HIGH while TxD is in HIGH state during EN transition.
- The low slope mode is entered when pin EN goes HIGH while TxD is in LOW state during EN transition. LIN transmitter gets on only after TxD returns to high after the state transition.
- The stand-by mode is entered automatically after power-up.
- In Stand-by and Sleep mode, the High state is achieved by internal pull-up resistor to V_{CC}.

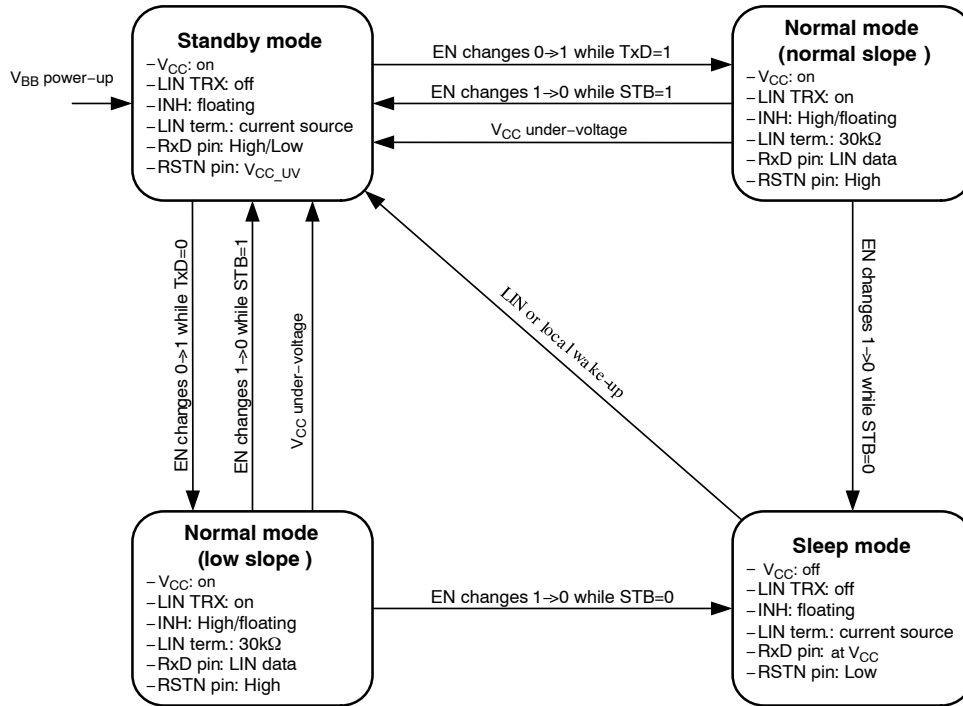


Figure 4. State Diagram

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Normal Slope Mode

In normal slope mode the transceiver can transmit and receive data via LIN bus with speed up to 20 kBaud. The transmit data stream of the LIN protocol is present on the TxD pin and converted by the transmitter into a LIN bus signal with controlled slew rate to minimize EMC emission. The receiver consists of the comparator that has a threshold with hysteresis in respect to the supply voltage and an input filter to remove bus noise. The LIN output is pulled HIGH via an internal 30 kΩ pull-up resistor. For master applications it is needed to put an external 1 kΩ resistor with a serial diode between LIN and V_{BB} (or INH) – see Figure 2.

The mode selection is done by EN=HIGH when TxD pin is HIGH. If STB pin is high during the standby-to-normal slope mode transition, INH pin is pulled high. Otherwise, it stays floating.

Low Slope Mode

In low slope mode the slew rate of the signal on the LIN bus is reduced (rising and falling edges of the LIN bus signal are longer). This further reduces the EMC emission. As a consequence the maximum speed on the LIN bus is reduced up to 10 kBaud. This mode is suited for applications where the communication speed is not critical. The mode selection

is done by EN=HIGH when TxD pin is LOW. In order not to transmit immediately a dominant state on the bus (because TxD = LOW), the LIN transmitter is enabled only after TxD returns to HIGH. If STB pin is high during the standby-to-low slope mode transition, INH pin is pulled high. Otherwise, it stays floating.

Stand-by Mode

The stand-by mode is always entered after power-up of the NCV7425. It can also be entered from normal mode when the EN pin is low and the stand-by pin is high. From sleep mode it can be entered after a local wake-up or LIN wakeup. In stand-by mode the V_{CC} voltage regulator for supplying external components (e.g. a microcontroller) stays active. Also the LIN receiver stays active to be able to detect a remote wake-up via bus. The LIN transmitter is disabled and the slave internal termination resistor of 30 kΩ between LIN and V_{BB} is disconnected in order to minimize current consumption. Only a pull-up current source between V_{BB} and LIN is active.

Sleep Mode

The Sleep Mode provides extremely low current consumption. This mode is entered when both EN and STB pins are LOW coming from normal mode. The internal termination resistor of 30 kΩ between LIN and V_{BB} is disconnected and also the V_{CC} regulator is switched off to minimize current consumption.

Wake-up

NCV7425 has two possibilities to wake-up from sleep or stand-by mode (see Figure 4):

Local wake-up: enables the transition from sleep mode to stand-by mode

Remote wake-up via LIN: enables the transition from sleep- to stand-by mode and can be also detected when already in standby mode.

A local wake-up is **only** detected in sleep mode if a transition from LOW to HIGH or from HIGH to LOW is seen on the wake pin.

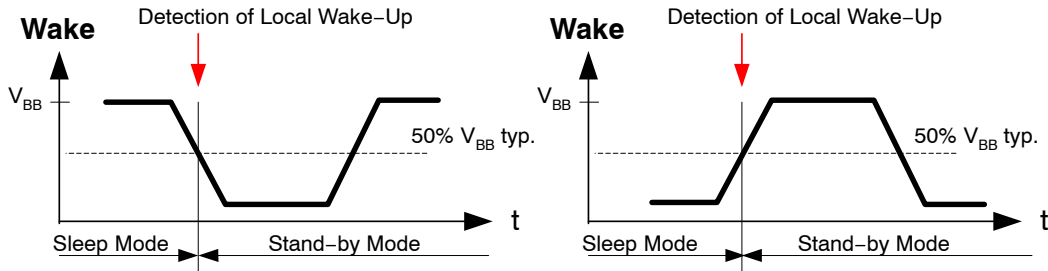


Figure 5. Local Wake-Up Signal

PC20060427.3

A remote wake-up is **only** detected if a combination of (1) a falling edge at the LIN pin (transition from recessive to dominant) is followed by (2) a dominant level maintained

for a time period > t_{WAKE} and (3) again a rising edge at pin LIN (transition from dominant to recessive) happens.

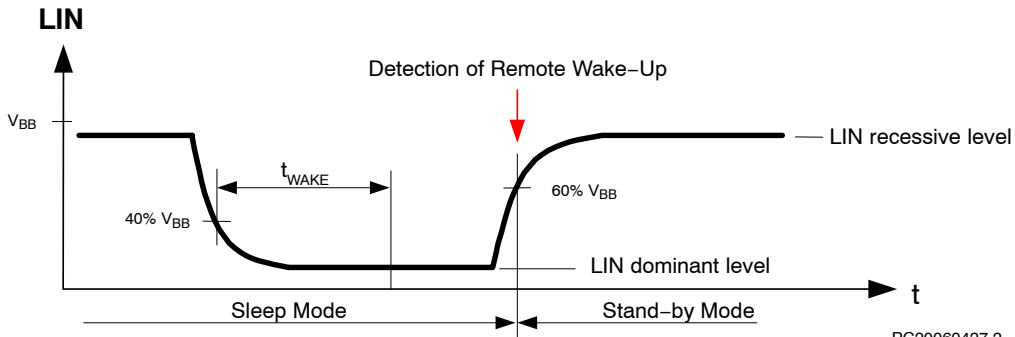


Figure 6. Remote Wake-Up Behavior

PC20060427.2

The wake-up source is distinguished by pin RxD in the stand-by mode:

RxD remains HIGH after power-up or local wake-up.

RxD is kept LOW until normal mode is entered after a remote wake-up (LIN)

V_{CC} Under-voltage Detection and RSTN Pin

In standby, normal and low-slope modes, the V_{CC} regulator is monitored. Whenever the regulator output falls below V_{CC_UV_THR} level (typically 90% of the nominal voltage) for longer than V_{CC_UV_deb} (typically 5 μs), an

NCV7425

under-voltage is detected. Output pin RSTN is pulled to Low level to indicate the under-voltage condition to the external load (a microcontroller). At the same time, the device enters automatically the standby mode. As soon as the regulator output returns above the under-voltage level, the RSTN Low level is extended by typically 6ms and only then released to High level in order to ensure microcontroller initialization under correct supply conditions.

In the sleep mode, RSTN pin is kept Low regardless the V_{CC} level – it means that RSTN becomes Low immediately at sleep mode entry even if the V_{CC} capacitor is still charged.

In all situations where RSTN pin is kept Low, the digital inputs to NCV7425 are discarded by the internal control logic and have no effect on its behavior.

The RSTN pin function is illustrated in Figure 7.

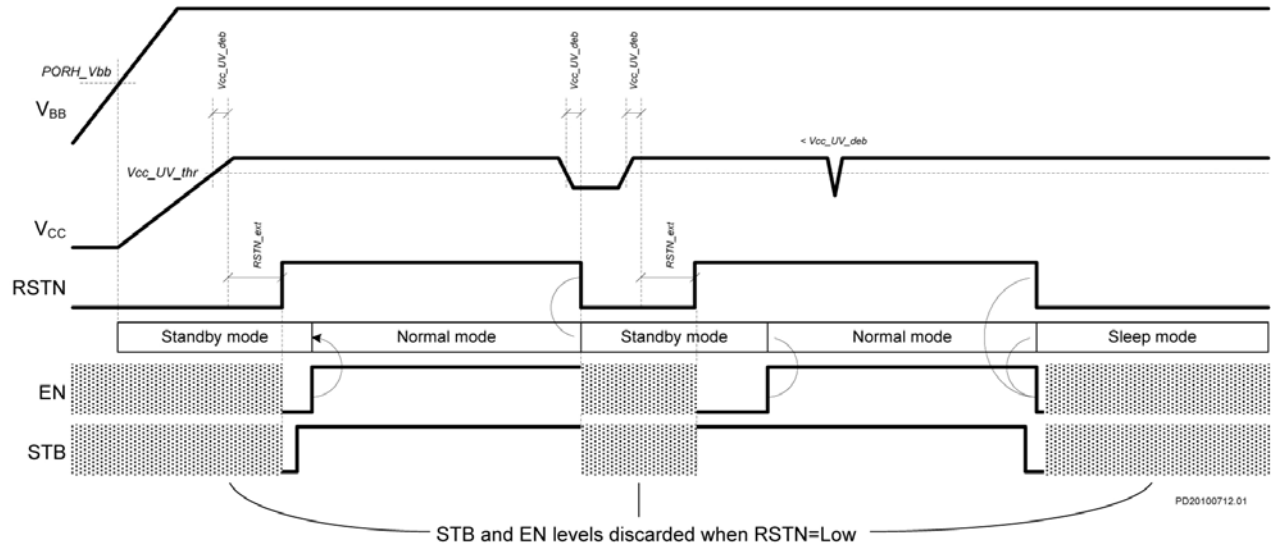


Figure 7. RSTN Pin Behavior

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND. Positive currents flow into the IC.

Table 5. ABSOLUTE MAXIMUM RATINGS – 3.3 V and 5 V VERSIONS

| Symbol | Parameter | Min. | Max. | Unit |
|---------------------|---|------|-----------------------|------|
| V _{BB} | Battery voltage on pin V _{BB} (Note 7) | -0.3 | +45 | V |
| V _{CC} | DC voltage on pin V _{CC} | 0 | +6 | V |
| I _{VCC} | Current delivered by the V _{CC} regulator | 150 | | mA |
| V _{LIN} | LIN bus voltage (Note 8) | -45 | +45 | V |
| V _{INH} | DC voltage on inhibit pin | -0.3 | V _{BB} + 0.3 | V |
| V _{WAKE} | Voltage on WAKE pin | -45 | 45 | V |
| V _{Dig_IO} | DC voltage on pins TxD, RxD, EN, STB, RSTN | -0.3 | V _{CC} + 0.3 | V |
| T _J | Maximum junction temperature | -40 | +165 | °C |
| V _{esd} | Electrostatic discharge voltage (INH, WAKE and V _{BB}) system Human Body Model (HBM) (Note 9) | -10 | +10 | kV |
| | Electrostatic discharge voltage (LIN pin, no external capacitor) HBM (Note 9) | -10 | +10 | |
| | Electrostatic discharge voltage (LIN pin, 220 pF) System HBM (Note 9) | -15 | +15 | |
| | Electrostatic discharge voltage (pins LIN, INH, WAKE and V _{BB}) HBM (Note 10) | -8 | +8 | |
| | Electrostatic discharge voltage (other pins) HBM (Note 10) | -4 | +4 | |
| | Electrostatic discharge voltage; charge device model (Note 11) | -250 | +250 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

7. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, and 5. The device complies with functional class C; class A can be reached depending on the application and external components.
8. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b. The device complies with functional class C; class A can be reached depending on the application and external components.
9. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor conform to IEC Standard 61000-4-2. The specified values are verified by external test house.
10. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor conform to MIL STD 883 method 3015.7.
11. Conform to EOS/ESD-DS5.3 (socket mode).

Table 6. DC CHARACTERISTICS – 3.3 V VERSION

V_{BB} = 5 V to 28 V; T_J = -40°C to +150°C; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--------------------------|---|-------|------|-------|------|
| DC CHARACTERISTICS SUPPLY – PINS V_{BB} AND V_{CC} | | | | | | |
| I _{BB_ON} | Supply current | Normal mode; LIN recessive | | | 1.6 | mA |
| I _{BB_STB} | Supply current | Stand-by mode, V _{BB} = 5 – 18 V, T _J < 105°C | | | 60 | μA |
| I _{BB_SLP} | Supply current | Sleep mode, V _{BB} = 5 – 18 V, T _J < 105°C | | | 20 | μA |
| DC CHARACTERISTICS – VOLTAGE REGULATOR | | | | | | |
| V _{CC_OUT} | Regulator output voltage | V _{CC} load 0 – 100 mA | 3.234 | 3.30 | 3.366 | V |
| | | 100 mA < V _{CC} load < 150 mA | 3.201 | 3.30 | 3.399 | |

12. Measured at output voltage V_{CC_OUT} = (V_{CC_OUT} @ V_{BB} = 5 V) – 2%.

13. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull up resistor. The drop at the switch is negligible. See Figure 2.

14. Guaranteed by design. Not tested

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Table 6. DC CHARACTERISTICS – 3.3 V VERSION

$V_{BB} = 5\text{ V to }28\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

DC CHARACTERISTICS – VOLTAGE REGULATOR

| | | | | | | |
|----------------------|---|--|------|------|------|----|
| I_{OUT_LIM} | Over-current limitation | | 150 | 225 | 300 | mA |
| $V_{CC_UV_THR}$ | Under-voltage detection threshold | | 2.80 | 2.97 | 3.13 | V |
| ΔV_{CC_OUT} | Line Regulation | $V_{BB} = 5 - 28\text{ V}$, $I_{out} = 5\text{ mA}$ $T_J = 25^\circ\text{C}$ | | 0.41 | | mV |
| | Load Regulation | $I_{out} = 1 - 100\text{ mA}$, $V_{BB} = 14\text{ V}$, $T_J = 25^\circ\text{C}$ | | 25 | | |
| V_{do} | Dropout Voltage ($V_{BB} - V_{CC_OUT}$) (Note 12) Figure 12 | $I_{out} = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 22 | | mV |
| | | $I_{out} = 50\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 108 | | |
| | | $I_{out} = 100\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 216 | | |

DC CHARACTERISTICS – LIN TRANSMITTER

| | | | | | | |
|-----------------------|---|--|-----|----|-----|---------------|
| $V_{LIN_dom_LoSup}$ | LIN dominant output voltage | TxD = low; $V_{BB} = 7.3\text{ V}$ | | | 1.2 | V |
| $V_{LIN_dom_HiSup}$ | LIN dominant output voltage | TxD = low; $V_{BB} = 18\text{ V}$ | | | 2.0 | V |
| V_{ser_diode} | LIN Voltage drop at serial diode (Note 13) | TxD = high; $I_{LIN} = 10\text{ }\mu\text{A}$ | 0.3 | | 1 | V |
| I_{LIN_lim} | Short circuit current limitation | $V_{LIN} = V_{BB(max)}$ | 40 | | 200 | mA |
| R_{slave} | Internal pull-up resistance | | 20 | 33 | 47 | k Ω |
| C_{LIN} | Capacitance on pin LIN (Note 14) | | | 25 | 35 | pF |
| $I_{LIN_off_dom}$ | LIN output current bus in dominant state | Driver off; $V_{BB} = 12\text{ V}$ | -1 | | | mA |
| $I_{LIN_off_rec}$ | LIN output current bus in recessive state | Driver off; $V_{BB} < 18\text{ V}$, $V_{BB} < V_{LIN} < 18\text{ V}$ | | | 1 | μA |
| $I_{LIN_no_GND}$ | Communication not affected | $V_{BB} = GND = 12\text{ V}$; $0 < V_{LIN} < 18\text{ V}$ | -1 | | 1 | mA |
| $I_{LIN_no_VBB}$ | LIN bus remains operational | $V_{BB} = GND = 0\text{ V}$; $0 < V_{LIN} < 18\text{ V}$ | | | 5 | μA |

DC CHARACTERISTICS – LIN RECEIVER

| | | | | | | |
|----------------|---------------------------------|---|-------|--|-------|----------|
| V_{BUS_dom} | bus voltage for dominant state | | | | 0.4 | V_{BB} |
| V_{BUS_rec} | bus voltage for recessive state | | 0.6 | | | V_{BB} |
| V_{rec_dom} | Receiver threshold | LIN bus recessive \rightarrow dominant | 0.4 | | 0.6 | V_{BB} |
| V_{rec_rec} | Receiver threshold | LIN bus dominant \rightarrow recessive | 0.4 | | 0.6 | V_{BB} |
| V_{rec_cnt} | Receiver centre voltage | $(V_{BUS_dom} + V_{BUS_rec}) / 2$ | 0.475 | | 0.525 | V_{BB} |
| V_{rec_hys} | Receiver hysteresis | | 0.05 | | 0.175 | V_{BB} |

DC CHARACTERISTICS – DIGITAL I/O PINS

PIN WAKE

| | | | | | | |
|-----------------|-----------------------|--|------|------|------|---------------|
| V_{WAKE_TH} | Threshold voltage | | 0.35 | | 0.65 | V_{BB} |
| I_{leak} | Input leakage current | $V_{WAKE} = 0\text{ V}$; $V_{BB} = 18\text{ V}$ | -1 | -0.5 | 1 | μA |
| $T_{WAKE(min)}$ | Debounce time | Sleep mode; rising and falling edge | 8 | | 54 | μs |

PINS TxD AND STB

| | | | | | | |
|----------|-------------------------|--|--|--|-----|---|
| V_{il} | Low level input voltage | | | | 0.8 | V |
|----------|-------------------------|--|--|--|-----|---|

12. Measured at output voltage $V_{CC_OUT} = (V_{CC_OUT} @ V_{BB} = 5\text{ V}) - 2\%$.

13. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull up resistor. The drop at the switch is negligible. See Figure 2.

14. Guaranteed by design. Not tested

Table 6. DC CHARACTERISTICS – 3.3 V VERSION

$V_{BB} = 5\text{ V to }28\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

DC CHARACTERISTICS – DIGITAL I/O PINS

PINS Tx/D AND STB

| | | | | | | |
|----------|--------------------------------|--|-----|--|-----|------------|
| V_{ih} | High level input voltage | | 2.0 | | | V |
| R_{pu} | Pull-up resistance to V_{CC} | | 50 | | 200 | k Ω |

PIN INH

| | | | | | | |
|--------------|-------------------------|------------------------------------|----|------|------|---------------|
| Delta_ V_H | High level voltage drop | $I_{INH} = 15\text{ mA}$ | | 0.35 | 0.75 | V |
| I_{leak} | Leakage current | Sleep mode; $V_{INH} = 0\text{ V}$ | -1 | | 1 | μA |

PIN EN

| | | | | | | |
|----------|--------------------------------|--|-----|--|-----|------------|
| V_{il} | Low level input voltage | | | | 0.8 | V |
| V_{ih} | High level input voltage | | 2.0 | | | V |
| R_{pd} | Pull-down resistance to ground | | 50 | | 200 | k Ω |

PIN Rx/D

| | | | | | | |
|----------|--|--|-----------------|----|------|------------|
| V_{ol} | Low level output voltage | $I_{sink} = 2\text{ mA}$ | | | 0.65 | V |
| V_{oh} | High level output voltage (In Normal mode) | Normal mode, $I_{source} = -2\text{ mA}$ | $V_{CC} - 0.65$ | | | V |
| R_{pu} | Pull-up resistance to V_{CC} (In Standby and Sleep mode) | Standby mode, Sleep mode | | 10 | | k Ω |

PIN RSTN

| | | | | | | |
|----------|--------------------------------|--------------------------|----|--|------|------------|
| V_{ol} | Low level output voltage | $I_{sink} = 2\text{ mA}$ | | | 0.65 | V |
| R_{pu} | Pull-up resistance to V_{CC} | | 50 | | 200 | k Ω |

DC CHARACTERISTICS

POWER-ON RESET

| | | | | | | |
|-----------------------|---|--|-----|--|-----|------------------|
| POR _{H_VBB} | V_{BB} POR high level detection threshold | | | | 4.5 | V |
| POR _{L_VBB} | V_{BB} POR low level detection threshold | | 1.7 | | 3.8 | V |
| POR _{VBB_sl} | Maximum slope on V_{BB} to guarantee POR | | | | 2 | V/ μs |

THERMAL SHUTDOWN

| | | | | | | |
|---------------|-----------------------------|--------------|-----|--|-----|------------------|
| T_{J_tsd} | Junction temperature | For shutdown | 165 | | 195 | $^\circ\text{C}$ |
| T_{J_hyst} | Thermal shutdown hysteresis | | 9 | | 18 | $^\circ\text{C}$ |

12. Measured at output voltage $V_{CC_OUT} = (V_{CC_OUT} @ V_{BB} = 5\text{ V}) - 2\%$.

13. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull up resistor. The drop at the switch is negligible. See Figure 2.

14. Guaranteed by design. Not tested

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Table 7. DC CHARACTERISTICS – 5 V VERSION

$V_{BB} = 6\text{ V to }28\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

DC CHARACTERISTICS SUPPLY – PINS V_{BB} AND V_{CC}

| | | | | | | |
|---------------|----------------|--|--|--|-----|---------------|
| I_{BB_ON} | Supply current | Normal mode; LIN recessive | | | 1.6 | mA |
| I_{BB_STB} | Supply current | Stand-by mode, $V_{BB} = 6 - 18\text{ V}$, $T_J < 105^\circ\text{C}$ | | | 60 | μA |
| I_{BB_SLP} | Supply current | Sleep mode, $V_{BB} = 6 - 18\text{ V}$, $T_J < 105^\circ\text{C}$ | | | 20 | μA |

DC CHARACTERISTICS – VOLTAGE REGULATOR

| | | | | | | |
|----------------------|--|--|------|------|------|----|
| V_{CC_OUT} | Regulator output voltage | V_{CC} load 0 – 100 mA | 4.9 | 5 | 5.1 | V |
| | | 100 mA < V_{CC} load < 150 mA | 4.85 | 5 | 5.15 | V |
| I_{OUT_LIM} | Over-current limitation | | 150 | 225 | 300 | mA |
| $V_{CC_UV_THR}$ | Under-voltage detection threshold | | 4.25 | 4.5 | 4.75 | V |
| ΔV_{CC_OUT} | Line Regulation | $V_{BB} 6 - 28\text{ V}$, $I_{out} = 5\text{ mA}$ $T_J = 25^\circ\text{C}$ | | 0.41 | | mV |
| | Load Regulation | $I_{out} 1 - 100\text{ mA}$, $V_{BB} = 14\text{ V}$, $T_J = 25^\circ\text{C}$ | | 22 | | mV |
| V_{do} | Dropout Voltage ($V_{BB} - V_{CC_OUT}$) (Note 15) (Figure 20) | $I_{out} = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 22 | | mV |
| | | $I_{out} = 50\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 108 | | mV |
| | | $I_{out} = 100\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 216 | | mV |

DC CHARACTERISTICS LIN TRANSMITTER

| | | | | | | |
|-----------------------|--|--|-----|----|-----|---------------|
| $V_{LIN_dom_LoSup}$ | LIN dominant output voltage | TxD = low; $V_{BB} = 7.3\text{ V}$ | | | 1.2 | V |
| $V_{LIN_dom_HiSup}$ | LIN dominant output voltage | TxD = low; $V_{BB} = 18\text{ V}$ | | | 2.0 | V |
| V_{ser_diode} | LIN Voltage drop at serial diode (Note 16) | TxD = high; $I_{LIN} = 10\ \mu\text{A}$ | 0.3 | | 1 | V |
| I_{LIN_lim} | Short circuit current limitation | $V_{LIN} = V_{BB(max)}$ | 40 | | 200 | mA |
| R_{slave} | Internal pull-up resistance | | 20 | 33 | 47 | k Ω |
| C_{LIN} | Capacitance on pin LIN (Note 17) | | | 25 | 35 | pF |
| $I_{LIN_off_dom}$ | LIN output current bus in dominant state | Driver off; $V_{BB} = 12\text{ V}$ | -1 | | | mA |
| $I_{LIN_off_rec}$ | LIN output current bus in recessive state | Driver off; $V_{BB} < 18\text{ V}$, $V_{BB} < V_{LIN} < 18\text{ V}$ | | | 1 | μA |
| $I_{LIN_no_GND}$ | Communication not affected | $V_{BB} = GND = 12\text{ V}$; $0 < V_{LIN} < 18\text{ V}$ | -1 | | 1 | mA |
| $I_{LIN_no_VBB}$ | LIN bus remains operational | $V_{BB} = GND = 0\text{ V}$; $0 < V_{LIN} < 18\text{ V}$ | | | 5 | μA |

DC CHARACTERISTICS LIN RECEIVER

| | | | | | | |
|----------------|---------------------------------|--|-------|--|-------|----------|
| V_{BUS_dom} | bus voltage for dominant state | | | | 0.4 | V_{BB} |
| V_{BUS_rec} | bus voltage for recessive state | | 0.6 | | | V_{BB} |
| V_{rec_dom} | Receiver threshold | LIN bus recessive \rightarrow dominant | 0.4 | | 0.6 | V_{BB} |
| V_{rec_rec} | Receiver threshold | LIN bus dominant \rightarrow recessive | 0.4 | | 0.6 | V_{BB} |
| V_{rec_cnt} | Receiver center voltage | $(V_{BUS_dom} + V_{BUS_rec}) / 2$ | 0.475 | | 0.525 | V_{BB} |
| V_{rec_hys} | Receiver hysteresis | | 0.05 | | 0.175 | V_{BB} |

15. Measured at output voltage $V_{CC_OUT} = (V_{CC_OUT} @ V_{BB} = 6\text{ V}) - 2\%$.

16. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull up resistor. The drop at the switch is negligible. See Figure 2.

17. Guaranteed by design. Not tested

NCV7425

Table 7. DC CHARACTERISTICS – 5 V VERSION

$V_{BB} = 6\text{ V to }28\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

DC CHARACTERISTICS – DIGITAL I/O PINS

PIN WAKE

| | | | | | | |
|-----------------|-----------------------|--|------|------|------|---------------|
| V_{WAKE_TH} | Threshold voltage | | 0.35 | | 0.65 | V_{BB} |
| I_{leak} | Input leakage current | $V_{WAKE} = 0\text{ V}$; $V_{BB} = 18\text{ V}$ | -1 | -0.5 | 1 | μA |
| T_{WAKE_MIN} | Debounce time | Sleep mode; rising and falling edge | 8 | | 54 | μs |

PINS Tx/D AND STB

| | | | | | | |
|----------|--------------------------------|--|-----|--|-----|-----------|
| V_{il} | Low level input voltage | | | | 0.8 | V |
| V_{ih} | High level input voltage | | 2.0 | | | V |
| R_{pu} | Pull-up resistance to V_{CC} | | 50 | | 200 | $k\Omega$ |

PIN INH

| | | | | | | |
|------------|-------------------------|------------------------------------|----|------|------|---------------|
| Delta_VH | High level voltage drop | $I_{INH} = 15\text{ mA}$ | | 0.35 | 0.75 | V |
| I_{leak} | Leakage current | Sleep mode; $V_{INH} = 0\text{ V}$ | -1 | | 1 | μA |

PIN EN

| | | | | | | |
|----------|--------------------------------|--|-----|--|-----|-----------|
| V_{il} | Low level input voltage | | | | 0.8 | V |
| V_{ih} | High level input voltage | | 2.0 | | | V |
| R_{pd} | Pull-down resistance to ground | | 50 | | 200 | $k\Omega$ |

PIN Rx/D

| | | | | | | |
|----------|--|--|-----------------|----|------|-----------|
| V_{ol} | Low level output voltage | $I_{sink} = 2\text{ mA}$ | | | 0.65 | V |
| V_{oh} | High level output voltage (In Normal mode) | Normal mode, $I_{source} = -2\text{ mA}$ | $V_{CC} - 0.65$ | | | V |
| R_{pu} | Pull-up resistance to V_{CC} (In Standby and Sleep mode) | Standby mode, Sleep mode | | 10 | | $k\Omega$ |

PIN RSTN

| | | | | | | |
|----------|--------------------------------|--------------------------|----|--|------|-----------|
| V_{ol} | Low level output voltage | $I_{sink} = 2\text{ mA}$ | | | 0.65 | V |
| R_{pu} | Pull-up resistance to V_{CC} | | 50 | | 200 | $k\Omega$ |

DC CHARACTERISTICS

POWER-ON RESET

| | | | | | | |
|-----------------|---|--|-----|--|-----|------------------------|
| POR_{H_VBB} | V_{BB} POR high level detection threshold | | | | 4.5 | V |
| POR_{L_VBB} | V_{BB} POR low level detection threshold | | 1.7 | | 3.8 | V |
| POR_{VBB_sl} | Maximum slope on V_{BB} to guarantee POR | | | | 2 | $\text{V}/\mu\text{s}$ |

THERMAL SHUTDOWN

| | | | | | | |
|---------------|-----------------------------|--------------|-----|--|-----|------------------|
| T_{J_tsd} | Junction temperature | For shutdown | 165 | | 195 | $^\circ\text{C}$ |
| T_{J_hyst} | Thermal shutdown hysteresis | | 9 | | 18 | $^\circ\text{C}$ |

15. Measured at output voltage $V_{CC_OUT} = (V_{CC_OUT} @ V_{BB} = 6\text{ V}) - 2\%$.

16. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull up resistor. The drop at the switch is negligible. See Figure 2.

17. Guaranteed by design. Not tested

NCV7425

Table 8. AC CHARACTERISTICS – 3.3 V AND 5 V VERSIONS

$V_{BB} = 7\text{ V to }18\text{ V}$; $T_J = -40^\circ\text{C to }+150^\circ\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--|-------|-----|-------|---------------|
| AC CHARACTERISTICS LIN TRANSMITTER | | | | | | |
| D1 | Duty Cycle 1 = $t_{BUS_rec(min)} / (2 \times T_{Bit})$ see Figure 24 | normal slope mode $TH_{rec(max)} = 0.744 \times V_{BB}$ $TH_{dom(max)} = 0.581 \times V_{BB}$ $T_{Bit} = 50\ \mu\text{s}$ $V_{BB} = 7\text{ V to }18\text{ V}$ | 0.396 | | 0.5 | |
| D2 | Duty Cycle 2 = $t_{BUS_rec(max)} / (2 \times T_{Bit})$ see Figure 24 | normal slope mode $TH_{rec(min)} = 0.422 \times V_{BB}$ $TH_{dom(min)} = 0.284 \times V_{BB}$ $T_{Bit} = 50\ \mu\text{s}$ $V_{BB} = 7.6\text{ V to }18\text{ V}$ | 0.5 | | 0.581 | |
| D3 | Duty Cycle 3 = $t_{BUS_rec(min)} / (2 \times T_{bit})$ see Figure 24 | normal slope mode $TH_{rec(max)} = 0.778 \times V_{BB}$ $TH_{dom(max)} = 0.616 \times V_{BB}$ $T_{Bit} = 96\ \mu\text{s}$ $V_{BB} = 7\text{ V to }18\text{ V}$ | 0.417 | | 0.5 | |
| D4 | Duty Cycle 4 = $t_{BUS_rec(max)} / (2 \times T_{bit})$ see Figure 24 | normal slope mode $TH_{rec(min)} = 0.389 \times V_{BB}$ $TH_{dom(min)} = 0.251 \times V_{BB}$ $T_{Bit} = 96\ \mu\text{s}$ $V_{BB} = 7.6\text{ V to }18\text{ V}$ | 0.5 | | 0.590 | |
| T_{fall_norm} | LIN falling edge | Normal slope mode; $V_{BB} = 12\text{ V}$; L1, L2 (Note 18) | | | 22.5 | μs |
| T_{rise_norm} | LIN rising edge | Normal slope mode; $V_{BB} = 12\text{ V}$; L1, L2 (Note 18) | | | 22.5 | μs |
| T_{sym_norm} | LIN slope symmetry | Normal slope mode; $V_{BB} = 12\text{ V}$; L1, L2 (Note 18) | -4 | | 4 | μs |
| T_{fall_norm} | LIN falling edge | Normal slope mode; $V_{BB} = 12\text{ V}$; L3 (Note 18) | | | 27 | μs |
| T_{rise_norm} | LIN rising edge | Normal slope mode; $V_{BB} = 12\text{ V}$; L3 (Note 18) | | | 27 | μs |
| T_{sym_norm} | LIN slope symmetry | Normal slope mode; $V_{BB} = 12\text{ V}$; L3 (Note 18) | -5 | | 5 | μs |
| T_{fall_low} | LIN falling edge | Low slope mode (Note 19); $V_{BB} = 12\text{ V}$; L3 (Note 18) | | | 62 | μs |
| T_{rise_low} | LIN rising edge | Low slope mode (Note 19); $V_{BB} = 12\text{ V}$; L3 (Note 18) | | | 62 | μs |
| T_{WAKE} | Dominant time-out for wake-up via LIN bus | | 30 | | 150 | μs |
| T_{dom} | TxD dominant time-out | TxD = low | 6 | | 20 | ms |
| $V_{CC_UV_deb}$ | V_{CC} under-voltage detection debounce time | | 1.5 | 5 | 10 | μs |
| R_{STN_ext} | Extension time of RSTN Low pulse beyond V_{CC} under-voltage | | 3 | 6 | 10 | ms |

AC CHARACTERISTICS LIN RECEIVER

| | | | | | | |
|-----------------------|--|---|-----|--|---|---------------|
| $T_{rec_prop_down}$ | Propagation delay of receiver falling edge | | 0.1 | | 6 | μs |
| $T_{rec_prop_up}$ | Propagation delay of receiver rising edge | | 0.1 | | 6 | μs |
| T_{rec_sym} | Propagation delay symmetry | $T_{rec_prop_down} - T_{rec_prop_up}$ | -2 | | 2 | μs |

18. The AC parameters are specified for following RC loads on the LIN bus: L1 = 1 k Ω / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF.

19. Low slope mode is not compliant to the LIN 1.3 or LIN 2.0/2.1 standard.

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS

(3.3 V Version)

Load Transient Responses

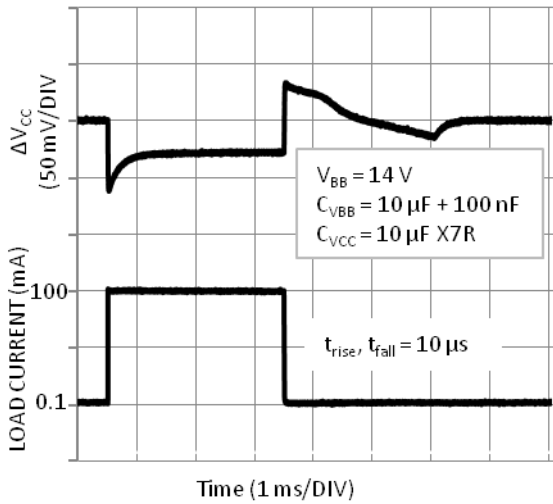


Figure 8. Load Transient Response
(I_{CC} 100 μ A to 100 mA)

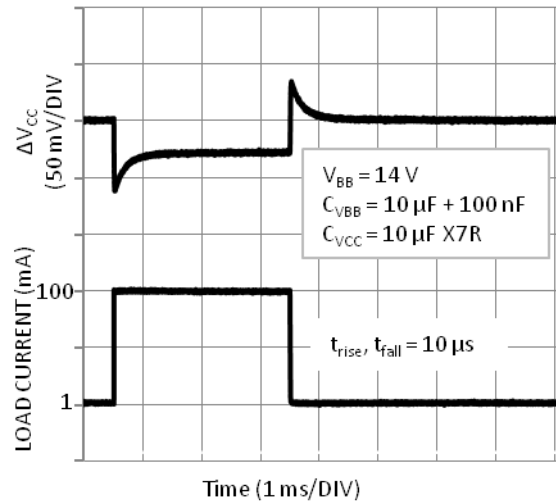


Figure 9. Load Transient Response
(I_{CC} 1 mA to 100 mA)

Line Transient Responses

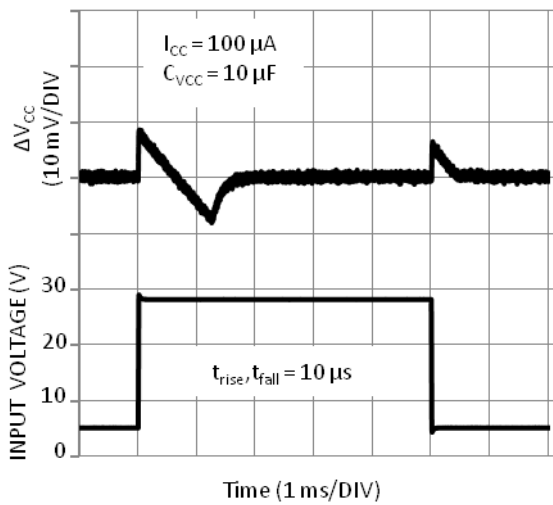


Figure 10. Line Transient Response
(V_{BB} 5 V to 28 V)

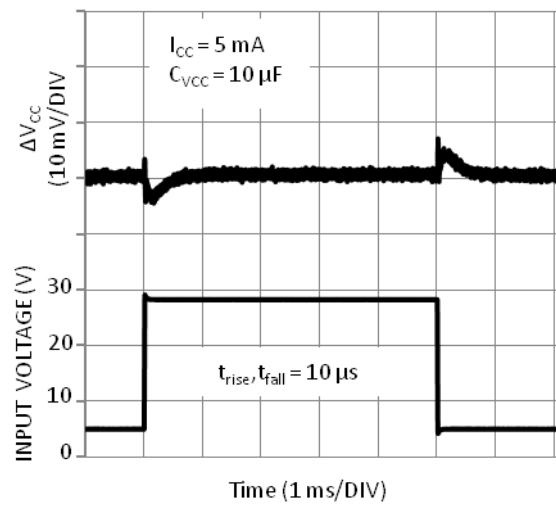


Figure 11. Line Transient Response
(V_{BB} 5 V to 28 V)

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS

(3.3 V Version)

Static Characteristics

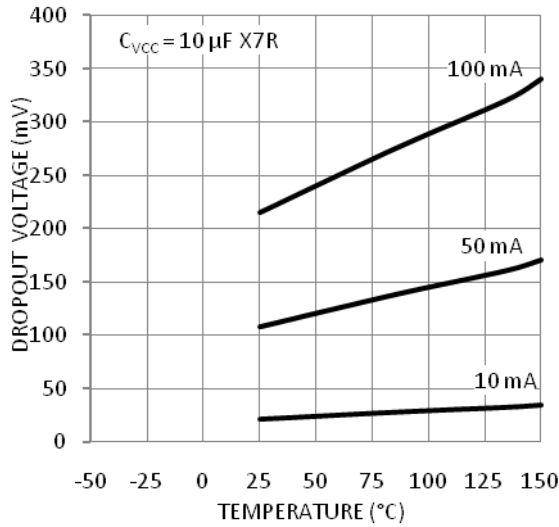


Figure 12. Dropout Voltage vs. Temperature

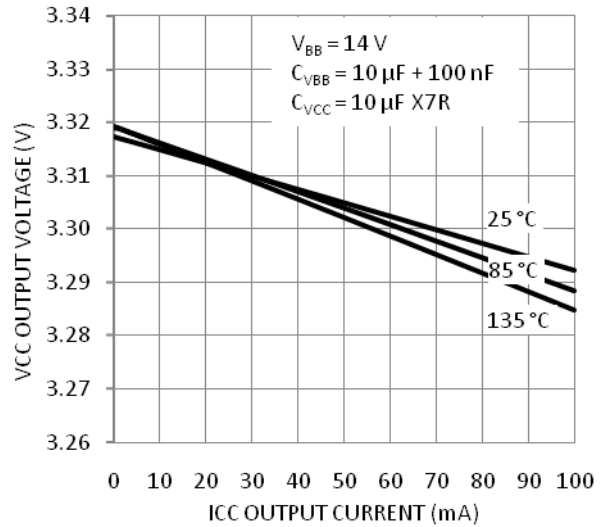


Figure 13. Output Voltage vs. Output Current

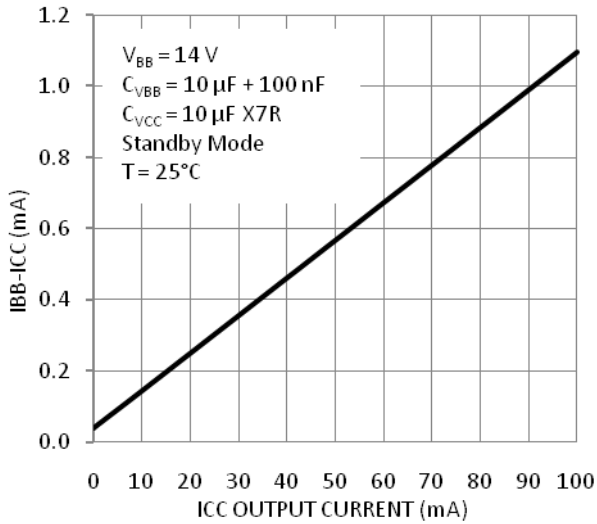


Figure 14. Ground Current vs. Output Current

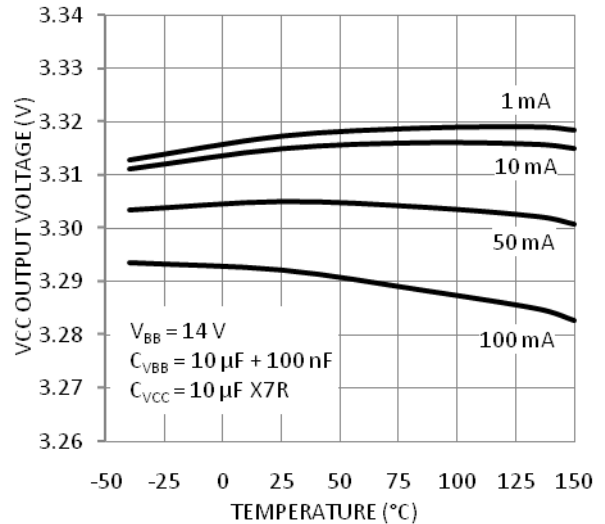


Figure 15. Output Voltage vs. Temperature

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS

(5 V Version)

Load Transient Responses

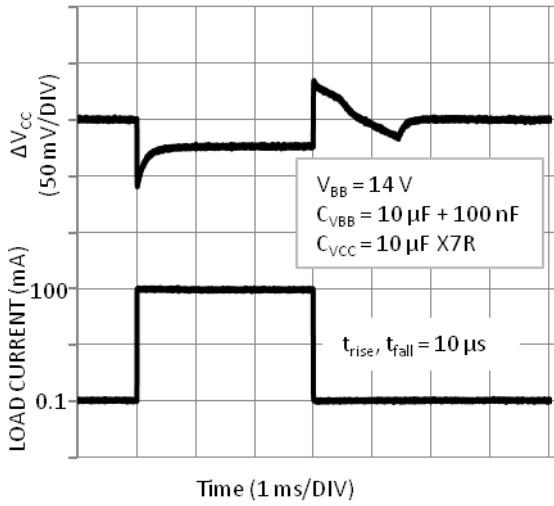


Figure 16. Load Transient Response
(I_{CC} 100 µA to 100 mA)

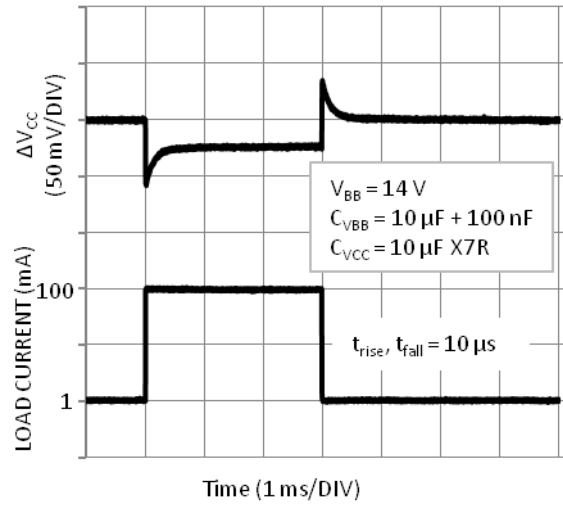


Figure 17. Load Transient Response
(I_{CC} 1 mA to 100 mA)

Line Transient Responses

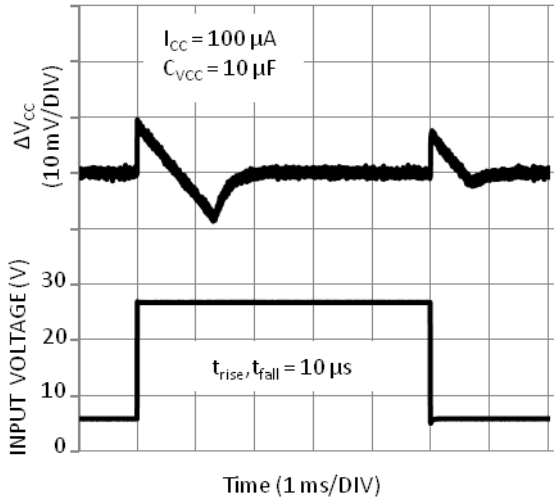


Figure 18. Line Transient Response
(V_{BB} 6 V to 28 V)

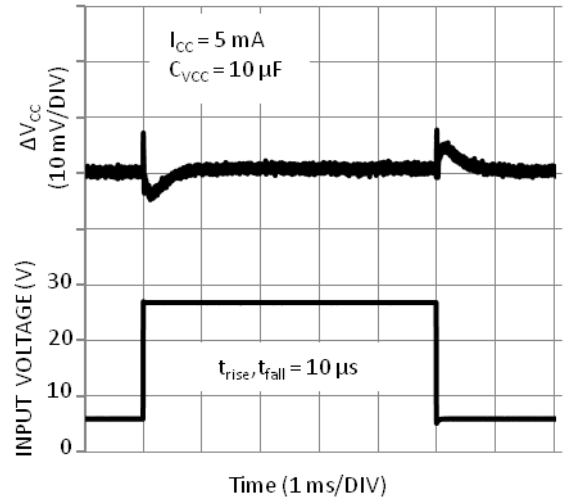


Figure 19. Line Transient Response
(V_{BB} 6 V to 28 V)

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS

(5 V Version)

Static Characteristics

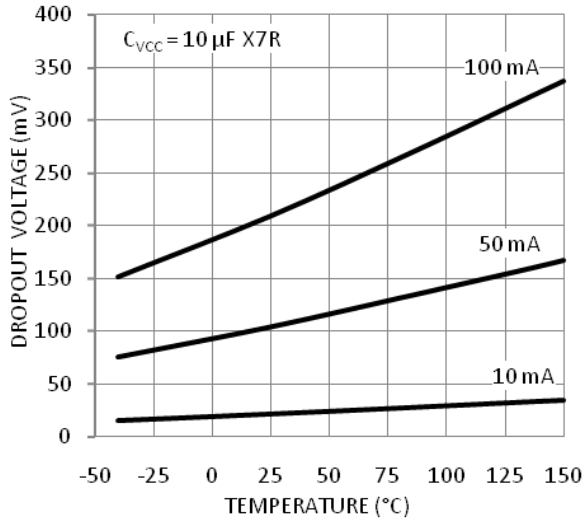


Figure 20. Dropout Voltage vs. Temperature

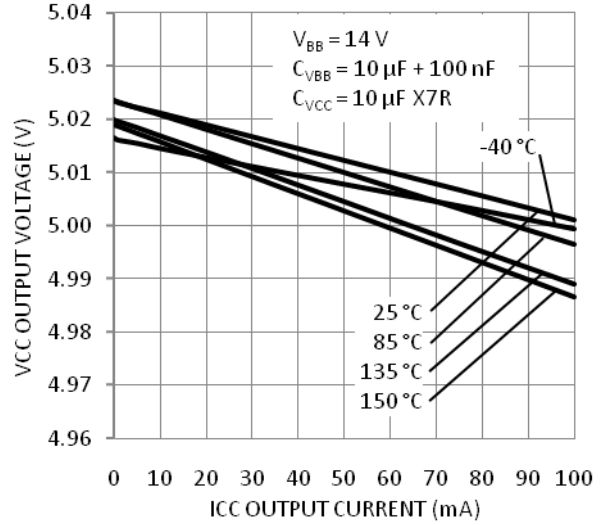


Figure 21. Output Voltage vs. Output Current

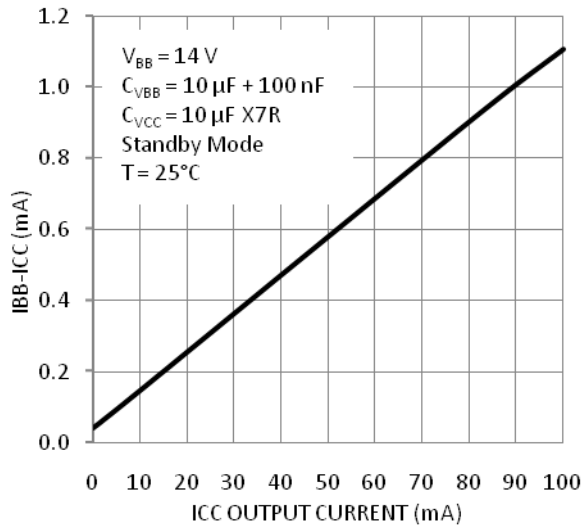


Figure 22. Ground Current vs. Output Current

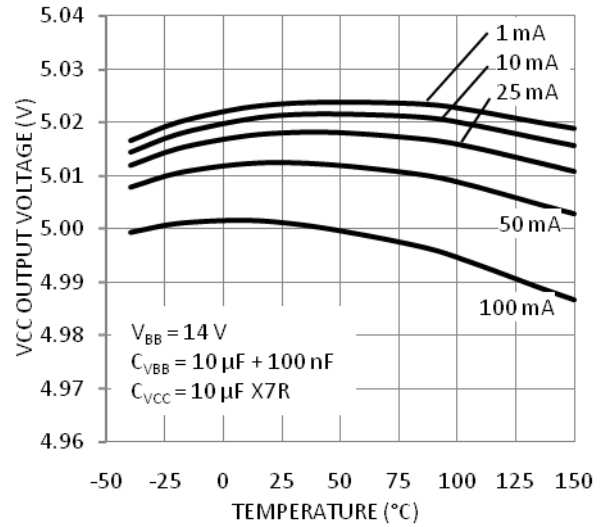


Figure 23. Output Voltage vs. Temperature

NCV7425

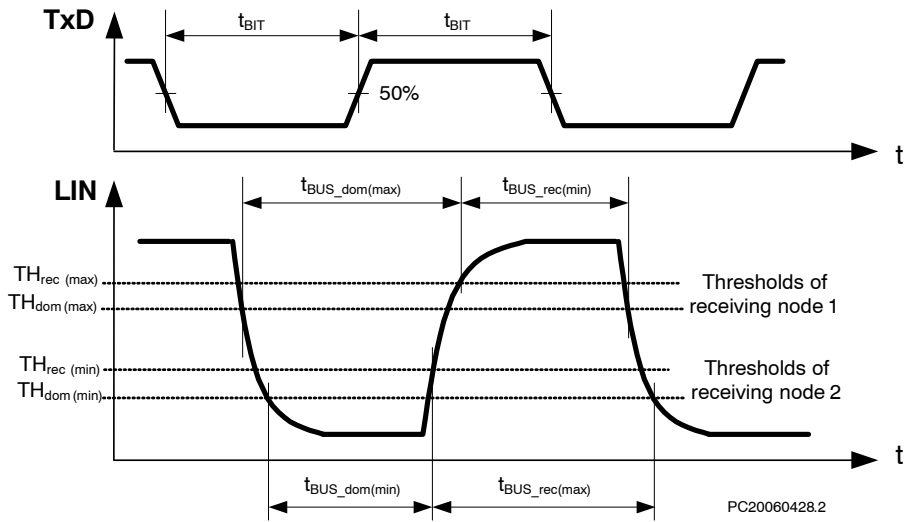


Figure 24. LIN Transmitter Duty Cycle

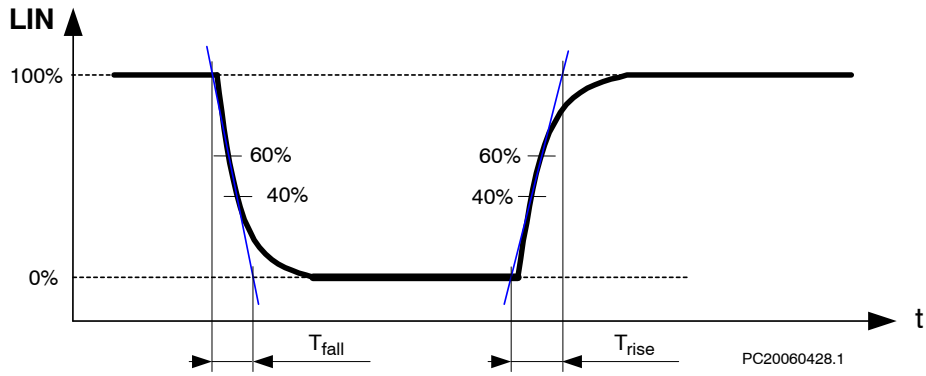


Figure 25. LIN Transmitter Rising and Falling Times

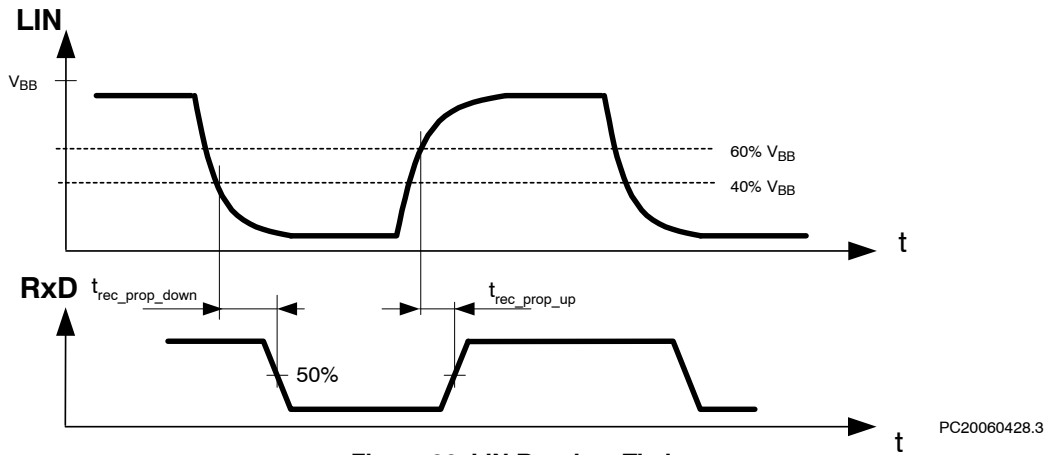


Figure 26. LIN Receiver Timing

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ORDERING INFORMATION

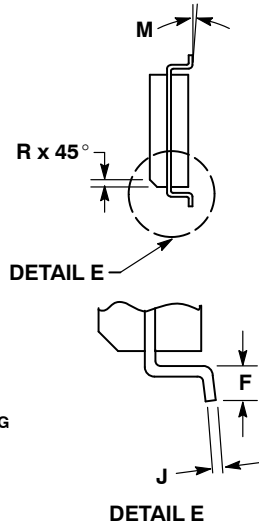
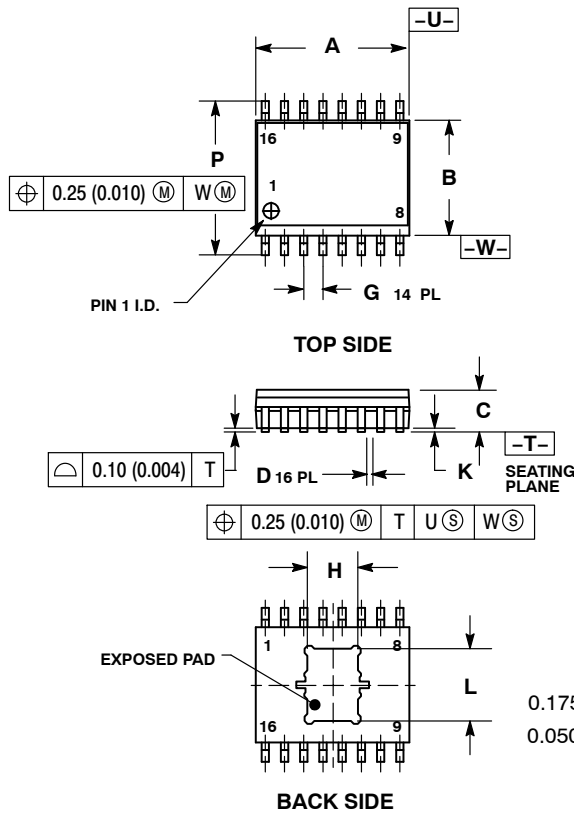
| Device | Description | Temperature Range | Package | Shipping† |
|---------------|--|-------------------|------------------------------|--------------------|
| NCV7425DW0G | LIN Transceiver + 3.3 V Regulator + Reset Pin | -40°C to 125°C | SOIC-16, WB, EP (Pb-Free) | 46 Units / Tube |
| NCV7425DW0R2G | | | | 1500 / Tape & Reel |
| NCV7425DW5G | LIN Transceiver + 5 V Regulator + Reset Pin | | | 46 Units / Tube |
| NCV7425DW5R2G | | | | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV7425

PACKAGE DIMENSIONS

SOIC-16 LEAD WIDE BODY, EXPOSED PAD PDW SUFFIX CASE 751AG ISSUE A

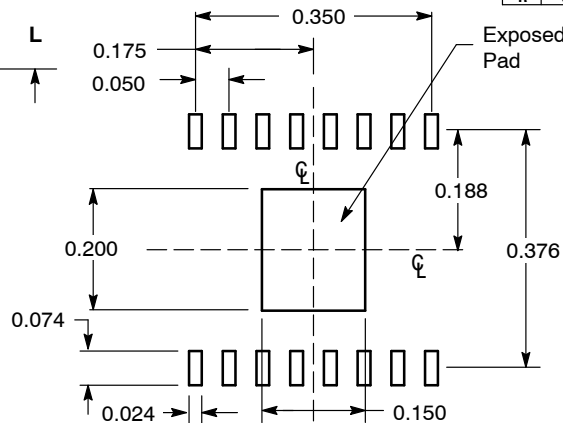


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R-01 OBSOLETE, NEW STANDARD 751R-02.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 10.15 | 10.45 | 0.400 | 0.411 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 3.45 | 3.66 | 0.136 | 0.144 |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.00 | 0.10 | 0.000 | 0.004 |
| L | 4.72 | 4.93 | 0.186 | 0.194 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

SOLDERING FOOTPRINT*



DIMENSIONS: INCHES

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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