

# TB62214AFG, TB62214AFTG

## BiCD Constant-Current Two-Phase Bipolar Stepping Motor Driver IC

The TB62214AFG/AFTG is a two-phase bipolar stepping motor driver using a PWM chopper controlled by clock input.

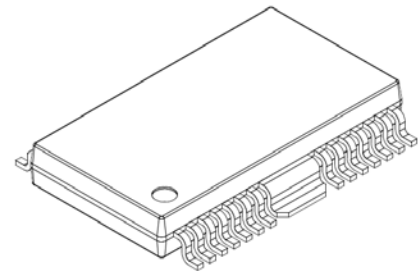
Fabricated with the BiCD process, the TB62214AFG/AFTG is rated at 40 V/2.0 A.

The on-chip voltage regulator allows control of a stepping motor with a single VM power supply.

### Features

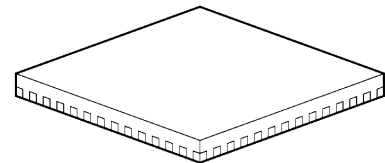
- Bipolar stepping motor driver
- PWM constant-current drive
- Clock input control
- Allows two-phase, 1-2-phase and W1-2-phase excitations.
- BiCD process: Uses DMOS FETs as output power transistors.
- High voltage and current: 40 V/2.0 A (absolute maximum ratings)
- Thermal shutdown (TSD), overcurrent shutdown (ISD), and power-on-resets (PORs)
- Packages: HSOP28-P-0450-0.80  
QFN48-P-0707-0.50

TB62214AFG



HSOP28-P-0450-0.80

TB62214AFTG



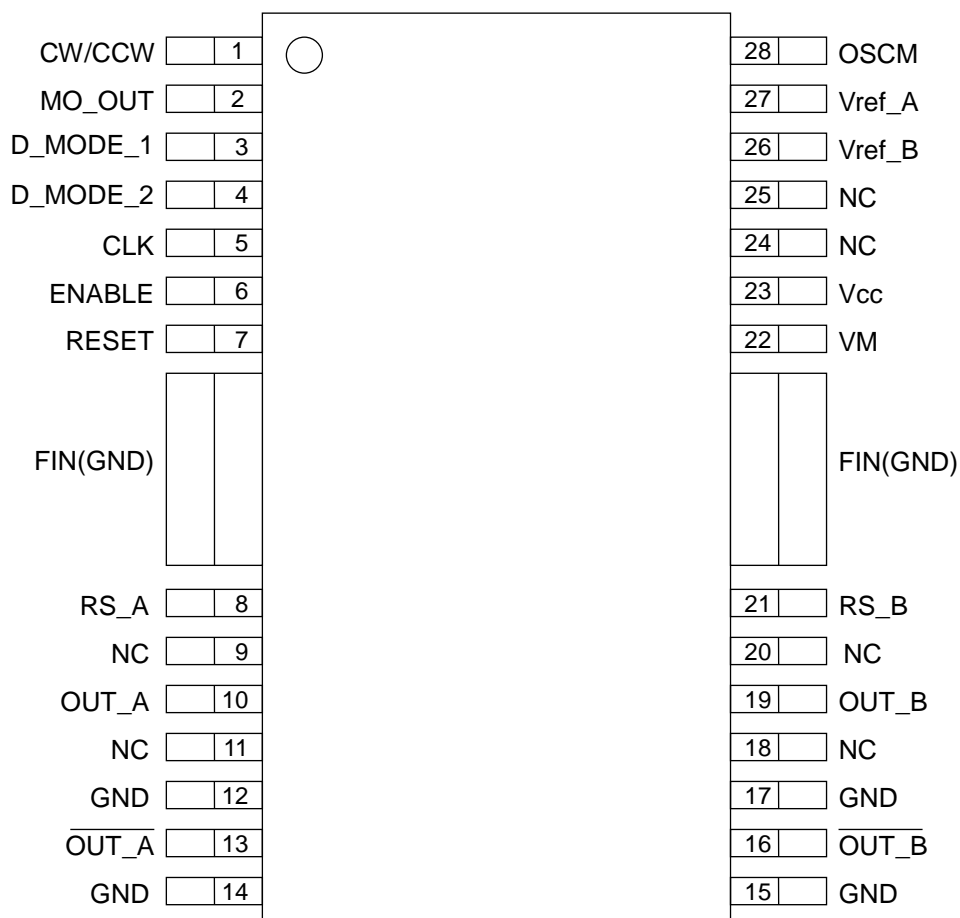
QFN48-P-0707-0.50

### Weight

HSOP28-P-0450-0.80 : 0.79 g (typ.)

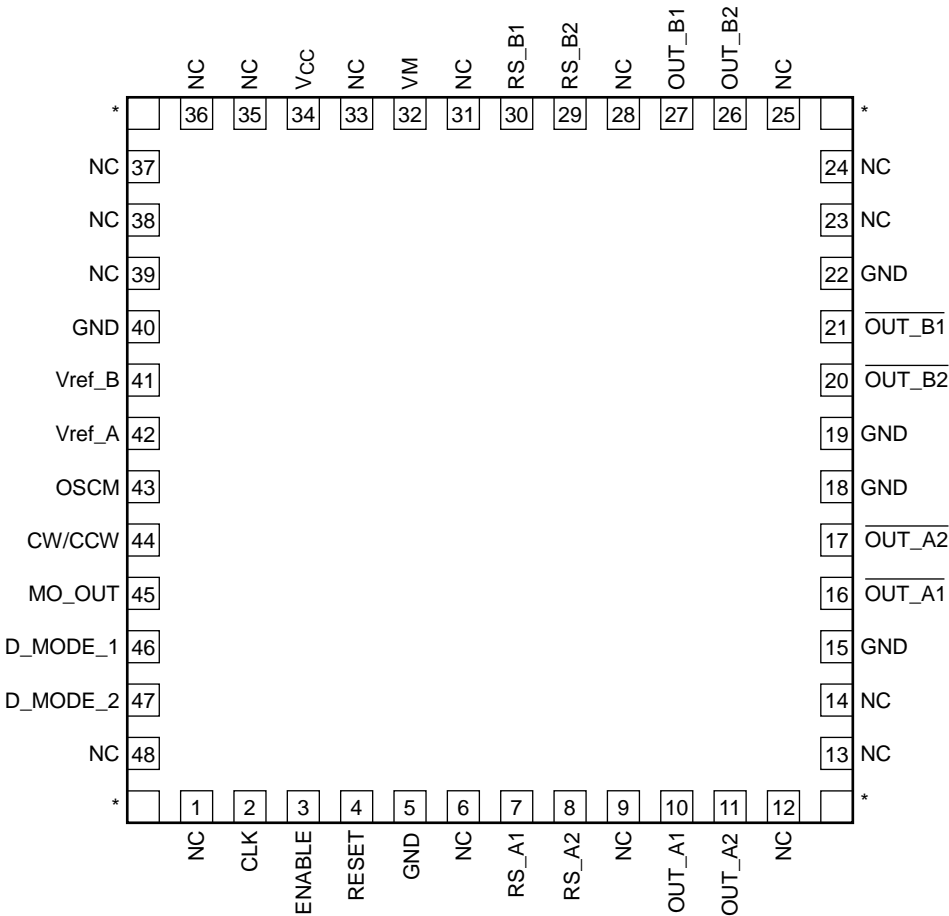
QFN48-P-0707-0.50 : 0.14 g (typ.)

**TB62214AFG (HSOP28)**



Pin Assignment

TB62214AFTG (QFN48)



\*Mark PAD: It must be connected to GND

The diagram illustrates the internal architecture of the DRV8834 stepper motor driver. Key components and their interconnections include:

- Inputs:** RESET, CW/CCW, ENABLE, D\_MODE\_1, D\_MODE\_2, and CLK are connected to the Step Decoder (Input Logic).
- Power and Grounding:** Vcc is connected to the Vcc Voltage Regulator and the OSCM pin. VM is connected to the Vcc Voltage Regulator and the VM pin. MO\_OUT is connected to the Vcc Voltage Regulator.
- Control Logic:** The Step Decoder (Input Logic) provides signals to the Current Level Set and the Output Control (Mixed Decay Control).
- Current Feedback:** The Current Level Set provides a reference current (Vref) to the Current Feedback (x2) block. The Current Feedback (x2) block contains a Vrs block and an Rs COMP block. The Vrs block is connected to the VM pin and the RS pin. The Rs COMP block is connected to the VM pin and the Output Control (Mixed Decay Control).
- Output Stage:** The Output Control (Mixed Decay Control) drives the Output (H-Bridgex2) block, which is connected to the Stepping Motor. The Output (H-Bridgex2) block also provides feedback to the Output Control (Mixed Decay Control).
- Timing and Oscillation:** The Chopper OSC block contains an OSC block and a CR-CLK Converter. The OSC block is connected to the VM pin and the OSCM pin. The CR-CLK Converter is connected to the OSC block and the Output Control (Mixed Decay Control).
- Protection and Detection:** The VMR Detect block is connected to the VM pin and the Output Control (Mixed Decay Control). The ISD (Inter-Segment Detection) and TSD (Thermal Shutdown) blocks are connected to the Output Control (Mixed Decay Control) and the Output (H-Bridgex2) block.

**Note:** All the grounding wires of the TB62214AFG/AFTG must run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.

Also, utmost care should be taken for pattern designing and implementation of the TB62214AFG/AFTG since it has the power supply pins (V<sub>M</sub>, RS\_A, RS\_B, OUT\_A, OUT\_A, OUT\_B, OUT\_B, GND) particularly a large current can run through. If these pins are wired incorrectly, an operation error or even worse a destruction of the TB62214AFG/AFTG may occur.

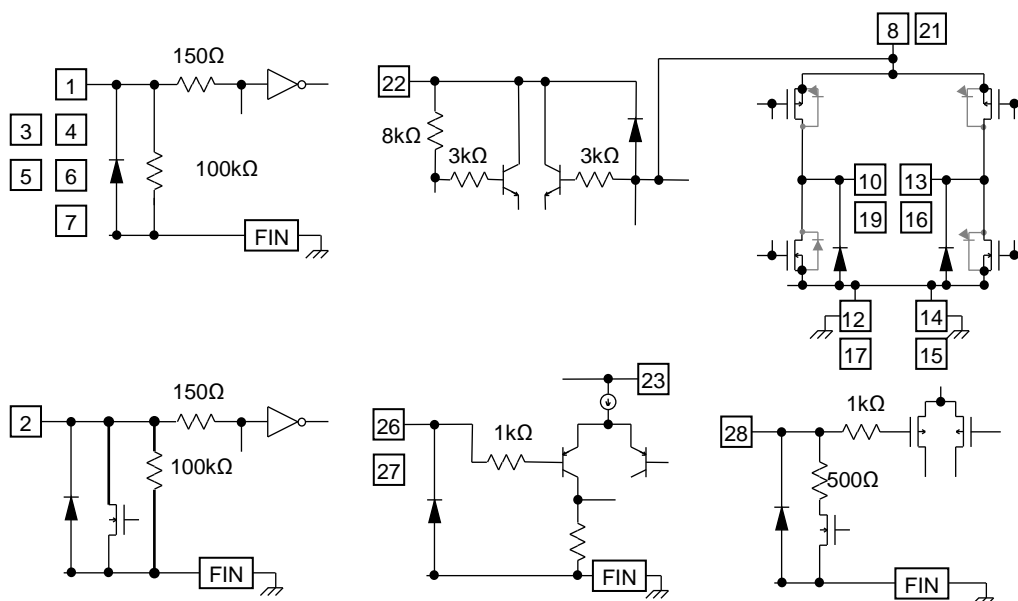
Please note the above when designing and implementing IC patterns.

## Pin Function

### TB62214AFG (HSOP28)

Pin No.	Pin Name	Function
1	CW/CCW	Motor rotation: forward/reverse
2	MO_OUT	Electric angle monitor
3	D_MODE_1	Excitation mode control
4	D_MODE_2	Excitation mode control
5	CLK	An electrical angle leads on the rising edge of the clock input. A motor rotation count depends on the input frequency.
6	ENABLE	A-/B-channel output enable
7	RESET	Electric angle reset
8	RS_A	The sink current sensing of A-phase motor coil
9	NC	No-connect
10	OUT_A	A-phase positive driver output
11	NC	No-connect
12	GND	Motor power ground
13	OUT_A	A-phase negative driver output
14	GND	Motor power ground
15	GND	Motor power ground
16	OUT_B	B-phase negative driver output
17	GND	Motor power ground
18	NC	No-connect
19	OUT_B	B-phase positive driver output
20	NC	No-connect
21	RS_B	The sink current sensing of B-phase motor coil
22	VM	Power supply
23	VCC	Smoothing filter for logic power supply
24	NC	No-connect
25	NC	No-connect
26	Vref_B	Tunes the current level for B-phase motor drive.
27	Vref_A	Tunes the current level for A-phase motor drive.
28	OSCM	Oscillator pin for PWM chopper

### Pin Interfaces (HSOP28)

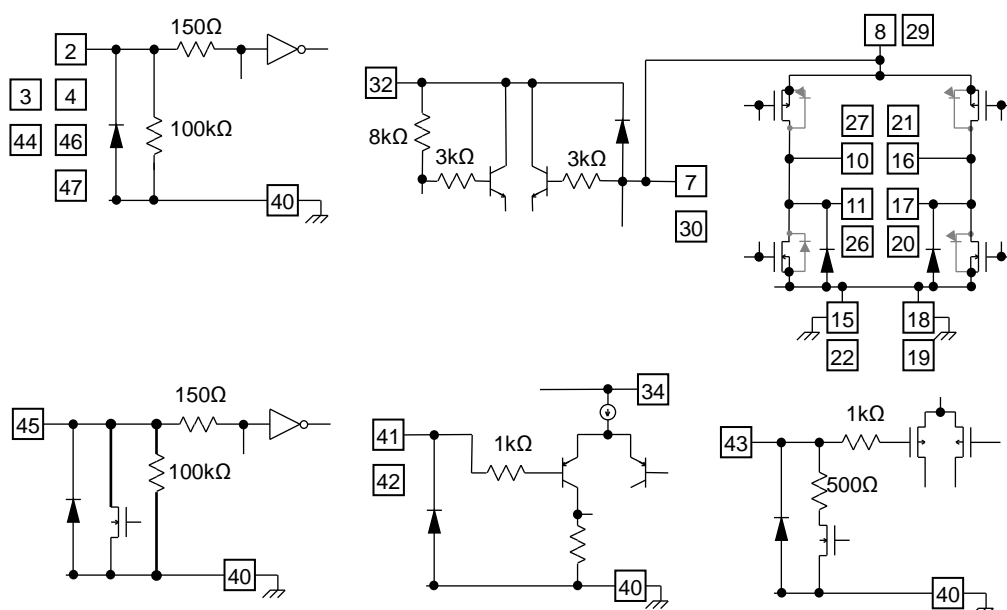


The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes. Absolute precision of the chip internal resistance is +/-30%.

## TB62214AFTG (QFN48)

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	NC	No-connect	25	NC	No-connect
2	CLK	An electrical angle leads on the rising edge of the clock input. A motor rotation count depends on the input frequency.	26	OUT_B2	B-phase positive driver output
3	ENABLE	A-/B-channel output enable	27	OUT_B1	
4	RESET	Electric angle reset	28	NC	No-connect
5	GND	Logic ground	29	RS_B2	Power supply of B-phase motor coil and the sink current sensing of B-phase motor coil
6	NC	No-connect	30	RS_B1	
7	RS_A1	Power supply of A-phase motor coil and the sink current sensing of A-phase motor coil	31	NC	No-connect
8	RS_A2		32	VM	Power supply
9	NC	No-connect	33	NC	No-connect
10	OUT_A1	A-phase positive driver output	34	V <sub>CC</sub>	Smoothing filter for logic power supply
11	OUT_A2		35	NC	No-connect
12	NC	No-connect	36	NC	No-connect
13	NC	No-connect	37	NC	No-connect
14	NC	No-connect	38	NC	No-connect
15	GND	Motor power ground	39	NC	No-connect
16	OUT_A1	A-phase negative driver output	40	GND	Logic ground
17	OUT_A2		41	Vref_B	Tunes the current level for B-phase motor drive.
18	GND	Motor power ground	42	Vref_A	Tunes the current level for A-phase motor drive.
19	GND	Motor power ground	43	OSCM	Oscillator pin for PWM chopper
20	OUT_B2	B-phase negative driver output	44	CW/CCW	Motor rotation: forward/reverse
21	OUT_B1		45	MO_OUT	Electric angle monitor
22	GND	Motor power ground	46	D_MODE_1	Excitation mode control
23	NC	No-connect	47	D_MODE_2	Excitation mode control
24	NC	No-connect	48	NC	No-connect

## Pin Interfaces (QFN48)



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes. Absolute precision of the chip internal resistance is +/-30%.

## CLK Function

The electrical angle leads one by one in the manner of the clocks. The clock signal is reflected to the electrical angle on the rising edge.

CLK Input	Function
Rise	The electrical angle leads by one on the rising edge.
Fall	Remains at the same position.

## ENABLE Function

The ENABLE pin controls whether or not to let the current flow through a given phase for a stepper motor drive. This pin serves to select if the motor is stopped in Off mode or activated. The pin must be fixed to Low on the power-on or power-down of the TB62214AFG/AFTG. During power on, once the VM voltage has reached the voltage required to operate the motor, set this to High.

ENABLE Input	Function
H	Output transistors are enabled (normal operation mode).
L	Output transistors are disabled (high impedance state).

## CW/CCW Function

The CW/CCW pin switches rotation direction of stepper motors.

The CW pin outputs the A-phase current 90° behind than the B-phase current.

The CCW pin outputs the A-phase current 90° ahead of the B-phase current.

CW/CCW Input	Function
H	Forward (CW)
L	Reverse (CCW)

## Excitation Mode Select Function

D_MODE_1	D_MODE_2	Function
L	L	OSC_M, output transistors are disabled (in Standby mode)
L	H	Two-phase excitation
H	L	1-2-phase excitation
H	H	W1-2-phase excitation

## RESET Function

The RESET function resets the electrical angle. Always set this to H during power on. Once the VM voltage has reached the voltage required to operate the motor, release RESET.

RESET Input	Function
L	Normal operation mode
H	The electrical angle is reset.

The phase current while RESET is applied is shown in the table below. MO\_OUT is Low at this time.

Excitation Mode	A-phase Current	B-phase Current
2 Phase	100%	100%
1 – 2 Phase	100%	100%
W1-2 Phase	71%	71%

**Detection Features**

(1) Thermal shutdown (TSD)

The thermal shutdown circuit turns off all the outputs when the junction temperature ( $T_j$ ) exceeds 150°C (typ.). The outputs retain the current states.

The TB62214AFG/AFTG exits TSD mode and resume normal operation when the TB62214AFG/AFTG is rebooted or both the D\_MODE\_1 and D\_MODE\_2 pins are switched to Low.

(2) Power-ON-resets (PORs) for V<sub>MR</sub> and V<sub>CCR</sub> (V<sub>M</sub> and V<sub>CC</sub> voltage monitor)

The outputs are forced off until V<sub>M</sub> and V<sub>CC</sub> reach the rated voltages.

(3) Overcurrent shutdown (ISD)

Each phase has an overcurrent shutdown circuit, which turns off the corresponding outputs when the output current exceeds the shutdown trip threshold (above the maximum current rating: 2.0 A minimum).

The TB62214AFG/AFTG exits ISD mode and resumes normal operation when the TB62214AFG/AFTG is rebooted or both the D\_MODE\_1 and D\_MODE\_2 pins are switched to Low.

This circuit provides protection against a short-circuit by temporarily disabling the device. Important notes on this feature will be provided later.



**Absolute Maximum Ratings (Ta = 25°C)**

Characteristics		Symbol	Rating	Unit	Remarks
Motor power supply		V <sub>M</sub>	40	V	—
Motor output voltage		V <sub>OUT</sub>	40	V	—
Motor output current		I <sub>OUT</sub>	2.0	A per phase	(Note 1)
Digital input voltage		V <sub>IN</sub>	-0.5 to 6.0	V	—
Vref standard voltage		V <sub>ref</sub>	5.0	V	—
MO output voltage		V <sub>MO</sub>	6.0	V	—
MO output sink current		I <sub>MO</sub>	30.0	mA	—
Power dissipation	QFN48	P <sub>D</sub>	1.3	W	(Note 2)
	HSOP28	P <sub>D</sub>	1.3	W	(Note 2)
Operating temperature		T <sub>opr</sub>	−20 to 85	°C	—
Storage temperature		T <sub>stg</sub>	−55 to 150	°C	—
Junction temperature		T <sub>j</sub> (MAX)	150	°C	—

Note 1: As a guide, the maximum output current should be kept below 1.4 A per phase. The maximum output current may be further limited by thermal considerations, depending on ambient temperature and board conditions.

Note 2: Stand-alone (Ta = 25°C)

If Ta is over 25°C, derating is required at 10.4 mW/°C.

Ta: Ambient temperature

Topr: Ambient temperature while the TB62214AFG/AFTG is active

Tj: Junction temperature while the TB62214AFG/AFTG is active. The maximum junction temperature is limited by the thermal shutdown (TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj (MAX), will not exceed 120°C.

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

Exceeding the rating (s) may cause breakdown, damage or deterioration of the device, and may result in injury by explosion or combustion.

The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The TB62214AFG/AFTG does not have overvoltage protection. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.

All voltage ratings including supply voltages must always be followed. The other notes and considerations described later should also be referred to.

**Operating Ranges (Ta=0 to 85°C)**

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	V <sub>M</sub>	10.0	24.0	38.0	V	—
Motor output current	I <sub>OUT</sub>	—	1.4	2.0	A	Per phase (Note 1)
Digital input voltage	V <sub>IN</sub> (H)	2.0	—	5.5	V	High-level logic
	V <sub>IN</sub> (L)	-0.4	—	1.0	V	Low-level logic
MO output voltage	V <sub>MO</sub>	—	3.3	5.5	V	With a pull-up resistor
Clock input frequency	f <sub>CLK</sub>	—	—	100	kHz	—
Chopper frequency	f <sub>chop</sub>	40.0	100.0	150	kHz	—
V <sub>ref</sub> reference voltage	V <sub>ref</sub>	GND	—	3.6	V	—
Voltage across the current-sensing resistor pins	V <sub>RS</sub>	0.0	±1.0	±1.5	V	Referenced to the V <sub>M</sub> pin (Note 2)

Note 1: The actual maximum current may be limited by the operating environment (operating conditions such as excitation mode or operating duration, or by the surrounding temperature or board heat dissipation). Determine a realistic maximum current by calculating the heat generated under the operating environment.

Note 2: The maximum V<sub>RS</sub> voltage should not exceed the maximum rated voltage.

## Electrical Characteristics 1 (Ta = 25°C, VM = 24 V, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input hysteresis voltage		VIN (HIS)	DC	Digital input pins (Note1)	100	200	300	mV
Digital input current (Note2)	High	IIN (H)	DC	VIN = 5 V at the digital input pins under test	35	50	75	μA
	Low	IIN (L)	DC	VIN = 0 V at the digital input pins under test	—	—	1	μA
MO output voltage	High	VOH (MO)	—	IOH = 24 mA when the output is High	2.4	—	—	V
	Low	VOL (MO)	—	IOL = 24 mA when the output is Low	—	—	0.5	V
Supply current		IM1	DC	Outputs open, In standby mode	—	2	3	mA
		IM2	DC	Outputs open, ENABLE = Low	—	3.5	5	mA
		IM3	DC	Outputs open (two-phase excitation)	—	5	7	mA
Output leakage current	High-side	IOH	DC	VRS = VM = 40 V, VOUT = 0 V	—	—	1	μA
	Low-side	IOL	DC	VRS = VM = VOUT = 40 V	1	—	—	μA
Channel-to-channel differential		ΔIOUT1	DC	Channel-to-channel error	−5	0	5	%
Output current error relative to the predetermined value		ΔIOUT2	DC	IOUT = 1 A (Note3)	−5	0	5	%
RS pin current		IRS	DC	VRS = VM = 24 V	0	—	10	μA
Drain-source ON-resistance of the output transistors (upper and lower sum)		RON (D-S)	DC	IOUT = 2.0 A, Tj = 25°C	—	1.0	1.5	Ω

Note1: VIN (L → H) is defined as the VIN voltage that causes the outputs (OUT\_A1, OUT\_A2, OUT\_B1 and OUT\_B2) to change when a pin under test is gradually raised from 0 V. VIN (H → L) is defined as the VIN voltage that causes the outputs (OUT\_A1, OUT\_A2, OUT\_B1 and OUT\_B2) to change when the pin is then gradually lowered.

The difference between VIN (L → H) and VIN (H → L) is defined as the input hysteresis.

Note2: The circuit design has been designed so that electromotive force or leak current from signal input does not occur when VM voltage is not supplied, even if the logic input signal is input. Even so, regulate logic input signals before resupply of VM voltage so that the motor does not operate when voltage is reapplied.

Note 3: If the supply voltage for internal circuitry (VCC) is split with an external resistor and used as Vref input supply voltage, the accuracy of the output current setting will be at ±8% when the VCC output voltage accuracy and the Vref damping ratio accuracy are combined.

**Electrical Characteristics 2 (Ta = 25°C, VM = 24 V, unless otherwise specified)**

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Vref input current	Iref	DC	Vref = 3.0 V	—	0	1	μA
Vref decay rate	Vref (GAIN)	DC	Vref = 2.0 V	1/4.8	1/5.0	1/5.2	—
TSD threshold (Note 1)	TjTSD	DC	—	140	150	170	°C
VM recovery voltage	VMR	DC	—	7.0	8.0	9.0	V
Overcurrent trip threshold (Note 2)	ISD	DC	—	2.0	3.0	4.0	A
Supply voltage for internal circuitry	VCC	DC	ICC = 5.0 mA	4.75	5.00	5.25	V

**Note 1: Thermal shutdown (TSD) circuitry**

When the junction temperature of the device has reached the threshold, the TSD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors.

The TSD circuitry is tripped at a temperature between 140°C (min) and 170°C (max). Once tripped, the TSD circuitry keeps the output transistors off until both the D\_MODE\_1 and D\_MODE\_2 pins are switched to Low or the TB62214AFG/AFTG is rebooted.

The thermal shutdown circuit is provided to turn off all the outputs when the IC is overheated. For this reason, please avoid using TSD for other purposes.

**Note 2: Overcurrent shutdown (ISD) circuitry**

When the output current has reached the threshold, the ISD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors.

To prevent the ISD circuitry from being tripped due to switching noise, it has a masking time of four CR oscillator cycles. Once tripped, it takes a maximum of four cycles to exit ISD mode and resume normal operation.

The ISD circuitry remains active until both the D\_MODE\_1 and D\_MODE\_2 pins are switched to Low or the TB62214AFG/AFTG is rebooted.

The TB62214AFG/AFTG remains in Standby mode while in ISD mode.

**Back-EMF**

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.

If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB62214AFG/AFTG or other components will be damaged or fail due to the motor back-EMF.

**Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)**

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.

If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.

The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

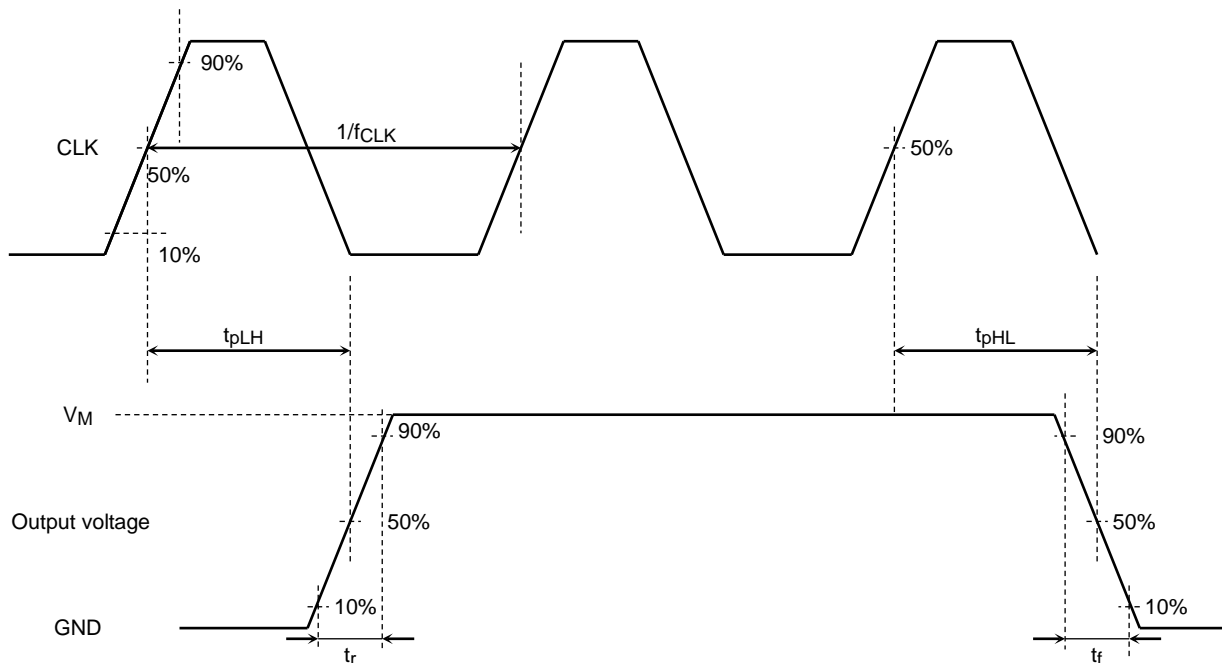
**IC Mounting**

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

**AC Electrical Characteristics ( $T_a = 25^\circ\text{C}$ ,  $V_M = 24\text{ V}$ ,  $6.8\text{ mH}/5.7\Omega$ )**

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock input frequency	$f_{\text{CLK}}$	AC	$f_{\text{OSC}} = 1600\text{ kHz}$	—	—	100	kHz
Minimum high pulse width of CLK input filter	$T_{\text{CLK (H)}}$	AC	High time of the clock input frequency	300	—	—	ns
Minimum low pulse width of CLK input filter	$T_{\text{CLK (L)}}$	AC	Low time of the clock input frequency	250	—	—	ns
Output transistor switching characteristics	$t_r$	AC	—	100	150	200	ns
	$t_f$	AC	—	100	150	200	ns
	$t_{\text{pLH (CLK)}}$	AC	CLK to OUT	—	1000	—	ns
	$t_{\text{pHL (CLK)}}$	AC	CLK to OUT	—	1500	—	ns
Blanking time for current spike prevention	$t_{\text{BLANK}}$	AC	$I_{\text{OUT}} = 1.0\text{ A}$	200	300	500	ns
OSC_M oscillation frequency	$f_{\text{OSC}}$	AC	$C_{\text{OSC}} = 270\text{ pF}$ , $R_{\text{OSC}} = 3.6\text{ k}\Omega$	1200	1600	2000	kHz
Chopper frequency range	$f_{\text{chop(RANGE)}}$	AC	$V_M = 24\text{ V}$ , Output ACTIVE ( $I_{\text{out}} = 1.0\text{ A}$ )	40	100	150	kHz
Chopper setting frequency	$f_{\text{chop}}$	AC	Output ACTIVE ( $I_{\text{out}} = 1.0\text{ A}$ ), $\text{CR} = 1600\text{ kHz}$	—	100	—	kHz
ISD masking time	$t_{\text{ISD (Mask)}}$	AC	After ISD threshold is exceeded due to an output short-circuit to power or ground	—	4	—	—
ISD on-time	$t_{\text{ISD}}$	AC	After ISD threshold is exceeded due to an output short-circuit to power or ground. (Note1)	4	—	8	

Note1: In the output short-to-power or -ground, I counted in OSC\_M number of clocks from beyond the ISD threshold.

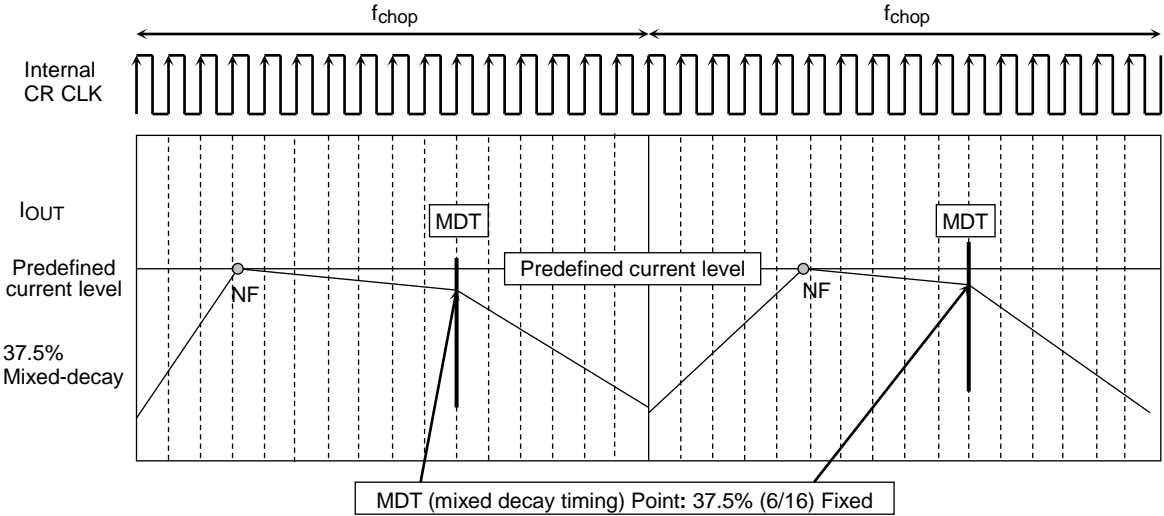
**Timing Charts of Output Transistors Switching**


Timing charts may be simplified for explanatory purposes.

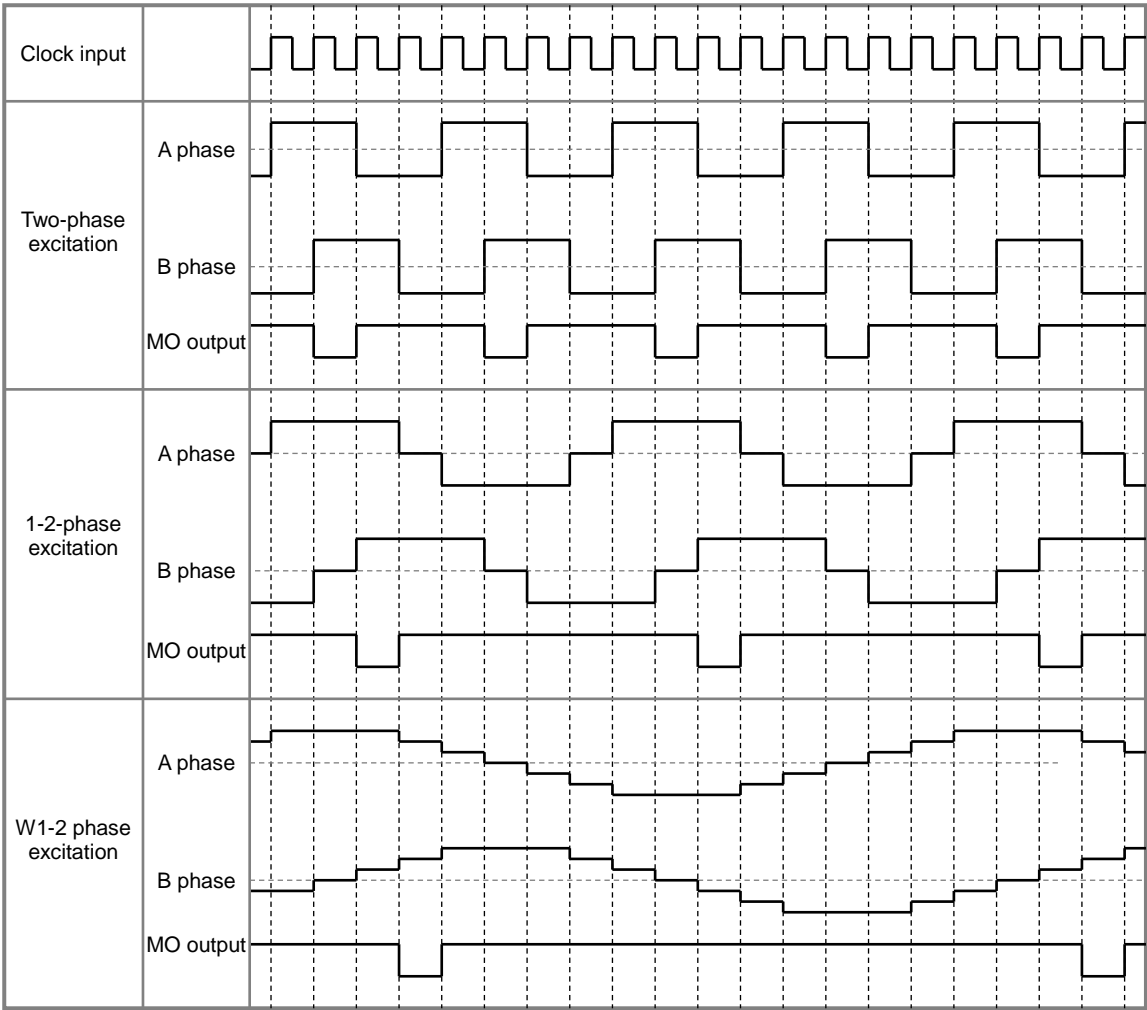
● Current Waveform in Mixed-Decay Mode

Timing charts may be simplified for explanatory purposes.

Mixed-Decay mode, the purpose of which is constant-current control, starts out in Fast-Decay mode for 37.5% of the whole period and then is followed by Slow-Decay mode for the remainder of the period.



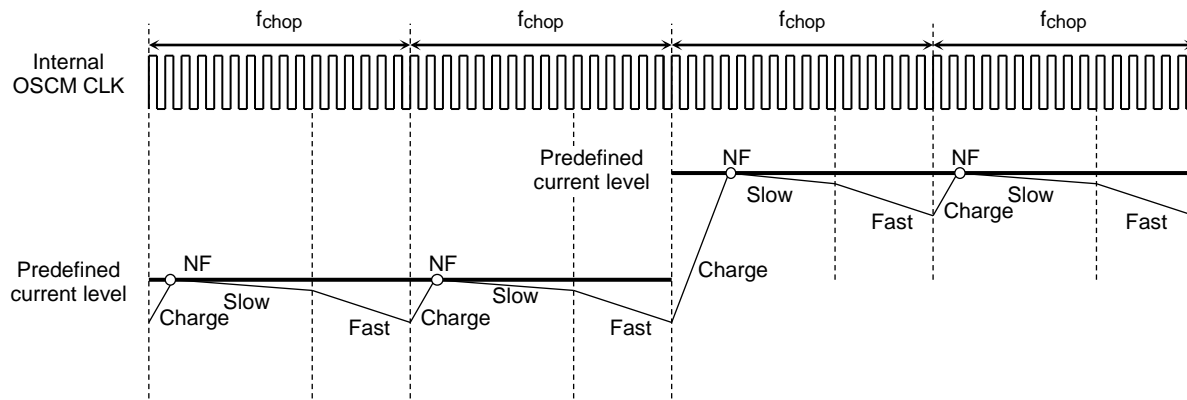
● Timing Charts of CLK, Output Current and MO Output



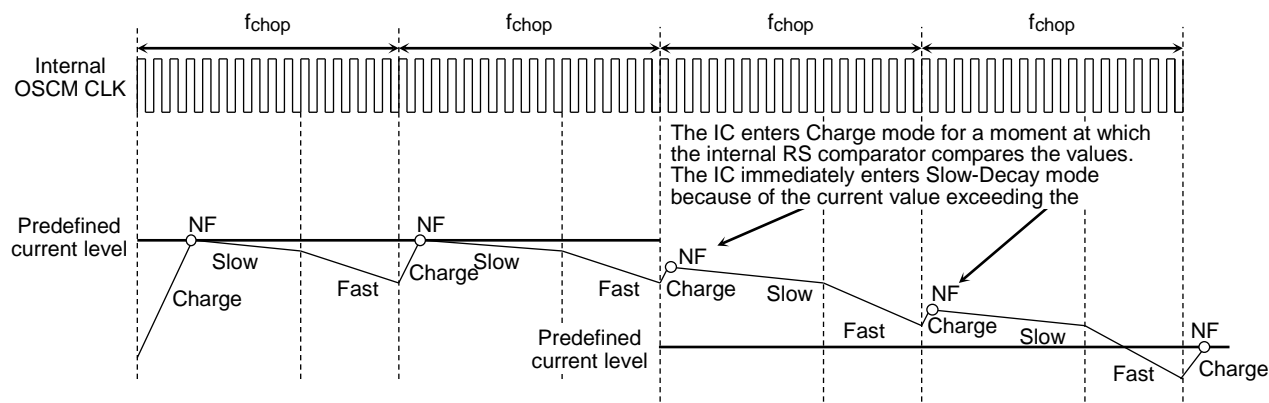
Timing charts may be simplified for explanatory purposes.

## ● Current Waveform in Mixed (Slow + Fast) Decay Mode

When a current value increases (Mixed-Decay point is fixed to 37.5%)



When a current value decreases (Mixed-Decay point is fixed to 37.5%)



The Charge period starts as the internal oscillator clock starts counting. When the output current reaches the predefined current level, the internal RS comparator detects the predefined current level (NF); as a result, the IC enters Slow-Decay mode.

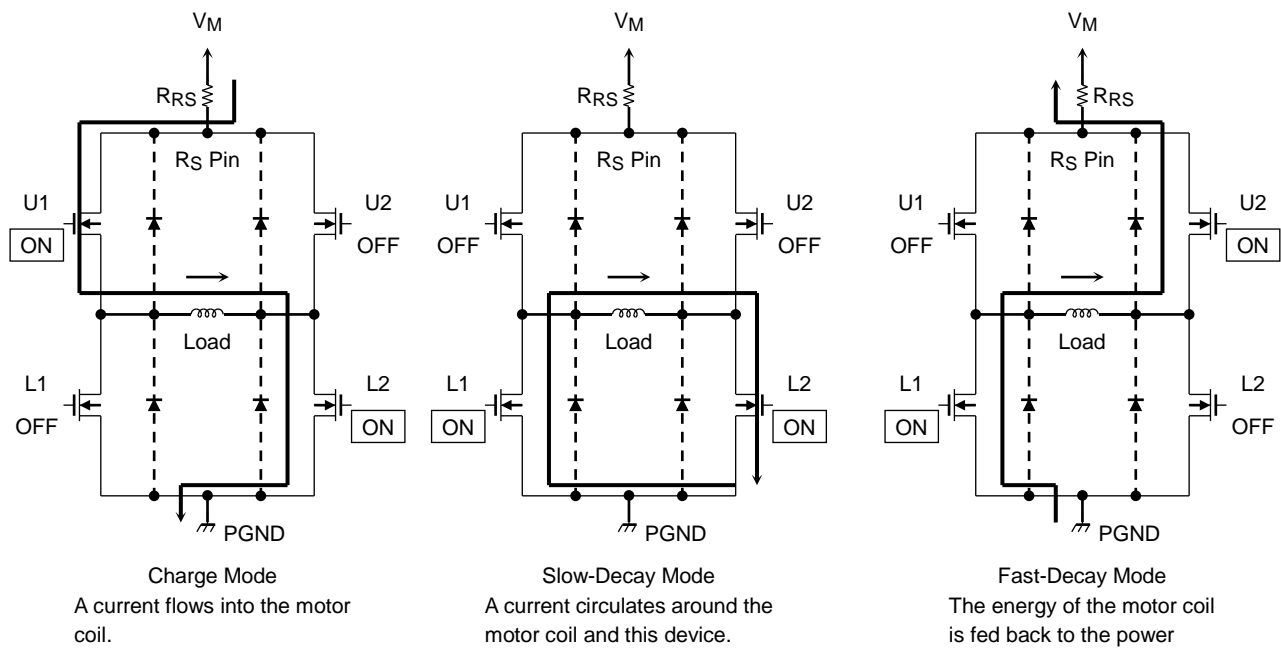
The TB62214AFG/AFTG transits from Slow-Decay mode to Fast-Decay mode at the point 37.5 of a PWM frequency (one chopping frequency) remains in a whole PWM frequency period (on the rising edge of the 11th clock of the OSCM clock).

When the OSCM pin clock counter clocks 16 times, the Fast-Decay mode ends; and at the same time, the counter is reset, which brings the TB62214AFG/AFTG into Charge mode again.

**Note:** These figures are intended for illustrative purposes only. If designed more realistically, they would show transient response curves.

Timing charts may be simplified for explanatory purposes.

● Output Transistor Operating Modes



Output Transistor Operating Modes

CLK	U1	U2	L1	L2
Charge	ON	OFF	OFF	ON
Slow-decay Mode	OFF	OFF	ON	ON
Fast-decay Mode	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the figures shown above. If the current flows in the opposite direction, refer to the following table.

CLK	U1	U2	L1	L2
Charge	OFF	ON	ON	OFF
Slow-decay Mode	OFF	OFF	ON	ON
Fast-decay Mode	ON	OFF	OFF	ON

The TB62214AFG/AFTG switches among Charge, Slow-Decay and Fast-Decay modes automatically for constant-current control.

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Calculation of the Predefined Output Current

For PWM constant-current control, the TB62214AFG/AFTG uses a clock generated by the CR oscillator. The peak output current can be set via the current-sensing resistor (RRS) and the reference voltage (Vref), as follows:

$I_{OUT} = V_{ref}/5 \div R_S (\Omega)$

where, 1/5 is the Vref decay rate, Vref (GAIN). For the value of Vref (GAIN), see the Electrical Characteristics table.

For example, when Vref = 3 V, to generate an output current (IOUT) of 0.8 A, RRS is calculated as:

$R_{RS} = (V_{ref}/5) \div I_{OUT} = (3/5) \div 0.8 = 0.75\Omega. (\geq 0.5 \text{ W})$

## IC Power Consumption

The power consumed by the TB62214AFG/AFTG is approximately the sum of the following two: 1) the power consumed by the output transistors, and 2) the power consumed by the digital logic and pre-drivers.

The power consumed by the output transistors is calculated, using the  $R_{ON}$  (D-S) value of  $1.0\Omega$ .

Whether in Charge, Fast Decay or Slow Decay mode, two of the four transistors comprising each H-bridge contribute to its power consumption at a given time.

Thus the power consumed by each H-bridge is given by:

$$P(\text{out}) = I_{OUT}(\text{A}) \times V_{DS}(\text{V}) = 2 \times I_{OUT}^2 \times R_{ON} \dots\dots\dots (1)$$

In two-phase excitation mode (in which two phases have a phase difference of  $90^\circ$ ), the average power consumption in the output transistors is calculated as follows:

$$\begin{aligned} R_{ON} &= 1.0 \Omega \text{ (@2.0 A), the sum of the high-side DMOS and low-side DMOS} \\ I_{OUT}(\text{Peak}) &= 1.0 \text{ A} \\ V_M &= 24 \text{ V} \end{aligned}$$

$$P(\text{out}) = 2H_{sw} \times 1.0^2 (\text{A}) \times 1.0 (\Omega) = 2.0 (\text{W}) \dots\dots\dots (2)$$

The power consumption in the  $I_M$  domain is calculated separately for normal operation and standby modes:

$$\begin{aligned} \text{Normal operation mode: } I(I_{M3}) &= 5.0 \text{ mA (typ.)} \\ \text{Standby mode: } I(I_{M1}) &= 2.0 \text{ mA (typ.)} \end{aligned}$$

The current consumed in the digital logic portion of the TB62214AFG/AFTG is indicated as  $I_{MX}$ . The digital logic operates off a voltage regulator that is internally connected to the  $V_M$  power supply. It consists of the digital logic connected to  $V_M$  (24 V) and the network affected by the switching of the output transistors. The total power consumed by  $I_{MX}$  can be estimated as:

$$P(I_M) = 24 (\text{V}) \times 0.005 (\text{A}) = 0.12 (\text{W}) \dots\dots\dots (3)$$

Hence, the total power consumption of the TB62214AFG/AFTG is:

$$P = P(\text{out}) + P(I_M) = 2.12 (\text{W})$$

The standby power consumption is given by:

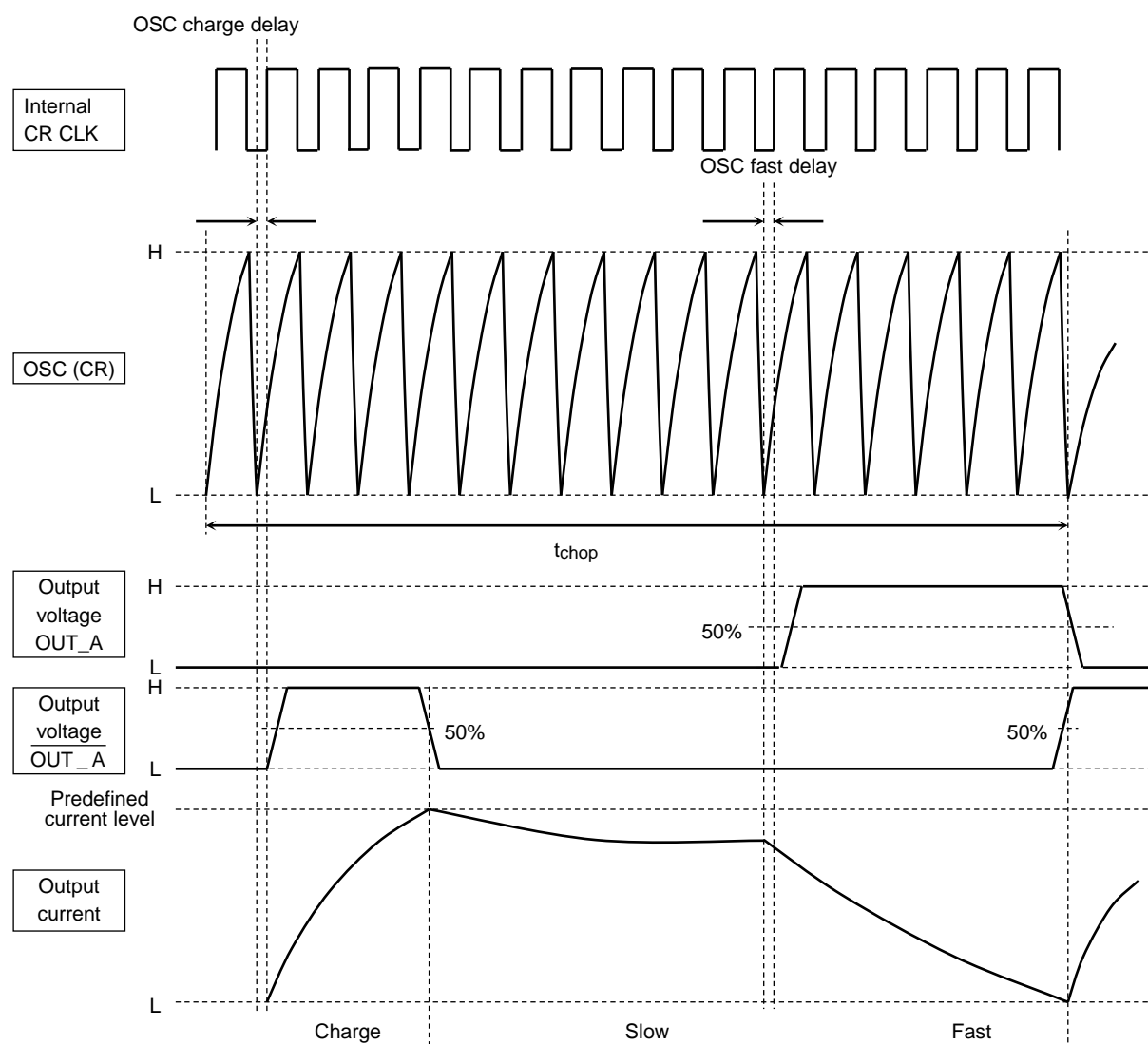
$$P(\text{Standby}) + P(\text{out}) = 24 (\text{V}) \times 0.002 (\text{A}) = 0.048 (\text{W})$$

Board design should be fully verified, taking thermal dissipation into consideration.



## ● OSC-Charge Delay

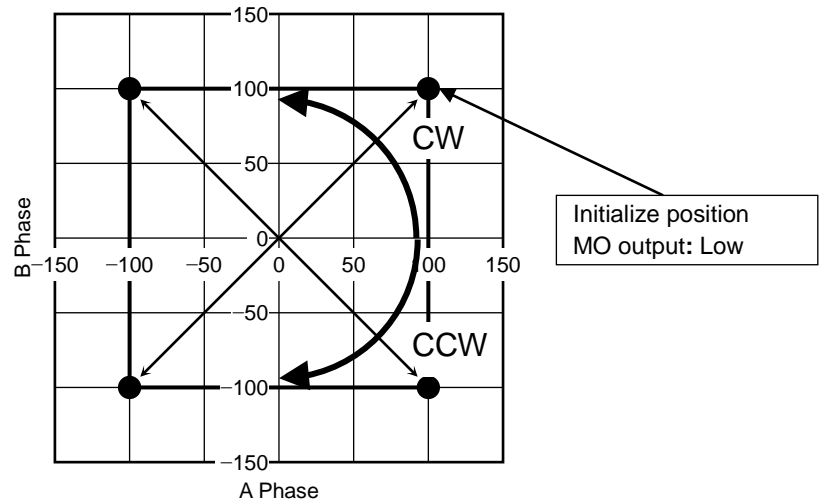
Since the rising level of the OSC waveform is referenced to convert it into the internal CR CLK waveform, about up to 1  $\mu$ s (when CR = 1600 kHz) of a delay occurs between the OSC waveform and internal CR CLK waveform.



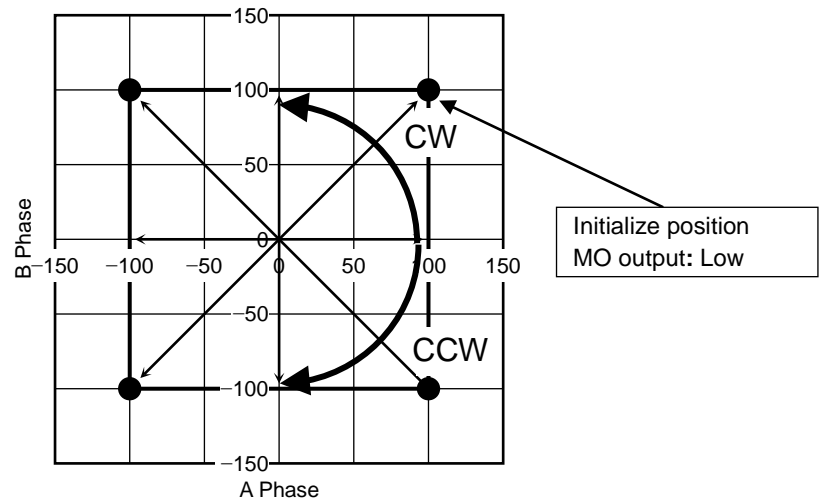
Timing Waveforms of OSC and Internal CR CLK

Timing charts may be simplified for explanatory purposes.

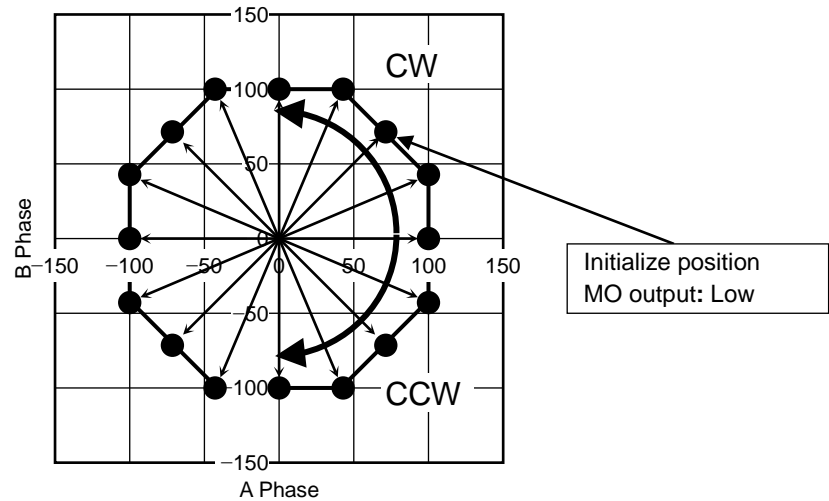
**Phase Sequences**  
**Two-Phase Excitation Mode**



**1-2-Phase Excitation Mode**

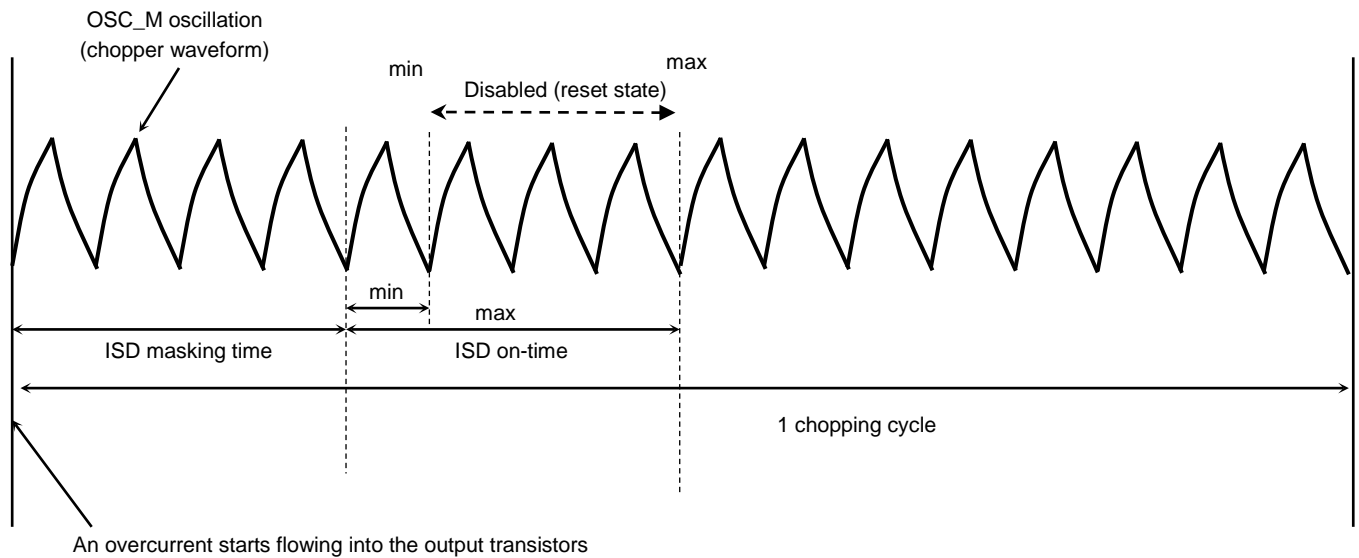


**W1-2-Phase Excitation Mode**



## Overcurrent Shutdown (ISD) Circuitry

### ISD Masking Time and ISD On-Time



The overcurrent shutdown (ISD) circuitry has a masking time to prevent current spikes during  $I_{rr}$  and switching from erroneously tripping the ISD circuitry. The masking time is a function of the chopper frequency obtained by CR:

$$\text{masking\_time} = 4 \times \text{CR\_frequency}$$

The minimum and maximum times taken to turn off the output transistors since an overcurrent flows into them are:

$$\text{Min: } 4 \times \text{CR\_frequency}$$

$$\text{Max: } 8 \times \text{CR\_frequency}$$

It should be noted that these values assume a case in which an overcurrent condition is detected in an ideal manner. The ISD circuitry might not work, depending on the control timing of the output transistors.

Therefore, a protection fuse must always be added to the VM power supply as a safety precaution. The optimal fuse capacitance varies with usage conditions, and one that does not adversely affect the motor operation or exceed the power dissipation rating of the TB62214AFG/AFTG should be selected.

## Calculating OSCM Oscillating Frequency

The OSCM oscillating frequency can be approximated using the following equation:

$$f_{\text{OSCM}} = \frac{1}{0.56 \times C \times (R_1 + 500)}$$

Where:

C = Capacitor capacity

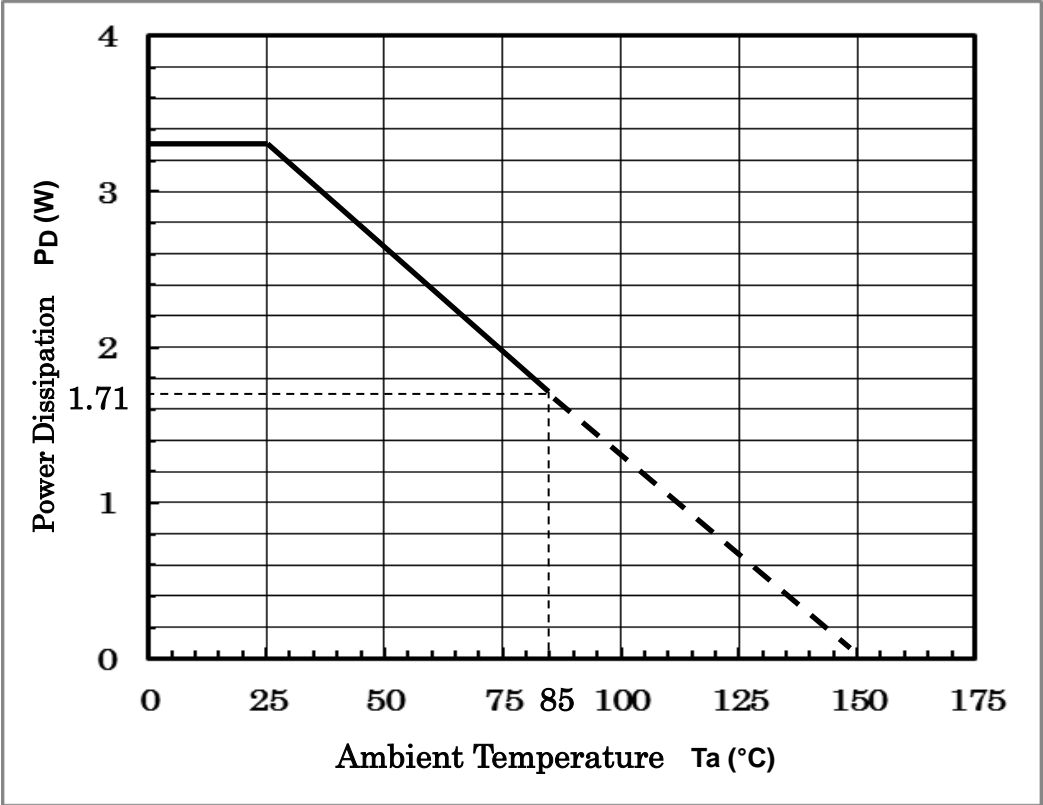
R1= Resistance

Assigning  $C = 270 \times 10^{-12}$  [F],  $R_1 = 3600$  [ $\Omega$ ] to get:

$$f_{\text{OSCM}} = 1.61 \times 10^6 \Rightarrow 1.6 \text{ MHz}$$

**$P_D - T_a$  (Package Power Dissipation)**

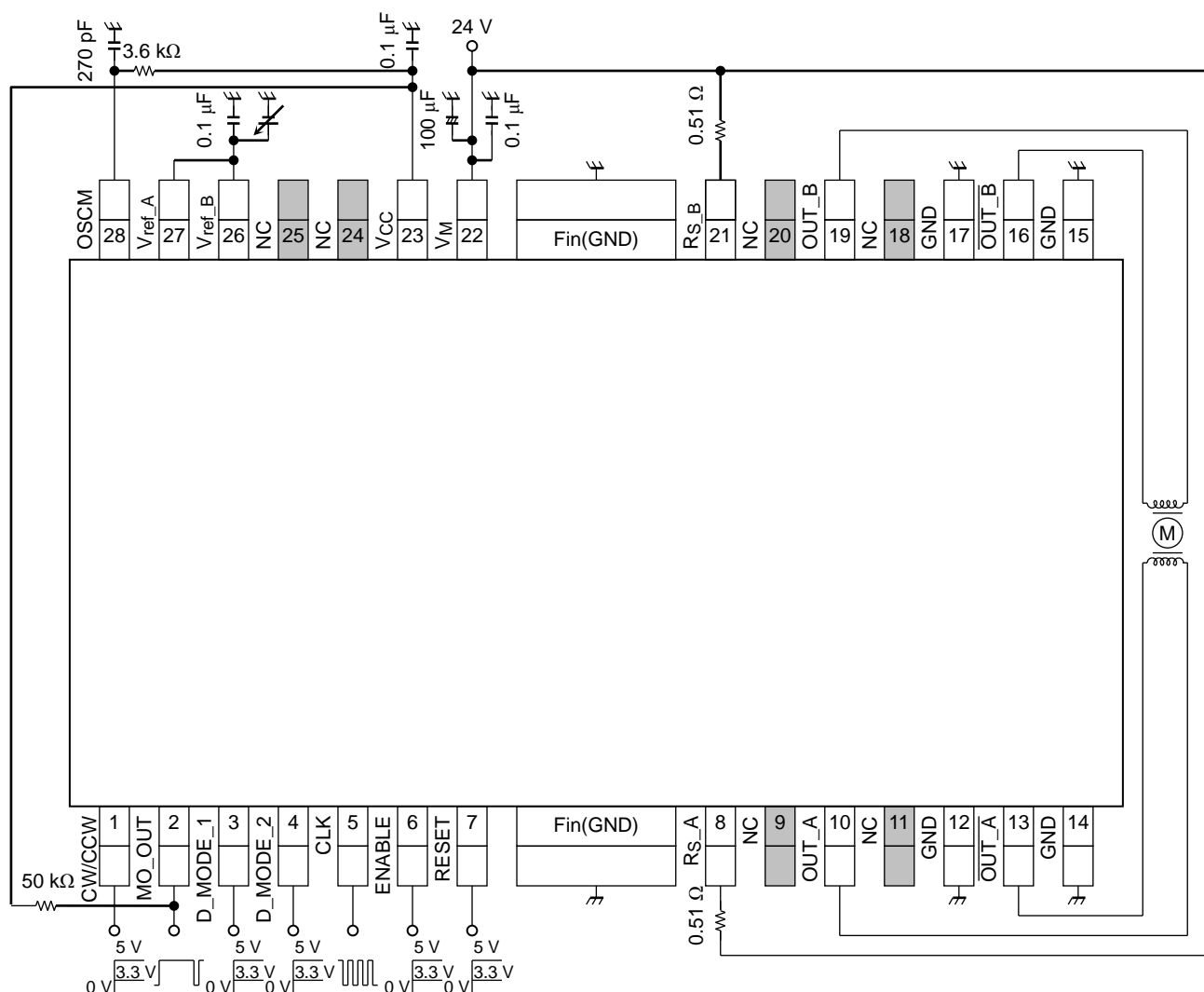
2 layer glass epoxy board  
(Board Layer: 2 layer Cu thickness: 55  $\mu$ m, Board size: 85 mm  $\times$  85 mm  $\times$  1.6 mm)  
 $\theta_{j-a}$ : 38°C/W (typ.)



## Example Application Circuits

### TB62214AFG

The values shown in the following figure are typical values. For input conditions, see Operating Ranges.



**Note:** Bypass capacitors should be added as necessary.

It is recommended to use a single ground plane for the entire board whenever possible, and a grounding method should be considered for efficient heat dissipation.

In cases where mode setting pins are controlled via switches, either pull-down or pull-up resistors should be added to them to avoid floating states.

For a description of the input values, see the function tables.

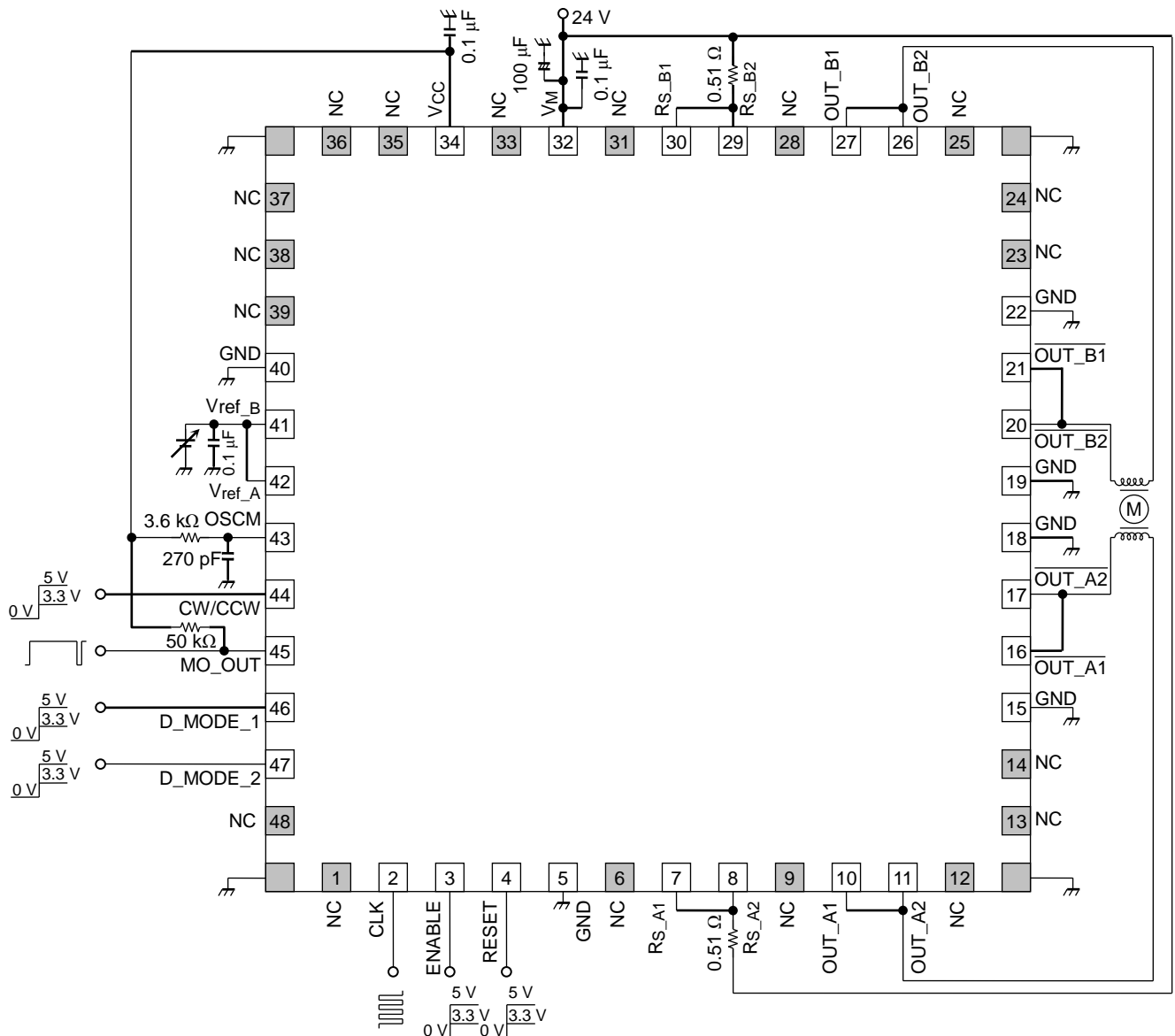
The above application circuit example is presented only as a guide and should be fully evaluated prior to production. Also, no intellectual property right is ceded in any way whatsoever in regard to its use.

The external components in the above diagram are used to test the electrical characteristics of the device; it is not guaranteed that no system malfunction or failure will occur.

Careful attention should be paid to the layout of the output,  $V_{DD}$  ( $V_M$ ) and GND traces to avoid short-circuits across output pins or to the power supply or ground. If such a short-circuit occurs, the TB62214AFG/AFTG may be permanently damaged. Also, if the device is installed in a wrong orientation, a high voltage might be applied to components with lower voltage ratings, causing them to be damaged. The TB62214AFG/AFTG does not have an overvoltage protection circuit. Thus, if a voltage exceeding the rated maximum voltage is applied, the TB62214AFG/AFTG will be damaged; it should be ensured that it is used within the specified operating conditions.

## TB62214AFTG

The values shown in the following figure are typical values. For input conditions, see the Operating Ranges.



**Note:** Bypass capacitors should be added as necessary.

It is recommended to use a single ground plane for the entire board whenever possible, and a grounding method should be considered for efficient heat dissipation.

In cases where mode setting pins are controlled via switches, either pull-down or pull-up resistors should be added to them to avoid floating states.

For a description of the input values, see the function tables.

The above application circuit example is presented only as a guide and should be fully evaluated prior to production. Also, no intellectual property right is ceded in any way whatsoever in regard to its use.

The external components in the above diagram are used to test the electrical characteristics of the device: it is not guaranteed that no system malfunction or failure will occur.

Careful attention should be paid to the layout of the output, V<sub>DD</sub> (V<sub>M</sub>) and GND traces to avoid short-circuits across output pins or to the power supply or ground. If such a short-circuit occurs, the TB62214AFG/AFTG may be permanently damaged. Also, if the device is installed in a wrong orientation, a high voltage might be applied to components with lower voltage ratings, causing them to be damaged. The TB62214AFG/AFTG does not have an overvoltage protection circuit. Thus, if a voltage exceeding the rated maximum voltage is applied, the TB62214AFG/AFTG will be damaged; it should be ensured that it is used within the specified operating conditions.

## HSOP28-P-0450-0.80

Technical drawing of the 128K1601 memory module, showing top, side, and detail views with dimensions.

**Top View Dimensions:**

- Pin 1 location: INDEX
- Pin 14 to Pin 28 distance:  $3.24^{+0.08}_{-0.12}$
- Pin 1 to Pin 14 distance:  $0.37^{+0.08}_{-0.12}$
- Pin 1 to Pin 1 distance:  $(0.965)$
- Pin 1 to Pin 1 distance:  $0.8$
- Pin 1 to Pin 1 distance:  $2.235$
- Pin 1 to Pin 1 distance:  $0.16(M)$
- Pin 1 to Pin 1 distance:  $0.88 \pm 0.2$
- Pin 1 to Pin 1 distance:  $12.0 \pm 0.3$

**Side View Dimensions:**

- Pin 1 to Pin 1 distance:  $16.5 \text{ MAX}$
- Pin 1 to Pin 1 distance:  $16.0 \pm 0.2$
- Pin 1 to Pin 1 distance:  $2.3 \pm 0.2$
- Pin 1 to Pin 1 distance:  $2.7 \text{ MAX}$
- Pin 1 to Pin 1 distance:  $0.1^{+0.1}_{-0.05}$
- Pin 1 to Pin 1 distance:  $0.10(S)$

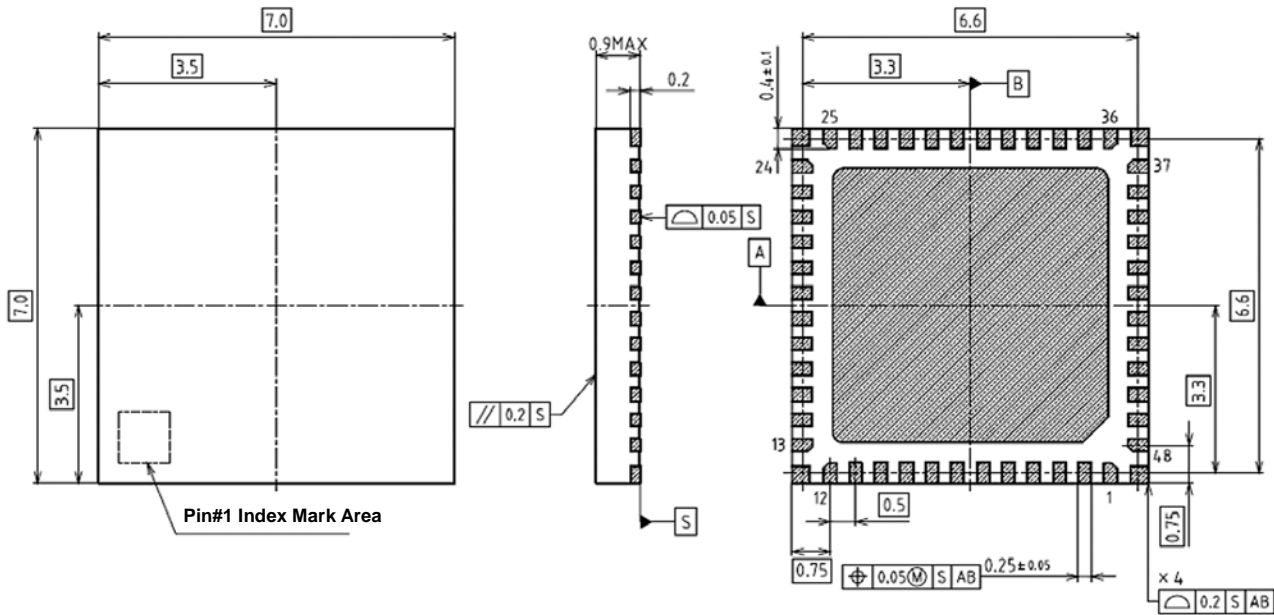
**Detail View Dimensions:**

- Pin 1 to Pin 1 distance:  $0.27^{+0.08}_{-0.07}$
- Pin 1 to Pin 1 distance:  $0.92 \pm 0.2$

2014-10-01

QFN48-P-0707-0.50

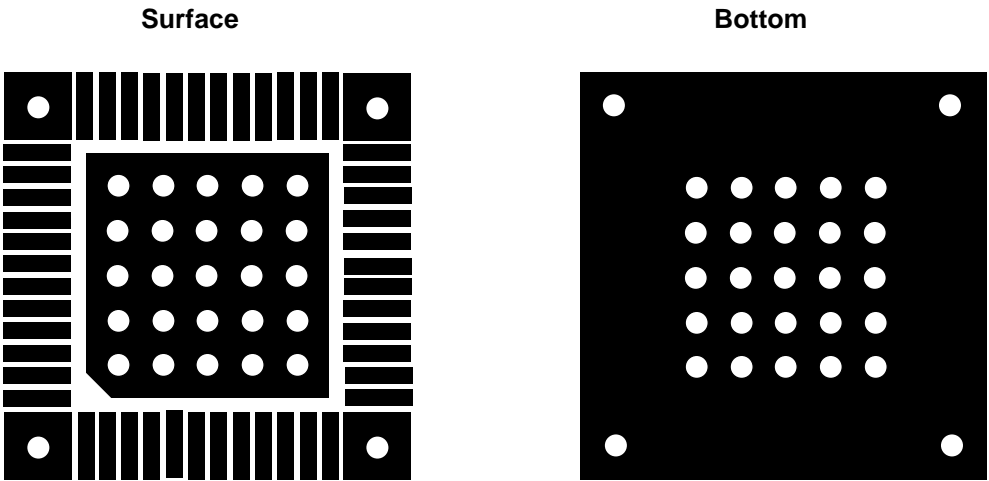
Unit: mm



Backside heatsink: 5.4 mm × 5.4 mm  
Corner chamfers: C0.5  
Chamfer radius: 3-R0.2

Weight: 0.14 g (typ.)

Land Pattern Example (double-sided board)



White dots: 0.2-mm through holes



**Notes on Contents****Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

**Equivalent Circuits**

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**Timing Charts**

Timing charts may be simplified for explanatory purposes.

**Application Circuits**

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

**Test Circuits**

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

**IC Usage Considerations****Notes on handling of ICs**

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device that has been inserted incorrectly.
- (5) Please take extra care when selecting external components (such as power amps and regulators) or external devices (for instance, speakers). When large amounts of leak current occurs from capacitors, the DC output level may increase. If the output is connected to devices such as speakers with low resist voltage, overcurrent or IC failure may cause smoke or ignition. (The over-current may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

**Points to remember on handling of ICs****Over current Protection Circuit**

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

**Thermal Shutdown Circuit**

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

**Heat Radiation Design**

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (TJ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

**Back-EMF**

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flows back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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