# NCS20081, NCV20081, NCS20082, NCV20082, NCS20084, NCV20084

# Operational Amplifier, Rail-to-Rail Input and Output, 1.2 MHz

The NCS2008 series operational amplifiers provide rail−to−rail input and output operation, 1.2 MHz bandwidth, and are available in single, dual, and quad configurations. Rail−to−rail operation gives designers use of the entire supply voltage range while taking advantage of the 1.2 MHz bandwidth. The NCS2008 can operate on supply voltages from 1.8 to 5.5 V over a temperature range from −40 to 125°C. At a 1.8 V supply, this device has a slew rate of 0.4 V/μs while consuming only 42 μA of quiescent current per channel. Since this is a CMOS device, high input impedance and low bias currents make it ideal for interfacing to a wide variety of signal sensors. The NCS2008 devices are available in a variety of compact packages.

### Features

- Rail−to−Rail Input and Output
- Wide Supply Range: 1.8 to 5.5 V
- Wide Bandwidth: 1.2 MHz
- High Slew Rate: 0.4 V/μs at $V_S$ = 1.8 V
- Low Supply Current: 42 μA per Channel at $V_S$ = 1.8 V
- Low Input Bias Current: 1 pA Typical
- Wide Temperature Range: −40 to 125°C
- Available in a Variety of Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Unity Gain Buffer
- Battery Powered / Low Quiescent Current Applications
- Low Cost Current Sensing
- Automotive

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

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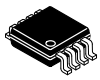
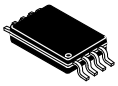
**SC70−5**
**CASE 419A**

**TSOP−5/SOT23−5**
**CASE 483**

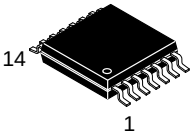


**Micro8™/MSOP8**
**CASE 846A**

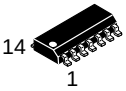
**SOIC−8**
**CASE 751**



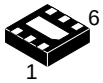
**TSSOP−8**
**CASE 948S**




**TSSOP−14**
**CASE 948G**




**SOIC−14**
**CASE 751A**




**UDFN6**
**CASE 517AP**

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

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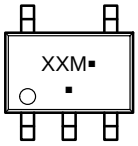
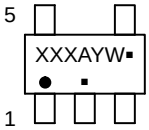
## MARKING DIAGRAMS

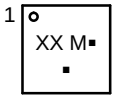
**Single Channel Configuration**
**NCS20081, NCV20081**




**SC70−5**
**CASE 419A**

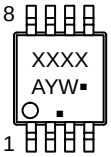



**TSOP−5/SOT23−5**
**CASE 483**

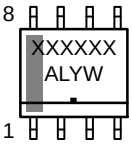



**UDFN6**
**CASE 517AP**

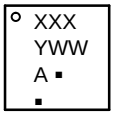
**Dual Channel Configuration**
**NCS20082, NCV20082**




**Micro8™/MSOP8**
**CASE 846A**

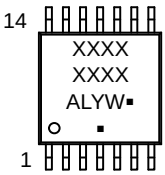



**SOIC−8**
**CASE 751**

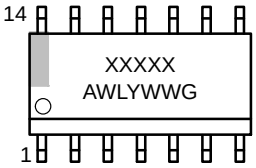



**TSSOP−8**
**CASE 948S**

**Quad Channel Configuration**
**NCS20084, NCV20084**




**TSSOP−14**
**CASE 948G**

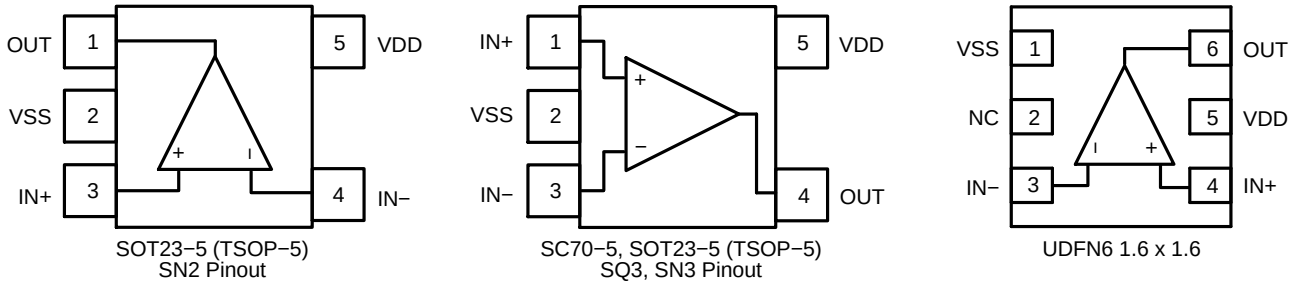



**SOIC−14**
**CASE 751A**

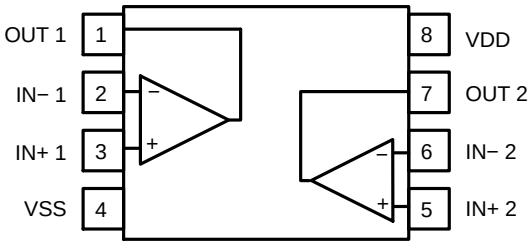
XXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

**Single Channel Configuration**
NCS20081, NCV20081




**Dual Channel Configuration**
NCS20082, NCV20082




**Quadruple Channel Configuration**
NCS20084, NCV20084

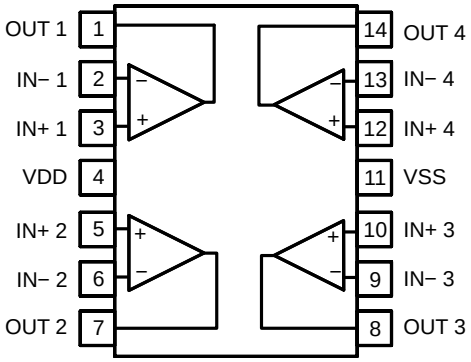



**Figure 1. Pin Connections**

**ORDERING INFORMATION**

| Device | Configuration | Automotive | Marking | Package | Shipping† |
|---|---|---|---|---|---|
| NCS20081SQ3T2G | Single** | No | AAK | SC70 | Contact local sales office for more information |
| NCS20081SN2T1G | | | K81 | SOT23−5/TSOP−5 | |
| NCS20081SN3T1G | | | K81 | SOT23−5/TSOP−5 | |
| NCS20081MUTAG | | | P2 | UDFN6 | |
| NCV20081SQ3T2G* | | Yes | AAK | SC70 | |
| NCV20081SN2T1G* | | | K81 | SOT23−5/TSOP−5 | |
| NCV20081SN3T1G* | | | K81 | SOT23−5/TSOP−5 | |
| NCV20081MUTAG* | | | P2 | UDFN6 | |
| NCS20082DMR2G | Dual | No | 2K82 | Micro8/MSOP8 | |
| NCS20082DR2G | | | NCS20082 | SOIC−8 | |
| NCS20082DTBR2G | | | K82 | TSSOP−8 | |
| NCV20082DMR2G* | | Yes | 2K82 | Micro8/MSOP8 | |
| NCV20082DR2G* | | | NCS20082 | SOIC−8 | |
| NCV20082DTBR2G* | | | K82 | TSSOP−8 | |
| NCS20084_ | Quad** | No | TBD | SOIC−14 | |
| NCS20084_ | | | TBD | SOP−14 | |
| NCS20084_ | | | TBD | TSSOP−14 | |
| NCV20084_ | | Yes | TBD | SOIC−14 | |
| NCV20084_ | | | TBD | SOP−14 | |
| NCV20084_ | | | TBD | TSSOP−14 | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

**In Development. Not yet released.

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

| Rating | Symbol | Limit | Unit |
|---|---|---|---|
| Supply Voltage ($V_{DD}$ – $V_{SS}$) (Note 2) | $V_S$ | 7 | V |
| Input Voltage | $V_I$ | $V_{SS}$ − 0.5 to $V_{DD}$ + 0.5 | V |
| Differential Input Voltage | $V_{ID}$ | $\pm V_S$ | V |
| Maximum Input Current | $I_I$ | ±10 | mA |
| Maximum Output Current | $I_O$ | ±100 | mA |
| Continuous Total Power Dissipation (Note 2) | $P_D$ | 200 | mW |
| Maximum Junction Temperature | $T_J$ | 150 | °C |
| Storage Temperature Range | $T_{STG}$ | −65 to 150 | °C |
| Mounting Temperature (Infrared or Convection – 20 sec) | $T_{mount}$ | 260 | °C |
| ESD Capability (Note 3) Human Body Model<br>Machine Model<br>Charge Device Model | $ESD_{HBM}$<br>$ESD_{MM}$<br>$ESD_{CDM}$ | 2000<br>100<br>2000 | V |
| Latch−Up Current (Note 4) | $I_{LU}$ | 100 | mA |
| Moisture Sensitivity Level (Note 5) | MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS for Safe Operating Area.
2. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of the maximum output current rating over the long term may adversely affect reliability. Shorting output to either VDD or VSS will adversely affect reliability.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)
4. Latch−up Current tested per JEDEC standard: JESD78
5. Moisture Sensitivity Level tested per IPC/JEDEC standard: J−STD−020A

**THERMAL INFORMATION**

| Parameter | Symbol | Channels | Package | Single Layer Board (Note 6) | Multi−Layer Board (Note 7) | Unit |
|---|---|---|---|---|---|---|
| Junction to Ambient Thermal Resistance | $\theta_{JA}$ | Single | SC−70 | | | °C/W |
| | | | SOT23−5/TSOP−5 | | | |
| | | | UDFN6 | | | |
| | | Dual | Micro8/MSOP8 | 236 | 167 | |
| | | | SOIC−8 | 190 | 131 | |
| | | | TSSOP−8 | 253 | 194 | |
| | | Quad | SOIC−14 | | | |
| | | | SOP−14 | | | |
| | | | TSSOP−14 | | | |

6. Value based on 1S standard PCB according to JEDEC51−3 with 1.0 oz copper and a 300 $mm^2$ copper area
7. Value based on 1S2P standard PCB according to JEDEC51−7 with 1.0 oz copper and a 100 $mm^2$ copper area

**OPERATING RANGES**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Supply Voltage | $V_S$ | 1.8 | 5.5 | V |
| Differential Input Voltage | $V_{ID}$ | | $V_S$ | V |
| Input Common Mode Range | $V_{ICM}$ | $V_{SS}$ – 0.2 | $V_{DD}$ + 0.2 | V |
| Ambient Temperature | $T_A$ | −40 | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS AT $V_S$ = 1.8 V

$T_A$ = 25°C; $R_L \geq 10$ kΩ; $V_{CM} = V_{OUT}$ = mid−supply unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = −40°C to 125°C. (Note 8)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | 0.5 | 3.5 | mV |
| | | | | | **4** | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1 | | μV/°C |
| Input Bias Current (Note 8) | $I_{IB}$ | | | 1 | | pA |
| | | | | | **1500** | pA |
| Input Offset Current (Note 8) | $I_{OS}$ | | | 1 | | pA |
| | | | | | **1100** | pA |
| Channel Separation | XTLK | DC | | 125 | | dB |
| Differential Input Resistance | $R_{ID}$ | | | 10 | | GΩ |
| Common Mode Input Resistance | $R_{IN}$ | | | 10 | | GΩ |
| Differential Input Capacitance | $C_{ID}$ | | | 1 | | pF |
| Common Mode Input Capacitance | $C_{CM}$ | | | 5 | | pF |
| Common Mode Rejection Ratio | CMRR | $V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$ | 48 | 73 | | dB |
| | | $V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$ | **45** | | | |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | | 86 | 120 | | dB |
| | | | **80** | | | |
| Short Circuit Current | $I_{SC}$ | Output to positive rail, sinking current | | 15 | | mA |
| | | Output to negative rail, sourcing current | | 11 | | |
| Output Voltage High | $V_{OH}$ | Voltage output swing from positive rail | | 3 | 19 | mV |
| | | | | | **20** | |
| Output Voltage Low | $V_{OL}$ | Voltage output swing from negative rail | | 3 | 19 | mV |
| | | | | | **20** | |
| **AC CHARACTERISTICS** | | | | | | |
| Unity Gain Bandwidth | UGBW | | | 1.2 | | MHz |
| Slew Rate at Unity Gain | SR | $V_{ID}$ = 1.2 Vpp, Gain = 1 | | 0.4 | | V/μs |
| Phase Margin | $\psi_m$ | | | 60 | | ° |
| Gain Margin | $A_m$ | | | 19 | | dB |
| Settling Time | $t_S$ | $V_{IN}$ = 1.2 Vpp, Gain = 1; Settling time to 0.1% | | 5 | | μs |
| | | $V_{IN}$ = 1.2 Vpp, Gain = 1; Settling time to 0.01% | | 6 | | |
| Open Loop Output Impedance | $Z_{OL}$ | f = 100 Hz | | 0.8 | | Ω |
| **NOISE CHARACTERISTICS** | | | | | | |
| Total Harmonic Distortion plus Noise | THD+N | $V_{IN}$ = 1.2 Vpp, f = 1 kHz, Av = 1 | | 0.005 | | % |
| Input Referred Voltage Noise | $e_n$ | f = 1 kHz | | 30 | | nV/√Hz |
| | | f = 10 kHz | | 24 | | |
| Input Referred Current Noise | $i_n$ | f = 1 kHz | | 300 | | fA/√Hz |
| **SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Rejection Ratio | PSRR | No Load | 67 | 90 | | dB |
| | | | **64** | | | |
| Power Supply Quiescent Current | $I_{DD}$ | Per channel, no load | | 42 | **60** | μA |

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

## ELECTRICAL CHARACTERISTICS AT $V_S$ = 3.3 V

$T_A$ = 25°C; $R_L \geq 10$ kΩ; $V_{CM} = V_{OUT}$ = mid−supply unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = −40°C to 125°C. (Note 9)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | 0.5 | 3.5 | mV |
| | | | | | **4** | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1 | | μV/°C |
| Input Bias Current (Note 9) | $I_{IB}$ | | | 1 | | pA |
| | | | | | **1500** | pA |
| Input Offset Current (Note 9) | $I_{OS}$ | | | 1 | | pA |
| | | | | | **1100** | pA |
| Channel Separation | XTLK | DC | | 125 | | dB |
| Differential Input Resistance | $R_{ID}$ | | | 10 | | GΩ |
| Common Mode Input Resistance | $R_{IN}$ | | | 10 | | GΩ |
| Differential Input Capacitance | $C_{ID}$ | | | 1 | | pF |
| Common Mode Input Capacitance | $C_{CM}$ | | | 5 | | pF |
| Common Mode Rejection Ratio | CMRR | $V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$ | 53 | 76 | | dB |
| | | $V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$ | **48** | | | |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | | 90 | 120 | | dB |
| | | | **86** | | | |
| Short Circuit Current | $I_{SC}$ | Output to positive rail, sinking current | | 15 | | mA |
| | | Output to negative rail, sourcing current | | 11 | | |
| Output Voltage High | $V_{OH}$ | Voltage output swing from positive rail | | 3 | 24 | mV |
| | | | | | **25** | |
| Output Voltage Low | $V_{OL}$ | Voltage output swing from negative rail | | 3 | 24 | mV |
| | | | | | **25** | |
| **AC CHARACTERISTICS** | | | | | | |
| Unity Gain Bandwidth | UGBW | | | 1.2 | | MHz |
| Slew Rate at Unity Gain | SR | $V_{IN}$ = 2.5 Vpp, Gain = 1 | | 0.4 | | V/μs |
| Phase Margin | $\psi_m$ | | | 60 | | ° |
| Gain Margin | $A_m$ | | | 18 | | dB |
| Settling Time | $t_S$ | $V_{IN}$ = 2.5 Vpp, Gain = 1; Settling time to 0.1% | | 5 | | μs |
| | | $V_{IN}$ = 2.5 Vpp, Gain = 1; Settling time to 0.01% | | 6 | | |
| Open Loop Output Impedance | $Z_{OL}$ | f = 100 Hz | | 0.8 | | Ω |
| **NOISE CHARACTERISTICS** | | | | | | |
| Total Harmonic Distortion plus Noise | THD+N | $V_{IN}$ = 2.5 Vpp, f = 1 kHz, Av = 1 | | 0.005 | | % |
| Input Referred Voltage Noise | $e_n$ | f = 1 kHz | | 30 | | nV/√Hz |
| | | f = 10 kHz | | 24 | | |
| Input Referred Current Noise | $i_n$ | f = 1 kHz | | 300 | | fA/√Hz |
| **SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Rejection Ratio | PSRR | No Load | 67 | 90 | | dB |
| | | | **64** | | | |
| Power Supply Quiescent Current | $I_{DD}$ | Per channel, no load | | 42 | **60** | μA |

9. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

## ELECTRICAL CHARACTERISTICS AT $V_S$ = 5.5 V

$T_A$ = 25°C; $R_L \geq 10$ kΩ; $V_{CM} = V_{OUT}$ = mid−supply unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = −40°C to 125°C. (Note 10)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | | 0.5 | 3.5 | mV |
| | | | | | **4** | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1 | | μV/°C |
| Input Bias Current (Note 10) | $I_{IB}$ | | | 1 | | pA |
| | | | | | **1500** | pA |
| Input Offset Current (Note 10) | $I_{OS}$ | | | 1 | | pA |
| | | | | | **1100** | pA |
| Channel Separation | XTLK | DC | | 125 | | dB |
| Differential Input Resistance | $R_{ID}$ | | | 10 | | GΩ |
| Common Mode Input Resistance | $R_{IN}$ | | | 10 | | GΩ |
| Differential Input Capacitance | $C_{ID}$ | | | 1 | | pF |
| Common Mode Input Capacitance | $C_{CM}$ | | | 5 | | pF |
| Common Mode Rejection Ratio | CMRR | $V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$ | 55 | 79 | | dB |
| | | $V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$ | **51** | | | |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | | 90 | 120 | | dB |
| | | | **86** | | | |
| Short Circuit Current | $I_{SC}$ | Output to positive rail, sinking current | | 15 | | mA |
| | | Output to negative rail, sourcing current | | 11 | | |
| Output Voltage High | $V_{OH}$ | Voltage output swing from positive rail | | 3 | 24 | mV |
| | | | | | **25** | |
| Output Voltage Low | $V_{OL}$ | Voltage output swing from negative rail | | 3 | 24 | mV |
| | | | | | **25** | |
| **AC CHARACTERISTICS** | | | | | | |
| Unity Gain Bandwidth | UGBW | | | 1.2 | | MHz |
| Slew Rate at Unity Gain | SR | $V_{ID}$ = 5 Vpp, Gain = 1 | | 0.4 | | V/μs |
| Phase Margin | $\psi_m$ | | | 60 | | ° |
| Gain Margin | $A_m$ | | | 17 | | dB |
| Settling Time | $t_S$ | $V_{IN}$ = 5 Vpp, Gain = 1; Settling time to 0.1% | | 5 | | μs |
| | | $V_{IN}$ = 5 Vpp, Gain = 1; Settling time to 0.01% | | 6 | | |
| Open Loop Output Impedance | $Z_{OL}$ | f = 100 Hz | | 0.8 | | Ω |
| **NOISE CHARACTERISTICS** | | | | | | |
| Total Harmonic Distortion plus Noise | THD+N | $V_{IN}$ = 5 Vpp, f = 1 kHz, Av = 1 | | 0.005 | | % |
| Input Referred Voltage Noise | $e_n$ | f = 1 kHz | | 30 | | nV/√Hz |
| | | f = 10 kHz | | 24 | | |
| Input Referred Current Noise | $i_n$ | f = 1 kHz | | 300 | | fA/√Hz |
| **SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Rejection Ratio | PSRR | No Load | 67 | 90 | | dB |
| | | | **64** | | | |
| Power Supply Quiescent Current | $I_{DD}$ | Per channel, no load | | 48 | **70** | μA |

10. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $R_L$ ≥ 10 kΩ, $V_{CM}$ = $V_{OUT}$ = mid−supply unless otherwise specified

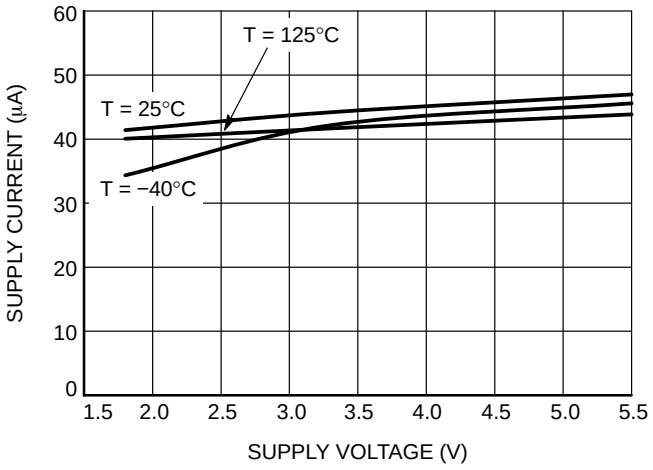



**Figure 2. Quiescent Current per Channel vs. Supply Voltage**

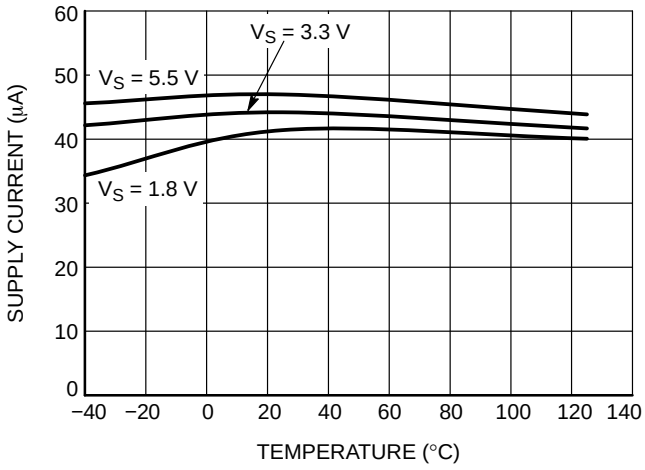



**Figure 3. Quiescent Current vs. Temperature**

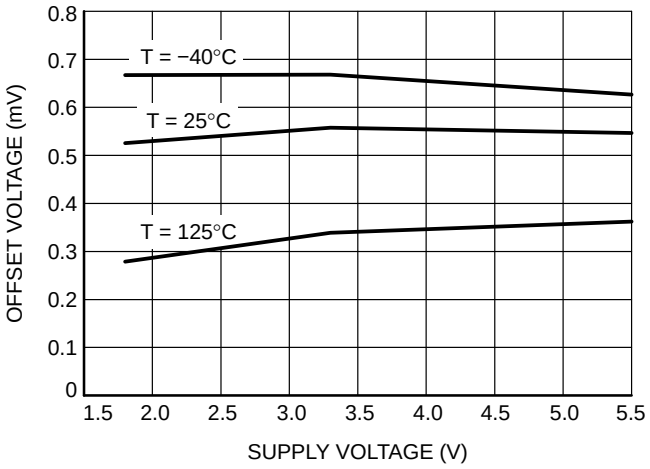



**Figure 4. Offset Voltage vs. Supply Voltage**

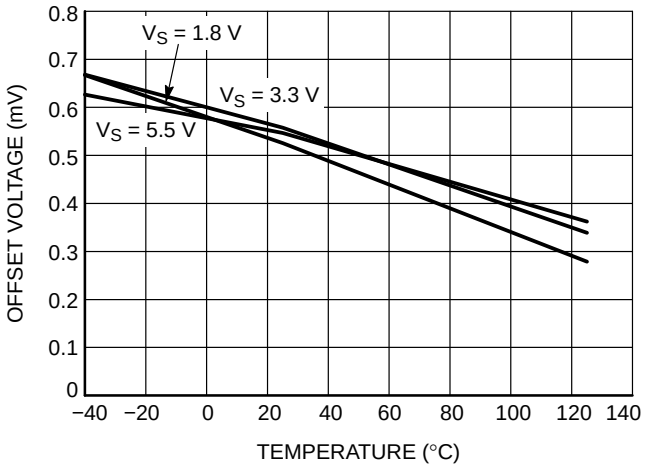



**Figure 5. Offset Voltage vs. Temperature**

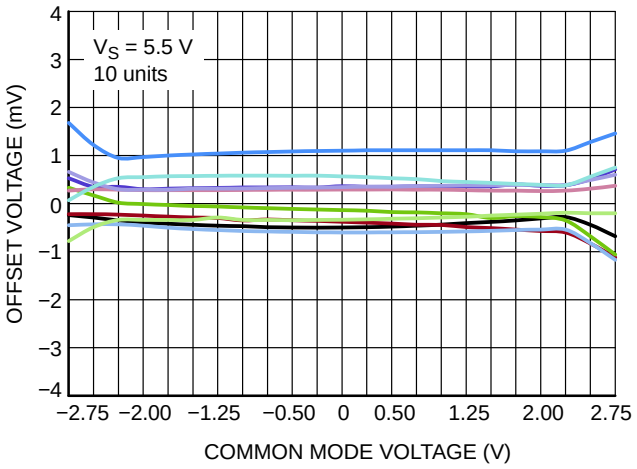



**Figure 6. Offset Voltage vs. Common Mode Voltage**

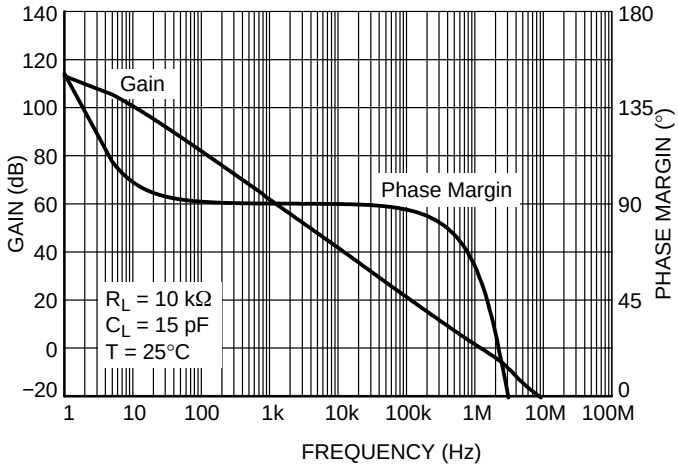



**Figure 7. Open−loop Gain and Phase Margin vs. Frequency**

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $R_L \geq 10\ k\Omega$, $V_{CM} = V_{OUT}$ = mid−supply unless otherwise specified

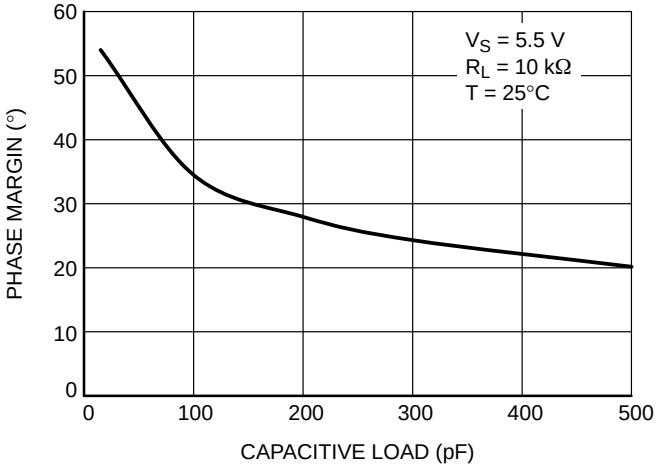



**Figure 8. Phase Margin vs. Capacitive Load**

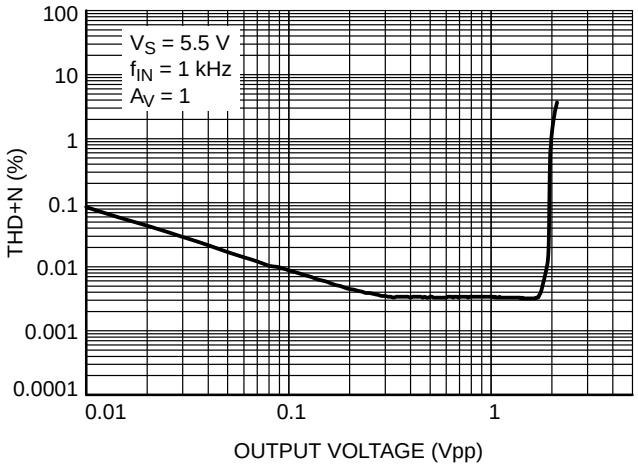



**Figure 9. THD + N vs. Output Voltage**

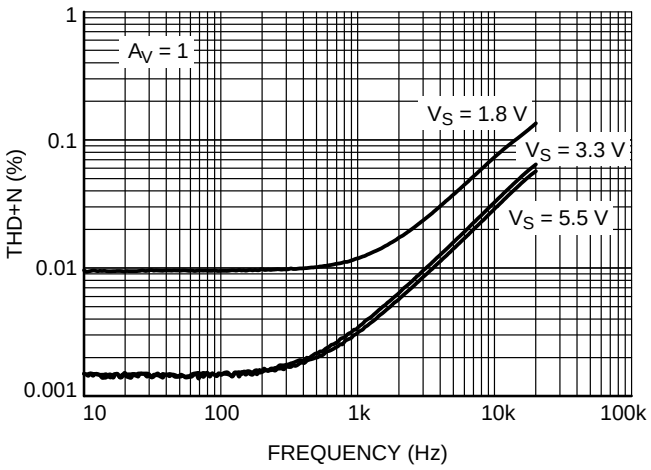



**Figure 10. THD + N vs. Frequency**

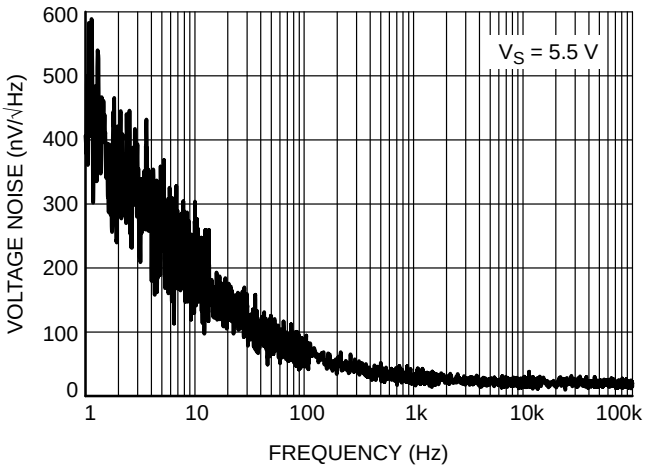



**Figure 11. Input Voltage Noise vs. Frequency**

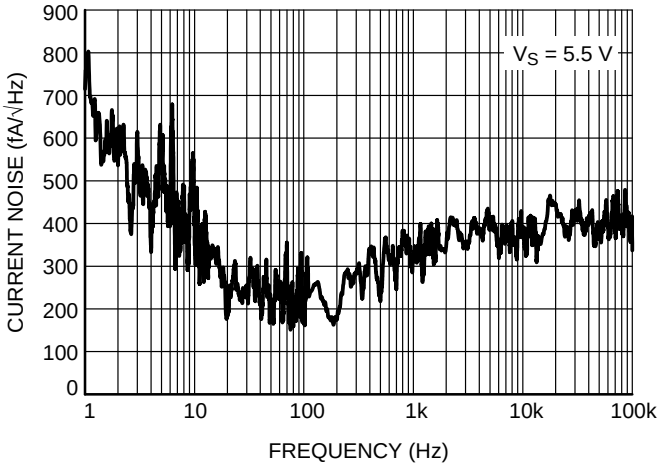



**Figure 12. Input Current Noise vs. Frequency**

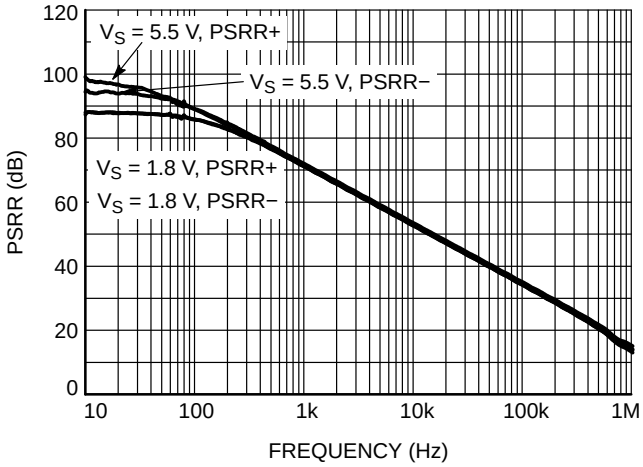



**Figure 13. PSRR vs. Frequency**

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $R_L$ ≥ 10 kΩ, $V_{CM}$ = $V_{OUT}$ = mid−supply unless otherwise specified

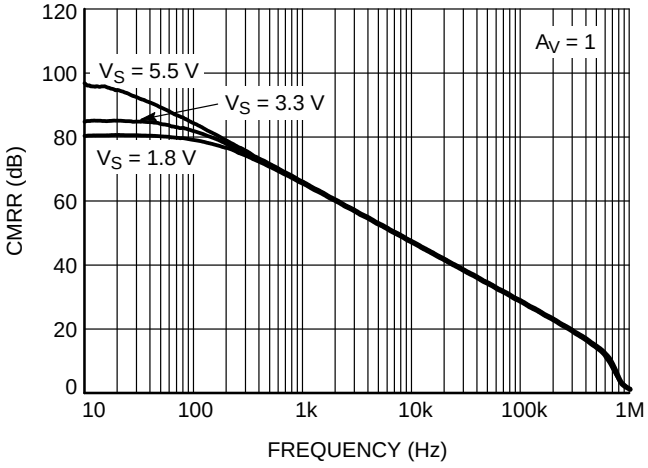



**Figure 14. CMRR vs. Frequency**

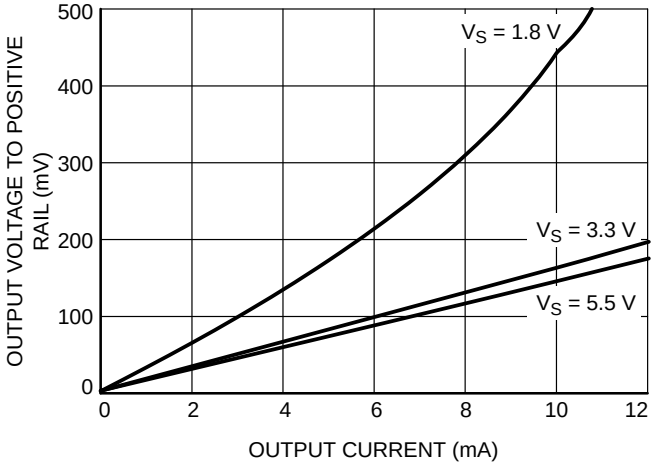



**Figure 15. Output Voltage High to Rail**

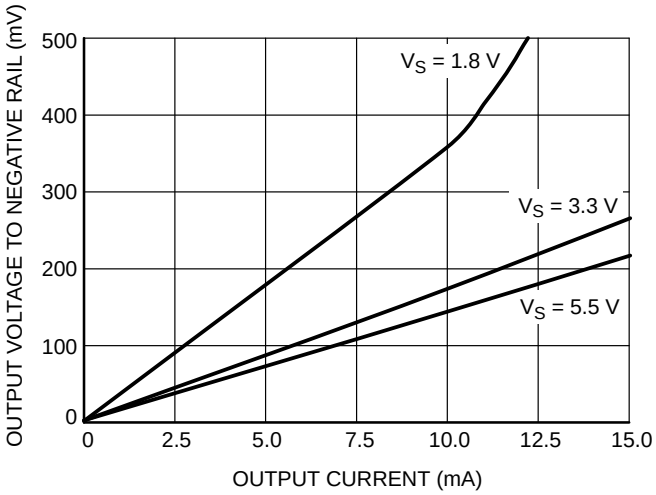



**Figure 16. Output Voltage Low to Rail**

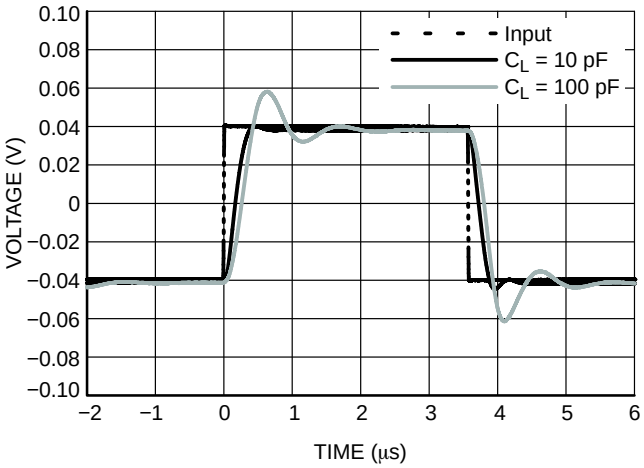



**Figure 17. Non−Inverting Small Signal Transient Response**

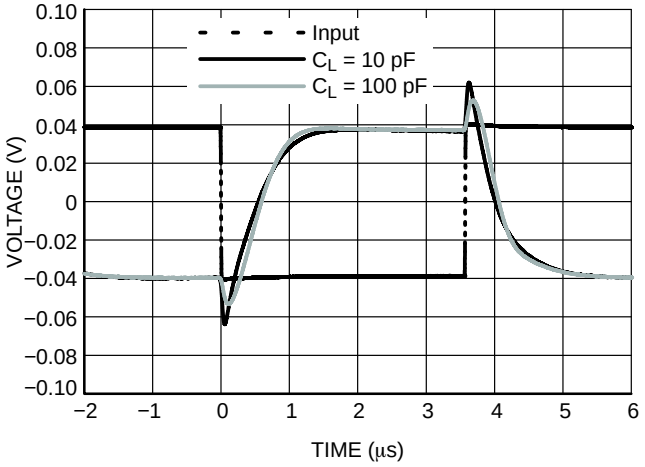



**Figure 18. Inverting Small Signal Transient Response**

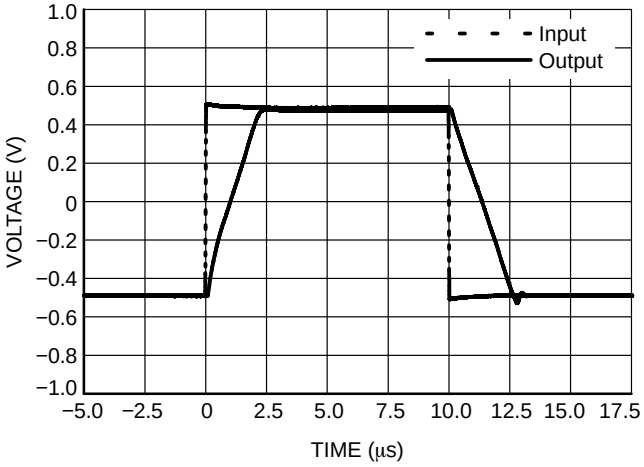



**Figure 19. Non−Inverting Large Signal Transient Response**

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $R_L$ ≥ 10 kΩ, $V_{CM}$ = $V_{OUT}$ = mid−supply unless otherwise specified

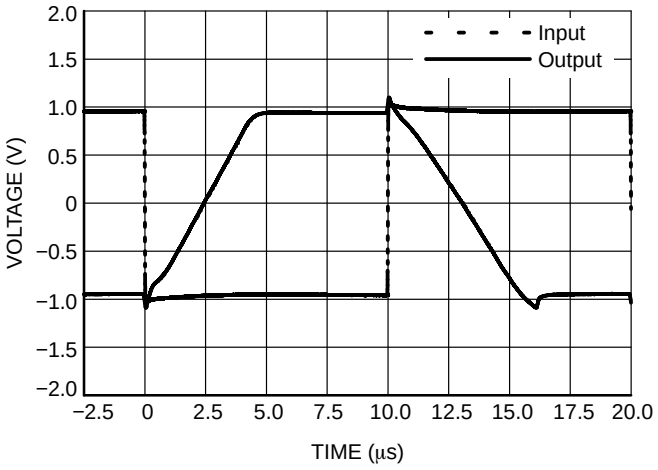



**Figure 20. Inverting Large Signal Transient Response**

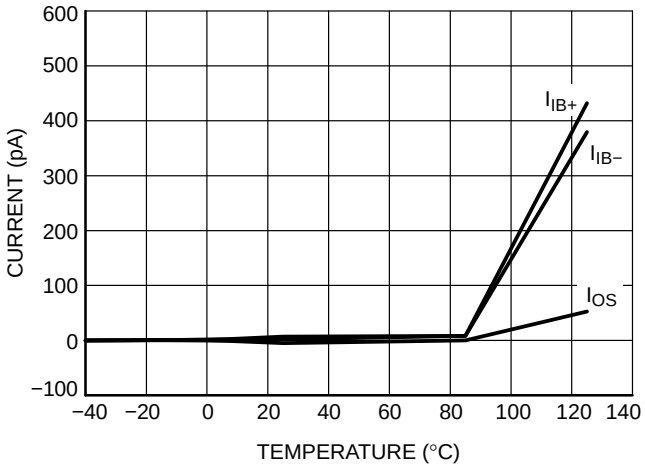



**Figure 21. Input Bias and Offset Current vs. Temperature**

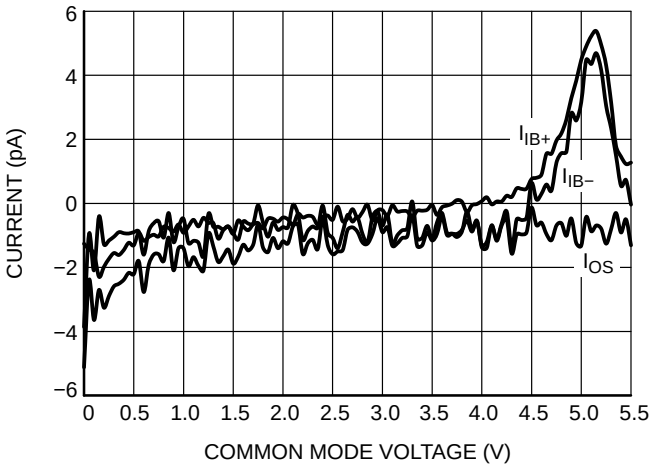



**Figure 22. Input Bias Current vs. Common Mode Voltage**

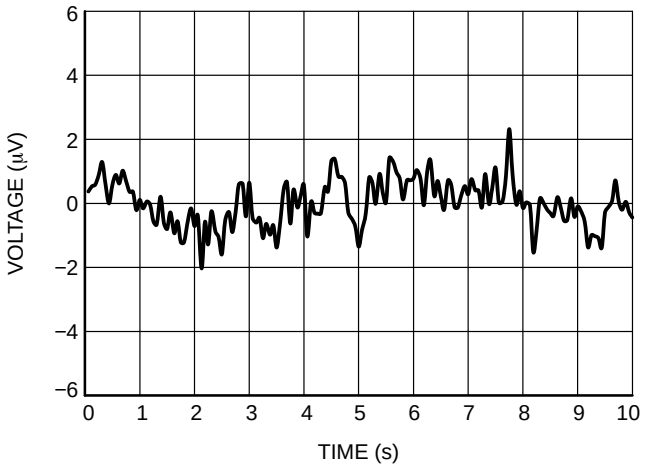



**Figure 23. 0.1 Hz to 10 Hz Noise**

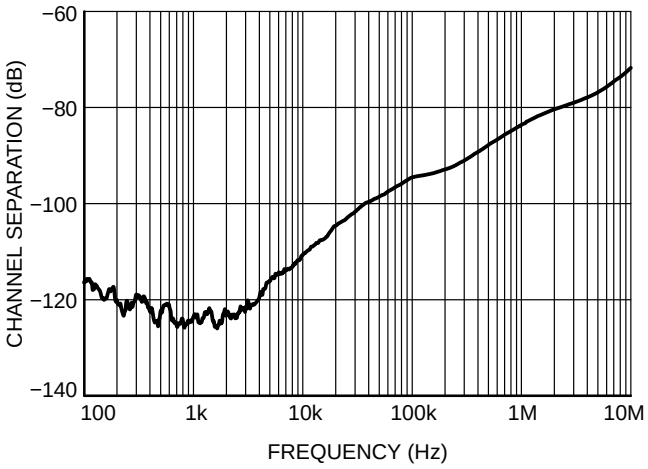



**Figure 24. Channel Separation vs. Frequency**

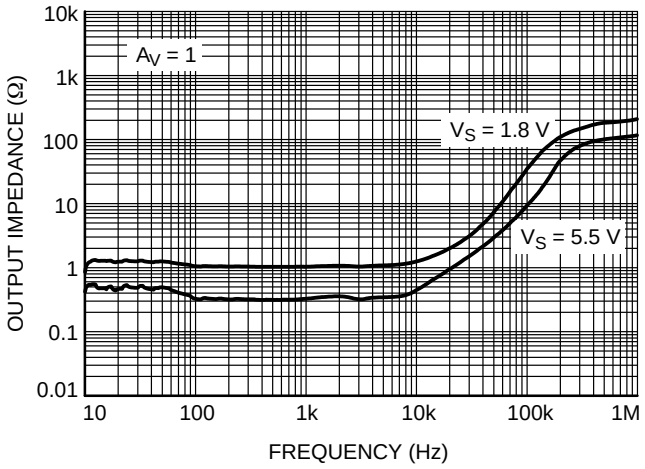



**Figure 25. Output Impedance vs. Frequency**

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $R_L \geq 10$ kΩ, $V_{CM} = V_{OUT}$ = mid−supply unless otherwise specified

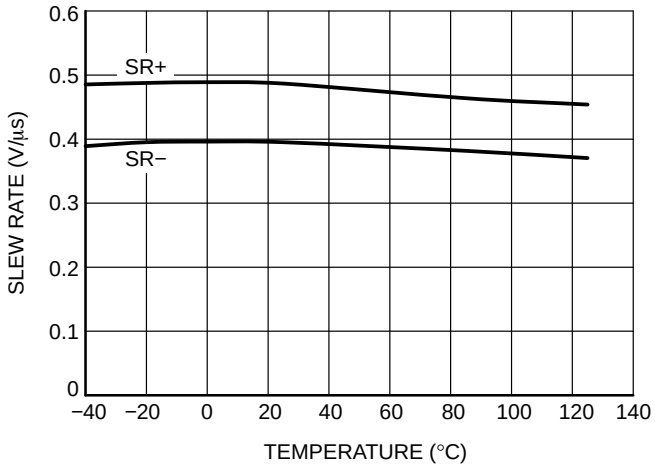
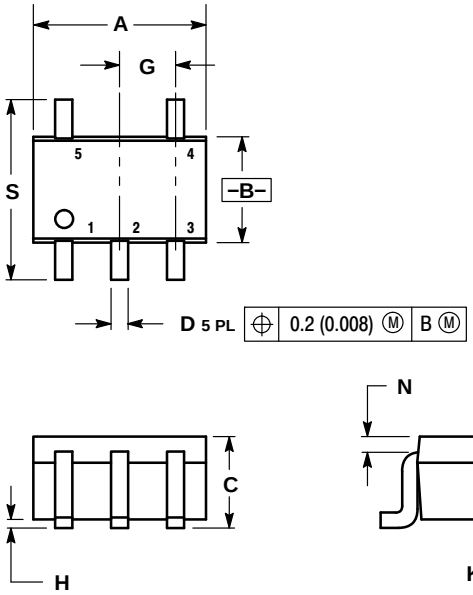



**Figure 26. Slew Rate vs. Temperature**

## PACKAGE DIMENSIONS

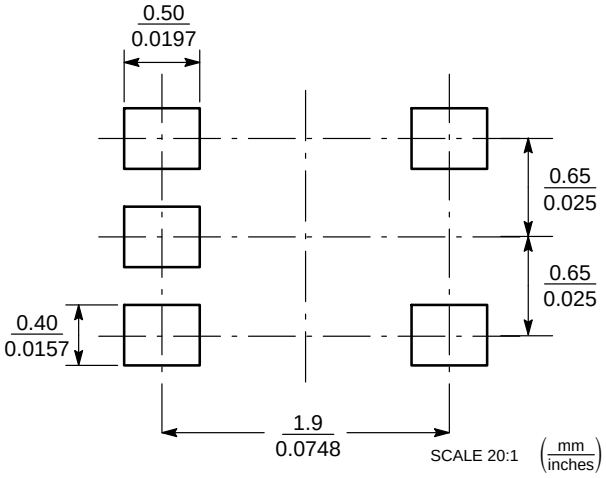
**SC−88A (SC−70−5/SOT−353)**
CASE 419A−02
ISSUE L




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

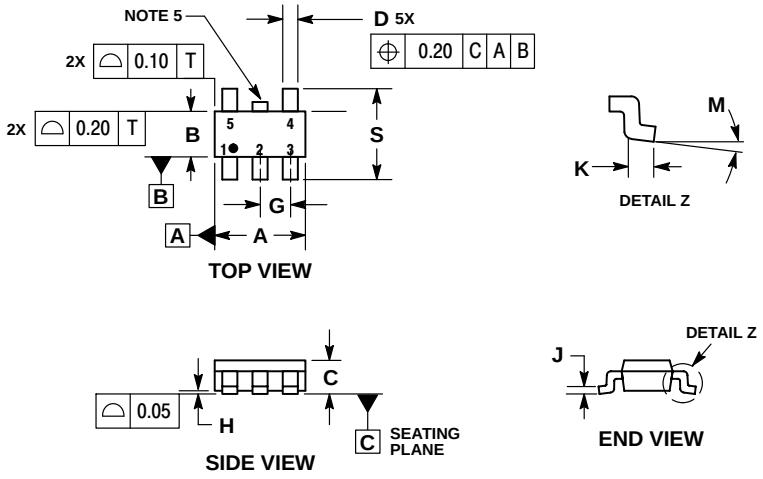
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

## SOLDER FOOTPRINT



## PACKAGE DIMENSIONS

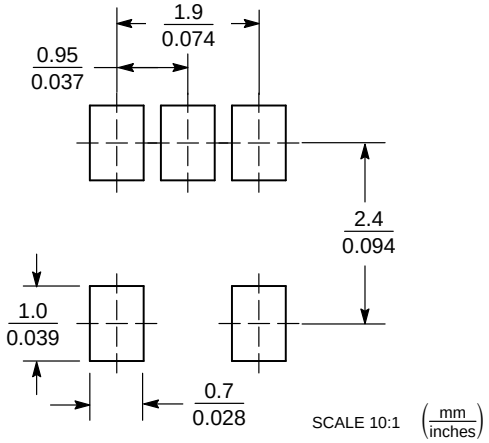
**TSOP−5**
CASE 483
ISSUE L




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 3.00 BSC | |
| B | 1.50 BSC | |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| M | 0 ° | 10 ° |
| S | 2.50 | 3.00 |

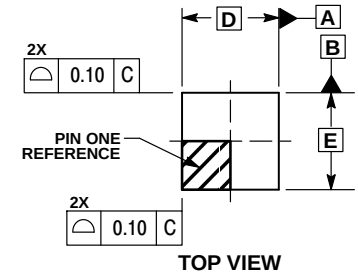
## SOLDERING FOOTPRINT*



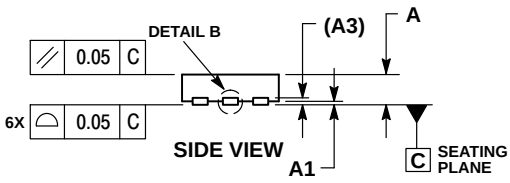

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

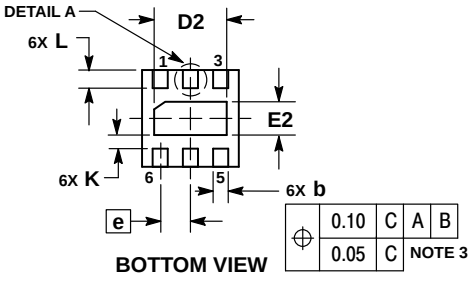
## PACKAGE DIMENSIONS

**UDFN6 1.6x1.6, 0.5P**
CASE 517AP
ISSUE O

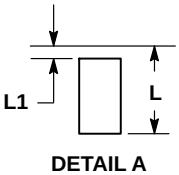



TOP VIEW

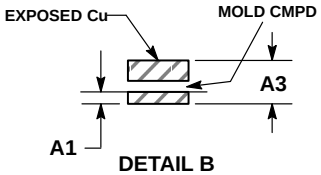



BOTTOM VIEW




**DETAIL A**
**OPTIONAL CONSTRUCTION**

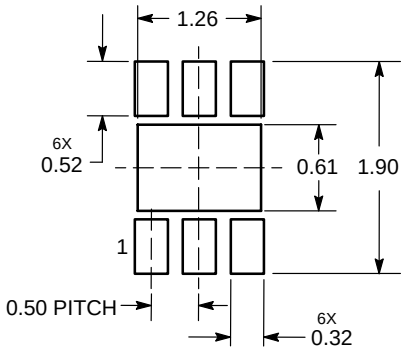



**DETAIL B**
**OPTIONAL CONSTRUCTION**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.20 | 0.30 |
| D | 1.60 BSC | |
| E | 1.60 BSC | |
| e | 0.50 BSC | |
| D2 | 1.10 | 1.30 |
| E2 | 0.45 | 0.65 |
| K | 0.20 | --- |
| L | 0.20 | 0.40 |
| L1 | 0.00 | 0.15 |

**SOLDERMASK DEFINED MOUNTING FOOTPRINT***

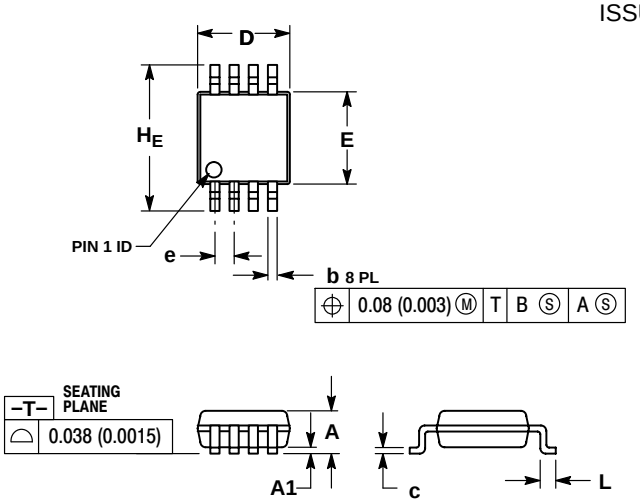



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

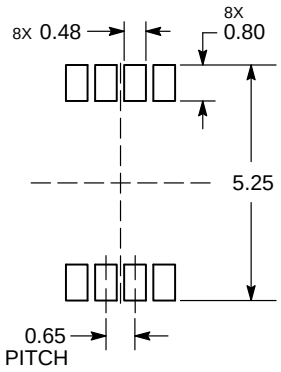
**Micro8™**
CASE 846A−02
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | −− | −− | 1.10 | −− | −− | 0.043 |
| A1 | 0.05 | 0.08 | 0.15 | 0.002 | 0.003 | 0.006 |
| b | 0.25 | 0.33 | 0.40 | 0.010 | 0.013 | 0.016 |
| c | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.40 | 0.55 | 0.70 | 0.016 | 0.021 | 0.028 |
| $H_E$ | 4.75 | 4.90 | 5.05 | 0.187 | 0.193 | 0.199 |

## RECOMMENDED SOLDERING FOOTPRINT*

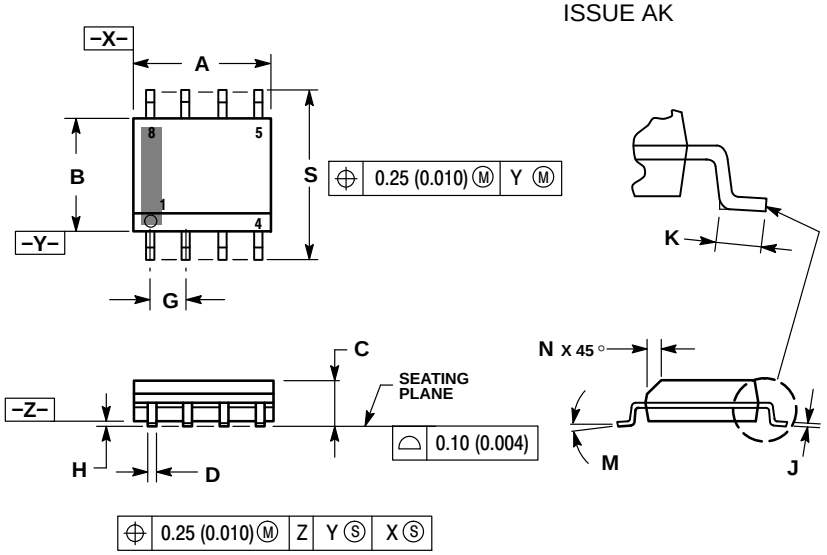



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**SOIC−8 NB**
CASE 751−07
ISSUE AK

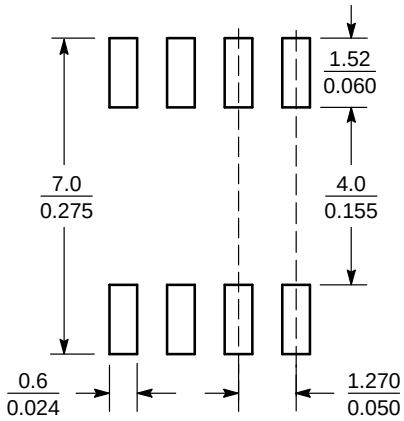



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

## SOLDERING FOOTPRINT*

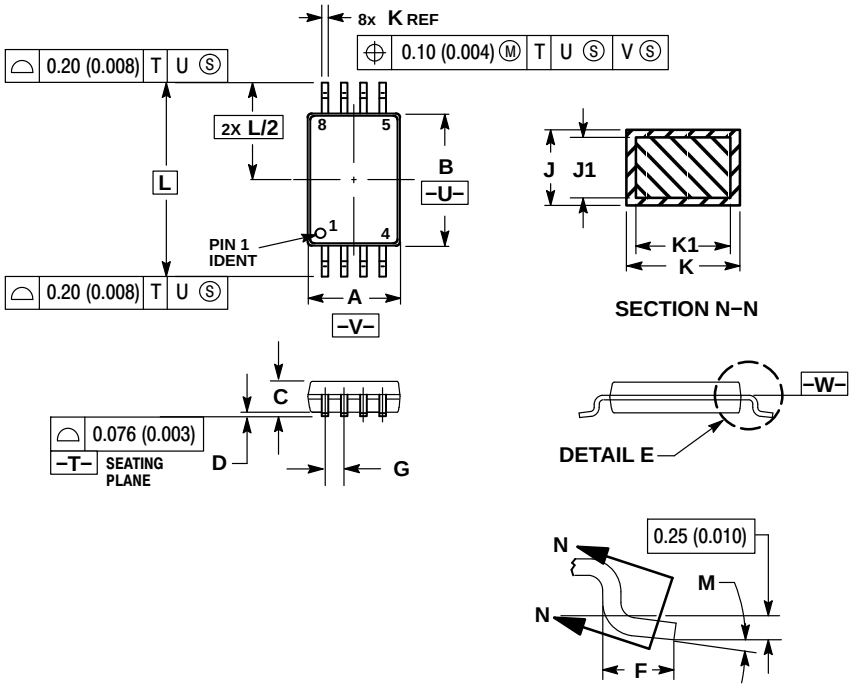



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**TSSOP−8**
CASE 948S
ISSUE C

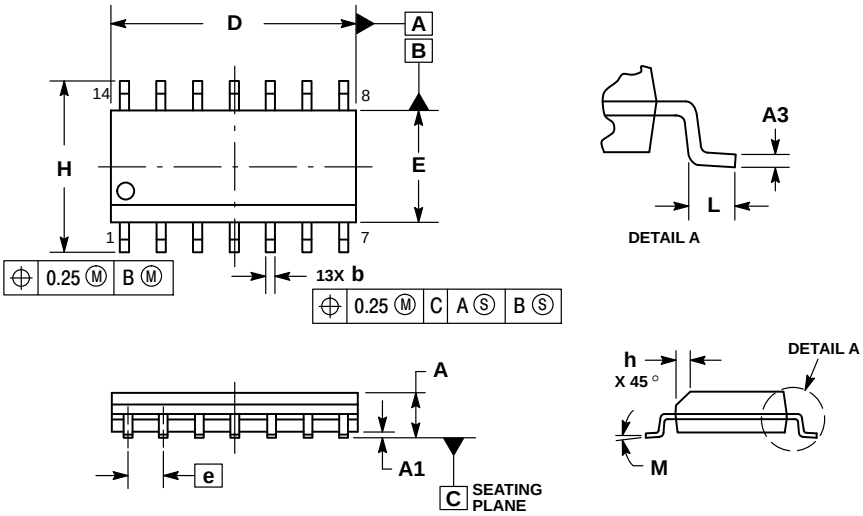



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.70 | 0.020 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

## PACKAGE DIMENSIONS

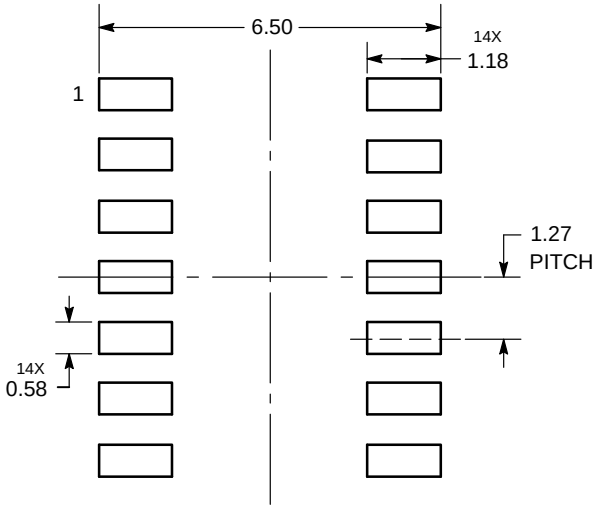
**SOIC−14 NB**
CASE 751A−03
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |

### SOLDERING FOOTPRINT*

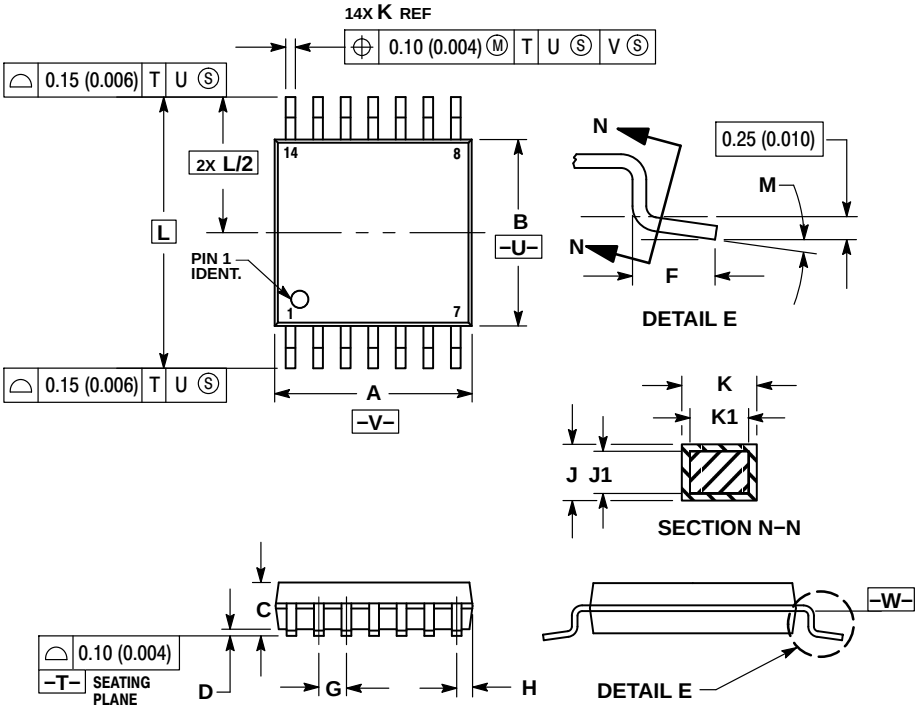



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

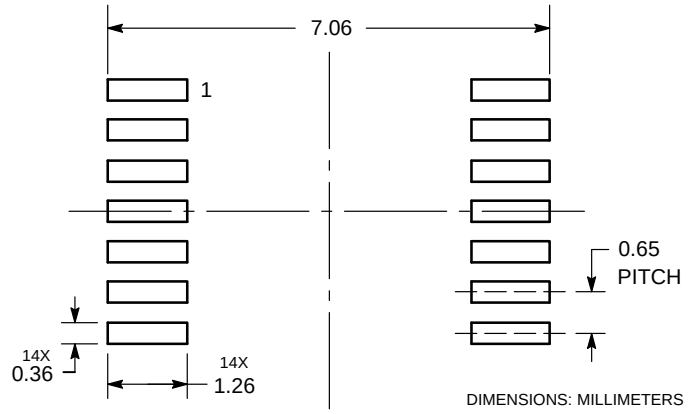
**TSSOP−14**
CASE 948G
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

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