

## 32-Channel, 256 Gray-Shade High Voltage Driver

### Features

- ▶ HVCMOS® technology
- ▶ 5.0V CMOS inputs
- ▶ Output voltage up to +80V
- ▶ PWM gray shade conversion
- ▶ Capable of 256 levels of gray shading
- ▶ 10MHz shift and count clock frequency
- ▶ 20MHz data throughput rate
- ▶ 8 bit data bus
- ▶ 32 outputs per device
- ▶ BLANK function
- ▶ Output polarity control

### Applications

- ▶ Field Emission Displays (FED)
- ▶ Polymer Liquid Crystal Displays (PLCD)
- ▶ Vacuum Fluorescent Displays (VFD)

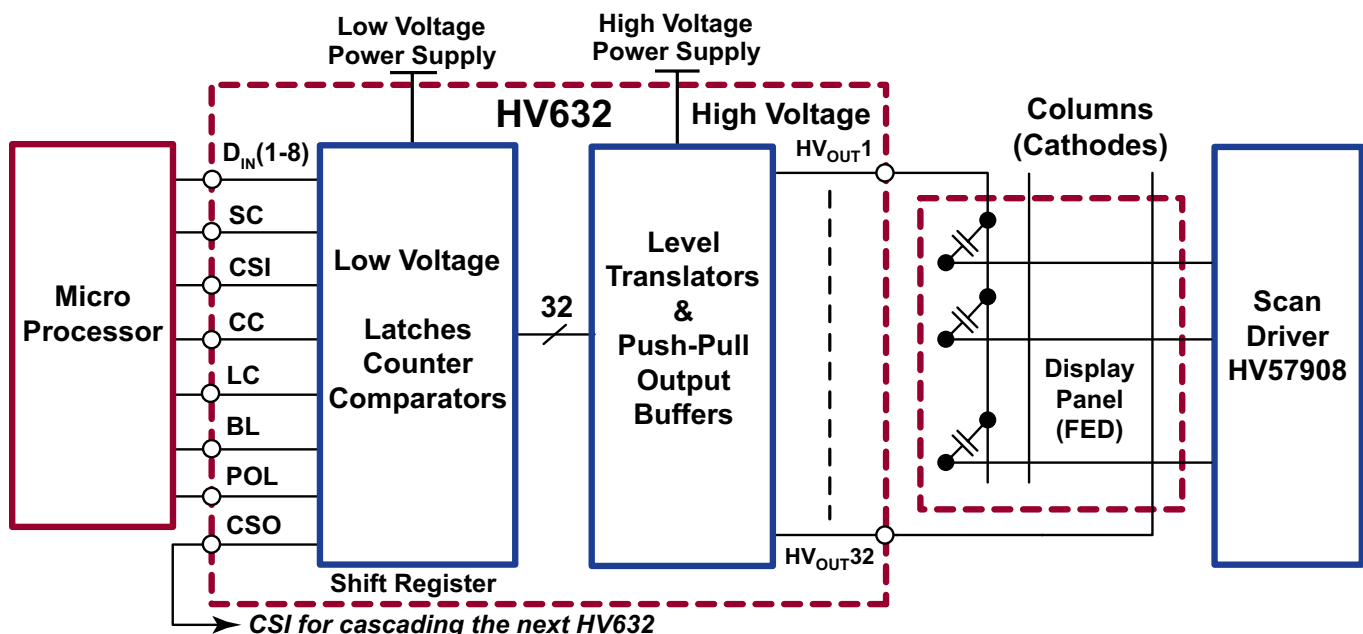
### General Description

The HV632 is a 32-channel gray-shade column driver IC designed for driving electrofluorescent displays. Using Supertex's unique HVCMOS® technology, it is capable of 256 levels of gray shading by PWM conversion.

Input data, in groups of eight, is latched into a set of data latches on both edges of the shift clock. The data shifted in the first data latch corresponds to  $HV_{OUT1}$ , the second data latch corresponds to  $HV_{OUT2}$ , and so on. These data are compared to the contents of the master binary counter which counts on both edges of the count clock. Each time the master counter begins to decrement from 1111 1111, the data in the data latches are compared with the contents of the counter; if they match, the corresponding outputs will go high. The master counter counts down to 00000001 and then starts to count up again. The outputs that are at high will stay at high until the contents of the counter match the data in the data latches again. Therefore, the higher the binary data in the data latches, the longer the outputs will stay at high. Thus, different high voltage pulse widths are produced. When the counter reaches its 1111 1111 count while counting up, the device is ready for the next operation cycle. A data value of 0000 0000 produces no pulse; the output stays low.

The BLANK input signal will reset the master counter to all ones (1111 1111) and set all high voltage outputs to low, or will set all high voltage outputs to high state, when the POL is low. The POL input signal, forced low, will invert the polarity of the output pulse. If left unconnected, POL input will be pulled high to  $V_{DD}$  by an on-chip resistor.

### Typical Application Circuit

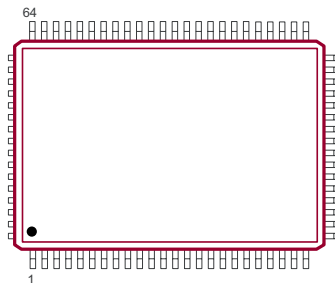


## Ordering Information

Part Number	Package Option	Packing
HV632PG-G	64-Lead PQFP	66/Tray

-G denotes a lead (Pb)-free / RoHS compliant package

## Pin Configuration



**64-Lead PQFP**  
(top view)

## Absolute Maximum Ratings

Parameter	Value
Supply voltage, $V_{DD}$	-0.5V to +7.5V
Supply voltage, $V_{PP}$	-0.5V to +90V
Logic input levels	-0.5V to $V_{DD} + 0.5V$
Continuous total power dissipation <sup>1</sup>	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

**Note:**

- For operation above 25°C ambient derate linearly to 85°C at 20mW/°C

## Product Marking

Top Marking

L = Lot Number  
 YY = Year Sealed  
 WW = Week Sealed  
 C = Country of Origin  
 A = Assembler ID  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

**64-Lead PQFP**

## Typical Thermal Resistance

Package	$\theta_{ja}$
64-Lead PQFP	41°C/W

## Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
$V_{DD}$	Logic supply voltage	4.5	5.5	V
$V_{PP}$	Positive high voltage supply	12	80	V
$V_{IL}$	Low-level input voltage	0	1.0	V
$V_{IH}$	High-level input voltage	$V_{DD} - 1$	$V_{DD}$	V
$T_A$	Operating temperature	-40	+85	°C

## Electrical Characteristics (over recommended operating conditions of $V_{DD} = 5.0V$ , $V_{PP} = 80V$ , and $T_A = 25^\circ C$ unless noted)

Sym	Parameter	Min	Max	Units	Conditions
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### Low Voltage DC Characteristics (Digital)

$V_{DD}$	Low voltage digital supply voltage	4.5	5.5	V	---
$I_{DD}$	$V_{DD}$ supply current	-	25	mA	$f_{SC} = 10MHz, f_{CC} = 10MHz$
$I_{DDQ}$	Quiescent $V_{DD}$ supply current	-	150	$\mu A$	All $V_{IN} = GND$ , Count Clock = $V_{DD}$
$I_{IH}$	High-level input current	-	10	$\mu A$	$V_{IN} = V_{DD}$
$I_{IL}$	Low-level input current	-	-10	$\mu A$	$V_{IL} = GND$
$I_{OH}$	High level output current	-1.0	-	mA	$V_{OUT} = 0.9V_{DD}$
$I_{OL}$	Low level output current	1.0	-	mA	$V_{OUT} = 0.1V_{DD}$

**Electrical Characteristics** (over recommended operating conditions of  $V_{DD} = 5.0V$ ,  $V_{PP} = 80V$ , and  $T_A = 25^\circ C$  unless noted)

Sym	Parameter	Min	Max	Units	Conditions
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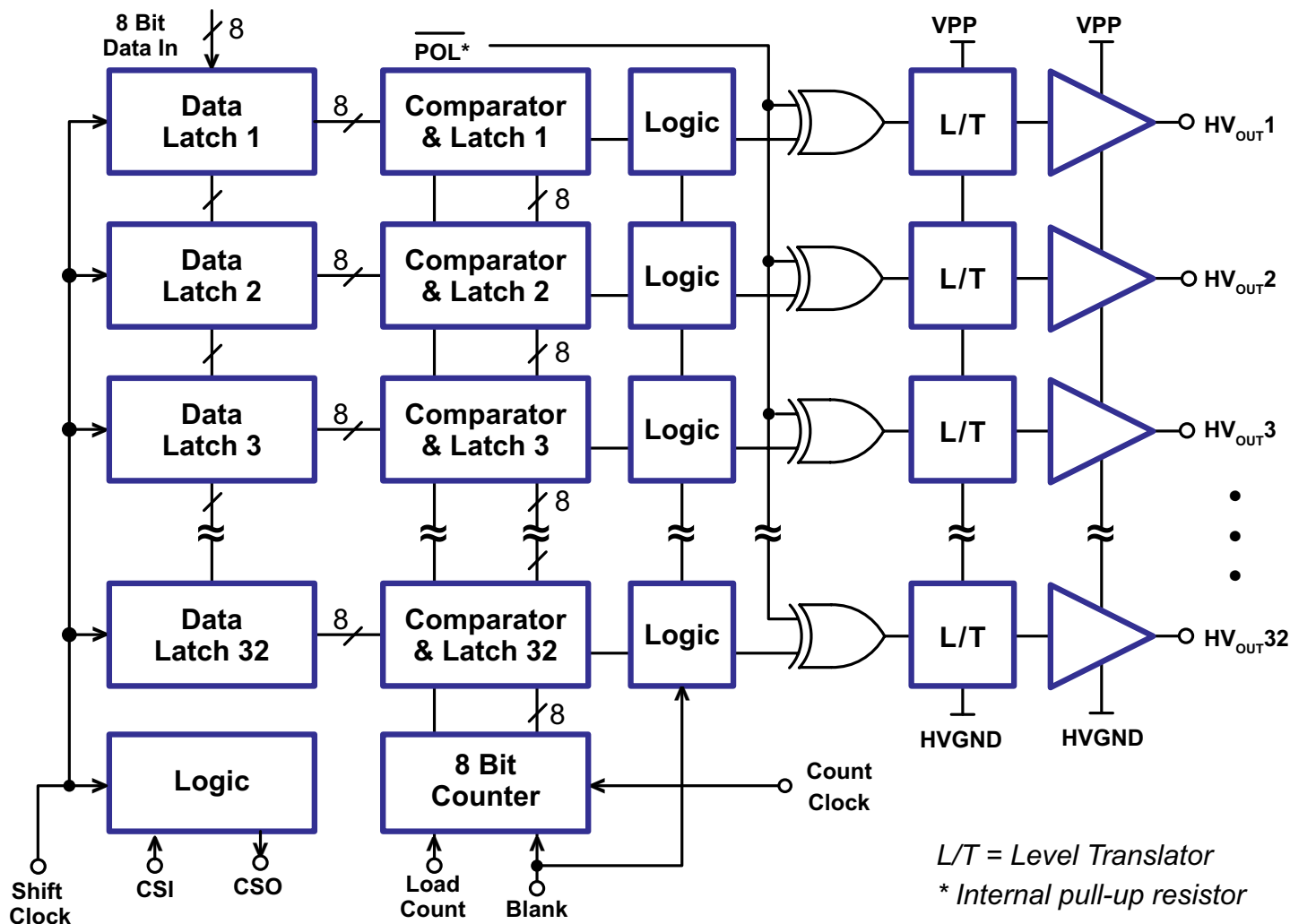
**High Voltage DC Characteristics**

$I_{PPQ}$	Quiescent $V_{PP}$ supply current	-	100	$\mu A$	All $HV_{OUT}$ low or high
$I_{OUT(p)}$	P-channel output current	-4.0	-	mA	$HV_{OUT} = 75V$
$I_{OUT(n)}$	N-channel output current	4.0	-	mA	$HV_{OUT} = 5.0V$
$I_{PP}$	$V_{PP}$ supply current	-	1.1	mA	$C_L = 0pF$ , $F_{CC} = 10MHz$

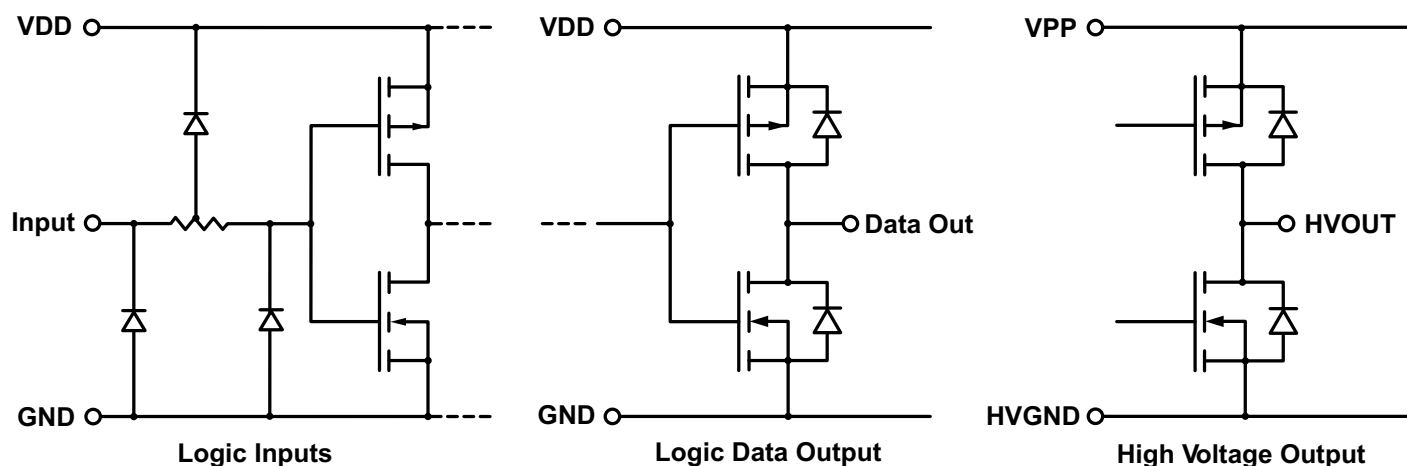
**AC Characteristics**

$f_{SC}$	Shift clock frequency	-	10	MHz	---
$f_{CC}$	Count clock frequency	-	10	MHz	---
$f_{DIN}$	Data In frequency	-	20	MHz	---
$t_{CW}$	Chip select pulse width	80	-	ns	---
$t_{CSS}$	Chip select to shift clock set-up time	5.0	-	ns	---
$t_{CSH}$	Chip select to shift clock hold time	15	-	ns	---
$t_{SCC}$	Shift clock cycle time	100	-	ns	---
$t_{DSS}$	Data to shift clock set-up time	10	-	ns	---
$t_{DSH}$	Data to shift clock hold time	40	-	ns	---
$t_{DW}$	Data In pulse width	50	-	ns	---
$t_{LCW}$	Load count pulse width	75	-	ns	---
$t_{CCW}$	Count clock pulse width	50	-	ns	---
$t_{CCC}$	Count clock cycle time	100	-	ns	---
$t_{LCD}$	Load count to count clock delay	100	-	ns	---
$t_{CCD}$	Count clock to $HV_{OUT}$ turn-on/turn-off	-	300	ns	$C_L = 15pF$
$t_{BLW}$	BLANK pulse width	700	-	ns	---
$t_{BLD}$	BLANK to $HV_{OUT}$ delay	-	500	ns	$C_L = 15pF$
$t_{CDD}$	Count clock delay between count down and count up cycles	150	-	ns	---
$t_{CSOH}$	CSO delay output for High	-	40	ns	$C_L = 15pF$
$t_{CSOL}$	CSO delay output for Low	-	40	ns	$C_L = 15pF$

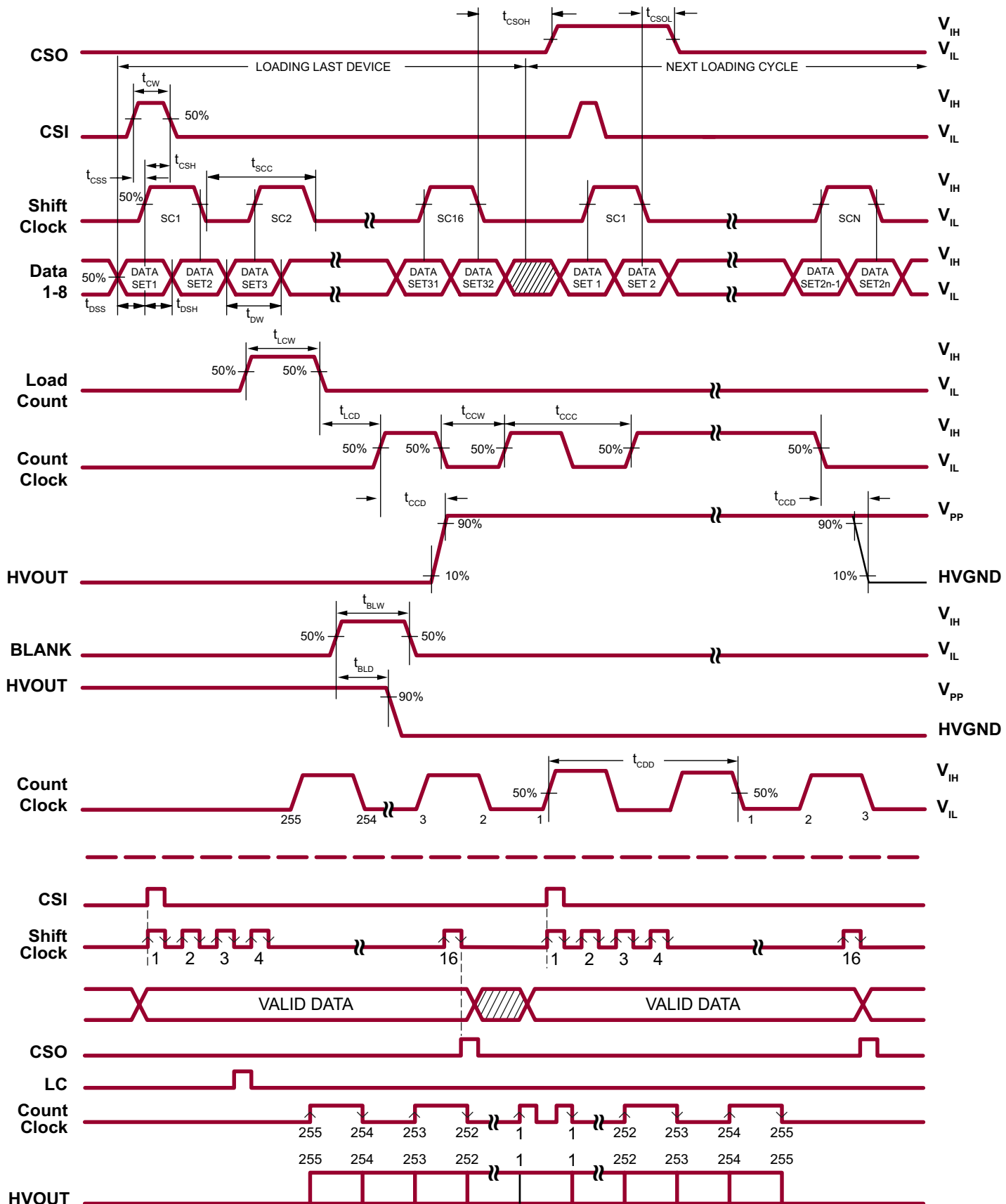
### Functional Block Diagram



### Input and Output Equivalent Circuits



Timing Diagrams



**Function Table**

Sequence	Function	Data In (D1 - D8)	CSI	CSO	Shift Clock	Load Count	Count Clock	HV <sub>OUT</sub>
1	Shift data from HV <sub>OUT</sub> 1 to HV <sub>OUT</sub> 32	H	-	Output	-	L	L	L
		L						H
2	Load shift register	X	Pre-define by 1 or 2		-	L	L	-
3	Load counter	X			L	-	L	-
4	Counting/voltage conversion	X			L	L	-	-

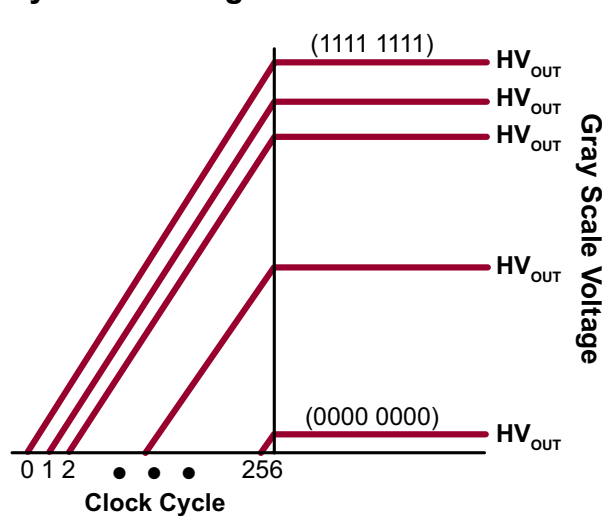
**Blank Polarity Table**

Blank	Polarity	HV <sub>OUT</sub>
0	0	Current output state.
0	1	Inverts current output state.
1	0	Sets all outputs high.
1	1	Sets all outputs low.

**Gray Shade Decoding Scheme**

Shade Number	D8	D7	D6	D5	D4	D3	D2	D1
256	1	1	1	1	1	1	1	1
255	1	1	1	1	1	1	1	0
254	1	1	1	1	1	1	0	1
253	1	1	1	1	1	1	0	0
252	1	1	1	1	1	0	1	1
251	1	1	1	1	1	0	1	0
250	1	1	1	1	1	0	0	1
249	1	1	1	1	1	0	0	0
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
7	0	0	0	0	0	1	1	0
6	0	0	0	0	0	1	0	1
5	0	0	0	0	0	1	0	0
4	0	0	0	0	0	0	1	1
3	0	0	0	0	0	0	1	0
2	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0

**Gray Scale Voltage**



## Pin Description

Pin #	Function	Description
1	NC	No connect
2	NC	
3	NC	
4	HV <sub>OUT</sub> 17	High-voltage outputs
5	HV <sub>OUT</sub> 18	
6	HV <sub>OUT</sub> 19	
7	HV <sub>OUT</sub> 20	
8	HV <sub>OUT</sub> 21	
9	HV <sub>OUT</sub> 22	
10	HV <sub>OUT</sub> 23	
11	HV <sub>OUT</sub> 24	
12	HV <sub>OUT</sub> 25	
13	HV <sub>OUT</sub> 26	
14	HV <sub>OUT</sub> 27	
15	HV <sub>OUT</sub> 28	
16	HV <sub>OUT</sub> 29	
17	HV <sub>OUT</sub> 30	
18	HV <sub>OUT</sub> 31	
19	HV <sub>OUT</sub> 32	
20	GND	Digital ground
21	GND	
22	HVGND	High voltage ground
23	VPP	Positive high-voltage supply
24	CSI	Chip select input to enable the device to accept data
25	CSO	Chip select output to enable the next device
26	BLANK	Input to reset the counter and HVOUT
27	D1	Inputs for binary-format parallel data (D8 is the most significant bit)
28	D2	
29	D3	
30	D4	
31	Count clock	Input to the counter
32	POL	Output polarity control
33	Load count	Input to initiate the counting

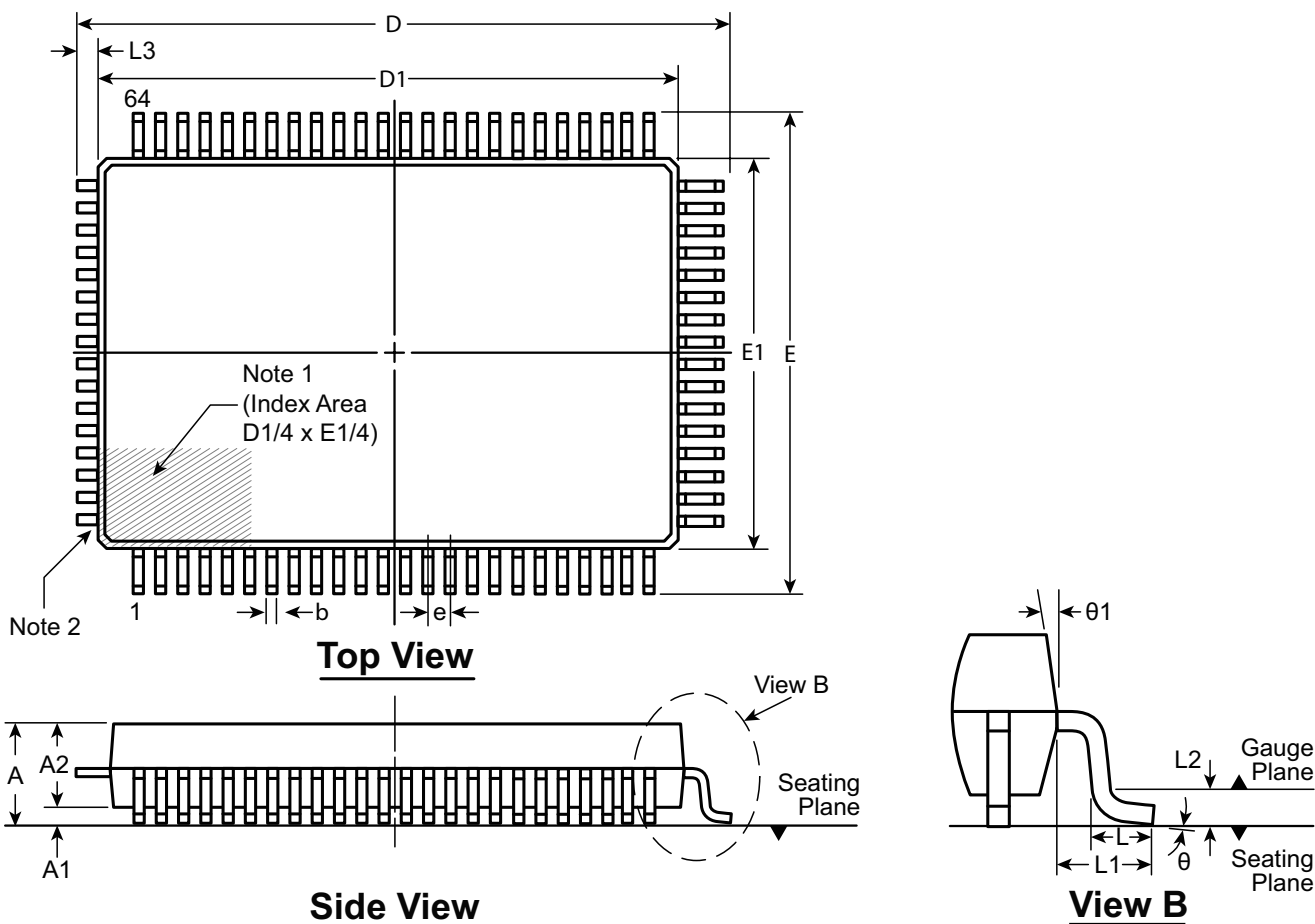
## Pin Description

Pin #	Function	Description
34	Shift clock	Triggers data on both edges
35	NC	No connect
36	D5	Inputs for binary-format parallel data (D8 is the most significant bit)
37	D6	
38	D7	
39	D8	
40	VDD	Low-voltage digital supply voltage
41	NC	No connect
42	NC	
43	VPP	Positive high-voltage supply
44	HVGND	High voltage ground
45	NC	No connect
46	HV <sub>OUT1</sub>	High-voltage outputs
47	HV <sub>OUT2</sub>	
48	HV <sub>OUT3</sub>	
49	HV <sub>OUT4</sub>	
50	HV <sub>OUT5</sub>	
51	HV <sub>OUT6</sub>	
52	HV <sub>OUT7</sub>	
53	HV <sub>OUT8</sub>	
54	HV <sub>OUT9</sub>	
55	HV <sub>OUT10</sub>	
56	HV <sub>OUT11</sub>	
57	HV <sub>OUT12</sub>	
58	HV <sub>OUT13</sub>	
59	HV <sub>OUT14</sub>	
60	HV <sub>OUT15</sub>	
61	HV <sub>OUT16</sub>	
62	NC	No connect
63	NC	
64	NC	



# 64-Lead PQFP (3-Sided) Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



- Note:**
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
  2. The leads on this side are trimmed.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	L3	θ	θ1	
Dimension (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0.55 REF	0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		0.88				3.5°	-
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7°	16°

Drawings not to scale.  
Supertex Doc. #: DSPD-64PQFP, Version NR090608.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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