MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

Synchronous Presettable Binary Counter

The MC74AC161/74ACT161 and MC74AC163/74ACT163 are high−speed synchronous modulo−16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters.

The MC74AC161/74ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC163/74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High−Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- ′ACT161 and ′ACT163 Have TTL Compatible Inputs
- **These devices are available in Pb−free package(s). Specifications herein apply to both standard and Pb−free devices. Please see our website at www.onsemi.com for specific Pb−free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

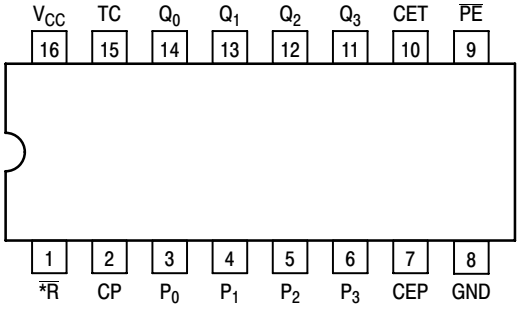

Figure 1. Pinout: 16−Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$	(′161) Asynchronous Master Reset Input
$\overline{SR}$	(′163) Synchronous Reset Input
P_0−P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0−Q_3	Flip−Flop Outputs
TC	Terminal Count Output

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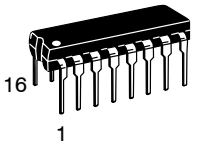
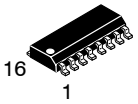
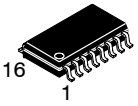


DIP−16
N SUFFIX
CASE 648



SO−16
D SUFFIX
CASE 751B



EIAJ−16
M SUFFIX
CASE 966

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 11 of this data sheet.

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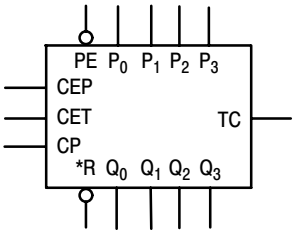


*$\overline{MR}$ for ′161
*$\overline{SR}$ for ′163

Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC161/ACT161 and MC74AC163/ACT163 count modulo−16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip−flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the ′161) occur as a result of, and synchronous with, the LOW−to−HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (′161), synchronous reset (′163), parallel load, count−up and hold. Five control inputs − Master Reset ($\overline{MR}$, ′161), Synchronous Reset ($\overline{SR}$, ′163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) −□determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip−flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (′161) or $\overline{SR}$ (′163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC161/ACT161 and MC74AC163/ACT163 use D−type edge−triggered flip−flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip−flops, counters or registers.

Logic Equations:

$$\text{Count Enable} = CEP \cdot CET \cdot \overline{PE}$$
$$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$$

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	**Action on the Rising Clock Edge ( )**
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For ′163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

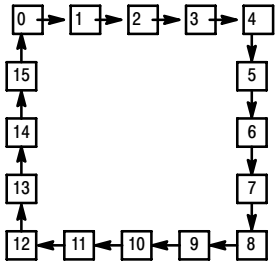
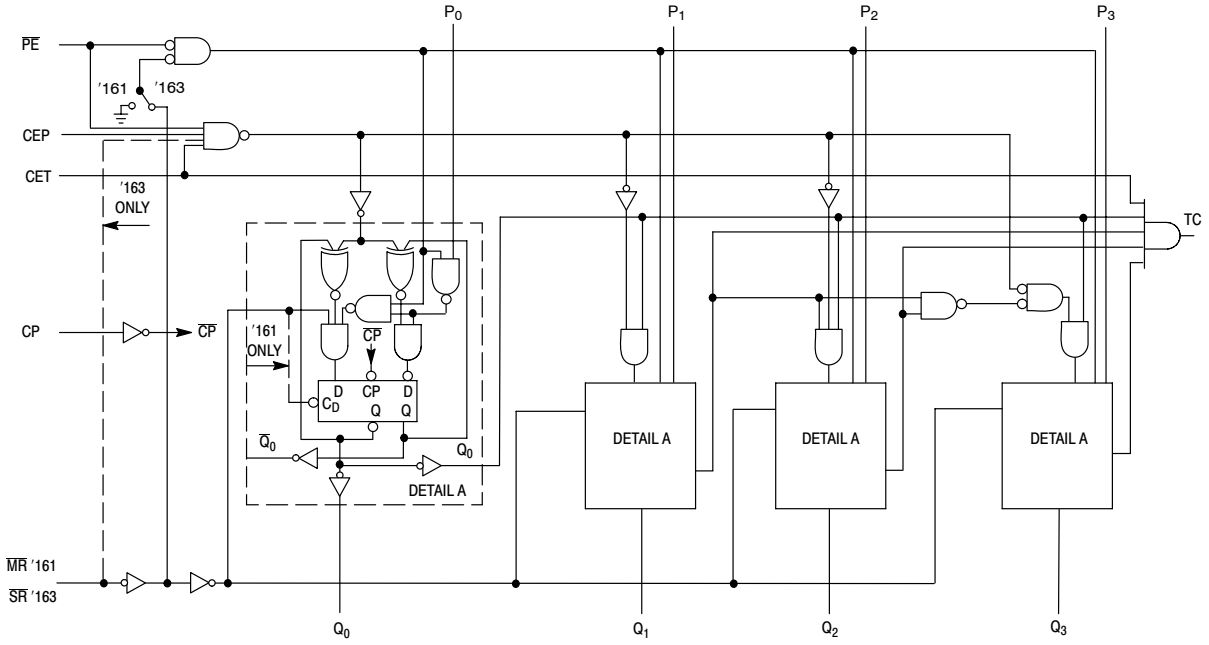


Figure 3. State Diagram



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 4. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current – High		–	–	−24	mA
I_{OL}	Output Current – Low		–	–	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		74AC T_A = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	–	2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5	–	3.86	3.76		I_{OH} −24 mA
		5.5	–	4.86	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	–	0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5	–	0.36	0.44		I_{OL} 24 mA
		5.5	–	0.36	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC161 T_A = +25°C C_L = 50 pF			74AC161 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	111 167	− −	60 95	− −	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.0 5.0	12.0 9.0	1.5 1.0	13.5 9.5	ns	3−6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	7.0 5.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3−6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.0 6.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	8.5 6.5	14.0 11.0	2.5 2.0	15.5 11.5	ns	3−6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	5.5 3.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3−6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	6.5 5.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	2.0 1.5	6.0 5.5	12.0 9.5	1.5 1.5	13.5 10.0	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0	3.5 2.5	10.0 8.5	15.0 13.0	3.0 2.5	17.5 13.5	ns	3−6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC163 T_A = +25°C C_L = 50 pF			74AC163 T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	95 140	− −	60 95	− −	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.5 1.0	13.5 9.5	ns	3−6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3−6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	2.5 2.0	15.5 11.5	ns	3−6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3−6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3−6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC161 T_A = +25°C C_L = 50 pF		74AC161 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	6.0 3.5	13.5 8.5	16.0 10.5	ns	3–9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −4.0	−1.0 0	−0.5 0	ns	3–9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	6.5 4.0	11.5 7.5	14.0 8.5	ns	3–9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−6.0 −3.5	0 0.5	0 1.0	ns	3–9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.0 2.0	6.0 4.5	7.0 5.0	ns	3–9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−3.5 −2.0	0 0	0 0.5	ns	3–9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	2.0 2.0	3.5 2.5	4.0 3.0	ns	3–6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	2.0 2.0	4.0 3.0	4.5 3.5	ns	3–6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	3.0 2.5	5.5 4.5	7.5 6.0	ns	3–6
t_{rec}	Recovery TIme $\overline{MR}$ to CP	3.3 5.0	−2.0 −1.0	−0.5 0	0 0.5	ns	3–9

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC163 T_A = +25°C C_L = 50 pF		74AC163 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0	13.5 8.5	16.0 10.5	ns	3–9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0	−1.0 0	−0.5 0	ns	3–9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14 9.5	16.5 11.0	ns	3–9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5	−0.5 0	ns	3–9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5	14.0 8.5	ns	3–9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5	−0.5 0	ns	3–9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	7.0 5.0	ns	3–9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0	0 0.5	ns	3–9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	4.0 3.0	ns	3–6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	4.5 3.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT		74ACT	Unit	Conditions
			T_A = +25°C		T_A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = –50 μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} –24 mA I_{OH} –24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	–	1.5	mA	V_I = V_{CC} – 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT161 T_A = +25°C, C_L = 50 pF			74ACT161 T_A = −40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	115	125	−	100	−	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	8.0	9.5	1.5	10.5	ns	3−6
t_{PHL}	Propagation Delay CP or Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	8.0	10.5	1.5	11.5	ns	3−6
t_{PLH}	Propagation Delay CP to TC	5.0	2.0	11.0	11.0	1.5	12.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	5.0	1.5	11.0	12.5	1.5	13.5	ns	3−6
t_{PLH}	Propagation Delay CET to TC	5.0	1.5	7.5	8.5	1.5	10.0	ns	3−6
t_{PHL}	Propagation Delay CET to TC	5.0	1.5	8.0	9.5	1.5	10.5	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	8.0	10.0	1.5	11.0	ns	3−6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	2.5	10.0	13.5	2.0	14.5	ns	3−6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT163 T_A = +25°C, C_L = 50 pF			74ACT163 T_A = −40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120	140	−	105	−	MHz	3−3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	10.0	1.5	11.0	ns	3−6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	11.0	1.5	12.0	ns	3−6
t_{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5	2.0	13.5	ns	3−6
t_{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5	2.0	15.0	ns	3−6
t_{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0	1.5	10.5	ns	3−6
t_{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0	2.0	11.0	ns	3−6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT161 T_A = +25°C C_L = 50 pF		74ACT161 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	7.0	9.5	11.5	ns	3–9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	–3.0	0	0	ns	3–9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	6.0	8.5	9.5	ns	3–9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	–3.5	– 0.5	– 0.5	ns	3–9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	4.0	5.5	6.5	ns	3–9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	–2.0	0	0	ns	3–9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3–6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3–6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0	7.5	ns	3–6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0	0.5	ns	3–9

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT163 T_A = +25°C C_L = 50 pF		74ACT163 T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	10.0	12.0	ns	3–9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0.5	0.5	ns	3–9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0	11.5	ns	3–9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5	−0.5	ns	3–9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5	10.5	ns	3–9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5	0	ns	3–9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3–9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0	0.5	ns	3–9
t_w	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5	ns	3–6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5	3.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

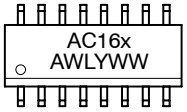
CAPACITANCE

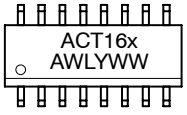
Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

MARKING DIAGRAMS

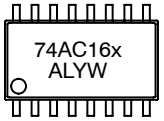
DIP−16

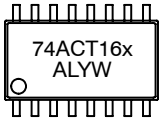
SO−16





EIAJ−16





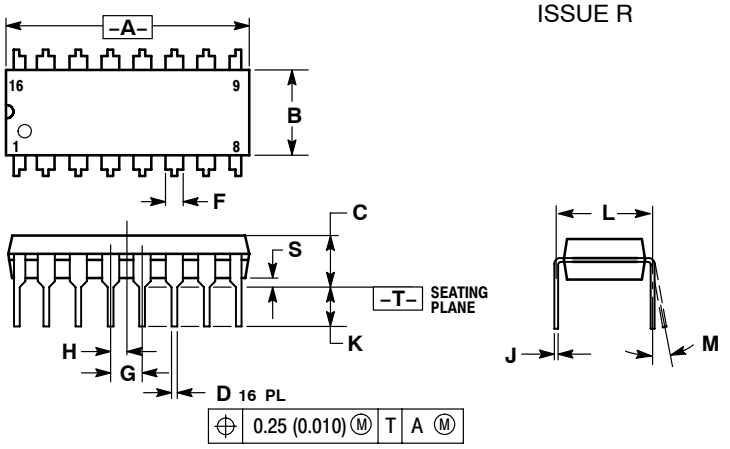
x = 1 or 3
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74AC161N	PDIP−16	25 Units/Rail
MC74ACT161N	PDIP−16	25 Units/Rail
MC74AC161D	SOIC−16	48 Units/Rail
MC74AC161DR2	SOIC−16	2500 Tape & Reel
MC74ACT161D	SOIC−16	48 Units/Rail
MC74ACT161DR2	SOIC−16	2500 Tape & Reel
MC74AC161M	EIAJ−16	50 Units/Rail
MC74ACT161MEL	EIAJ−16	2000 Tape & Reel
MC74AC163N	PDIP−16	25 Units/Rail
MC74ACT163N	PDIP−16	25 Units/Rail
MC74AC163D	SOIC−16	48 Units/Rail
MC74AC163DR2	SOIC−16	2500 Tape & Reel
MC74ACT163D	SOIC−16	48 Units/Rail
MC74ACT163DR2	SOIC−16	2500 Tape & Reel
MC74AC163MEL	EIAJ−16	2000 Tape & Reel
MC74ACT163MEL	EIAJ−16	2000 Tape & Reel

PACKAGE DIMENSIONS

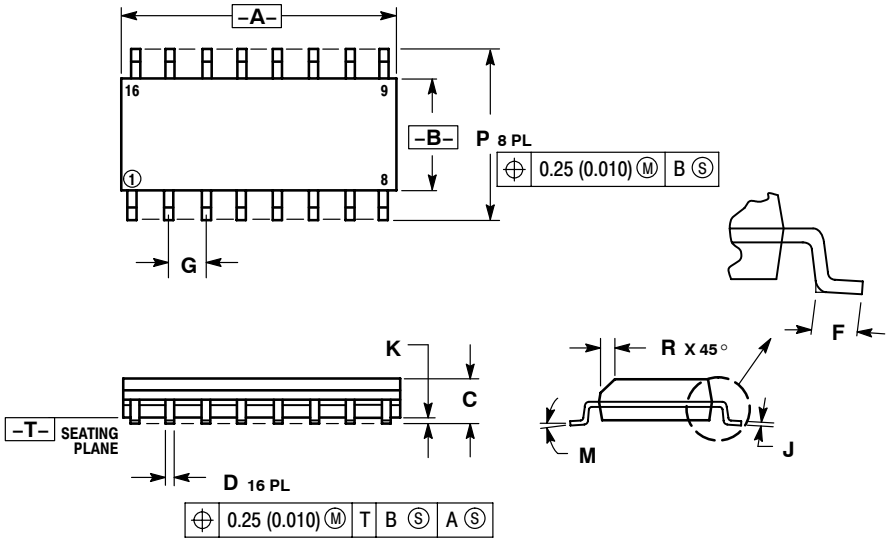
PDIP–16
N SUFFIX
16 PIN PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SO–16
D SUFFIX
16 PIN PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

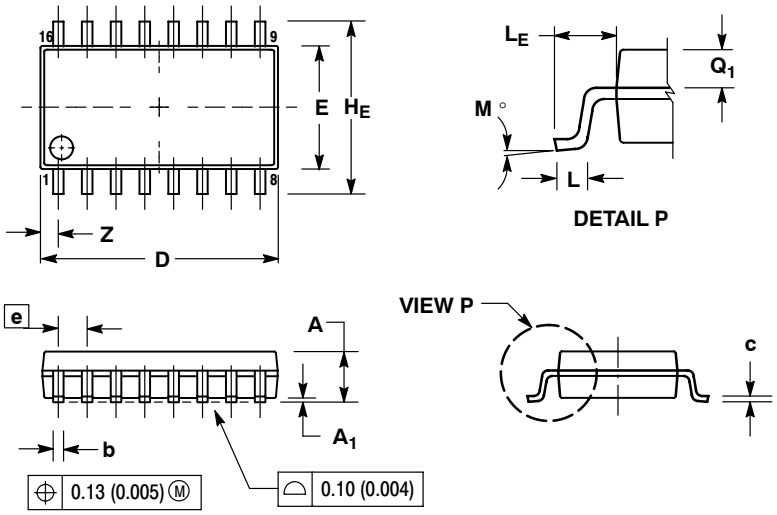


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

EIAJ−16
M SUFFIX
16 PIN PLASTIC EIAJ PACKAGE
CASE966−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А