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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

August 2016

FDMC8030

Dual N-Channel Power Trench® MOSFET

40 V, 12 A, 10 mΩ

Features

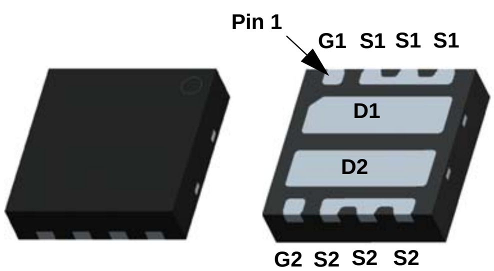
- Max $r_{DS(on)}$ = 10 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 14 mΩ at V_{GS} = 4.5 V, I_D = 10 A
- Max $r_{DS(on)}$ = 28 mΩ at V_{GS} = 3.2 V, I_D = 4 A
- Termination is Lead-free and RoHS Compliant

General Description

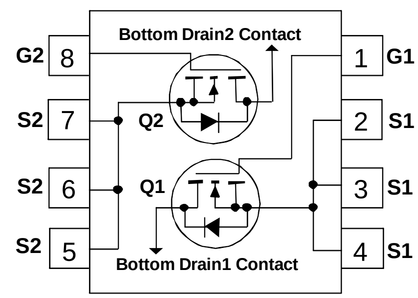
This device includes two 40V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Applications

- Battery Protection
- Load Switching
- Point of Load



Power 33



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage		(Note 4)	±12	V
I_D	Drain Current -Continuous	T_A = 25 °C	(Note 1a)	12	A
	-Pulsed			50	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	21	mJ
P_D	Power Dissipation	T_C = 25 °C		14	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	1.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		9.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	155	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8030	FDMC8030	Power 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	1.0	1.5	2.8	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A		8	10	mΩ
		V_{GS} = 4.5 V, I_D = 10 A		10	14	
		V_{GS} = 3.2 V, I_D = 4 A		19	28	
		V_{GS} = 10 V, I_D = 12 A T_J = 125 °C		13	16	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 12 A		57		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V f = 1MHz		1462	1975	pF
C_{oss}	Output Capacitance			321	430	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF
R_g	Gate Resistance			0.9	2.5	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20 V, I_D = 12 A V_{GS} = 10 V, R_{GEN} = 6 Ω		7	13	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	33	ns
t_f	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 20 V, I_D = 12 A		21	30	nC
	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 20 V, I_D = 12 A		12	17	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 12 A		2.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.5		nC

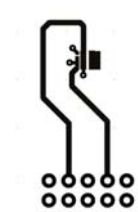
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 12 A (Note 2)		0.83	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 12 A, di/dt = 100 A/μs		25	40	ns
Q_{rr}	Reverse Recovery Charge			9	18	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 65 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 155 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 21 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 12 A, V_{DD} = 36 V, V_{GS} = 10 V. 100% tested at L = 3 mH, I_{AS} = 5 A.
4. As an N-ch device, the negative V_{gs} rating is for low duty cycle pulse occurence only. No continuous rating is implied.

Typical Characteristics T_J = 25°C unless otherwise noted.

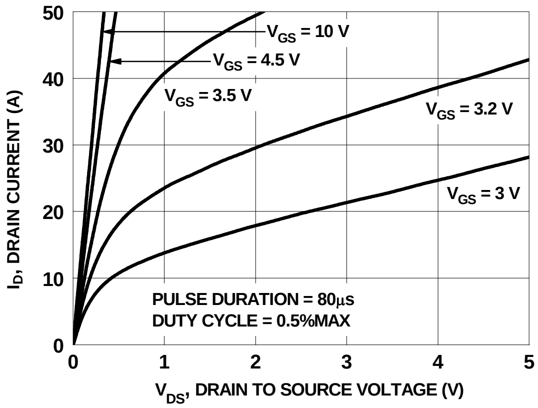


Figure 1. On-Region Characteristics

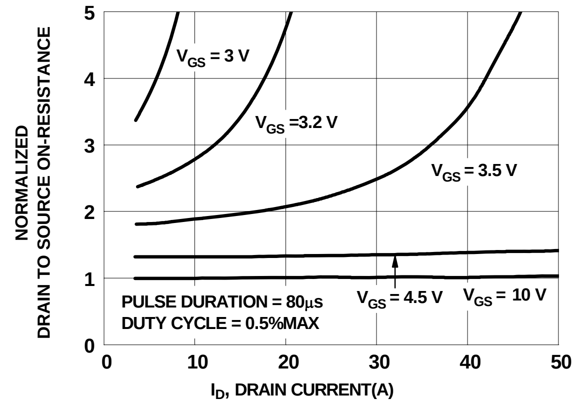


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

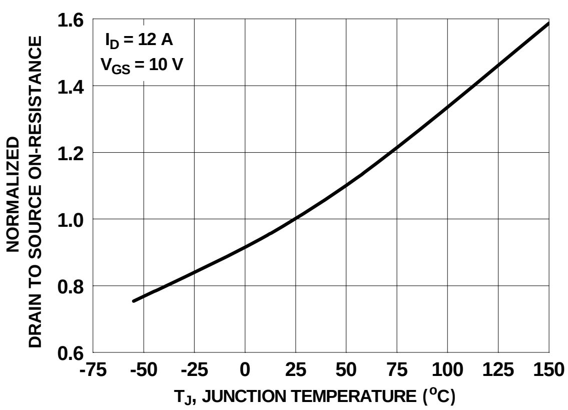


Figure 3. Normalized On-Resistance vs. Junction Temperature

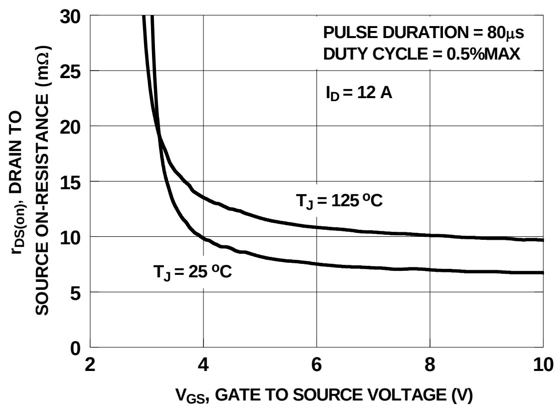


Figure 4. On-Resistance vs. Gate to Source Voltage

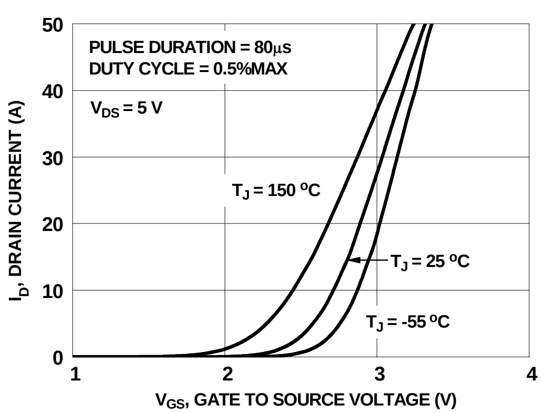


Figure 5. Transfer Characteristics

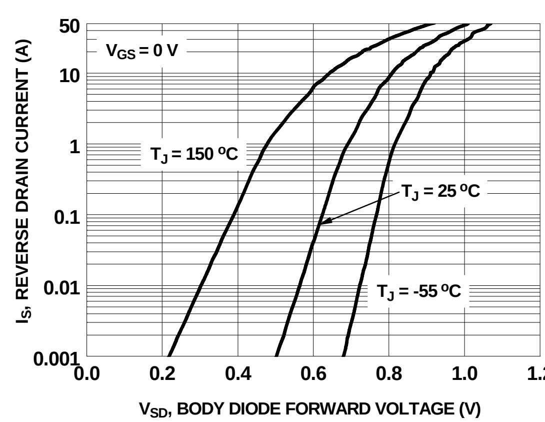


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25°C$ unless otherwise noted.

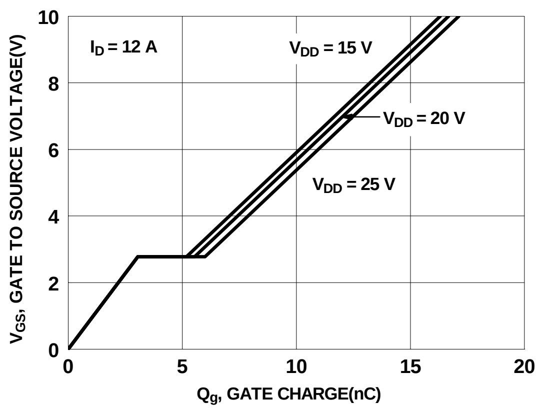


Figure 7. Gate Charge Characteristics

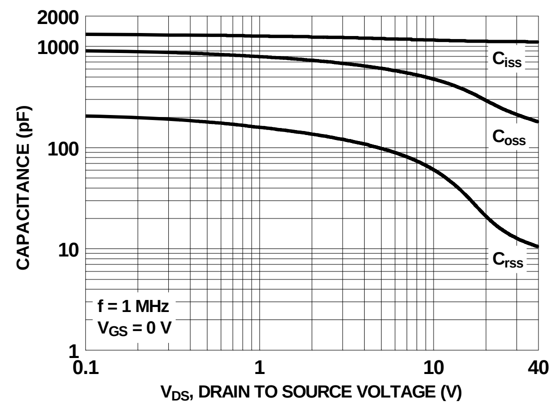


Figure 8. Capacitance vs. Drain to Source Voltage

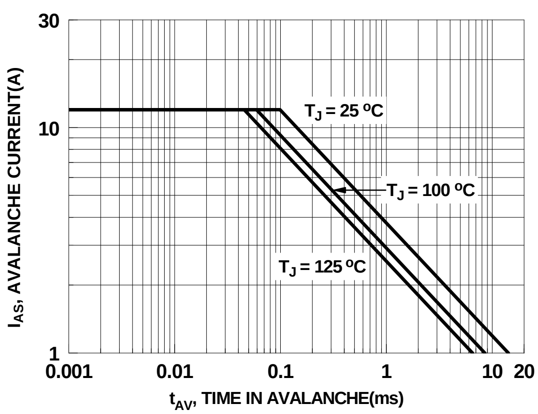


Figure 9. Unclamped Inductive Switching Capability

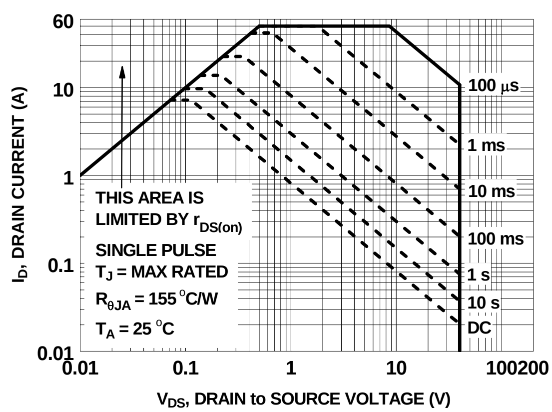


Figure 10. Forward Bias Safe Operating Area

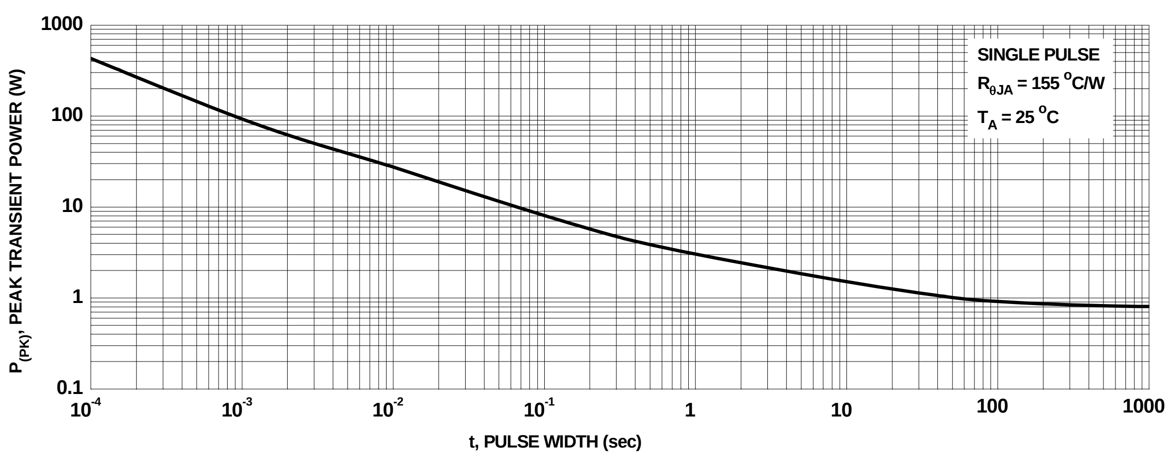


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted.

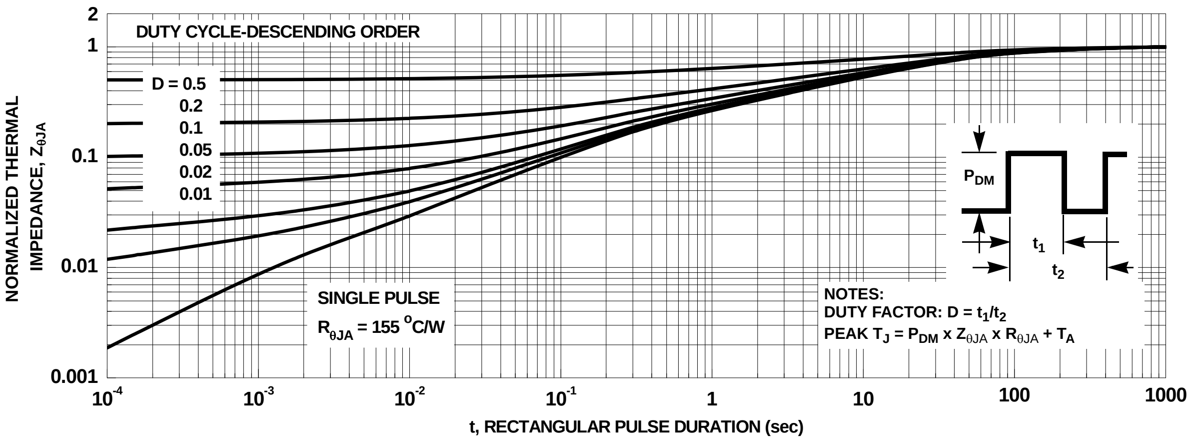
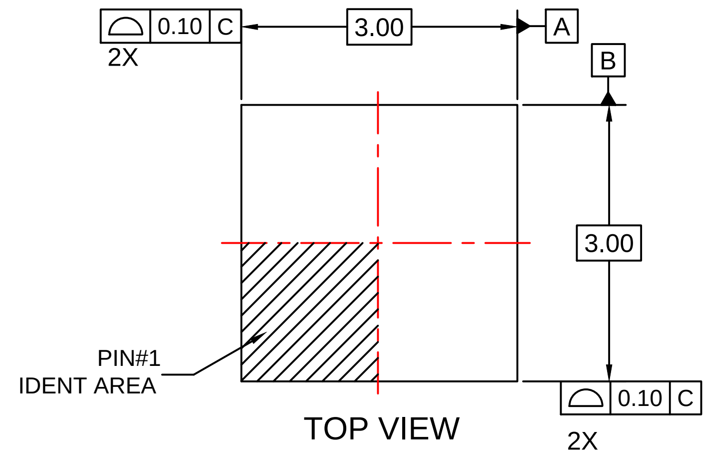
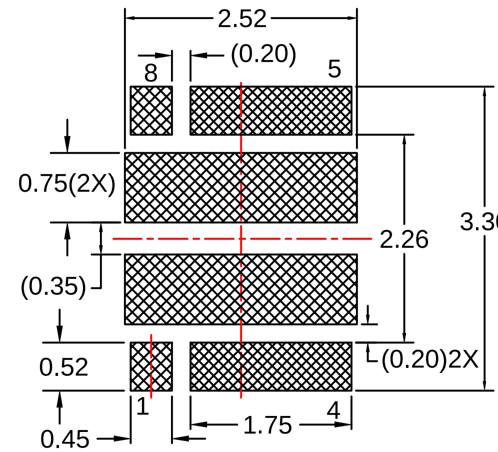


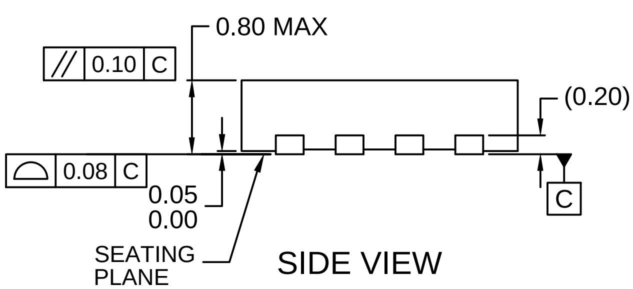
Figure 12. Junction-to-Ambient Transient Thermal Response Curve



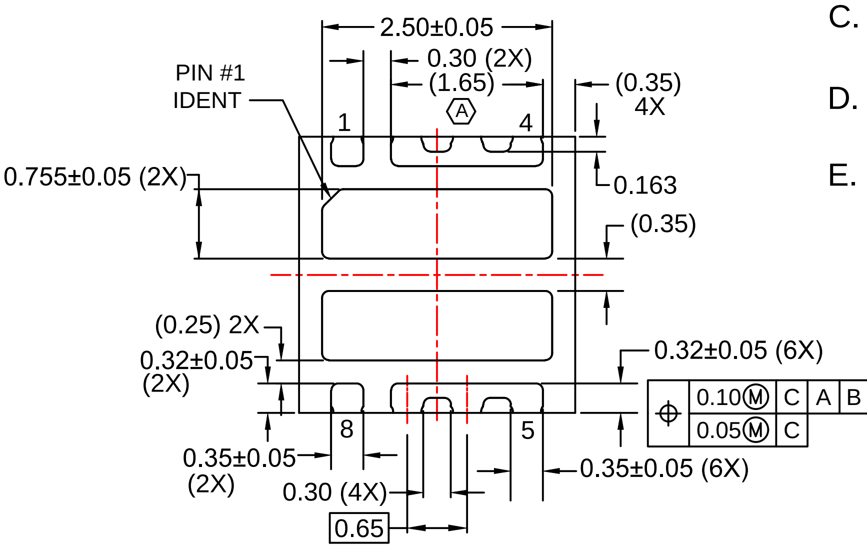
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY

E. DRAWING FILE NAME: MKT-MLP08Xrev2.

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