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August 2016

# FDMC8030

## Dual N-Channel Power Trench<sup>®</sup> MOSFET 40 V, 12 A, 10 mΩ

### Features

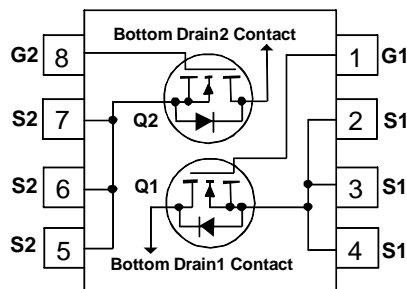
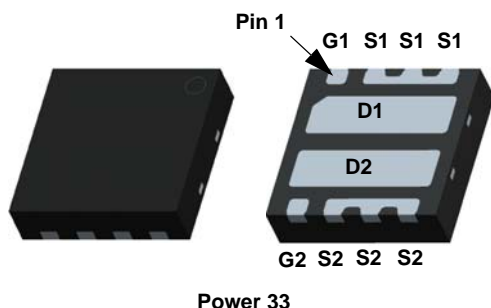
- Max  $r_{DS(on)}$  = 10 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 12\text{ A}$
- Max  $r_{DS(on)}$  = 14 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 10\text{ A}$
- Max  $r_{DS(on)}$  = 28 mΩ at  $V_{GS} = 3.2\text{ V}$ ,  $I_D = 4\text{ A}$
- Termination is Lead-free and RoHS Compliant

### General Description

This device includes two 40V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

### Applications

- Battery Protection
- Load Switching
- Point of Load



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 12$	V
$I_D$	Drain Current -Continuous $T_A = 25\text{ °C}$ (Note 1a)	12	A
	-Pulsed	50	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	21	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	14	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	1.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	9.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	65	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	155	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8030	FDMC8030	Power 33	13 "	12 mm	3000 units

# Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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## Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		19		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}$ , $V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 12\ \text{V}$ , $V_{DS} = 0\ \text{V}$			100	nA

## On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	1.0	1.5	2.8	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 12\ \text{A}$		8	10	m $\Omega$
		$V_{GS} = 4.5\ \text{V}$ , $I_D = 10\ \text{A}$		10	14	
		$V_{GS} = 3.2\ \text{V}$ , $I_D = 4\ \text{A}$		19	28	
		$V_{GS} = 10\ \text{V}$ , $I_D = 12\ \text{A}$ $T_J = 125^\circ\text{C}$		13	16	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\ \text{V}$ , $I_D = 12\ \text{A}$		57		S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\ \text{V}$ , $V_{GS} = 0\ \text{V}$ $f = 1\ \text{MHz}$		1462	1975	pF
$C_{oss}$	Output Capacitance			321	430	pF
$C_{rss}$	Reverse Transfer Capacitance			20	30	pF
$R_g$	Gate Resistance			0.9	2.5	$\Omega$

## Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\ \text{V}$ , $I_D = 12\ \text{A}$ $V_{GS} = 10\ \text{V}$ , $R_{GEN} = 6\ \Omega$		7	13	ns
$t_r$	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	33	ns
$t_f$	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 20\ \text{V}$ $I_D = 12\ \text{A}$	21	30	nC
	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$		12	17	nC
$Q_{gs}$	Gate to Source Charge			2.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.5		nC

## Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = 12\ \text{A}$ (Note 2)		0.83	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 12\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$		25	40	ns
$Q_{rr}$	Reverse Recovery Charge			9	18	nC

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $65^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $155^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

- $E_{AS}$  of 21 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.3\ \text{mH}$ ,  $I_{AS} = 12\ \text{A}$ ,  $V_{DD} = 36\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ . 100% tested at  $L = 3\ \text{mH}$ ,  $I_{AS} = 5\ \text{A}$ .

- As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

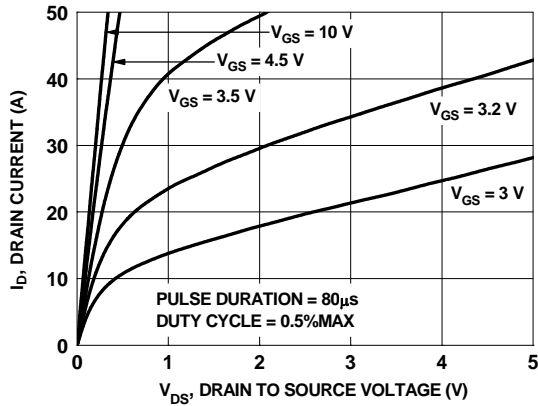


Figure 1. On-Region Characteristics

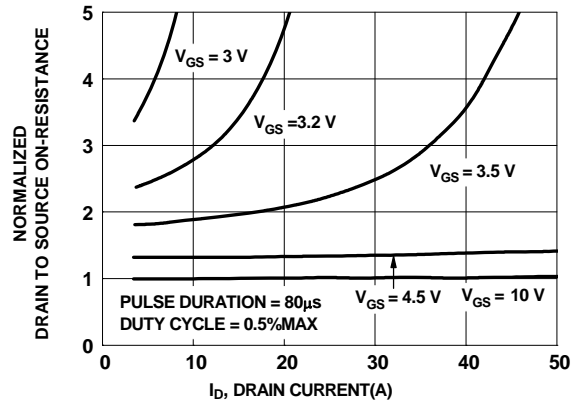


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

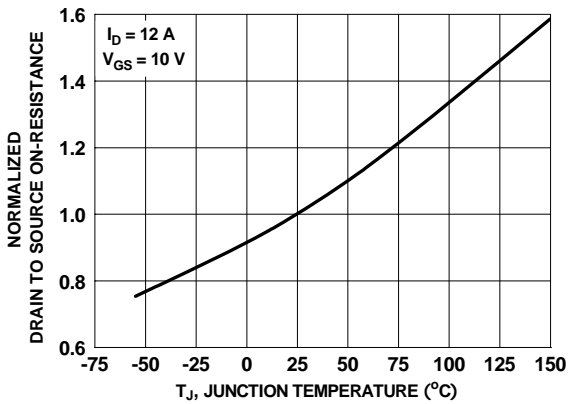


Figure 3. Normalized On-Resistance vs. Junction Temperature

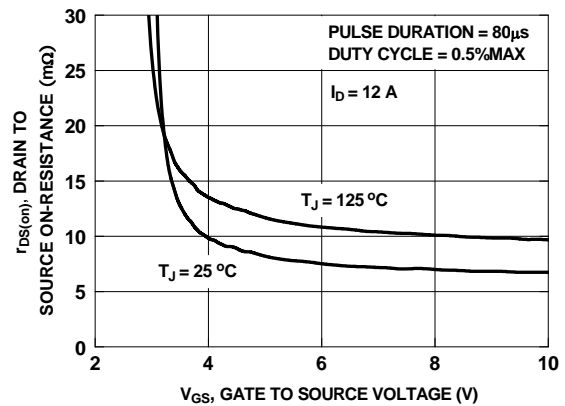


Figure 4. On-Resistance vs. Gate to Source Voltage

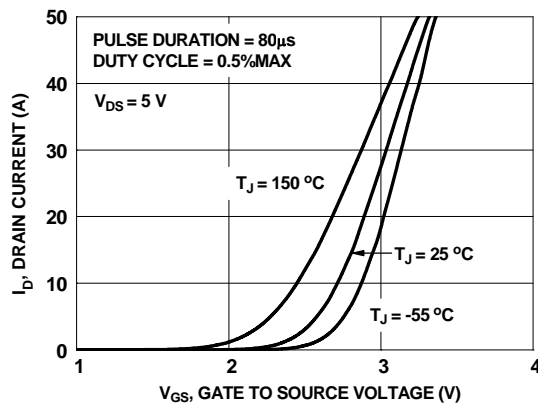


Figure 5. Transfer Characteristics

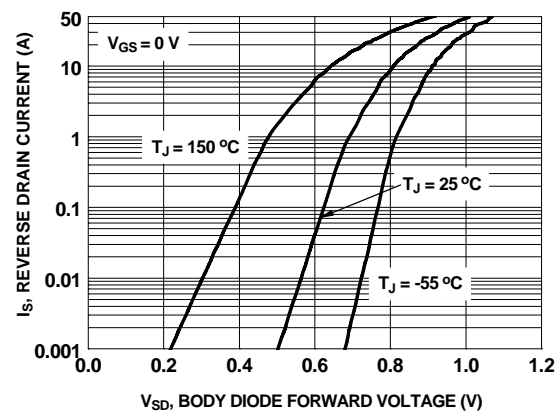


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

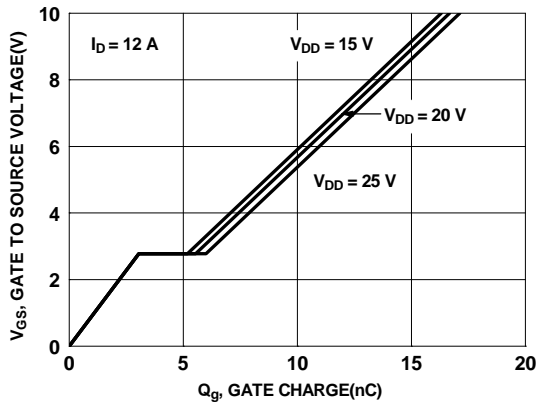


Figure 7. Gate Charge Characteristics

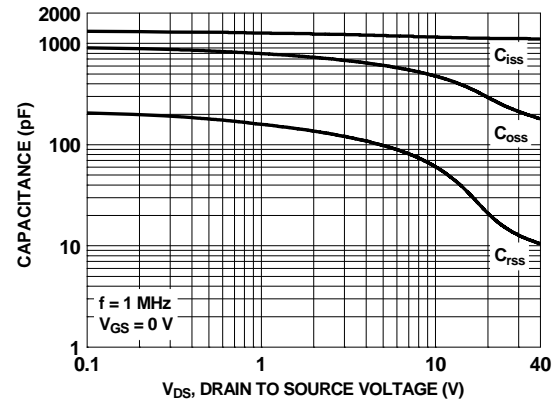


Figure 8. Capacitance vs. Drain to Source Voltage

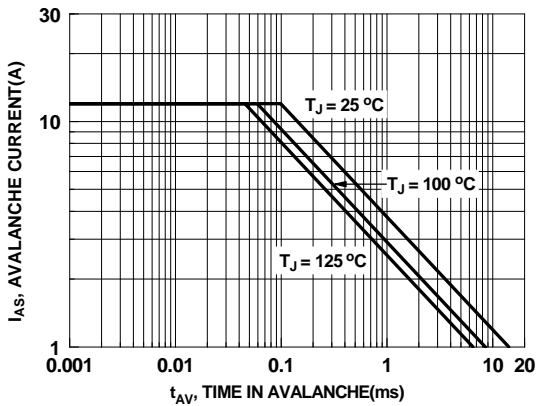


Figure 9. Unclamped Inductive Switching Capability

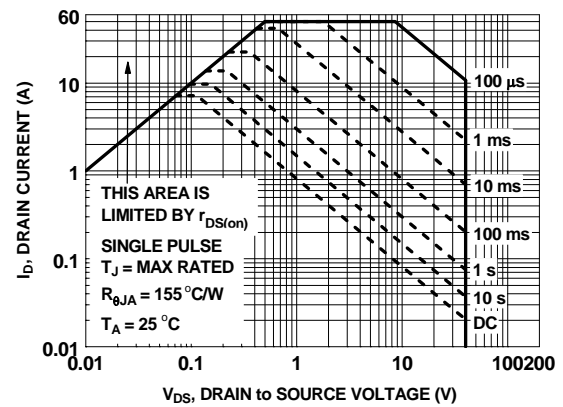


Figure 10. Forward Bias Safe Operating Area

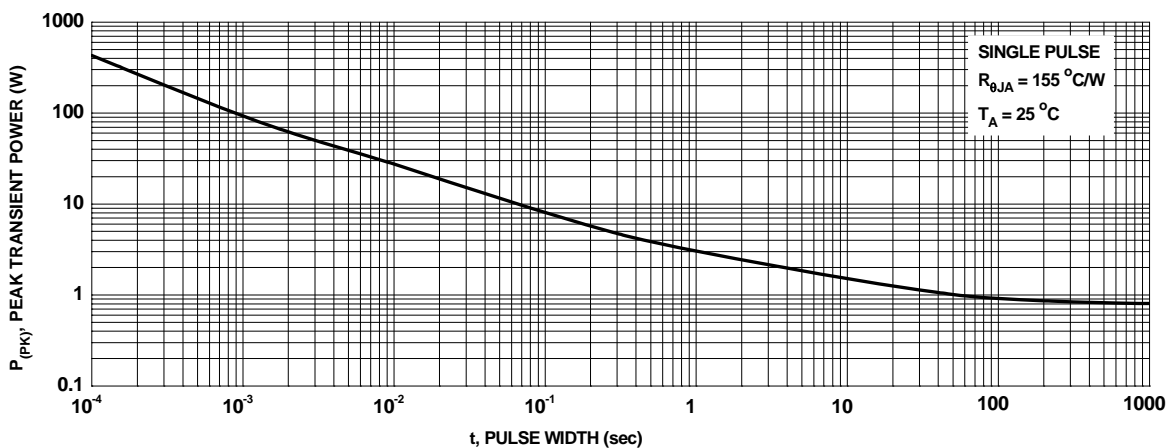
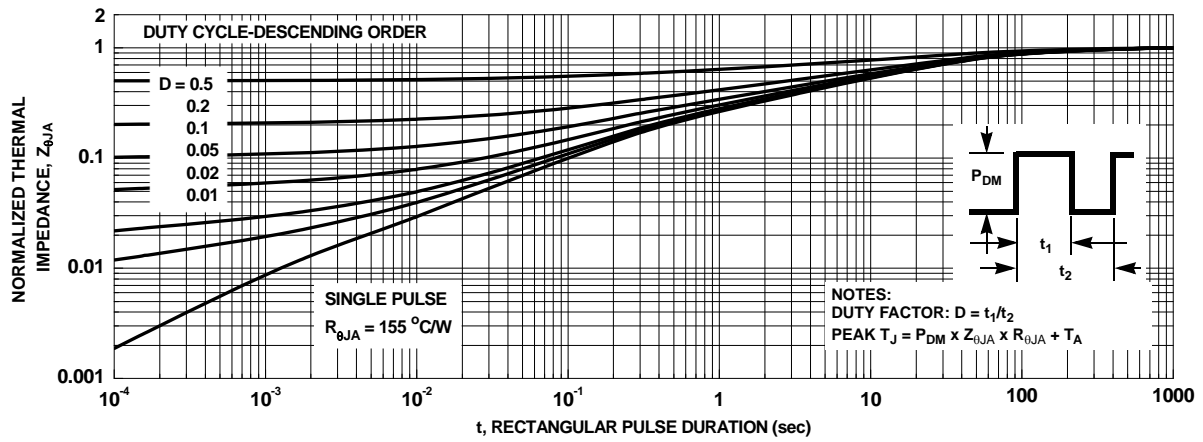


Figure 11. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.





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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

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Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А