Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

September 2015

FDMS8350LET40

N-Channel PowerTrench® MOSFET

40 V, 300 A, 0.85 mΩ

Features

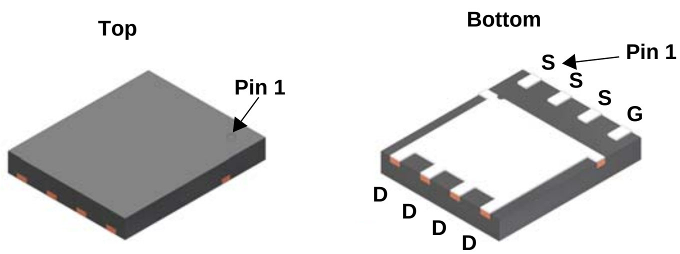
- Max $r_{DS(on)}$ = 0.85 mΩ at V_{GS} = 10 V, I_D = 47 A
- Max $r_{DS(on)}$ = 1.2 mΩ at V_{GS} = 4.5 V, I_D = 38 A
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

General Description

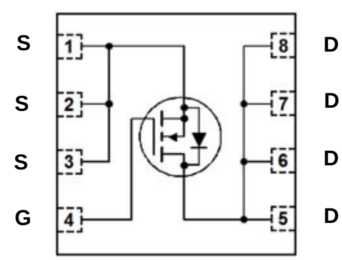
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch



Power 56



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C	(Note 5)	300	A
	-Continuous	T_C = 100 °C	(Note 5)	212	
	-Continuous	T_A = 25 °C	(Note 1a)	49	
	-Pulsed		(Note 4)	1464	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	1176	mJ
P_D	Power Dissipation	T_C = 25 °C		125	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	3.33	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to + 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	45	

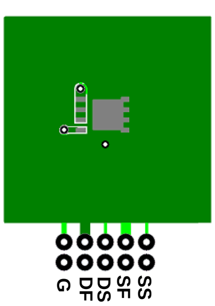
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8350L	FDMS8350LET40	Power 56	13 ”	12 mm	3000 units

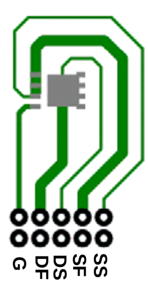
Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		17		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 47 A		0.68	0.85	mΩ
		V_{GS} = 4.5 V, I_D = 38 A		0.96	1.2	
		V_{GS} = 10 V, I_D = 47 A, T_J = 150 °C		1.1	1.4	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 47 A		247		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		11850	16590	pF
C_{oss}	Output Capacitance			3430	4805	pF
C_{rss}	Reverse Transfer Capacitance			69	100	pF
R_g	Gate Resistance		0.1	1.2	2.4	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20 V, I_D = 47 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		32	51	ns
t_r	Rise Time			19	34	ns
$t_{d(off)}$	Turn-Off Delay Time			74	118	ns
t_f	Fall Time			15	27	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 20 V, I_D = 47 A		156	219	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 20 V, I_D = 47 A		73	102	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 47 A		33		nC
Q_{gd}	Gate to Drain “Miller” Charge			16		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 47 A (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 47 A, di/dt = 100 A/μs		81	129	ns
Q_{rr}	Reverse Recovery Charge			82	131	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 45 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 115 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 1176 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 28 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 87 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25°C unless otherwise noted.

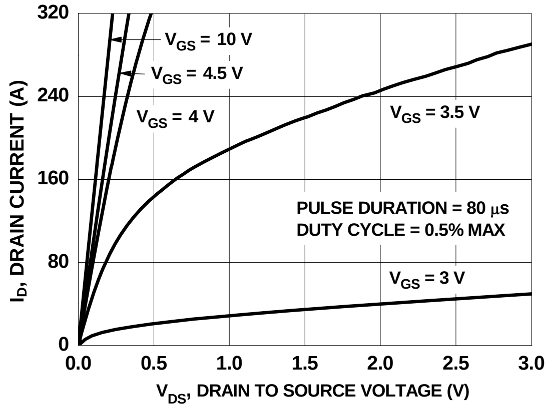


Figure 1. On Region Characteristics

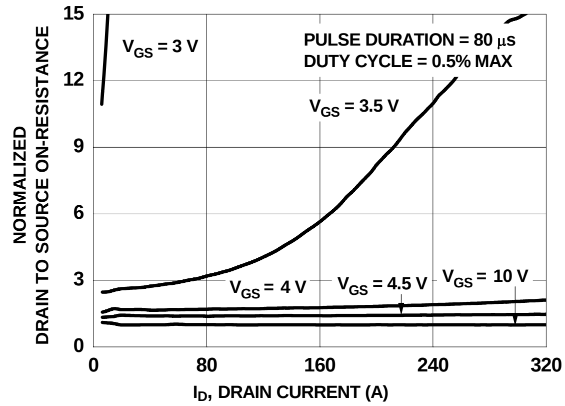


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

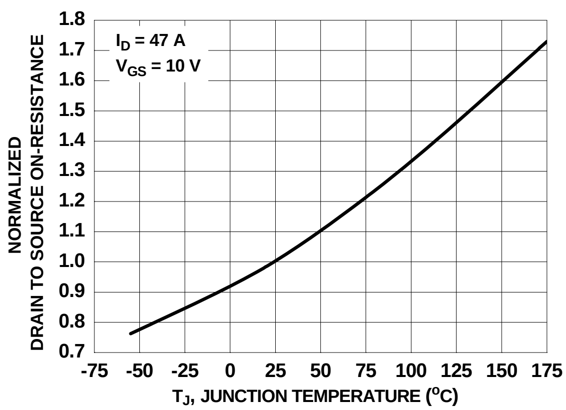


Figure 3. Normalized On Resistance vs. Junction Temperature

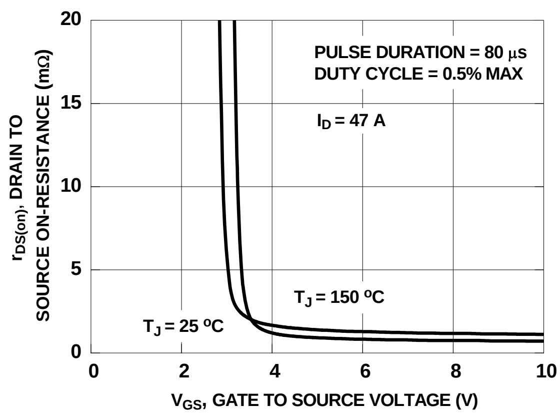


Figure 4. On-Resistance vs. Gate to Source Voltage

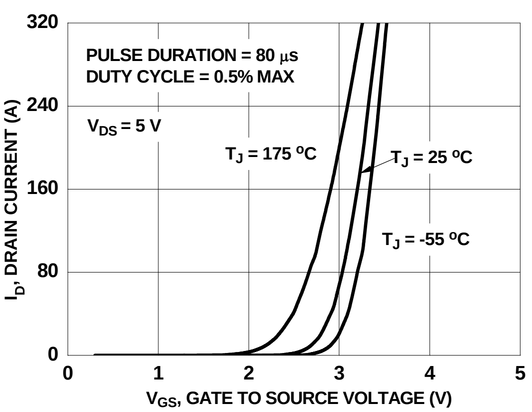


Figure 5. Transfer Characteristics

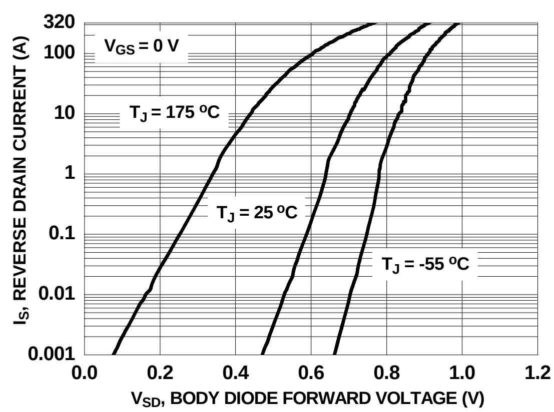


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25°C unless otherwise noted.

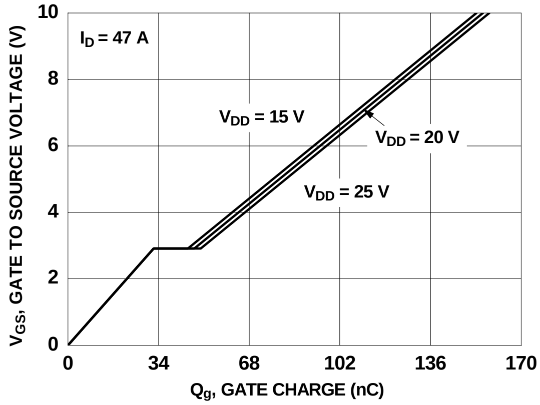


Figure 7. Gate Charge Characteristics

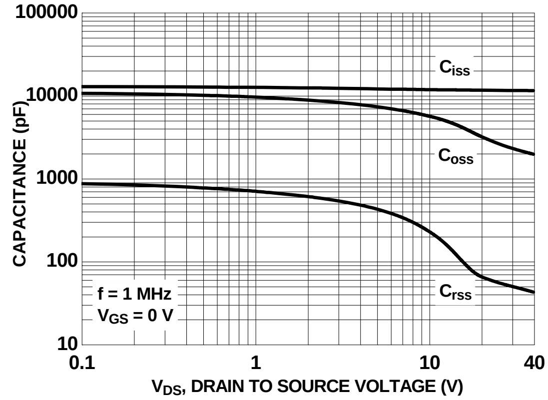


Figure 8. Capacitance vs. Drain to Source Voltage

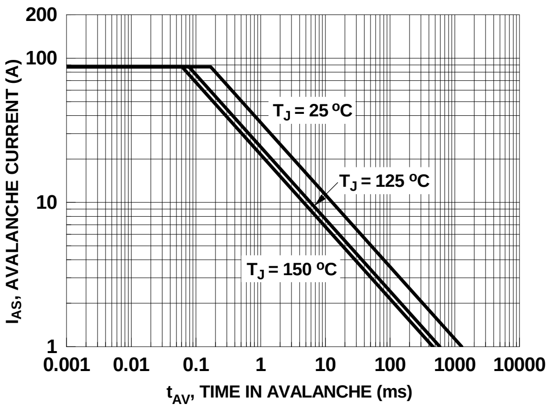


Figure 9. Unclamped Inductive Switching Capability

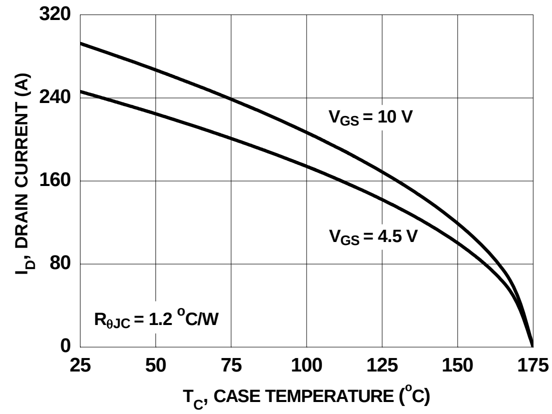


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

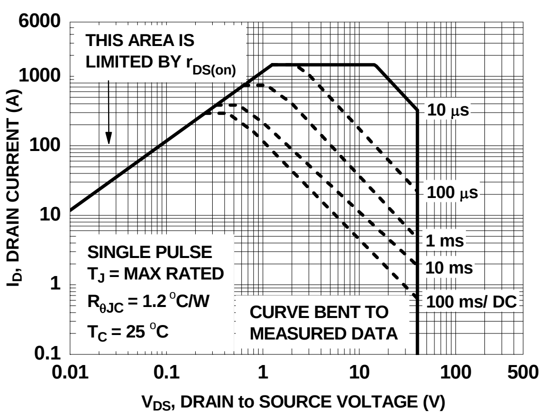


Figure 11. Forward Bias Safe Operating Area

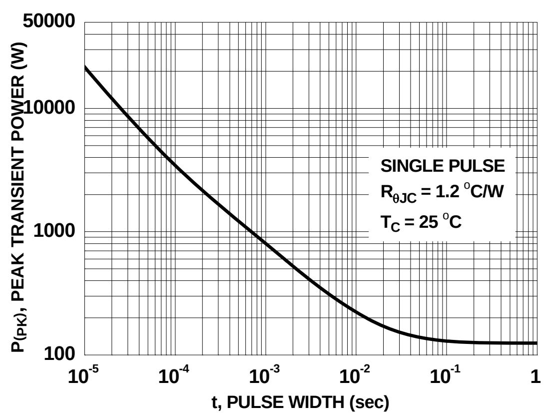


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted.

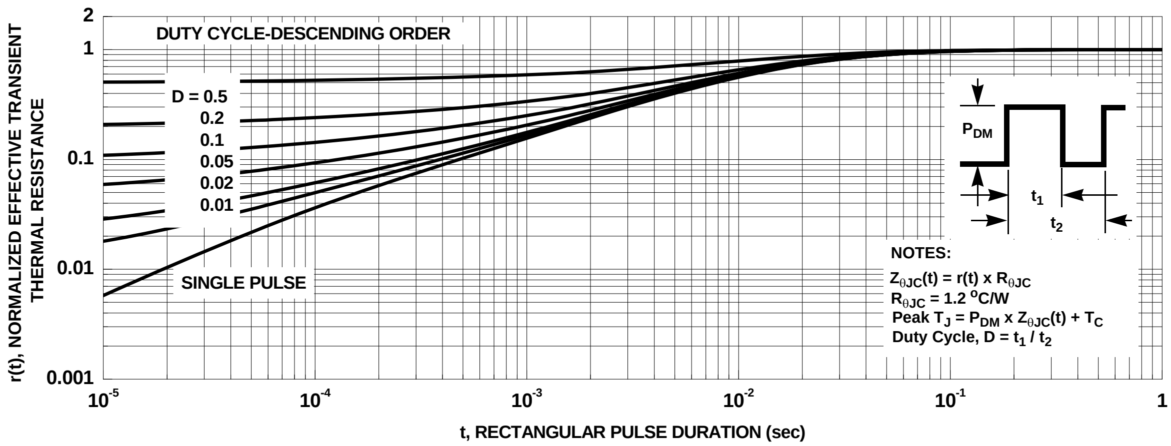
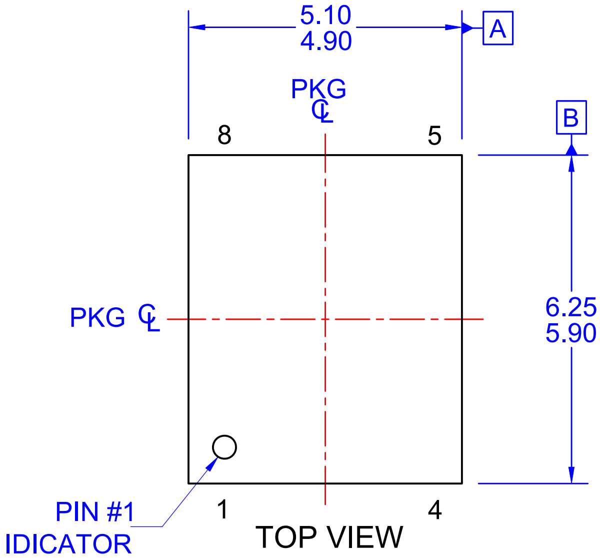
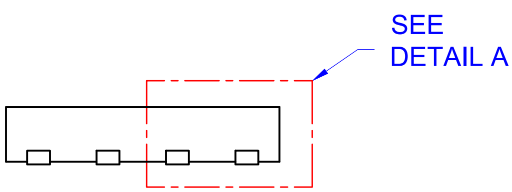


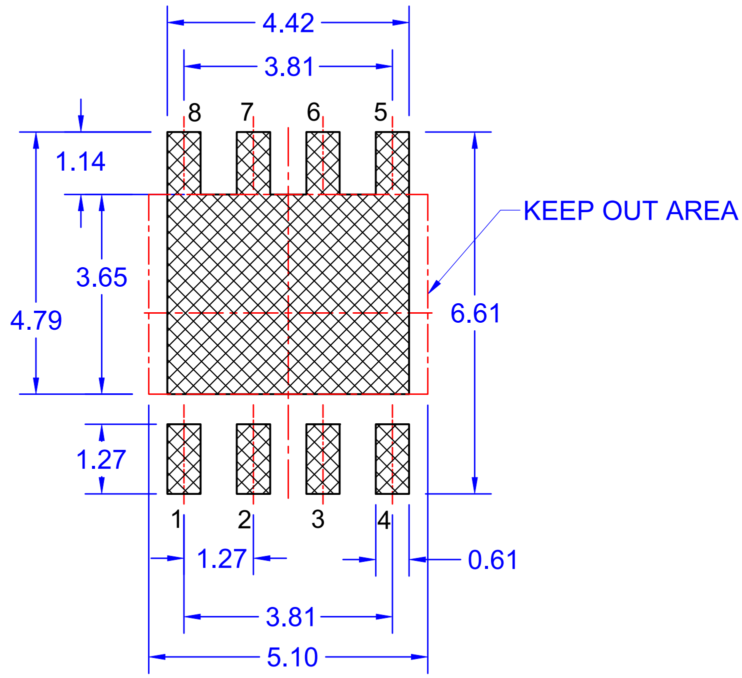
Figure 13. Junction-to-Case Transient Thermal Response Curve



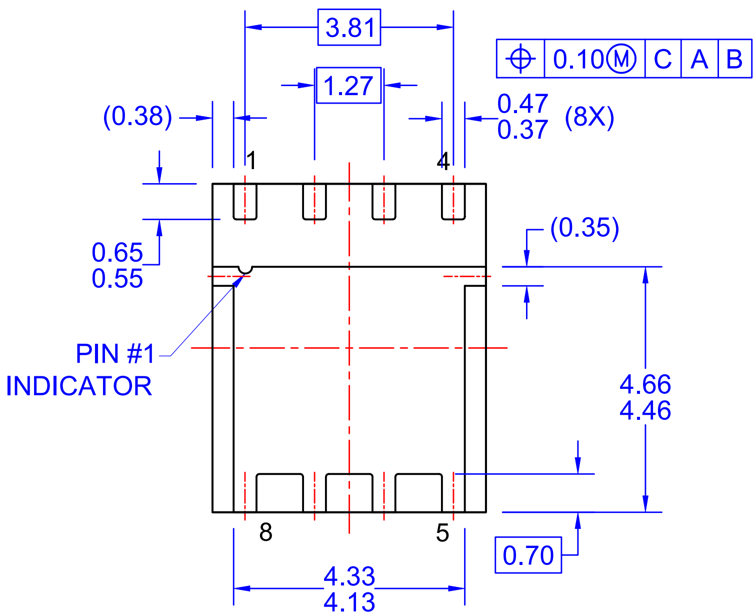
TOP VIEW



SIDE VIEW



LAND PATTERN
RECOMMENDATION

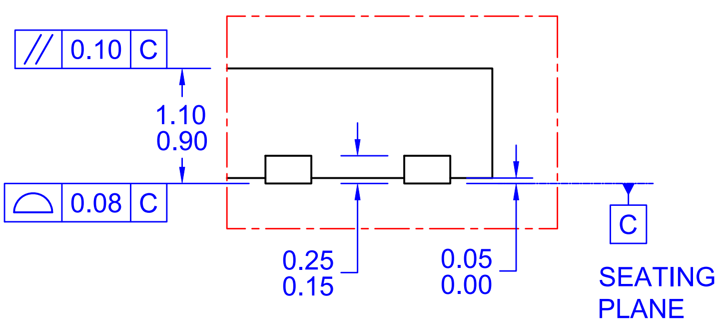


BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
F) DRAWING FILE NAME: PQFN08JREV3.

FAIRCHILD™



DETAIL A

SCALE: 2:1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative