

**FEATURES****Ultralow on-resistance:**0.5  $\Omega$  typical0.8  $\Omega$  maximum at 5 V supply**Excellent audio performance, ultralow distortion:**0.13  $\Omega$  typical0.24  $\Omega$  maximum  $R_{ON}$  flatness**High current carrying capability:**

400 mA continuous current

600 mA peak current at 5 V

**Automotive temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$** **Rail-to-rail operation****Typical power consumption ( $<0.01 \mu\text{W}$ )****Pin-compatible upgrade for the ADG749 and ADG779****APPLICATIONS**

Cellular phones

PDAs

Battery-powered systems

Audio and video signal routing

Modems

PCMCIA cards

Hard drives

Relay replacement

**GENERAL DESCRIPTION**

The ADG849 is a monolithic, CMOS SPDT (single pole, double throw) switch that operates with a supply range of 1.8 V to 5.5 V. It is designed to offer ultralow on-resistance values of typically 0.5  $\Omega$ . This design makes the ADG849 an ideal solution for applications that require minimal distortion through the switch. The ADG849 also has the capability of carrying large amounts of current, typically 600 mA at 5 V operation.

Each switch of the ADG849 conducts equally well in both directions when on. The device exhibits break-before-make switching action, thus preventing momentary shorting when switching channels.

The ADG849 is available in a tiny, 6-lead SC70 package, making it the ideal candidate for space-constrained applications.

**FUNCTIONAL BLOCK DIAGRAM**

Figure 1.

**PRODUCT HIGHLIGHTS**

1. Very low on-resistance, 0.5  $\Omega$  typical.
2. Tiny, 6-lead SC70 package.
3. Low power dissipation. The CMOS construction ensures low power dissipation.
4. High current carrying capability.
5. Low THD + noise (0.01% typ).

**Rev. 0**

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## REVISION HISTORY

7/04—Revision 0: Initial Version

## SPECIFICATIONS

Table 1.  $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ <sup>1</sup>

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On-Resistance ( $R_{ON}$ )	0.5			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -100\text{ mA}$
	0.6	0.7	0.8	$\Omega$ max	See Figure 15
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.05			$\Omega$ typ	$V_S = 0.85\text{ V}$ , $I_{DS} = -100\text{ mA}$
	0.095	0.11	0.125	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.13			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -100\text{ mA}$
	0.18	0.22	0.24	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.01$			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ , see Figure 16
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.04$			nA typ	$V_S = V_D = 1\text{ V}$ , or $V_S = V_D = 4.5\text{ V}$ , see Figure 17
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current					
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	11			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	15	17	18	ns max	$V_S = 3\text{ V}$ , see Figure 18
$t_{OFF}$	9			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	13	14	15	ns max	$V_S = 3\text{ V}$ , see Figure 18
Break-Before-Make Time Delay, $t_{BBM}$	5			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3\text{ V}$ , see Figure 19
			1	ns min	
Charge Injection	50			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 20
Off Isolation	-64			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ see Figure 21
Channel-to-Channel Crosstalk	-64			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ , see Figure 22
Bandwidth: -3 dB	38			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 23
Insertion Loss	0.04			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 23
THD + N	0.01			%	$R_L = 32\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 2\text{ V p-p}$
$C_S$ (Off)	52			pF typ	
$C_D$ , $C_S$ (On)	145			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ , Digital Inputs = 0 V or 5.5 V
			1.0	$\mu\text{A}$ max	

<sup>1</sup>The temperature range for the Y version is  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

# ADG849

**Table 2.**  $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ <sup>1</sup>

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On-Resistance ( $R_{ON}$ )	0.72			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -100\text{ mA}$
	1.1	1.1	1.2	$\Omega$ max	See Figure 15
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.05			$\Omega$ typ	$V_S = 1.5\text{ V}$ , $I_{DS} = -100\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.095	0.11	0.125	$\Omega$ max	
	0.3			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -100\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 3.6\text{ V}$
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.01$			nA typ	$V_S = 3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3\text{ V}$ , see Figure 16
					$V_S = V_D = 1\text{ V}$ , or $V_S = V_D = 3\text{ V}$ ; see Figure 17
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	$V_{DD} = 3\text{ V to }3.6\text{ V}$
			0.7	V max	$V_{DD} = 2.7\text{ V}$
Input Current					
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	16			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	22	24	26	ns max	$V_S = 1.5\text{ V}$ , see Figure 18
$t_{OFF}$	13			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	18	20	22	ns max	$V_S = 1.5\text{ V}$ , see Figure 18
Break-Before-Make Time Delay, $t_{BBM}$	7			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 1.5\text{ V}$ , see Figure 19
			1	ns min	
Charge Injection	30			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 20
Off Isolation	-64			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ , see Figure 21
Channel-to-Channel Crosstalk	-64			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ , see Figure 22
Bandwidth: -3 dB	38			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 23
Insertion Loss	0.04			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 23
THD + N	0.02			%	$R_L = 32\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 1\text{ V p-p}$
$C_S$ (Off)	55			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	147			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 3.6\text{ V}$
			1.0	$\mu\text{A}$ max	Digital Inputs = 0 V or 3.6 V

<sup>1</sup>The temperature range for the Y version is  $-40^\circ\text{C to }+125^\circ\text{C}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

Table 3.  $T_A = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
Analog Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	400 mA
Operating Temperature Range	
Extended	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
SC70 Package	
$\theta_{JA}$ Thermal Impedance	332°C/W
$\theta_{JC}$ Thermal Impedance	120°C/W
Reflow Soldering	
Peak Temperature	260(0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

<sup>1</sup> Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 4. Truth Table

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

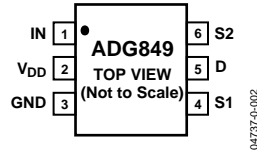


Figure 2. Pin Configuration

Table 5. Terminology

Mnemonic	Function
V <sub>DD</sub>	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
I <sub>DD</sub>	Positive Supply Current.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R <sub>ON</sub>	Ohmic Resistance between D and S.
ΔR <sub>ON</sub>	On-Resistance Match Between any Two Channels i.e., R <sub>ON</sub> Maximum to R <sub>ON</sub> Minimum.
R <sub>FLAT(ON)</sub>	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I <sub>S</sub> (Off)	Source Leakage Current with the Switch Off.
I <sub>D</sub> , I <sub>S</sub> (On)	Channel Leakage Current with the Switch On.
V <sub>D</sub> (V <sub>S</sub> )	Analog Voltage on Terminals D, S.
V <sub>INL</sub>	Maximum Input Voltage for Logic 0.
V <sub>INH</sub>	Minimum Input Voltage for Logic 1.
I <sub>INL</sub> (I <sub>INH</sub> )	Input Current of the Digital Input.
C <sub>S</sub> (Off)	Off Switch Source Capacitance. Measured with reference to ground.
C <sub>D</sub> , C <sub>S</sub> (On)	On Switch Capacitance. Measured with reference to ground.
t <sub>ON</sub>	Delay time between the 50% and 90% points of the digital input and switch on condition.
t <sub>OFF</sub>	Delay time between the 50% and 90% points of the digital input and switch off condition.
t <sub>BBM</sub>	On or off time measured between the 80% points of both switches when switching from one to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an off switch.
Bandwidth	The frequency at which the output is attenuated by 3 dB.
On-Response	The frequency response of the on switch.
Insertion Loss	The loss due to the on-resistance of the switch.
THD + N	The ratio of harmonic amplitudes plus the noise of a signal to the fundamental.

# TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. On-Resistance vs.  $V_D/V_S$ ,  $V_{DD} = 5 V \pm 10\%$

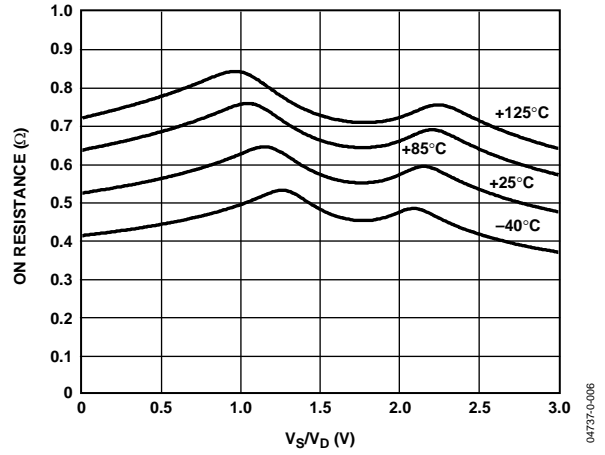


Figure 6. On-Resistance vs. Temperature,  $V_{DD} = 3 V$



Figure 4. On-Resistance vs.  $V_D/V_S$ ,  $V_{DD} = 2.5 V$  to  $3.6 V$

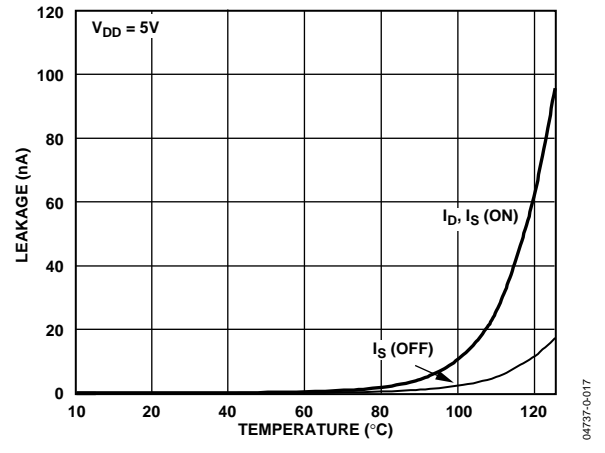


Figure 7. Leakage Currents vs. Temperature,  $V_{DD} = 5 V$



Figure 5. On-Resistance vs. Temperature,  $V_{DD} = 5 V$

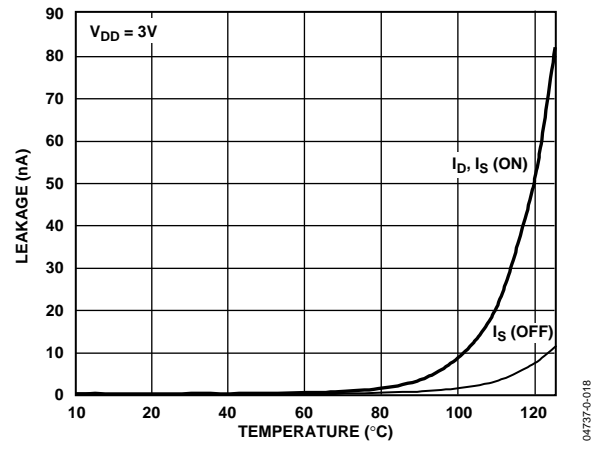


Figure 8. Leakage Currents vs. Temperature,  $V_{DD} = 3 V$

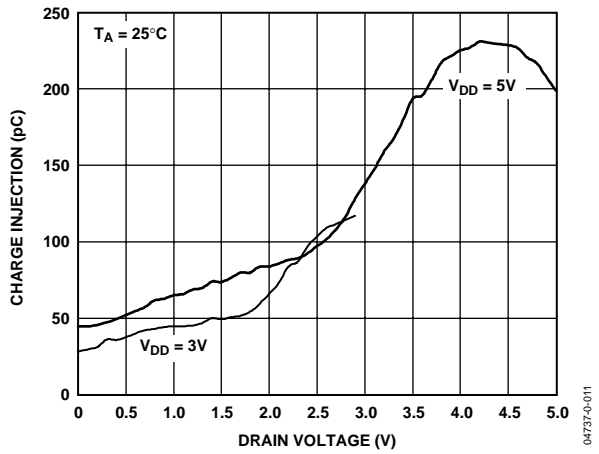


Figure 9. Charge Injection

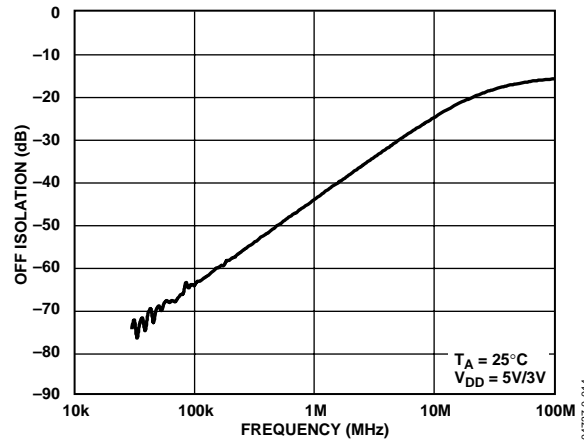


Figure 12. Off Isolation vs. Frequency

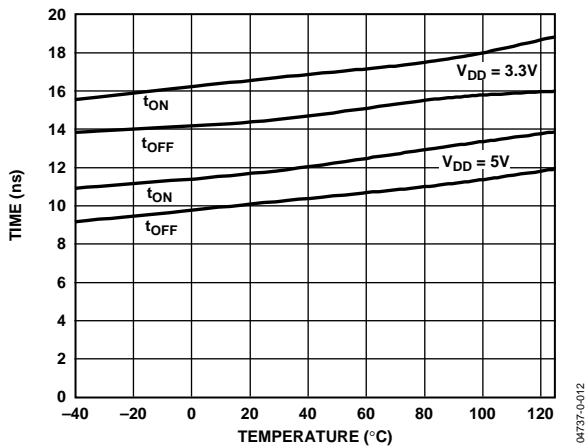


Figure 10.  $t_{ON}/t_{OFF}$  vs. Temperature

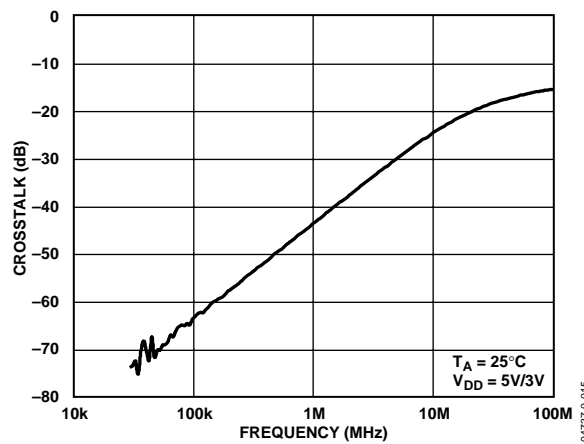


Figure 13. Crosstalk vs. Frequency

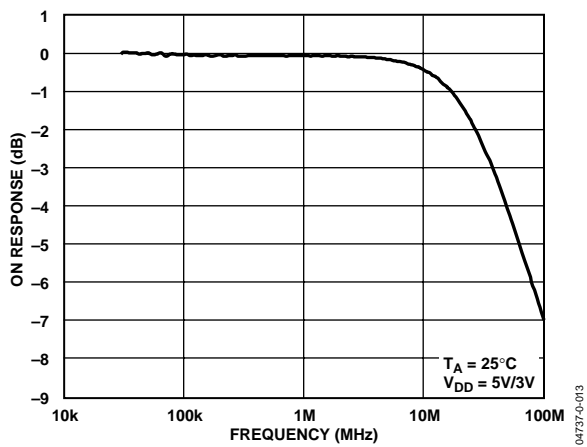


Figure 11. Bandwidth

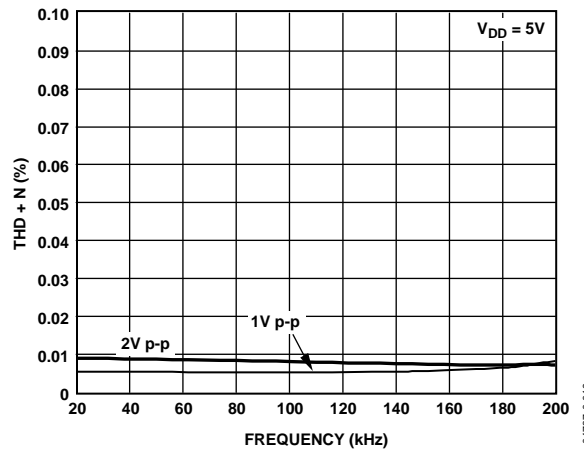


Figure 14. Total Harmonic Distortion + Noise



TEST CIRCUITS

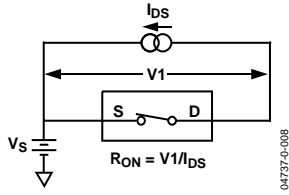


Figure 15. On-Resistance



Figure 16. Off-Leakage



Figure 17. On-Leakage

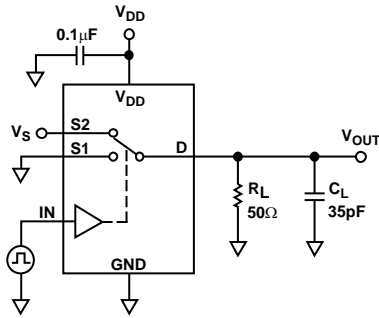


Figure 18. Switching Times,  $t_{ON}$ ,  $t_{OFF}$

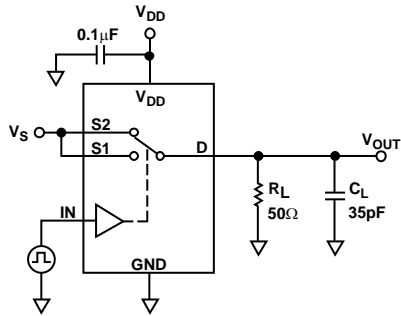


Figure 19. Break-Before-Make Time Delay,  $t_{BBM}$

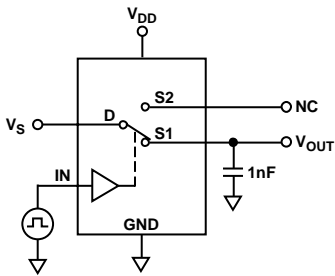


Figure 20. Charge Injection



Figure 21. Off Isolation



Figure 22. Channel-to-Channel Crosstalk

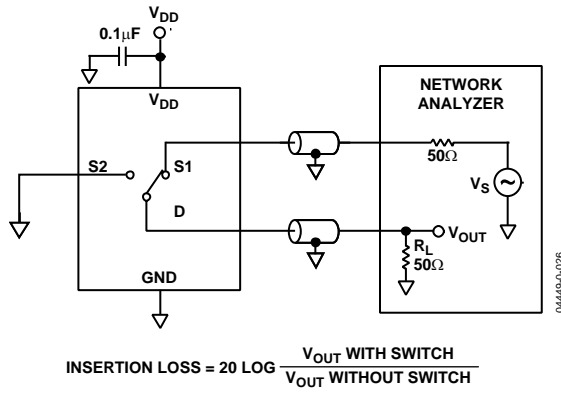
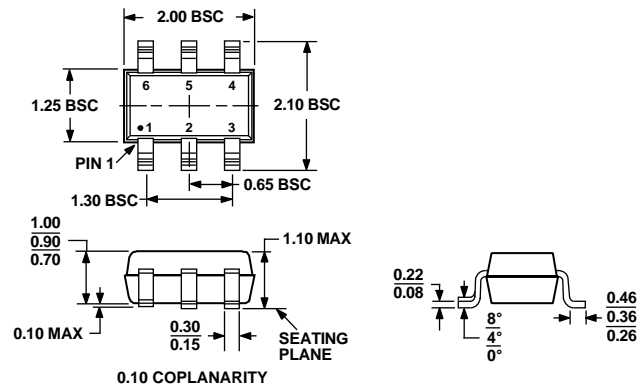


Figure 23. Bandwidth

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203AB

Figure 24. 6-Lead SC70 Package  
[KS-6]  
Dimensions shown in Millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding <sup>1</sup>
ADG849YKSZ-500RL <sup>2</sup>	-40°C to +125°C	SC70 (Plastic Surface Mount)	KS-6	SNA
ADG849YKSZ-REEL <sup>2</sup>	-40°C to +125°C	SC70 (Plastic Surface Mount)	KS-6	SNA
ADG849YKSZ-REEL7 <sup>2</sup>	-40°C to +125°C	SC70 (Plastic Surface Mount)	KS-6	SNA

<sup>1</sup> Branding on all packages is limited to three characters due to space constraints.  
<sup>2</sup> Z = Pb-free part.

**ADG849**

**NOTES**

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- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
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- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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