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March 2015

FDD6530A

FDD6530A

20V N-Channel PowerTrench[®] MOSFET

General Description

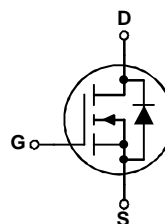
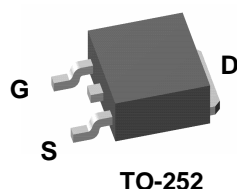
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

- DC/DC converter
- Motor drives

Features

- 21 A, 20 V $R_{DS(ON)} = 32 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 47 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Low gate charge (6.5 nC typical)
- Fast switching
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 8	V
I_D	Drain Current – Continuous (Note 3)	21	A
	– Pulsed (Note 1a)	100	
P_D	Power Dissipation (Note 1)	33	W
		3.3	
		1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+175$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	4.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	45	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6530A	FDD6530A	13"	16mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
W _{DSS}	Drain-Source Avalanche Energy	Single Pulse, V _{DD} = 10 V			55	mJ
I _{AR}	Drain-Source Avalanche Current				8	A
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		15		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 8 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –8 V, V _{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.4	0.9	1.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		–3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 4.5 V, I _D = 8 A V _{GS} = 2.5 V, I _D = 6.6 A V _{GS} = 4.5 V, I _D = 8 A, T _J = 125°C		26 36 36	32 47 48	mΩ
I _{D(on)}	On–State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	20			A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 8 A		21		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz		710		pF
C _{oss}	Output Capacitance			173		pF
C _{rss}	Reverse Transfer Capacitance			84		pF
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = 10 V, I _D = 1 A, V _{GS} = 4.5 V, R _{GEN} = 6		8	16	ns
t _r	Turn–On Rise Time			7	14	ns
t _{d(off)}	Turn–Off Delay Time			18	32	ns
t _f	Turn–Off Fall Time			4	8	ns
Q _g	Total Gate Charge	V _{DS} = 10 V, I _D = 8 A, V _{GS} = 4.5 V		6.5	9	nC
Q _{gs}	Gate–Source Charge			1.3		nC
Q _{gd}	Gate–Drain Charge			1.9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain–Source Diode Forward Current				2.7	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.7 A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA} = 45^\circ\text{C/W}$ when mounted on a
1in² pad of 2 oz copper



b) $R_{\theta JA} = 96^\circ\text{C/W}$ when mounted
on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

3. Maximum current is calculated as:

$$\sqrt{\frac{P_D}{P_{D(max)}}}$$

where P_D is maximum power dissipation at $T_C = 25^\circ\text{C}$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10\text{ V}$. Package current limitation is 21A

Typical Characteristics

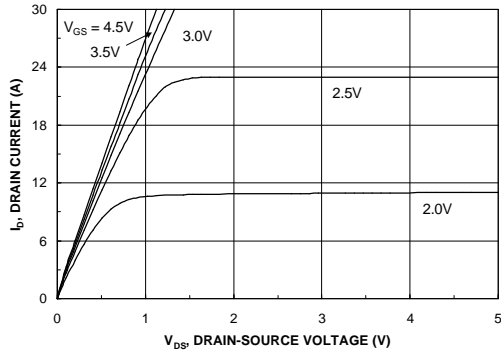


Figure 1. On-Region Characteristics.

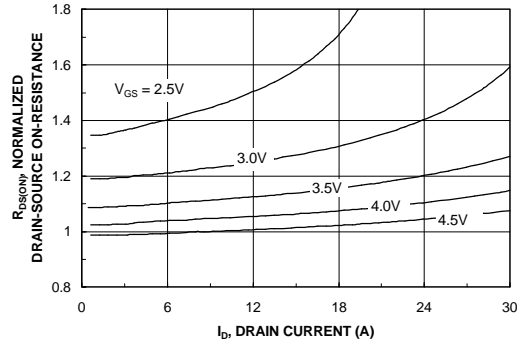


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

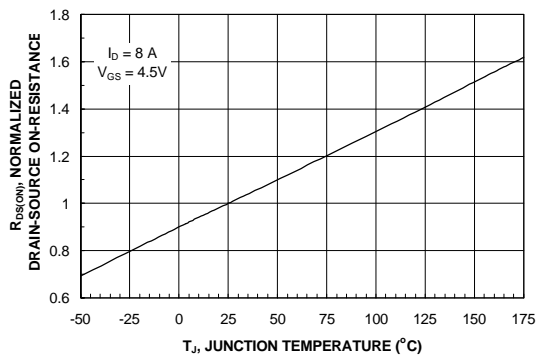


Figure 3. On-Resistance Variation with Temperature.

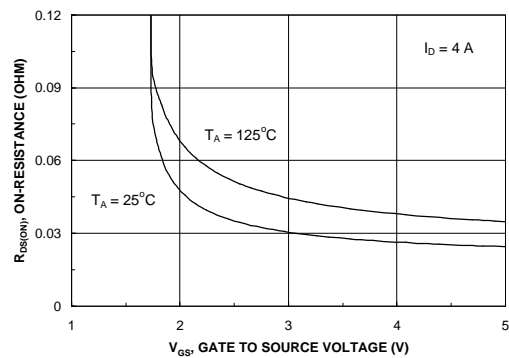


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

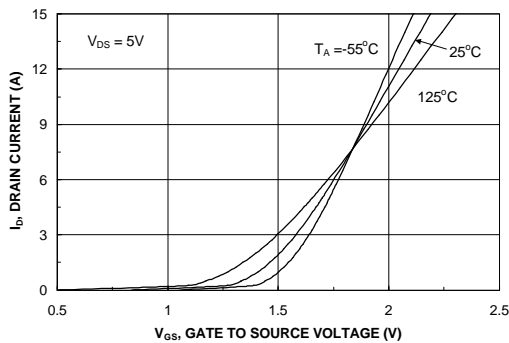


Figure 5. Transfer Characteristics.

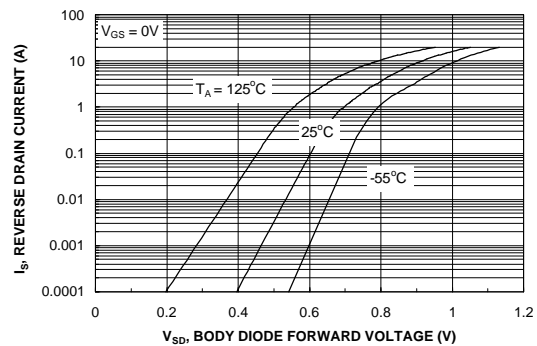


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

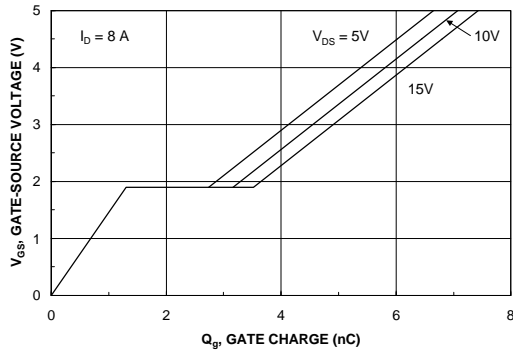


Figure 7. Gate Charge Characteristics.

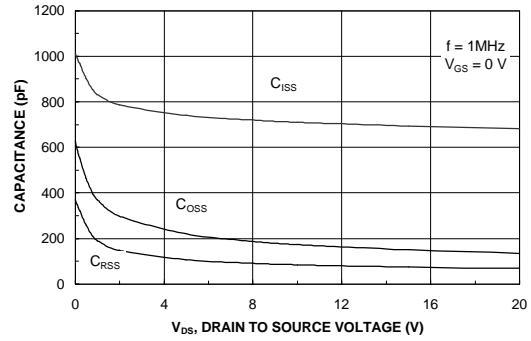


Figure 8. Capacitance Characteristics.

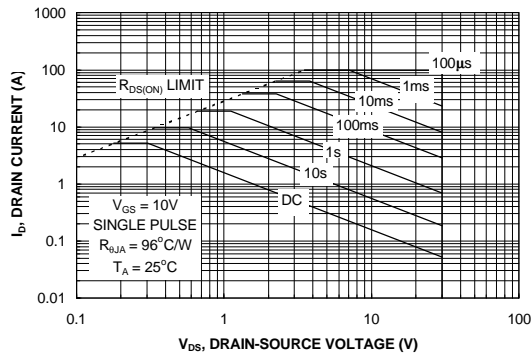


Figure 9. Maximum Safe Operating Area.

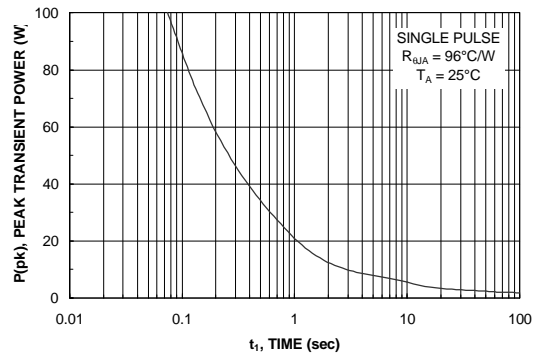


Figure 10. Single Pulse Maximum Power Dissipation.

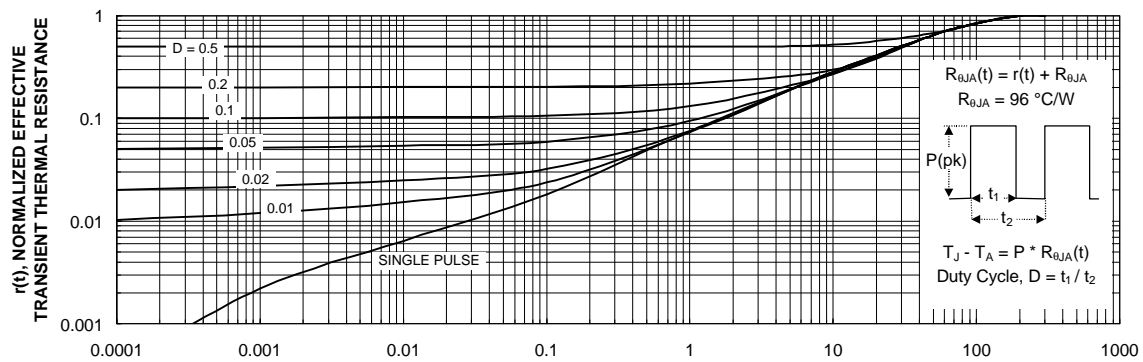
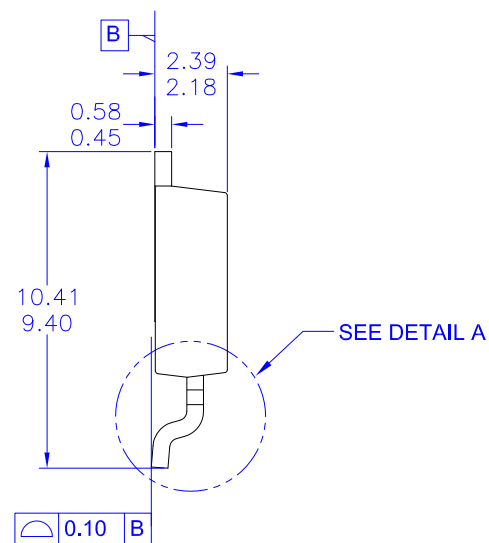
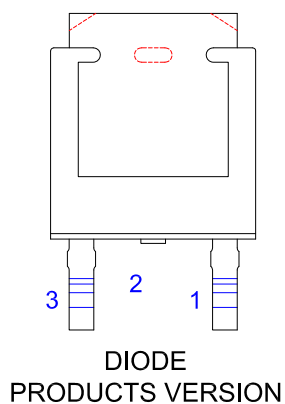
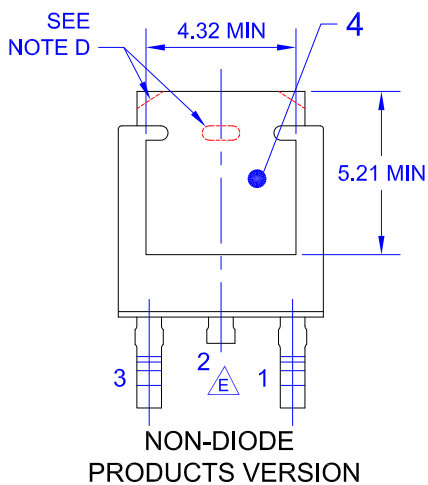
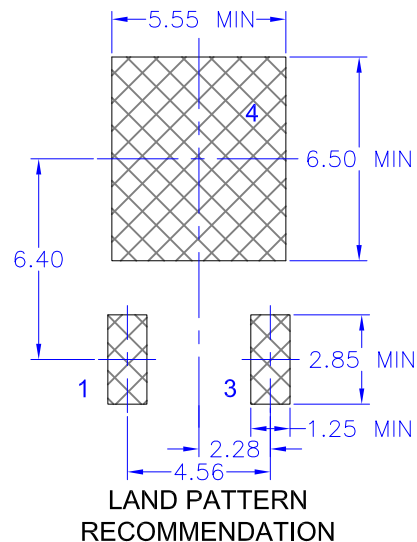
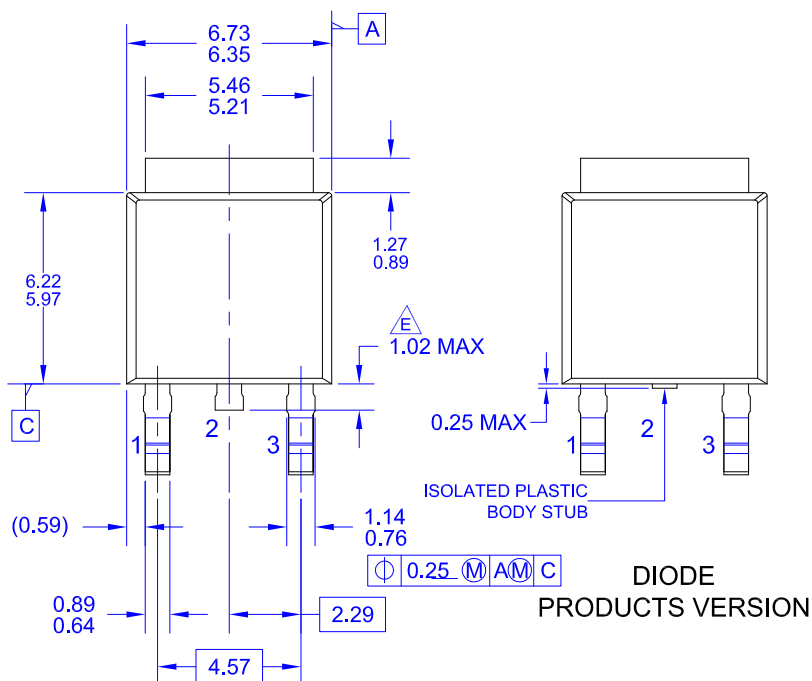


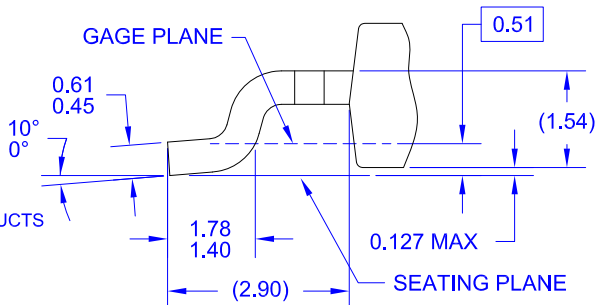
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X



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