

LV55K Series 2.5 V LVDS Clock Oscillators

November 2018



- Pletronics' LV55K Series is a quartz crystal controlled precision square wave generator with LVDS output.
- Improved phase noise performance.
- Tape and Reel or cut tape packaging is available.
- 3.2 x 5 mm LCC Ceramic Package
- Enable/Disable Function on pad 1
- Disable function includes low standby power mode
- 3rd Overtone Crystals used
- Improved circuit to minimize oscillator issues such as multi-mode output signal.
- Lowest Jitter Product

*** BEST OPTION FOR LOW JITTER REQUIREMENTS
50 fS Jitter 12.0 KHz to 20.0 MHz @156.25 MHz**

**Pletronics Inc. certifies this device is in accordance with the
RoHS 6/6 (2011/65/EC) and WEEE (2002/96/EC) directives.**

Pletronics Inc. guarantees the device does not contain the following:

Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

Weight of the Device: 0.09 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020D.1

Second Level Interconnect code: e4

Absolute Maximum Ratings:

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +4.6V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics

The maximum die or junction temperature is 125°C

The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.

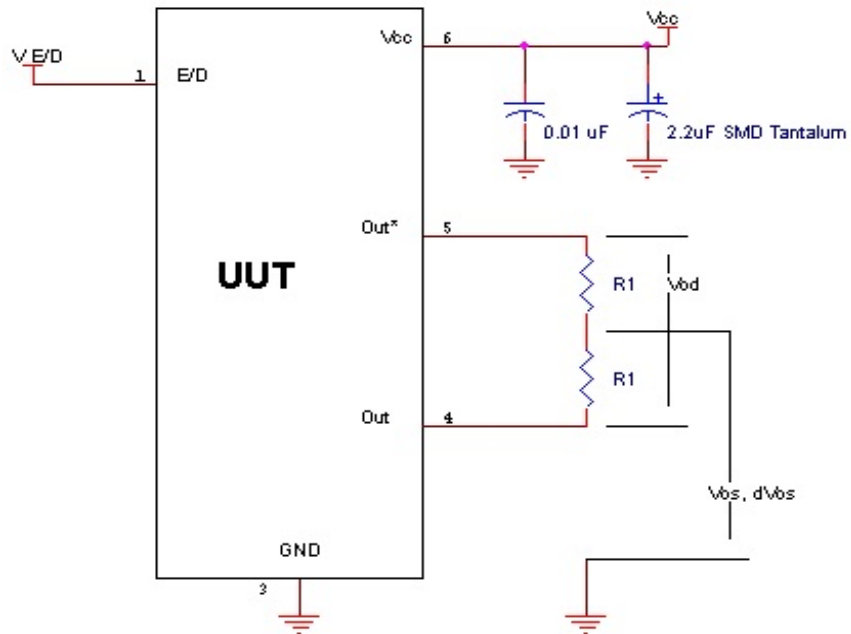
Electrical Specification for 2.50V $\pm 5\%$ over the specified temperature range and the frequency range of 100.0 to 212.50 MHz

Item	Min	Typ	Max	Unit	Condition
Frequency Accuracy "45"	-50	-	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures
"44"	-25	-	+25		
"20"	-20	-	+20		
Output Waveform	LVDS				
Output High Level	-	1.43	1.60	V	
Output Low Level	0.90	1.10	-	V	
Output Symmetry	45	-	55	%	at 50% point of V_{CC} (See load circuit)
Jitter ¹	-	50	-	fs RMS	12 KHz to 20 MHz from the output frequency @156.25 MHz
Output T_{RISE} and T_{FALL}	-	0.3	1.0	ns	V_{th} is 20% and 80% of waveform
V_{CC} Supply Current (I_{CC})	-	-	45	mA	
Enable/Disable Internal Pull-up	30	-	150	Kohm	to V_{CC} , measured with Pad 1 = 0.0 volts
V disable	-	-	20	% V_{CC}	
V enable	80	-	-	% V_{CC}	
Output leakage Current	-10	-	+10	μ A	
Enable time	-	-	2	ms	Time for output to reach a logic state, the output frequency is correct at the specified Start Time.
Disable time	-	-	200	ns	Time for output to reach a high Z state
Start up time	-	-	3	ms	Time for output to reach specified frequency
Operating Temperature Range	-10	-	+70	$^{\circ}$ C	Standard Temperature Range
	-20	-	+70	$^{\circ}$ C	Extended Temperature Range "C" Option
	-40	-	+85	$^{\circ}$ C	Extended Temperature Range "E" Option
Storage Temperature Range	-55	-	+125	$^{\circ}$ C	
Standby Current I_{CC}	-	-	15	μ A	Pad 1 low, device disabled

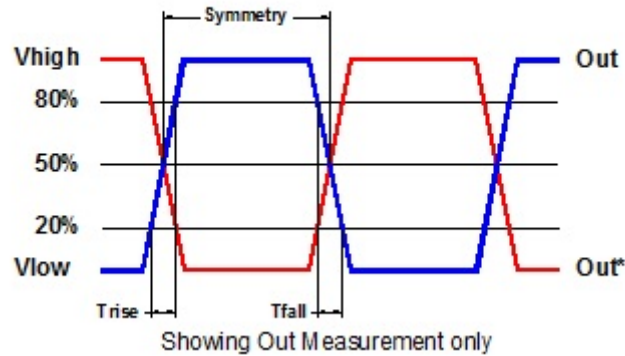
¹ Jitter computed from phase noise data at 156.25MHz

Specifications with Pad 1 E/D open circuit unless stated otherwise

Load Circuit



Test Waveform



Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

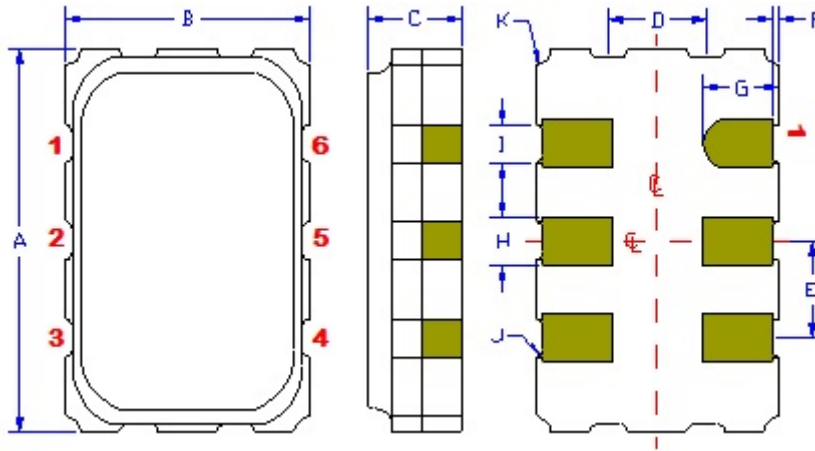
Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Courier New
Bar code is 39-Full ASCII

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Arial

P/N:	
	LV5545KW-156.25M
Customer P/N:	
	12345678
Qty:	
	1000
D/C	
	6KX-SG
MSL: 1	

RoHS Compliant
2nd LvL Interconnect
Category=e4
Max Safe Temp=260C for 10s 2X Max

Mechanical:



	Inches	mm
A	0.197 \pm 0.006	5.00 \pm 0.15
B	0.125 \pm 0.006	3.20 \pm 0.15
C	0.053 max	1.35 max
D ¹	0.050	1.27
E ¹	0.050	1.27
F ¹	0.004	0.10
G ¹	0.039	1.00
H ¹	0.025	0.63
I ¹	0.020	0.50
J ¹	0.004R	0.10R
K ¹	0.008R	0.20R

Contacts:

Gold 11.8 to 39.4 μ mches (0.3 to 1.0 μ m)
over
Nickel 50 to 350 μ mches (1.27 to 8.89 μ m)

¹ Typical dimensions

Not to Scale

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is <0.30 volts, the output will be inhibited (high impedance state.) Recommend connecting this pad to V _{CC} if the oscillator is to be always on.
2	No connect	There is no internal connection to this pad
3	Ground (GND)	
4	Output	Both outputs must be terminated and biased for proper operation. The ideal termination is 50 ohms connected to 2.0V below the Supply Voltage.
5	Output*	
6	Supply Voltage (V _{CC})	Recommend connecting appropriate power supply bypass capacitors as close as possible.

Layout and application information

Recommend connecting Pad 1 and Pad 2 together to permit the design to accept Enable/Disable input on either pad

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.

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