
USB 2.0 Hub and Flash Media Card Controller Combo

General Description

The USB2642 is a USB 2.0 compliant, hi-speed hub and card reader combo solution. This fully-integrated, single chip solution provides USB expansion and flash media reader/writer integration. The Microchip USB2642 provides an ultra fast interface between a USB host and today's popular flash media formats. The controller allows read/write capability to flash media including the following:

- Secure Digital™ (SD)
- SD High Capacity™ (SDHC)
- SD Extended Capacity™ (SDXC)
- MultiMediaCard™ (MMC)
- Embedded MultiMediaCard™ (eMMC)

The USB2642 offers a versatile, cost-effective and energy-efficient hub controller with 2 downstream USB 2.0 ports and a flash media interface. The flash media interface can support sustained transfer rates exceeding 35 MB/s.

Additionally, the USB2642 provides an I²C™ over USB bridge and an SD over USB bridge. The I²C bridge allows for control of any I²C slave device operating at 50KHz serial clock.

Highlights

- **PortMap**
 - Flexible port mapping and port disable sequencing supports multiple platform designs
- **PortSwap**
 - Programmable USB differential-pair pin locations eases PCB design by aligning USB signal traces directly to connectors
- **PHYBoost**
 - Programmable USB transceiver drive strength recovers signal integrity

Features

- Single-chip USB 2.0 hub controller with 2 exposed hi-speed downstream ports
- The dedicated flash media reader is internally attached to a 3rd downstream port of the hub as a USB compound device
- Hub and flash media reader/writer configuration from a single source:
 - Configures internal code using an external SPI ROM
 - Supports execution of external code from SPI Flash EEPROM
 - Supports custom vendor, product, and language ID when using an external EEPROM
- Supports full power management with individual or ganged power control of each downstream port
- Transaction Translator (TT) in the hub supports operation of FS and LS peripherals
- Single 24 MHz crystal support
- Control of peripheral I²C devices by USB host.
- Supports internally or externally regulated 1.8 V core voltage operation
- Supports storage addressability of up to 2TB
- RoHS compliant package
 - USB2642: 48-pin (7x7 mm²) QFN
- Temperature ranges:
 - Commercial Range (0 °C to +70 °C)
 - Industrial Range (-40 °C to +85 °C)

Target Applications

- Desktop and mobile PCs
- Monitors and televisions
- Mobile PC docking
- Consumer A/V
- Media players/viewers
- Printers
- Flash media card readers/writers

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1.0 OVERVIEW

1.1 Introduction

The USB2642 offers a USB 2.0 compliant, versatile, cost-effective and energy-efficient hi-speed hub controller with 2 downstream USB ports and an SD/MMC flash media card interface. The dedicated flash media reader is internally attached to a 3rd downstream port of the hub as a USB compound device. This combo solution supports today's popular multi-format flash media card formats. The flash media interface can support sustained transfer rates exceeding 35 MB/s if the media and host support those rates.

The USB2642 also provides I²C over USB. The I²C bridge allows for control of any I²C device operating at 50kHz clock.

The USB2642 will attach to an upstream port as either a full-speed or full-/hi-speed hub. The hub supports low-speed, full-speed, and hi-speed (if operating as a full-/hi-speed hub) downstream devices on all of the enabled downstream ports.

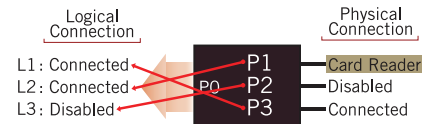
All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB2642 includes programmable features such as:

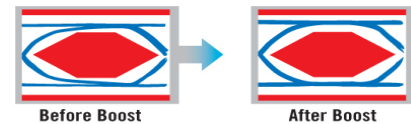
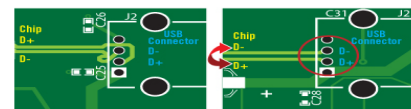
PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB2642 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB2642 automatically reorders the remaining ports to match the USB host controller's port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity. The diagram on the right shows an example of Hi-Speed USB eye diagrams before (PHYBoost at 0%) and after (PHYBoost at 12%) signal integrity restoration in a compromised system environment.



USB Port Virtualization



USB2642

1.2 Device Features

1.2.1 HARDWARE FEATURES

- Single-chip hub, flash media controller, and I²C device control over USB
- Supports commercial (0 °C to +70 °C) and industrial (-40 °C to +85 °C) temperature ranges
- Transaction Translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI
- Code execution via SPI ROM which must meet the following qualifications:
 - 60 MHz operation support
 - Single bit or dual bit mode support
 - Mode 0 or mode 3 SPI support

Compliant with the following flash media card specifications:

- Secure Digital 2.0
 - SDSC, SDHC, and SDXC
 - microSD and reduced form factor media
 - Supports storage addressability of up to 2TB
- MultiMediaCard 4.2
 - 1/4/8 bit
 - Includes support for eMMC devices
- Control of I²C device using the I²C over USB bridge
- Supports internal regulator for 1.8 V core operation
- Supports external regulator for 1.8 V core operation

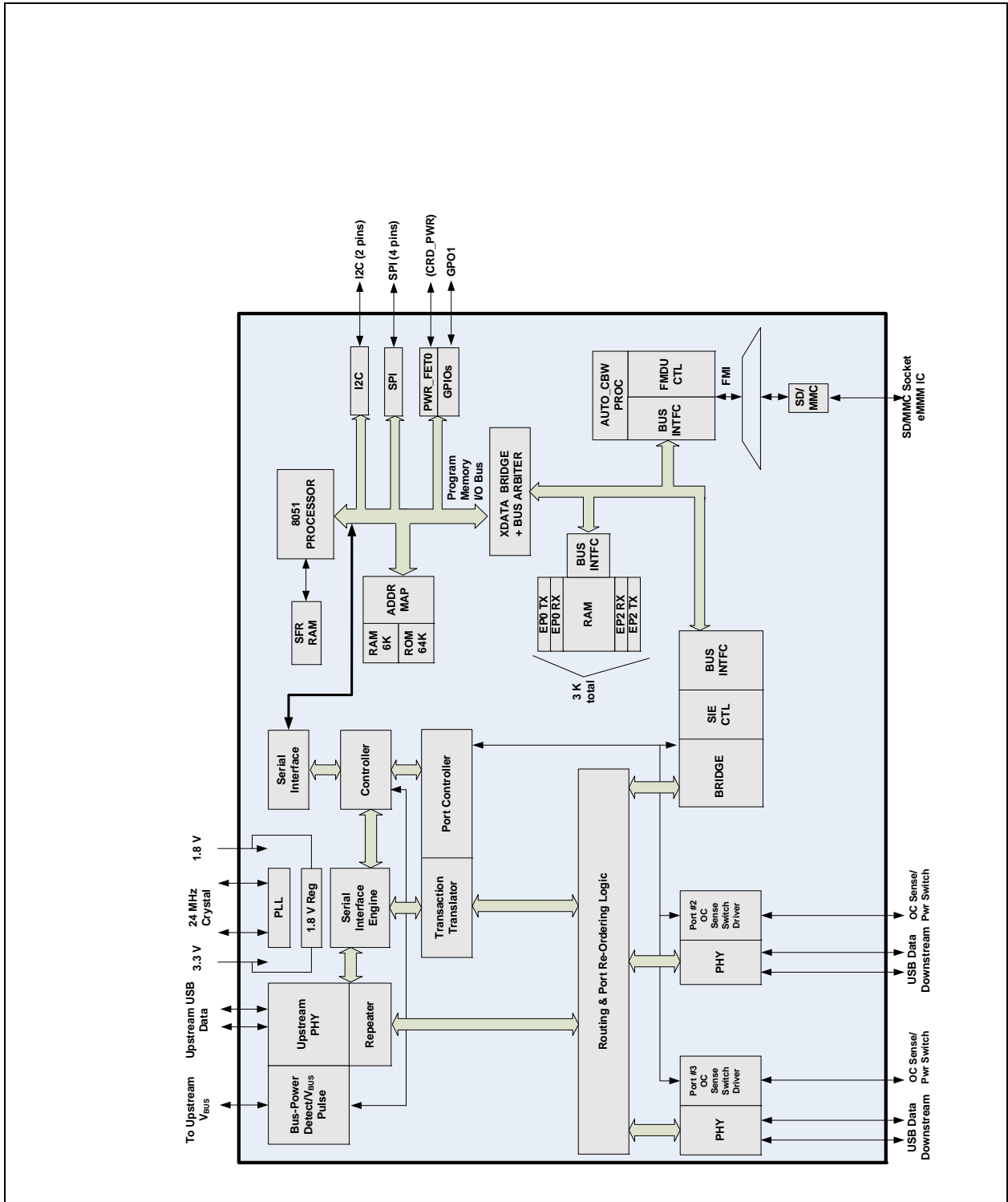
1.2.2 CONFIGURABLE FEATURES

Default configuration is loaded by USB2642 following a reset. The USB2642 may also be configured by an external I²C EEPROM or external SPI ROM flash, where the following features are supported:

- Customizable vendor ID, product ID, and device ID
- 12-hex digits maximum for the serial number string
- 29-character manufacturer ID and product strings for flash media reader/writer
- Compound device support on a port-by-port basis a port is permanently hardwired to a downstream USB peripheral device
- Select over-current sensing and port power control on an individual or ganged (all ports together) basis to match the circuit board component selection
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs
- Configure the delay time for turning on downstream port power
- Bus- or self-powered selection
- Hub port disable of non-removable configurations
- Flexible port mapping and disable sequencing supports multiple platform designs
- Programmable USB differential-pair pin location selection eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength improves USB signal integrity using 4 levels of signal drive strength
- Indicate the maximum current that the 2-port hub consumes from the USB upstream port
- Manage the maximum current required for the hub controller

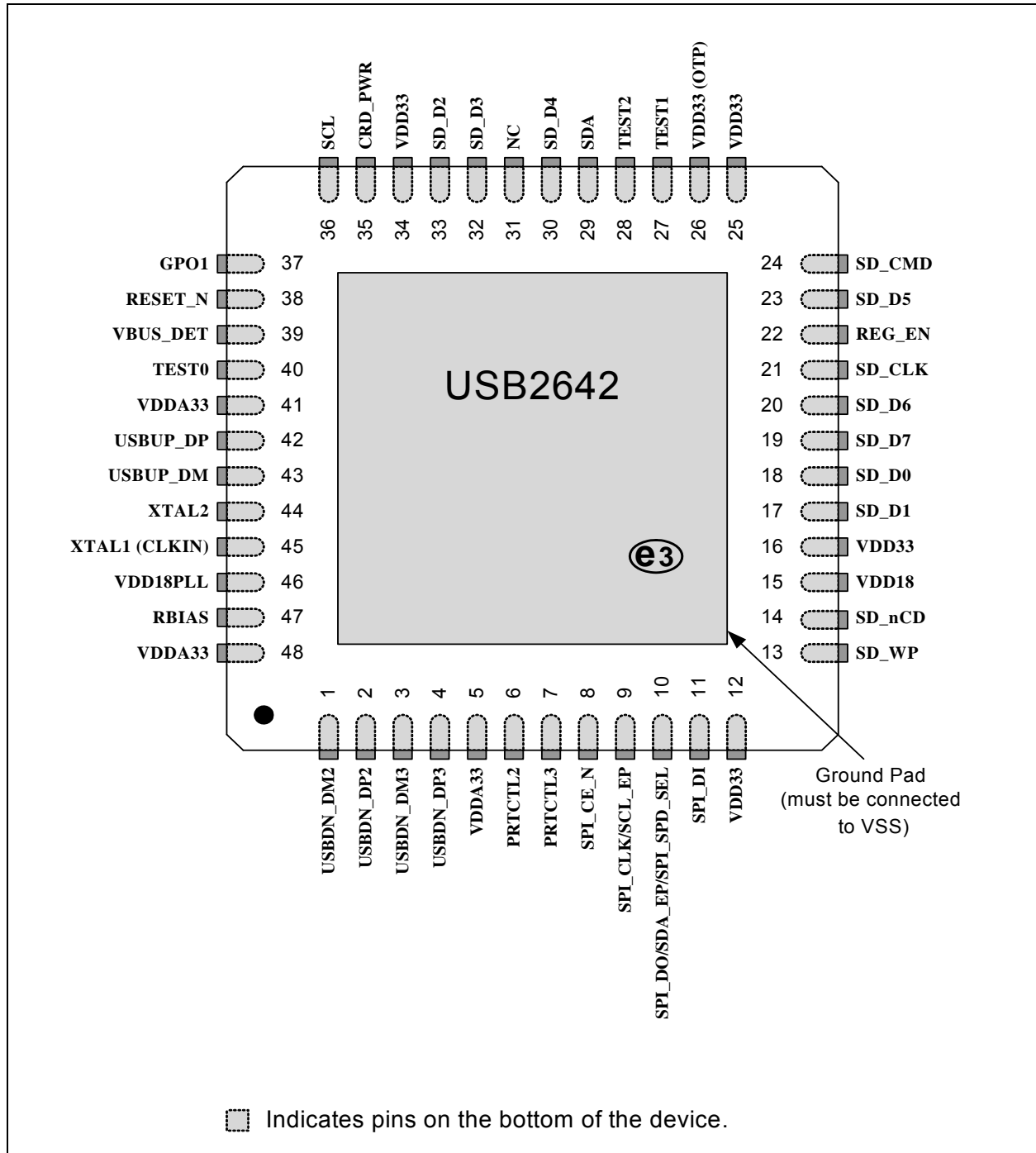
2.0 BLOCK DIAGRAM

FIGURE 2-1: USB2642 BLOCK DIAGRAM



3.0 USB2642 PIN CONFIGURATION

FIGURE 3-1: USB2642 48-PIN QFN - TOP VIEW



4.0 PIN TABLE

TABLE 4-1: USB2642 48-PIN TABLE (GROUPED BY FUNCTION)

| Secure Digital (12 pins) | | | |
|--|--------------------|-----------------------------------|---------|
| SD_D7 | SD_D6 | SD_D5 | SD_D4 |
| SD_D3 | SD_D2 | SD_D1 | SD_D0 |
| SD_CLK | SD_CMD | SD_nCD | SD_WP |
| USB 2.0 Interface (10 pins) | | | |
| USBUP_DP | USBUP_DM | XTAL1 (CLKIN) | XTAL2 |
| RBIAS | (3) VDDA33 | VDD18PLL | REG_EN |
| 2-PORT USB Interface (7 pins) | | | |
| USBDN_DP2 | USBDN_DM2 | PRTCTL2 | PRTCTL3 |
| USBDN_DP3 | USBDN_DM3 | VBUS_DET | - |
| SPI Interface (4 pins) | | | |
| SPI_CE_N | SPI_CLK/ SCL_EP | SPI_DO/ SDA_EP/ SPI_SPD_SEL | SPI_DI |
| I²C Interface (2 pins) | | | |
| SCL | SDA | | |
| MISC (7 pins) | | | |
| RESET_N | TEST0 | TEST1 | TEST2 |
| GPO1 | CRD_PWR | (1) NC | |
| POWER (6 pins) | | | |
| (4) VDD33 | VDD33 | VDD18 | |
| Total 48 | | | |

5.0 PIN DESCRIPTIONS

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in [Section 7.0, Configuration Options](#). The acronyms used in this chapter can be referenced in [Appendix A: "Acronyms"](#).

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

5.1 USB2642 Pin Description

TABLE 5-1: USB2642 PIN DESCRIPTIONS

| Symbol | 48-Pin QFN | Buffer Type | Description |
|--|--|-------------|--|
| Secure Digital Interface | | | |
| SD_D[7:0] | 19 20 23 30 32 33 17 18 | I/O12PU | Secure Digital Data 7-0 These are the bi-directional data signals SD_D0 - SD_D7 Note: The pull up resistance is a current source that is limited to VDD. |
| SD_CLK | 21 | O12 | Secure Digital Clock This is an output clock signal to SD/MMC device. |
| SD_CMD | 24 | I/O12PU | Secure Digital Command This is a bi-directional signal that connects to the CMD signal of the SD/MMC device. |
| SD_nCD | 14 | I/O12PU | Secure Digital Card Detect |
| SD_WP | 13 | I/O12 | Secure Digital Write Protect |
| I²C Interface | | | |
| SDA | 29 | I/O12 | Serial Data Signal |
| SCL | 36 | I/O12 | Serial Clock |
| USB Interface | | | |
| USBUP_DM USBUP_DP | 43 42 | I/O-U | USB Bus Data These pins connect to the upstream USB bus data signals (host port or upstream hub). USBUP_DM and USBUP_DP can be swapped using the PortSwap feature. |
| USBDN_DM [3:2] USBDN_DP [3:2] | 3 1 4 2 | I/O-U | USB Bus Data These pins connect to the downstream USB bus data signals and can be swapped using the PortSwap feature. |

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TABLE 5-1: USB2642 PIN DESCRIPTIONS

| Symbol | 48-Pin QFN | Buffer Type | Description |
|----------------------|---------------|-------------|---|
| PRTCTL[3:2] | 7 6 | I/OD12PU | <p>USB Power Enable</p> <p>As an output, these pins enables power downstream USB peripheral devices. See Section 5.3, "Port Power Control" for diagram and usage instructions.</p> <p>As an input, when the power is enabled, these pins monitor the over-current condition. When an over-current condition is detected, these pins turn the power off.</p> |
| VBUS_DET | 39 | I | <p>Detect Upstream VBUS Power</p> <p>The Microchip hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event).</p> <p>When designing a detachable hub, connect this pin to the VBUS power pin of the USB port that is upstream of the hub.</p> <p>For self-powered applications with a permanently attached host, this pin should be pulled up, typically to VDD33.</p> <p>VBUS is a 3.3 volt input. A resistor divider must be used when connecting to 5 volts of USB power.</p> |
| RBIAS | 47 | I-R | <p>USB Transceiver Bias</p> <p>A 12.0 kΩ, \pm1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.</p> |
| XTAL1 (CLKIN) | 45 | ICLKx | <p>24 MHz Crystal Input/External Clock Input</p> <p>This pin can be connected to one terminal of the crystal or it can be connected to an external 24 MHz clock when a crystal is not used.</p> |
| XTAL2 | 44 | OCLKx | <p>24 MHz Crystal Output</p> <p>This is the other terminal of the crystal, or a no connect pin, when an external clock source is used to drive XTAL1 (CLKIN).</p> |
| VDD18PLL | 46 | - | <p>1.8 V PLL Power Bypass</p> <p>This pin is the 1.8 V power bypass for the PLL. This pin requires an external bypass capacitor of 1.0 μF.</p> <p>If REG_EN is low, this pin serves as a power supply (1.8 V) for the device.</p> |
| VDDA33 | 5 41 48 | - | <p>3.3 V Analog Power</p> <ul style="list-style-type: none"> 48QFN - Pin 48 requires an external bypass capacitor of 4.7 μF. |
| SPI Interface | | | |
| SPI_CE_N | 8 | O12 | <p>SPI Chip Enable</p> <p>This is the active low chip enable output. If the SPI interface is enabled, drive this pin high in power down states.</p> |
| SPI_CLK/ | 9 | I/O12 | <p>SPI Clock</p> <p>This is the SPI clock out to the serial ROM. See Section 5.4, "ROM Boot Sequence" for diagram and usage instructions.</p> <p>During reset, this pin is driven low.</p> |
| SCL_EP | | | When configured, this is the I ² C EEPROM clock pin. |

TABLE 5-1: USB2642 PIN DESCRIPTIONS

| Symbol | 48-Pin QFN | Buffer Type | Description |
|-----------------------------|----------------------|-------------|--|
| SPI_DO/ | 10 | I/O12 | SPI Data Out This is the data out for the SPI port. See Section 5.4, "ROM Boot Sequence" for diagram and usage instructions. |
| SDA_EP | | | This pin is the data pin when the device is connected to the optional I ² C EEPROM. |
| SPI_SPD_SEL | | | This pin is used to pick the speed of the SPI interface. During RESET_N assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When RESET_N is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality. Additionally, the internal pull-down will be disabled. 0 : 30 MHz 1 : 60 MHz If the latched value is 1, then the pin is tri-stated when the chip is in the suspend state. If the latched value is 0, then the pin is driven low during a suspend state. |
| SPI_DI | 11 | I/O12PD | SPI Data In This is the data in to the controller from the SPI ROM. |
| Misc | | | |
| GPO1 | 37 | I/O12 | This general purpose pin is set to be used as an output. |
| CRD_PWR | 35 | I/O200 | Card power drive: 3.3 V (200 mA) This pin powers the multiplexed flash media interface (slot) for the SD/MMC interface. Bits 0, 1, 2, and 3 control FET 2 of Register A5h. See Section 7.4.2.11, "A4h-A5h: LUN 0 Power Configuration," on page 26 for more information. |
| NC | 31 | IPU | |
| REG_EN | 22 | IPU | Regulator Enable This pin is internally pulled up to enable the internal 1.8 V regulators. In order to disable the regulators, this pin will need to be externally connected to ground. When the internal regulator is enabled, the 1.8 V power pins must be left unconnected, except for the required bypass capacitors. |
| RESET_N | 38 | I | RESET input This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 μ s wide. |
| TEST[2:0] | 28 27 40 | IPD | TEST Input Tie these test pins to ground for normal operation. |
| Digital/Power/Ground | | | |
| VDD18 | 15 | - | 1.8 V Digital Core Power Bypass This pin requires an external bypass capacitor of 1.0 μ F. If REG_EN is low, this pin serves as a power supply (1.8 V) for the device. |
| VDD33 | 12 16 25 34 | - | 3.3 V Power and Regulator Input • 48QFN - Pin 16 requires an external bypass capacitor of 4.7 μ F minimum. |
| VDD33 (OTP) | 26 | - | 3.3 V Power |

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TABLE 5-1: USB2642 PIN DESCRIPTIONS

| Symbol | 48-Pin QFN | Buffer Type | Description |
|--------|------------|-------------|--|
| VSS | ePad | - | Ground Pad The ground pad is the only VSS for the device and must be tied to ground with multiple vias. |

5.2 Buffer Type Descriptions

TABLE 5-2: USB2642 BUFFER TYPE DESCRIPTIONS

| Buffer | Description |
|----------|--|
| I | Input |
| IPU | Input with weak internal pull-up |
| IS | Input with Schmitt trigger |
| I/O12 | Input/output buffer with 12 mA sink and 12 mA source |
| I/O200 | Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled |
| I/O12PD | Input/output buffer with 12 mA sink and 12 mA source, with an internal weak pull-down resistor |
| I/O12PU | Open drain, 12 mA sink with pull-up. Input with Schmitt trigger |
| I/OD12PU | Input/open drain output buffer with a 12 mA sink |
| O12 | Output buffer with a 12 mA sink and a 12 mA source |
| ICLKx | XTAL clock input |
| OCLKx | XTAL clock output |
| I/O-U | Analog input/output defined in <i>USB Specification (Appendix B)</i> |
| I-R | RBIAS |

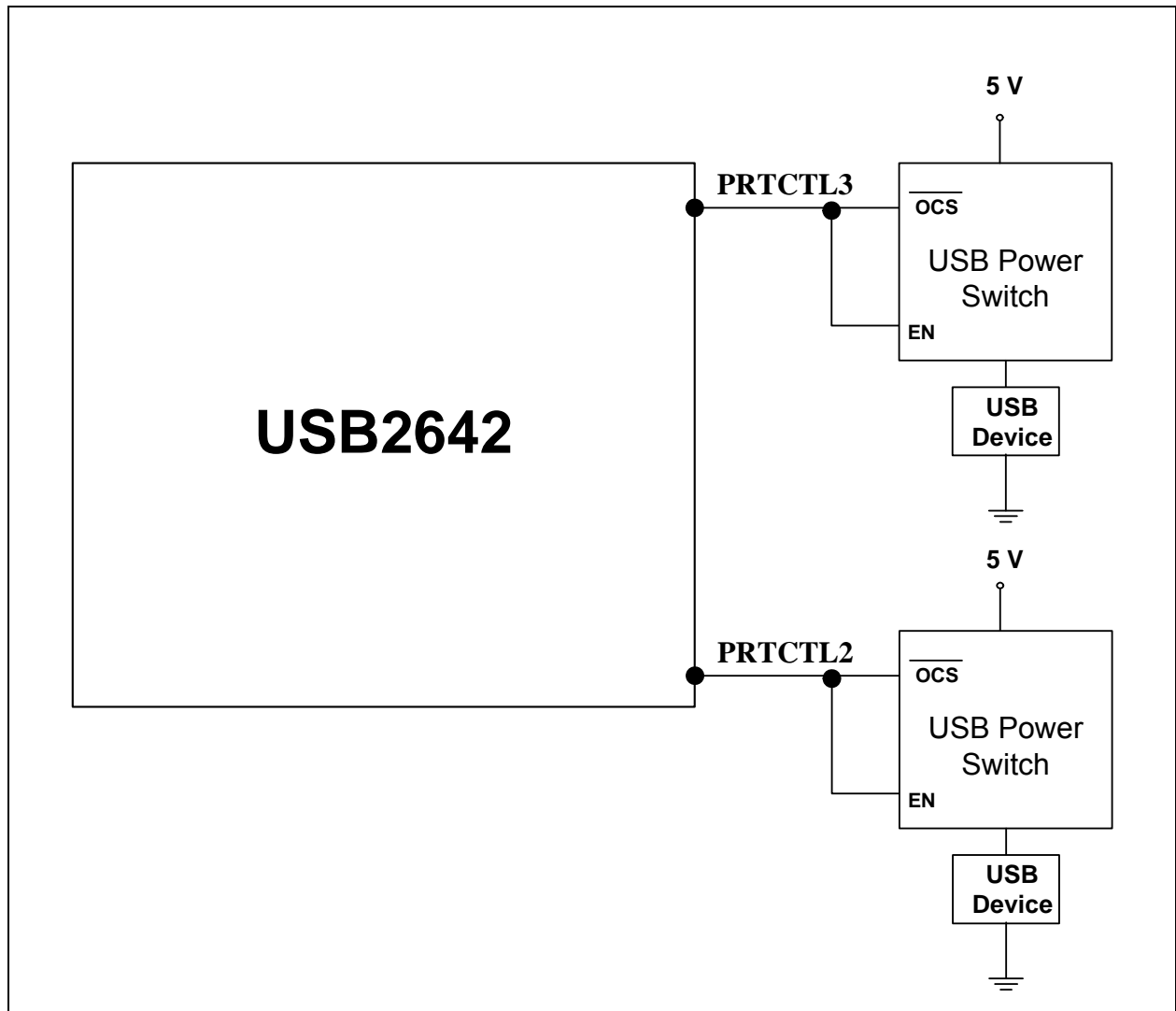
5.3 Port Power Control

5.3.1 PORT POWER CONTROL USING USB POWER SWITCH

The USB2642 has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a 0. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output.

If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

FIGURE 5-1: PORT POWER CONTROL WITH USB POWER SWITCH

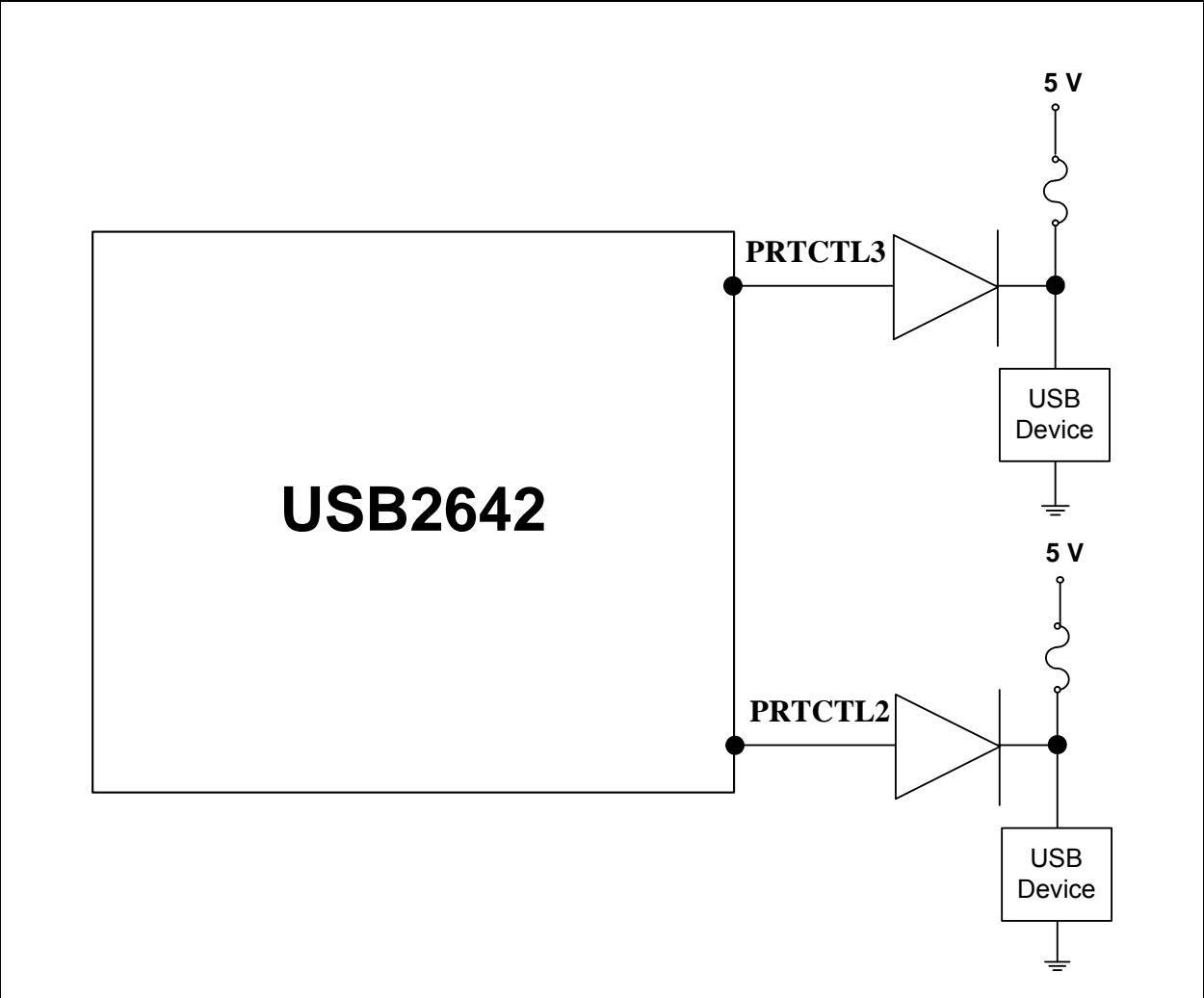


5.3.2 PORT POWER CONTROL USING A POLY FUSE

When using the USB2642 with a poly fuse, an external diode must be used (see [Figure 5-2](#)). When disabling port power, the USB2642 driver will drive a 0. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the USB2642 output driver is disabled, and the pull-up resistor is enabled which creates an open drain output. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to zero volts. The anode of the diode will be at 0.7 volts, and the Schmitt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

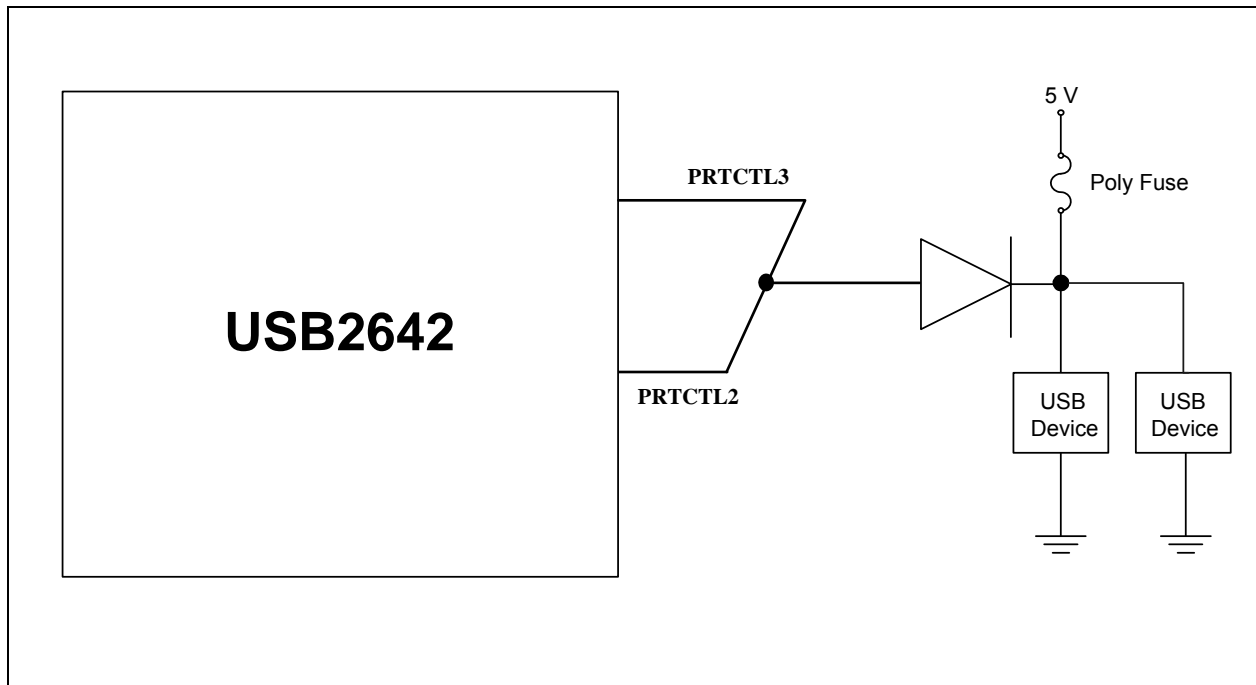
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FIGURE 5-2: PORT POWER CONTROL WITH SINGLE POLY FUSE AND MULTIPLE LOADS



When using a single poly fuse to power all devices, note that for the ganged situation, all power control pins must be tied together.

FIGURE 5-3: PORT POWER WITH GANGED CONTROL WITH POLY FUSE



5.4 ROM Boot Sequence

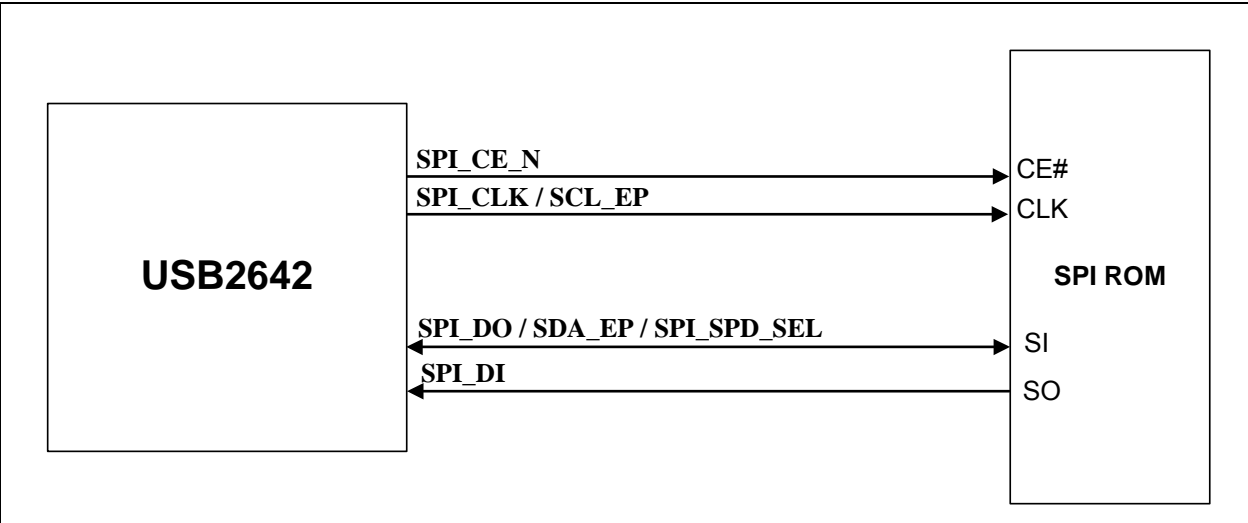
After power-on reset, the internal firmware checks for an external SPI flash device that contains a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and code execution begins at address 0x0000 in the external SPI device. Otherwise, code execution continues from the internal ROM.

The SPI ROM required for the USB2642 is a recommended minimum of 1 Mbit and support 60 MHz. The frequency used is set using the **SPI_SPD_SEL**. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor. **SPI_SPD_SEL** is used to choose the speed of the SPI interface. During **RESET_N** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **RESET_N** is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality, and the internal pull-down is disabled.

The firmware can determine the speed of operation on the SPI port by checking the **SPI_SPEED** in the SPI_CTL Register (0x2400 - RESET = 0x02). Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported.

USB2642

FIGURE 5-4: SPI ROM CONNECTION



6.0 PIN RESET STATES

TABLE 6-1: LEGEND FOR PIN RESET STATES

| Symbol | Description |
|--------|---|
| 0 | Output driven low |
| 1 | Output driven high |
| IP | Input enabled |
| PU | Hardware enables pull-up |
| PD | Hardware enables pull-down |
| none | Hardware disables pad |
| - | Hardware disables function |
| Z | Hardware disables pad. Both output driver and input buffers are disabled. |

6.1 Pin Reset States

TABLE 6-2: USB2642 RESET STATES

| Pin | Pin Name | Reset State | | |
|-----|---------------------------|-------------|------------------|-----------|
| | | Function | Input/ Output | PU/ PD |
| 1 | USBDN_DM2 | USBDN_DM2 | IP | PD |
| 2 | USBDN_DP2 | USBDN_DP2 | IP | PD |
| 3 | USBDN_DM3 | USBDN_DM3 | IP | PD |
| 4 | USBDN_DP3 | USBDN_DP3 | IP | PD |
| 6 | PRTCTL2 | PRTCTL | 0 | - |
| 7 | PRTCTL3 | PRTCTL | 0 | - |
| 8 | SPI_CE_N | SPI_CE_N | 1 | - |
| 9 | SPI_CLK/SCL_EP | IO | 0 | - |
| 10 | SPI_DO/SDA_EP/SPI_SPD_SEL | IO | 0 | - |
| 11 | SPI_DI | SPI_DI | IP | PD |
| 13 | SD_WP | IO | 0 | - |
| 14 | SD_nCD | IO | IP | PU |
| 17 | SD_D1 | none | Z | - |

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TABLE 6-2: USB2642 RESET STATES (CONTINUED)

| Pin | Pin Name | Reset State | | |
|-----|----------|-------------|------------------|-----------|
| | | Function | Input/ Output | PU/ PD |
| 18 | SD_D0 | none | Z | - |
| 19 | SD_D7 | none | Z | - |
| 20 | SD_D6 | none | Z | - |
| 21 | SD_CLK | none | Z | - |
| 22 | REG_EN | none | IP | PU |
| 23 | SD_D5 | none | Z | - |
| 24 | SD_CMD | none | Z | - |
| 27 | TEST1 | none | Z | - |
| 28 | TEST2 | none | Z | - |
| 29 | SDA | IO | IP | PU |
| 30 | SD_D4 | none | Z | - |
| 31 | NC | GPIO | IP | PU |
| 32 | SD_D3 | none | Z | - |
| 33 | SD_D2 | none | Z | - |
| 35 | CRD_PWR | IO | Z | - |
| 36 | SCL | IO | 0 | - |
| 37 | GPO1 | GPO | 0 | - |
| 38 | RESET_N | RESET_N | IP | - |
| 39 | VBUS_DET | VBUS_DET | IP | - |
| 40 | TEST0 | TEST | IP | PD |
| 42 | USBUP_DP | USBUP_DP | Z | - |
| 43 | USBUP_DM | USBUP_DM | Z | - |

7.0 CONFIGURATION OPTIONS

7.1 Hub

Microchip's USB2642 hub is fully compliant with the *Universal Serial Bus 2.0 Specification* ([References](#)). See Chapter 11 (Hub Specification) for general details regarding hub operation and functionality.

The hub provides a single Transaction Translator (TT) shared by both downstream ports. The TT contains 4 non-periodic buffers.

7.1.1 HUB CONFIGURATION OPTIONS

The Microchip hub supports a large number of configurable features (some are mutually exclusive). There are two principal ways to configure the hub:

- default settings
- settings loaded from an external EEPROM or SPI Flash device

7.1.1.1 Power Switching Polarity

The hub will only support active high power controllers.

7.1.2 VBUS DETECT

According to Section 7.2.1 of the *USB 2.0 Specification*, a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. The **VBUS_DET** pin on the hub monitors the state of the upstream VBUS signal and will not pull-up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.

7.2 Card Reader

The Microchip USB2642 is fully compliant with the following flash media card reader specifications:

- Secure Digital 2.0
 - SDSC, SDHC, and SDXC
 - microSD and reduced form factor media
 - Supports storage addressability of up to 2TB
- MultiMediaCard 4.2
 - 1/4/8 bit
 - includes support for eMMC devices

7.3 I²C over USB Bridge

USB2642 offers a I²C over USB bridge functionality. Host initiated SCSI pass-through commands are sent to USB2642 using Mass Storage Class driver to control I²C master interface. Additional support for detecting clock stretching during reads is also provided.

The following features are exposed through host side I²C API:

- Write_I2C_Stream
Send any length of data over the I²C interface.
The sequence follows the I²C protocol for writing data.
- WriteRead_I2C_Stream
Read any length of data over the I²C interface.
The sequence follows the I²C protocol for reading data.
- GPIO_1_SET_OUTPUT
This method allows an application to assert **GPIO1** pin. This can be driving RST of the I²C slave device.

For additional configuration information and protocol details, see “*USB2642 I²C Over USB Bridge User's Guide*”.

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7.4 System Configurations

7.4.1 EEPROM/SPI INTERFACE

The USB2642 can be configured via a 2-wire (I²C) EEPROM (512x8) or an external SPI flash device containing the firmware for the USB2642. If an external configuration device does not exist the internal default values will be used. If one of the external devices is used for configuration, the OEM can update the values through the USB interface. The hub will then attach to the upstream USB host.

The USBDM tool set is available in the Hub Card reader combo software release package.

7.4.2 EEPROM DATA DESCRIPTOR

TABLE 7-1: INTERNAL FLASH MEDIA CONTROLLER CONFIGURATIONS

| Address | Register Name | Description | Internal Default Value |
|---------|---------------|---------------------------------|---------------------------------------|
| 00h-19h | USB_SER_NUM | USB Serial Number | 000008264001 (Unicode) |
| 1Ah-1Bh | USB_VID | USB Card Reader Vendor ID | 0424 |
| 1Ch-1Dh | USB_PID | USB Card Reader Product ID | 4041 |
| 1Eh-21h | USB_LANG_ID | USB Language Identifier | 0409 (see Note 1) |
| 22h-5Dh | USB_MFR_STR | USB Manufacturer String | Generic (Unicode) |
| 5Eh-99h | USB_PRD_STR | USB Product String | Ultra Fast Media Reader (Unicode) |
| 9Ah | USB_BM_ATT | USB BmAttribute | 80h |
| 9Bh | USB_MAX_PWR | USB Max Power | 30h (96 mA) |
| 9Ch | ATT_LB | Attribute Lo byte | 40h (Reverse SD_WP only) |
| 9Dh | ATT_HLB | Attribute Hi Lo byte | 80h (Reverse SD2_WP only) |
| 9Eh | ATT_LHB | Attribute Lo Hi byte | 00h |
| 9Fh | ATT_HB | Attribute Hi byte | 00h |
| A0h-A3h | rsvd | | |
| A4h | LUN_PWR_LB | LUN Power Lo byte | 00h |
| A5h | LUN_PWR_HB | LUN Power Hi byte | 0Ah |
| A6h-BEh | rsvd | | |
| BFh-C5h | DEV3_ID_STR | Device 3 Identifier String | SD/MMC |
| C6h-CDh | INQ_VEN_STR | Inquiry Vendor String | Generic |
| CEh-D2h | INQ_PRD_STR | 48QFN Inquiry Product String | 2642 |
| D3h | DYN_NUM_LUN | Dynamic Number of LUNs | 01h |
| D4h-D7h | LUN_DEV_MAP | LUN to Device Mapping | FFh, 00h, 00h, 00h |
| D8h-DAh | rsvd | | |

TABLE 7-1: INTERNAL FLASH MEDIA CONTROLLER CONFIGURATIONS (CONTINUED)

| Address | Register Name | Description | Internal Default Value |
|--|-------------------|---------------------------------|---|
| DBh-DDh | SD_MMC_BUS_TIMING | SD/MMC Bus Timing Control | 59h, 56h, 97h (Note 2) |
| <p>Refer to Table 7-2, "Hub Controller Configurations," on page 22 for a continuation of the register values DEh-17Fh.</p> <p>Internal Flash Media Controller Extended Configurations: The registers below are enabled by setting bit 7 of bmAttribute.</p> | | | |
| 100h-106h | CLUN0_ID_STR | LUN 0 Identifier String | COMBO |
| 107h-10Dh | CLUN1_ID_STR | LUN 1 Identifier String | COMBO |
| 10Eh-114h | CLUN2_ID_STR | LUN 2 Identifier String | COMBO |
| 115h-11Bh | CLUN3_ID_STR | LUN 3 Identifier String | COMBO |
| 11Ch-122h | CLUN4_ID_STR | LUN 4 Identifier String | COMBO |
| 123h-129h | rsvd | | |
| 12Ah-145h | rsvd | | |
| 146h | DYN_NUM_EXT_LUN | Dynamic Number of Extended LUNs | 00h |
| 147h-14Bh | LUN_DEV_MAP | LUN to Device Mapping | FFh, FFh, FFh, FFh, FFh |
| 14Ch-17Bh | rsvd | | |
| 17Ch-17Fh | NVSTORE_SIG2 | Non-Volatile Storage Signature | ecf1 |

Note that the following applies to the system values and descriptions:

- rsvd = reserved for internal use; do not write to these registers

Note 1: Refer to the USB 2.0 Specification ([References](#)) for other language codes.

2: This register value must not be changed from the default value.

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TABLE 7-2: HUB CONTROLLER CONFIGURATIONS

| Address | Register Name | Description | Internal Default Value |
|---------|---------------|---|------------------------|
| DEh | VID_LSB | Vendor ID Least Significant Byte | 24h |
| DFh | VID_MSB | Vendor ID Most Significant Byte | 04h |
| E0h | PID_LSB | 48QFN Product ID Least Significant Byte | 40h |
| E1h | PID_MSB | Product ID Most Significant Byte | 26h |
| E2h | DID_LSB | Device ID Least Significant Byte | A2h |
| E3h | DID_MSB | Device ID Most Significant Byte | 08h |
| E4h | CFG_DAT_BYT1 | Configuration Data Byte 1 | 8Bh |
| E5h | CFG_DAT_BYT2 | Configuration Data Byte 2 | 28h |
| E6h | CFG_DAT_BYT3 | Configuration Data Byte 3 | 00h |
| E7h | NR_DEVICE | Non-Removable Devices | 02h |
| E8h | PORT_DIS_SP | Port Disable (Self) | 00h |
| E9h | PORT_DIS_BP | Port Disable (Bus) | 00h |
| EAh | MAX_PWR_SP | Max Power (Self) | 01h |
| EBh | MAX_PWR_BP | Max Power (Bus) | 32h |
| ECh | HC_MAX_C_SP | Hub Controller Max Current (Self) | 01h |
| EDh | HC_MAX_C_BP | Hub Controller Max Current (Bus) | 32h |
| EEh | PWR_ON_TIME | Power-on Time | 32h |
| EFh | BOOST_UP | Boost_Up | 00h |
| F0h | BOOST_3:2 | Boost_3:2 | 00h |
| F1h | PRT_SWP | PortSwap | 00h |
| F2h | PRTM12 | PortMap 12 | 00h |
| F3h | PRTM3 | PortMap 3 | 00h |

TABLE 7-3: OTHER INTERNAL CONFIGURATIONS

| Address | Register Name | Description | Internal Default Value |
|---------|----------------|---|------------------------|
| F4h | SD_CLK_LIM | SD Clock Limit for the Flash Media Controller | 00h |
| F5h | rsvd | | |
| F6h | MEDIA_SETTINGS | SD1 Timeout Configuration | 00h |
| F7h-FBh | rsvd | | |
| FCh-FFh | NVSTORE_SIG | Non-Volatile Storage Signature | ATA2 |

7.4.2.1 00h-19h: USB Serial Number Option

| Byte | Name | Description |
|------|-------------|--|
| 25:0 | USB_SER_NUM | Maximum string length is 12 hex digits. Must be unique to each device. |

7.4.2.2 1Ah-1Bh: USB Vendor Identifier Option

| Byte | Name | Description |
|------|---------|---|
| 1:0 | USB_VID | This ID is unique for every vendor, where the vendor ID is assigned by the USB Implementer's Forum. |

7.4.2.3 1Ch-1Dh: USB Product Identifier Option

| Byte | Name | Description |
|------|---------|--|
| 1:0 | USB_PID | This ID is unique for every product, where the product ID is assigned by the vendor. |

7.4.2.4 1Eh-21h: USB Language Identifier Option

| Byte | Name | Description |
|------|-------------|------------------------------|
| 3:0 | USB_LANG_ID | English language code = 0409 |

7.4.2.5 22h-5Dh: USB Manufacturer String Length

| Byte | Name | Description |
|------|-------------|---|
| 59:0 | USB_MFR_STR | Maximum string length is 29 characters. |

7.4.2.6 5Eh-99h: USB Product String Length

| Byte | Name | Description |
|------|-------------|---|
| 59:0 | USB_PRD_STR | This string is used during the USB enumeration process by Windows®. The maximum string length is 29 characters. |

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7.4.2.7 9Ah: USB BmAttribute (1 byte)

| Bit | Name | Description |
|-----|------------|--|
| 7:0 | USB_BM_ATT | <p>Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller).</p> <p>When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated.</p> <p>When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current.</p> <p>80 = Bus-powered operation C0 = Self-powered operation A0 = Bus-powered operation with remote wake-up E0 = Self-powered operation with remote wake-up</p> |

7.4.2.8 9Bh: USB MaxPower (1 byte)

| Bit | Name | Description |
|-----|-------------|--|
| 7:0 | USB_MAX_PWR | USB Max Power per USB Specification (References). Do NOT set this value greater than 100 mA. |

7.4.2.9 9Ch-9Fh: Attribute Byte Descriptions

| Byte | Name | Bit Number | Description |
|------|---------|------------|---|
| 0 | ATT_LB | 3:0 | Always read as 0 |
| | | 4 | Inquire Manufacturer and Product ID Strings 1 : use the Inquiry Manufacturer and Product ID Strings. 0 : (default) - use the USB Descriptor Manufacturer and Product ID Strings. |
| | | 5 | Always read as 0 |
| | | 6 | Reverse SD Card Write Protect Sense 1 : (default) - SD cards will be write protected when SW_nWP is high, and writable when SW_nWP is low. 0 : SD cards will be write protected when SW_nWP is low, and writable when SW_nWP is high. |
| | | 7 | Always read as 0 |
| 1 | ATT_HLB | 3:0 | Always read as 0 |
| | | 4 | Activity LED True Polarity 1 : Activity LED to Low True 0 : (default) Activity LED polarity to High True |
| | | 5 | Common Media Insert/Media Activity LED 1 : the activity LED will function as a common media inserted/media access LED. 0 : (default) the activity LED will remain in its idle state until media is accessed. |
| | | 6 | Always read as 0 |
| 2 | ATT_LHB | 0 | Attach on Card Insert/Detach on Card Removal 1 : attach on Insert is enabled 0 : (default) - attach on Insert is disabled |
| | | 1 | Always read as 0 |
| | | 2 | Use LUN Power Configuration 1 : custom LUN Power Configuration stored in the NVSTORE is used 0 : (default) - default LUN Power Configuration is used. |
| | | 7:3 | Always read as 0 |
| 3 | ATT_HB | 7:0 | Always read as 0 |

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7.4.2.10 A0h-A3h: Reserved

| Byte | Name | Description |
|------|------|-------------|
| 3:0 | rsvd | |

7.4.2.11 A4h-A5h: LUN 0 Power Configuration

The USB2642 has one internal FET which can be utilized for card power. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.
2. The power limit is set to 200 mA default for the internal FET, but can be set to 100 mA.

Each media uses two bytes to store its LUN power configuration. Bit 3 selects between internal or external. For internal FETs bits 0 through 2 are used for the power limit. Only 2 of the possible 8 values are currently specified.

TABLE 7-4: FET CONFIGURATION

| FET | Type | Bits | Bit Type | Description |
|-----|-------------|------|-------------|--|
| 0 | FET Lo Byte | 3:0 | Low Nibble | rsvd |
| 1 | | 7:4 | High Nibble | |
| 2 | FET Hi Byte | 3:0 | Low Nibble | 0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit 1010b Internal FET with 200 mA power limit |
| 3 | | 7:4 | High Nibble | rsvd |

7.4.2.12 A6h-BEh: Reserved

| Byte | Name | Description |
|------|------|-------------|
| 25:0 | rsvd | |

7.4.3 DEVICE ID STRINGS

7.4.3.1 BFh-C5h: Device 3 Identifier String

| Byte | Name | Description |
|------|-------------|---|
| 6:0 | DEV3_ID_STR | These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the LUN to device mapping bytes in applications where the OEM wishes to reorder and rename the LUNs. If this device is configured to be part of a COMBO LUN then this string is ignored for the appropriate CLUNx_ID_STR . |

7.4.3.2 C6h-CDh: Inquiry Vendor String

| Byte | Name | Description |
|------|-------------|---|
| 7:0 | INQ_VEN_STR | If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings. |

7.4.3.3 CEh-D2h: Inquiry Product String

| Byte | Name | Description |
|------|-------------|---|
| 4:0 | INQ_PRD_STR | If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings. |

7.4.3.4 D3h: Dynamic Number of LUNs

| Bit | Name | Description |
|-----|-------------|---|
| 7:0 | DYN_NUM_LUN | This byte is used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to <code>FF</code> , the program assumes that you are using the default value and icons will be configured per the default configuration. |

7.4.3.5 D4h-D7h: LUN to Device Mapping

| Byte | Name | Description |
|------|-------------|--|
| 3:0 | LUN_DEV_MAP | These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to <code>FF</code> , the program assumes that you are using the default values and LUNs will be configured per the default configuration. |

7.4.3.6 D8h-DAh: Reserved

| Bit | Name | Description |
|-----|------|-------------|
| 2:0 | rsvd | |

7.4.3.7 DBh-DDh: SD/MMC Bus Timing Control

| Byte | Name | Description |
|------|-------------------|--|
| 2:0 | SD_MMC_BUS_TIMING | The values for these bytes are set internally and must not be altered. |

7.4.3.8 DEh: Vendor ID (LSB)

| Bit | Name | Description |
|-----|---------|---|
| 7:0 | VID_LSB | Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum). |

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7.4.3.9 DFh: Vendor ID (MSB)

| Bit | Name | Description |
|-----|---------|--|
| 7:0 | VID_MSB | Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum). |

7.4.3.10 E0h: Product ID (LSB)

| Bit | Name | Description |
|-----|---------|---|
| 7:0 | PID_LSB | Least Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product. |

7.4.3.11 E1h: Product ID (MSB)

| Bit | Name | Description |
|-----|---------|--|
| 7:0 | PID_MSB | Most Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product. |

7.4.3.12 E2h: Device ID (LSB)

| Bit | Name | Description |
|-----|---------|---|
| 7:0 | DID_LSB | Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD (binary coded decimal) format. |

7.4.3.13 E3h: Device ID (MSB)

| Bit | Name | Description |
|-----|---------|---|
| 7:0 | DID_MSB | Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format. |

7.4.3.14 E4h: Configuration Data Byte 1 (CFG_DAT_BYT1)

| Bit | Name | Description |
|-----|--------------|--|
| 7 | SELF_BUS_PWR | <p>Self- or Bus-Power: Selects between self- and bus-powered operation.</p> <p>The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller).</p> <p>When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated.</p> <p>When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current.</p> <p>0 : bus-powered operation 1 : self-powered operation</p> |
| 6 | rsvd | |
| 5 | HS_DISABLE | <p>Hi-Speed Disable: Disables the capability to attach as either a Hi-/Full-Speed device, and forces attachment as Full-Speed only (i.e., no Hi-Speed support).</p> <p>0 : Hi-/Full-Speed 1 : Full-Speed-Only (Hi-Speed disabled!)</p> |
| 4 | rsvd | |
| 3 | EOP_DISABLE | <p>EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode.</p> <p>During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification (References) for additional details.</p> <p>0 : An EOP is generated at the EOF1 point if no traffic is detected. 1 : EOP generation at EOF1 is disabled (normal USB operation).</p> <p>Generation of an EOP at the EOF1 point may prevent a host controller (operating in FS mode) from placing the USB bus in suspend.</p> |
| 2:1 | CURRENT_SNS | <p>Over-Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a per port or ganged basis is dependent upon the hardware implementation.</p> <p>00 : ganged sensing (all ports together) 01 : individual (port-by-port) 1x : over-current sensing is not supported (must only be used with bus-powered configurations)</p> |
| 0 | PORT_PWR | <p>Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is dependent upon the hardware implementation.</p> <p>0 : ganged switching (all ports together) 1 : individual port-by-port switching</p> |

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7.4.3.15 E5h: Configuration Data Byte 2 (CFG_DAT_BYT2)

| Bit | Name | Description |
|-----|----------|---|
| 7:6 | rsvd | |
| 5:4 | OC_TIMER | OverCurrent Timer: Over-current timer delay. 00 : 50 ns 01 : 100 ns 10 : 200 ns 11 : 400 ns |
| 3 | COMPOUND | Compound Device: Allows OEM to indicate that the hub is part of a compound device per the USB 2.0 Specification. The applicable port(s) must also be defined as having a "non-removable device". When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 : no 1 : yes, the hub is part of a compound device |
| 2:0 | rsvd | |

7.4.3.16 E6h: Configuration Data Byte 3 (CFG_DAT_BYT3)

| Bit | Name | Description |
|-----|-----------|---|
| 7:4 | rsvd | |
| 3 | PRTMAP_EN | Port Mapping Enable: Selects the method used by the hub to assign port numbers and disable ports. 0 : Standard Mode. Strap options or the following registers are used to define which ports are enabled, and the ports are mapped as port 'n' on the hub is reported as port 'n' to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. Register 300Ah: Port disable for self-powered operation (reset = 0x00). Register 300Bh: Port disable for bus-powered operation (reset = 0x00). 1 : PortMap mode. The mode enables remapping via the registers defined below. Register 30FBh: PortMap 12 (reset = 0x00) Register 30FCh: PortMap 3 (reset = 0x00) |
| 2:0 | rsvd | |

7.4.3.17 E7h: Non-Removable Device

| Bit | Name | Description |
|-----|-----------|--|
| 7:0 | NR_DEVICE | <p>Indicates which port(s) include non-removable devices.</p> <p>0 : port is removable 1 : port is non-removable</p> <p>Informs the host if one of the active ports has a permanent device that is undetachable from the hub. The device must provide its own descriptor data.</p> <p>When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable.</p> <p>Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = controls physical port 1 Bit 0 = rsvd</p> <p>Note: Bit 1 must be set to a 1 by the firmware for proper identification of the card reader as a non-removable device.</p> |

7.4.3.18 E8h: Port Disable For Self-Powered Operation

| Bit | Name | Description |
|-----|-------------|--|
| 7:0 | PORT_DIS_SP | <p>Disables 1 or more ports.</p> <p>0 : port is available 1 : port is disabled</p> <p>During self-powered operation this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order since the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function.</p> <p>Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = controls physical port 1 Bit 0 = rsvd</p> <p>Note: Bit 1 must be set to '0' in order for the card reader to enumerate.</p> |

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7.4.3.19 E9h: Port Disable For Bus-Powered Operation

| Bit | Name | Description |
|-----|-------------|---|
| 7:0 | PORT_DIS_BP | <p>Disables 1 or more ports.</p> <p>0 : port is available 1 : port is disabled</p> <p>During self-powered operation, this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function.</p> <p>When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports.</p> <p>Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = controls physical port 1 Bit 0 = rsvd</p> <p>Note: Bit 1 must be set to 0 in order for the card reader to enumerate.</p> |

7.4.3.20 EAh: Max Power For Self-Powered Operation

| Bit | Name | Description |
|-----|------------|--|
| 7:0 | MAX_PWR_SP | <p>Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.</p> <p>Note: The USB 2.0 Specification (References) does not permit this value to exceed 100 mA.</p> |

7.4.3.21 EBh: Max Power For Bus-Powered Operation

| Bit | Name | Description |
|-----|------------|--|
| 7:0 | MAX_PWR_BP | <p>Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.</p> <p>Note: The USB 2.0 Specification does not permit this value to exceed 100 mA.</p> |

7.4.3.22 ECh: Hub Controller Max Current For Self-Powered Operation

| Bit | Name | Description |
|-----|-------------|--|
| 7:0 | HC_MAX_C_SP | <p>Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.</p> <p>Note: The USB 2.0 Specification (References) does not permit this value to exceed 100 mA. A value of 50 (decimal) indicates 100 mA, which is the default value.</p> |

7.4.3.23 EDh: Hub Controller Max Current For Bus-Powered Operation

| Bit | Name | Description |
|-----|-------------|---|
| 7:0 | HC_MAX_C_BP | <p>Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.</p> <p>A value of 50 (decimal) would indicate 100 mA, which is the default value.</p> |

7.4.3.24 EEh: Power-On Time

| Bit | Name | Description |
|-----|---------------|---|
| 7:0 | POWER_ON_TIME | <p>The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is adequate on that port. If the host requests the power-on time, the system software uses this value to determine how long to wait before accessing a powered-on port.</p> |

7.4.3.25 EFh: Boost_Up

| Bit | Name | Description |
|-----|------------|---|
| 7:2 | rsvd | |
| 1:0 | BOOST_IOUT | <p>USB electrical signaling drive strength boost bit for the upstream port 'A'.</p> <p>00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost)</p> <p>Note: "Boost" could result in non-USB Compliant parameters. OEM should use a 00 value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.</p> |

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7.4.3.26 F0h: Boost_3:2

| Bit | Name | Description |
|-----|--------------|--|
| 7:6 | rsvd | |
| 5:4 | BOOST_IOUT_3 | Upstream USB electrical signaling drive strength boost bit for downstream port 3. 00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost) |
| 3:2 | BOOST_IOUT_2 | Upstream USB electrical signaling drive strength boost bit for downstream port 2. 00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost) “Boost” could result in non-USB Compliant parameters. OEM should use a 00 value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels. |
| 1:0 | rsvd | |

7.4.3.27 F1h: PortSwap

| Bit | Byte Name | Description |
|-----|-----------|---|
| 7:0 | PRT_SWP | Swaps the upstream and downstream USB DP and DM pins for ease of board routing to devices and connectors. 0 : USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. 1 : USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = rsvd Bit 0 = controls physical port 0 |

7.4.3.28 F2h: PortMap 12

| Bit | Byte Name | Description | | | | | | | | | | | | | | | | | | | | | | |
|--|--------------|--|-----------|------|-----------------------------|------|---|------|---|------|---|--------------|---------------------|-----------|------|-----------------------------|------|---|------|---|------|---|--------------|---------------------|
| 7:0 | PRTM12 | <p>PortMap Register for Ports 1 and 2</p> <p>When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.</p> <p>The host's port number is referred to as <i>logical port number</i> and the physical port on the hub is the <i>physical port number</i>. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).</p> <p>Note: The OEM must ensure that contiguous logical port numbers are used, starting from number 1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</p> | | | | | | | | | | | | | | | | | | | | | | |
| TABLE 7-5: PORTMAP REGISTER FOR PORTS 1 & 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1"> <tbody> <tr> <td rowspan="5">Bit [7:4]</td> <td>0000</td> <td>Physical port 2 is disabled</td> </tr> <tr> <td>0001</td> <td>Physical port 2 is mapped to Logical port 1</td> </tr> <tr> <td>0010</td> <td>Physical port 2 is mapped to Logical port 2</td> </tr> <tr> <td>0011</td> <td>Physical port 2 is mapped to Logical port 3</td> </tr> <tr> <td>0100 to 1111</td> <td>Illegal; Do not use</td> </tr> <tr> <td rowspan="5">Bit [3:0]</td> <td>0000</td> <td>Physical port 1 is disabled</td> </tr> <tr> <td>0001</td> <td>Physical port 1 is mapped to Logical port 1</td> </tr> <tr> <td>0010</td> <td>Physical port 1 is mapped to Logical port 2</td> </tr> <tr> <td>0011</td> <td>Physical port 1 is mapped to Logical port 3</td> </tr> <tr> <td>0100 to 1111</td> <td>Illegal; Do not use</td> </tr> </tbody> </table> | | | Bit [7:4] | 0000 | Physical port 2 is disabled | 0001 | Physical port 2 is mapped to Logical port 1 | 0010 | Physical port 2 is mapped to Logical port 2 | 0011 | Physical port 2 is mapped to Logical port 3 | 0100 to 1111 | Illegal; Do not use | Bit [3:0] | 0000 | Physical port 1 is disabled | 0001 | Physical port 1 is mapped to Logical port 1 | 0010 | Physical port 1 is mapped to Logical port 2 | 0011 | Physical port 1 is mapped to Logical port 3 | 0100 to 1111 | Illegal; Do not use |
| Bit [7:4] | 0000 | Physical port 2 is disabled | | | | | | | | | | | | | | | | | | | | | | |
| | 0001 | Physical port 2 is mapped to Logical port 1 | | | | | | | | | | | | | | | | | | | | | | |
| | 0010 | Physical port 2 is mapped to Logical port 2 | | | | | | | | | | | | | | | | | | | | | | |
| | 0011 | Physical port 2 is mapped to Logical port 3 | | | | | | | | | | | | | | | | | | | | | | |
| | 0100 to 1111 | Illegal; Do not use | | | | | | | | | | | | | | | | | | | | | | |
| Bit [3:0] | 0000 | Physical port 1 is disabled | | | | | | | | | | | | | | | | | | | | | | |
| | 0001 | Physical port 1 is mapped to Logical port 1 | | | | | | | | | | | | | | | | | | | | | | |
| | 0010 | Physical port 1 is mapped to Logical port 2 | | | | | | | | | | | | | | | | | | | | | | |
| | 0011 | Physical port 1 is mapped to Logical port 3 | | | | | | | | | | | | | | | | | | | | | | |
| | 0100 to 1111 | Illegal; Do not use | | | | | | | | | | | | | | | | | | | | | | |

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7.4.3.29 F3h: PortMap 3

| Bit | Byte Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|--------------|--|-----------|-------|-------------|-----------|------|------|------|------|------|------|------|------|--------------|---------------------|-----------|------|-----------------------------|------|---|------|---|------|---|--------------|---------------------|
| 7:0 | PRTM3 | <p>PortMap Register for Port 3.</p> <p>When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.</p> <p>The host's port number is referred to as <i>logical port number</i> and the physical port on the hub is the <i>physical port number</i>. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).</p> <p>Note: The OEM must ensure that contiguous logical port numbers are used, starting from number 1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</p> | | | | | | | | | | | | | | | | | | | | | | | | | |
| <p>TABLE 7-6: PORTMAP REGISTER FOR PORT 3</p> <table border="1"> <thead> <tr> <th>Bit [7:4]</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td rowspan="5">Bit [7:4]</td> <td>0000</td> <td>rsvd</td> </tr> <tr> <td>0001</td> <td>rsvd</td> </tr> <tr> <td>0010</td> <td>rsvd</td> </tr> <tr> <td>0011</td> <td>rsvd</td> </tr> <tr> <td>0100 to 1111</td> <td>Illegal; Do not use</td> </tr> <tr> <td rowspan="5">Bit [3:0]</td> <td>0000</td> <td>Physical port 3 is disabled</td> </tr> <tr> <td>0001</td> <td>Physical port 3 is mapped to Logical port 1</td> </tr> <tr> <td>0010</td> <td>Physical port 3 is mapped to Logical port 2</td> </tr> <tr> <td>0011</td> <td>Physical port 3 is mapped to Logical port 3</td> </tr> <tr> <td>0100 to 1111</td> <td>Illegal; Do not use</td> </tr> </tbody> </table> | | | Bit [7:4] | Value | Description | Bit [7:4] | 0000 | rsvd | 0001 | rsvd | 0010 | rsvd | 0011 | rsvd | 0100 to 1111 | Illegal; Do not use | Bit [3:0] | 0000 | Physical port 3 is disabled | 0001 | Physical port 3 is mapped to Logical port 1 | 0010 | Physical port 3 is mapped to Logical port 2 | 0011 | Physical port 3 is mapped to Logical port 3 | 0100 to 1111 | Illegal; Do not use |
| Bit [7:4] | Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | |
| Bit [7:4] | 0000 | rsvd | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0001 | rsvd | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0010 | rsvd | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0011 | rsvd | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0100 to 1111 | Illegal; Do not use | | | | | | | | | | | | | | | | | | | | | | | | | |
| Bit [3:0] | 0000 | Physical port 3 is disabled | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0001 | Physical port 3 is mapped to Logical port 1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0010 | Physical port 3 is mapped to Logical port 2 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0011 | Physical port 3 is mapped to Logical port 3 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0100 to 1111 | Illegal; Do not use | | | | | | | | | | | | | | | | | | | | | | | | | |

7.4.3.30 F4h: SD Clock Limit for the Flash Media Controller

| Byte Name | Type | Bits | Description |
|------------|-------------------|------|--|
| SD_CLK_LIM | Upper Nibble Bits | 7:4 | 0 : SD/MMC - 48 MHz 1 : SD/MMC - 24 MHz 2 : SD/MMC - 20 MHz 3 : SD/MMC - 15 MHz |
| | Lower Nibble Bits | 3:0 | rsvd |

7.4.3.31 F5h: Reserved

| Bit | Name | Description |
|-----|------|-------------|
| 7:0 | rsvd | |

7.4.3.32 F6h: SD1/2 Timeout Options

| Bit | Name | Description |
|-----|----------------|--|
| 7:0 | MEDIA_SETTINGS | <p>The SD1 and SD2 Timeout Options:</p> <p>Bit 0 : rsvd Bit 1 : rsvd Bits 2-4 : SD1 timeout Bits 5-7 : rsvd</p> <p>A value of 001b equates to a timeout of 0.81 seconds, where 010b indicates an additional 0.81 seconds for a total of 1.62, and so on. The maximum value is 000b (default), which indicates a total timeout of 6.5 seconds.</p> |

7.4.3.33 F7h-FBh: Reserved

| Bit | Byte Name | Description |
|-----|-----------|-------------|
| 7:0 | rsvd | |

7.4.3.34 FCh-FFh: Non-Volatile Storage Signature

| Byte | Name | Description |
|------|-------------|--|
| 4:0 | NVSTORE_SIG | This signature is used to verify the validity of the data in the first 256 bytes of the configuration area. The signature must be set to ATA2. |

7.4.4 INTERNAL FLASH MEDIA CONTROLLER EXTENDED CONFIGURATIONS

Enable Registers 100h - 17Fh by setting bit 7 of bmAttribute.

7.4.4.1 100h-106h: Combo LUN 0 Identifier String

| Byte | Name | Description |
|------|--------------|--|
| 6:0 | CLUN0_ID_STR | If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings. |

7.4.4.2 107h-10Dh: Combo LUN 1 Identifier String

| Byte | Name | Description |
|------|--------------|--|
| 6:0 | CLUN1_ID_STR | If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings. |

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7.4.4.3 10Eh-114h: Combo LUN 2 Identifier String

| Byte | Name | Description |
|------|--------------|--|
| 6:0 | CLUN2_ID_STR | If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings. |

7.4.4.4 115h-11Bh: Combo LUN 3 Identifier String

| Byte | Name | Description |
|------|--------------|--|
| 6:0 | CLUN3_ID_STR | If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings. |

7.4.4.5 11Ch-122h: Combo LUN 4 Identifier String

| Byte | Name | Description |
|------|--------------|--|
| 6:0 | CLUN4_ID_STR | If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings. |

7.4.4.6 123h-145h: Reserved

| Byte | Name | Description |
|------|------|-------------|
| 27:0 | rsvd | |

7.4.4.7 146h: Dynamic Number of Extended LUNs

| Bit | Name | Description |
|-----|-----------------|---|
| 7:0 | DYN_NUM_EXT_LUN | <p>These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces.</p> <p>If this field is set to FF, the program assumes that you are using the default value and icons will be configured per the default configuration.</p> |

7.4.4.8 147h-14Bh: LUN to Device Mapping

| Byte | Name | Description |
|------|-------------|---|
| 4:0 | LUN_DEV_MAP | <p>These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces.</p> <p>If this field is set to FF, the program assumes that you are using the default value and icons will be configured per the default configuration.</p> |

7.4.4.9 14Eh-17Bh: Reserved

| Byte | Name | Description |
|------|------|-------------|
| 45:0 | rsvd | |

7.4.4.10 17Ch -17Fh: Non-Volatile Storage Signature for Extended Configuration

| Byte | Name | Description |
|------|--------------|--|
| 3:0 | NVSTORE_SIG2 | This signature is used to verify the validity of the data in the upper 256 bytes if a 512-byte EEPROM is used, otherwise this bank is a read-only configuration area. The signature must be set to <code>ecf1</code> . |

7.4.5 I²C EEPROM

The I²C EEPROM interface implements a subset of the I²C Master Specification (refer to the Philips Semiconductor Standard I²C-Bus Specification ([References](#)) for details on I²C bus protocols). The device's I²C EEPROM interface is designed to attach to a single dedicated I²C EEPROM, and it conforms to the Standard-mode I²C Specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

Note: Extensions to the I²C Specification are not supported. The device acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

7.4.5.1 Implementation Characteristics

The device will only access an EEPROM using the sequential read protocol.

7.4.5.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the **SPI_DO/SDA_EP/SPI_SPD_SEL** and **SPI_CLK/SCL_EP** lines (per SMBus 1.0 Specification ([References](#)) and EEPROM manufacturer guidelines) to VDD33 in order to assure proper operation.

7.4.5.3 I²C EEPROM Slave Address

Slave address is 1010000b. 10-bit addressing is NOT supported.

7.4.6 IN-CIRCUIT EEPROM PROGRAMMING

The EEPROM can be programmed via automatic test equipment (ATE) by pulling **RESET_N** low which tri-states the device's EEPROM interface and allows an external source to program the EEPROM.

7.5 Default Configuration Option

The Microchip device can be configured via its internal default configuration. Please see [Section 7.4.2, "EEPROM Data Descriptor"](#) for specific details on how to enable default configuration. Please refer to [Table 7-1](#) for the internal default values that are loaded when this option is selected.

7.6 Reset

There are two different resets that the device experiences. One is a hardware reset (either from the internal POR (power-on reset) circuit or via the **RESET_N** pin) and the second is a USB bus reset.

7.6.1 EXTERNAL HARDWARE RESET_N

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 μs after all power supplies are within operating range. While reset is asserted, the device (and its associated external circuitry) consumes less than IRST μA of current from the upstream USB power source.

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Assertion of **RESET_N** (external pin) causes the following:

1. All downstream ports are disabled, and PRTCTL power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.

7.6.1.1 RESET_N for EEPROM Configuration

FIGURE 7-1: RESET_N TIMING FOR EEPROM MODE

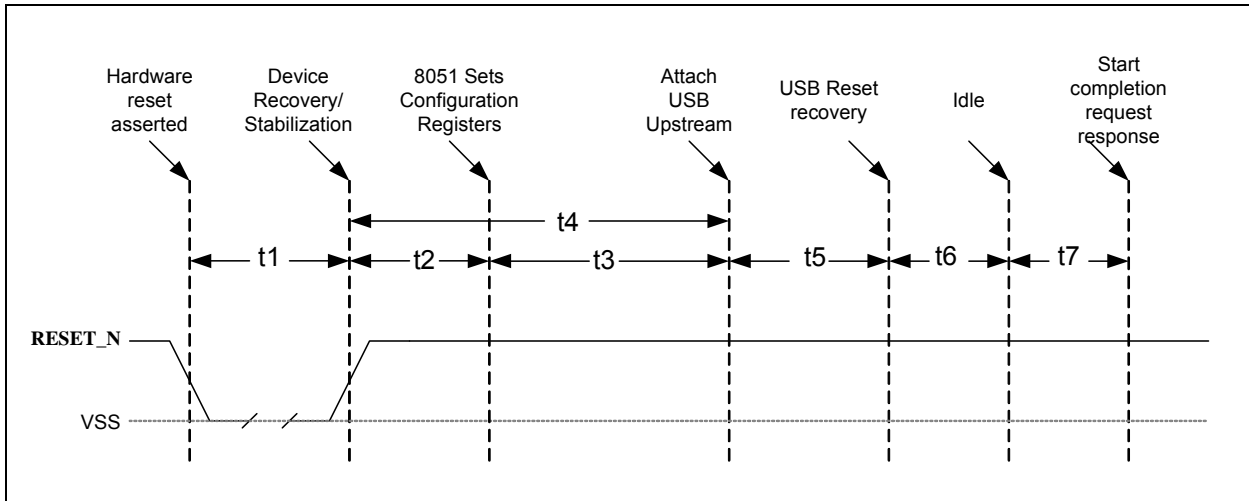


TABLE 7-7: RESET_N TIMING FOR EEPROM MODE

| Name | Description | Min | Typ | Max | Units |
|------|---|-----|-----------|-----|-------|
| t1 | RESET_N asserted | 1 | - | - | μsec |
| t2 | Device recovery/stabilization | - | - | 500 | μsec |
| t3 | 8051 programs device configuration | - | 20 | 50 | msec |
| t4 | USB attach (see Note 7-1) | - | - | 100 | msec |
| t5 | Host acknowledges attach and signals USB reset | 100 | - | - | msec |
| t6 | USB idle | - | Undefined | - | msec |
| t7 | Completion time for requests (with or without data stage) | - | - | 5 | msec |

Note 7-1 All power supplies must have reached the operating levels mandated in [Section 8.0, "DC Parameters"](#), prior to (or coincident with) the assertion of **RESET_N**.

7.6.2 USB BUS RESET

In response to the upstream port signaling a reset, the hub does the following:

Note: The hub does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0
2. Sets configuration to: unconfigured
3. Negates **PRTCTL[3:2]** to all downstream ports
4. Clears all TT buffers
5. Moves device from suspended to active (if suspended)
6. Complies with Section 11.10 of the *USB 2.0 Specification* ([References](#)) for behavior after completion of the reset sequence.

The host then configures the hub and the device's downstream port devices in accordance with the USB Specification.

8.0 DC PARAMETERS

8.1 Maximum Guaranteed Ratings

| Parameter | Symbol | Min | Max | Units | Comments |
|---------------------------|-------------------------------------|------|-------------------------|-------|--|
| Storage Temperature | T_{STOR} | -55 | 150 | °C | |
| 3.3 V supply voltage | $V_{\text{DD33}}, V_{\text{DDA33}}$ | -0.5 | 4.0 | V | |
| Voltage on CRD_PWD | - | -0.5 | $V_{\text{DD33}} + 0.3$ | V | When internal power FET operation of these pins are enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63 V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63 V and T_A is less than 70°C. |
| Voltage on any signal pin | - | -0.5 | $V_{\text{DD33}} + 0.3$ | V | |
| Voltage on XTAL1 | - | -0.5 | 3.6 | V | |

Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies the absolute maximum ratings must not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, a clamp circuit should be used.

8.2 Operating Conditions

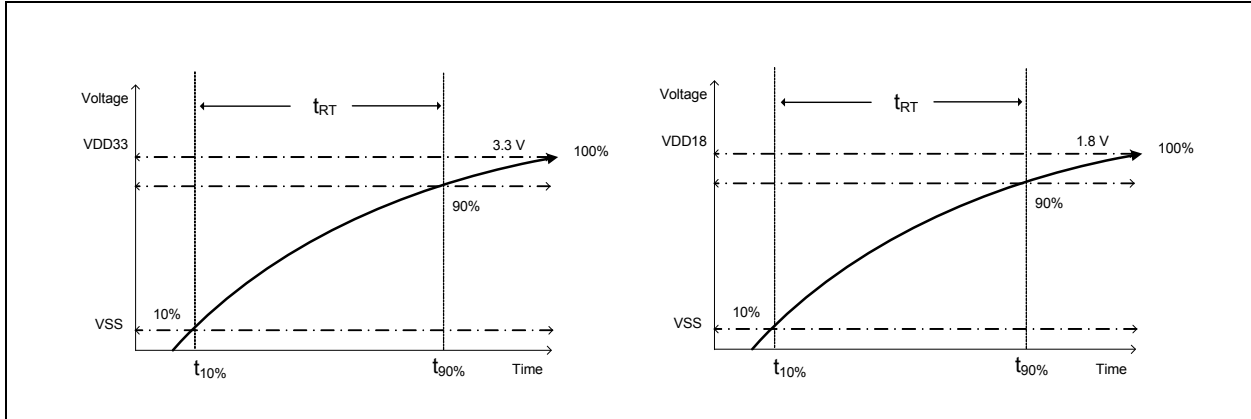
| Parameter | Symbol | Min | Max | Units | Comments |
|---------------------------|-------------------------------------|--------|-------------------|---------------|---|
| Operating Temperature | T_A | Note 1 | Note 2 | °C | Ambient temperature in still air. (See Note 3) |
| 3.3 V supply voltage | $V_{\text{DD33}}, V_{\text{DDA33}}$ | 3.0 | 3.6 | V | A 3.3 V regulator with an output tolerance of $\pm 1\%$ must be used if the output of the internal power FET's must support a 5% tolerance. |
| 3.3 V supply rise time | t_{RT} | 0 | 400 | μs | (Figure 8-1) |
| 1.8 V supply rise time | t_{RT} | 0 | 400 | μs | (Figure 8-1) |
| Voltage on any signal pin | - | -0.3 | V_{DD33} | V | |
| Voltage on XTAL1 | - | -0.3 | 2.0 | V | |

Note 1: 0°C for commercial version, -40°C for industrial version.

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- 2: +70°C for commercial version, +85°C for industrial version.
- 3: The T_J (junction temperature) must not exceed 125°C.
- 4: The 3.3 V supply should be at least at 75% of its operating condition before the 1.8 V supply is allowed to ramp up.

FIGURE 8-1: SUPPLY RISE TIME MODELS



8.3 Package Thermal Specifications

TABLE 8-1: 48-PIN QFN PACKAGE THERMAL PARAMETERS

| Parameter | Symbol | Value | Unit | Comments |
|----------------------------|---------------|-------|------|--|
| Thermal Resistance | Θ_{JA} | 28 | °C/W | Measured from the die to the ambient air |
| Junction-to-Top-of-Package | Ψ_{JT} | 0.2 | °C/W | - |

8.4 DC Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Comments |
|--------------------------------------|-----------|-----|-----|-----|-------|--|
| I, IPU, IPD Type Input Buffer | | | | | | |
| Low Input Level | V_{ILI} | | | 0.8 | V | See Note 11 for I buffer TTL Levels |
| High Input Level | V_{IHI} | 2.0 | | | V | |
| Pull Down | PD | | 72 | | μA | |
| Pull Up | PU | | 58 | | μA | |
| IS Type Input Buffer | | | | | | |
| Low Input Level | V_{ILI} | | | 0.8 | V | TTL Levels |
| High Input Level | V_{IHI} | 2.0 | | | V | |

| Parameter | Symbol | Min | Typ | Max | Units | Comments |
|---|------------|------------------|-----|-----|----------|---------------------------------------|
| ICLK Input Buffer | | | | | | |
| Low Input Level | V_{ILCK} | | | 0.5 | V | |
| High Input Level | V_{IHCK} | 1.4 | | | V | |
| Input Leakage | I_{IL} | -10 | | +10 | μ A | $V_{IN} = 0$ to V_{DD33} |
| Input Leakage (All I and IS buffers) | | | | | | |
| Low Input Leakage | I_{IL} | -10 | | +10 | μ A | $V_{IN} = 0$ V |
| High Input Leakage | I_{IH} | -10 | | +10 | μ A | $V_{IN} = V_{DD33}$ |
| O12 Type Buffer | | | | | | |
| Low Output Level | V_{OL} | | | 0.4 | V | $I_{OL} = 6$ mA @ $V_{DD33} = 3.3$ V |
| High Output Level | V_{OH} | $V_{DD33} - 0.4$ | | | V | $I_{OH} = -6$ mA @ $V_{DD33} = 3.3$ V |
| Output Leakage | I_{OL} | -10 | | +10 | μ A | $V_{IN} = 0$ to V_{DD33} (Note 5) |
| I/O12, I/O12PU & I/O12PD Type Buffer | | | | | | |
| Low Output Level | V_{OL} | | | 0.4 | V | $I_{OL} = 6$ mA @ $V_{DD33} = 3.3$ V |
| High Output Level | V_{OH} | $V_{DD33} - 0.4$ | | | V | $I_{OH} = -6$ mA @ $V_{DD33} = 3.3$ V |
| Output Leakage | I_{OL} | -10 | | +10 | μ A | $V_{IN} = 0$ to V_{DD33} (Note 5) |
| Pull Down | PD | | 72 | | μ A | |
| Pull Up | PU | | 58 | | μ A | |
| IO-U | | | | | | |
| | | | | | | (Note 6) |
| I-R | | | | | | |
| | | | | | | (Note 7) |
| Integrated Power FET set to 200 mA | | | | | | |
| Output Current (8:) | I_{OUT} | | 200 | | mA | $V_{dropFET} \approx 0.46$ V |
| Short Circuit Current Limit | I_{SC} | | 181 | | mA | $V_{outFET} = 0$ V |
| On Resistance (8:) | R_{DSON} | | | 2.1 | Ω | $I_{FET} = 70$ mA |
| Output Voltage Rise Time | t_{DSON} | | 800 | | μ s | $C_{LOAD} = 10$ μ F |

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| Parameter | Symbol | Min | Typ | Max | Units | Comments |
|---|----------------|-----|-----|------|---------|----------|
| Supply Current Unconfigured | | | | | | Note 9 |
| Hi-Speed Host | $I_{CCINTHS}$ | - | - | 75 | mA | |
| Full Speed Host | $I_{CCINITFS}$ | - | - | 70 | mA | |
| Supply Current Active HS Host (Note 10) | I_{CC} | - | - | 330 | mA | |
| Supply Current Suspend | I_{CSBY} | - | - | 2500 | μ A | |
| Supply Current Reset | I_{RST} | - | - | 2500 | μ A | |

5: Output leakage is measured with the current pins in high impedance.

6: See the *USB 2.0 Specification*, Chapter 7, for USB DC electrical characteristics

7: RBIAS is a 3.3 V tolerant analog pin.

8: Output current range is controlled by program software. The software disables the FET during short circuit condition.

9: Supply currents do not include power FET currents.

10: HS Host, 2 ports active.

11: Noise on the RESET_N signal can affect the startup, a clean 100us rise time is recommended for consistent startup.

8.5 Capacitance

$T_A = 25^\circ\text{C}$; $f_c = 1\text{ MHz}$; $V_{DD33} = 3.3\text{ V}$, $V_{DD18} = 1.8\text{ V}$

TABLE 8-2: PIN CAPACITANCE

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|----------------------------|------------|--------|-----|-----|------|---|
| | | Min | Typ | Max | | |
| XTAL Pin Input Capacitance | C_{XTAL} | - | - | 4 | pF | All pins (except USB pins and pins under test) are tied to AC ground. |
| Input Capacitance | C_{IN} | - | - | 10 | pF | |

9.0 AC SPECIFICATIONS

9.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

FIGURE 9-1: TYPICAL CRYSTAL CIRCUIT

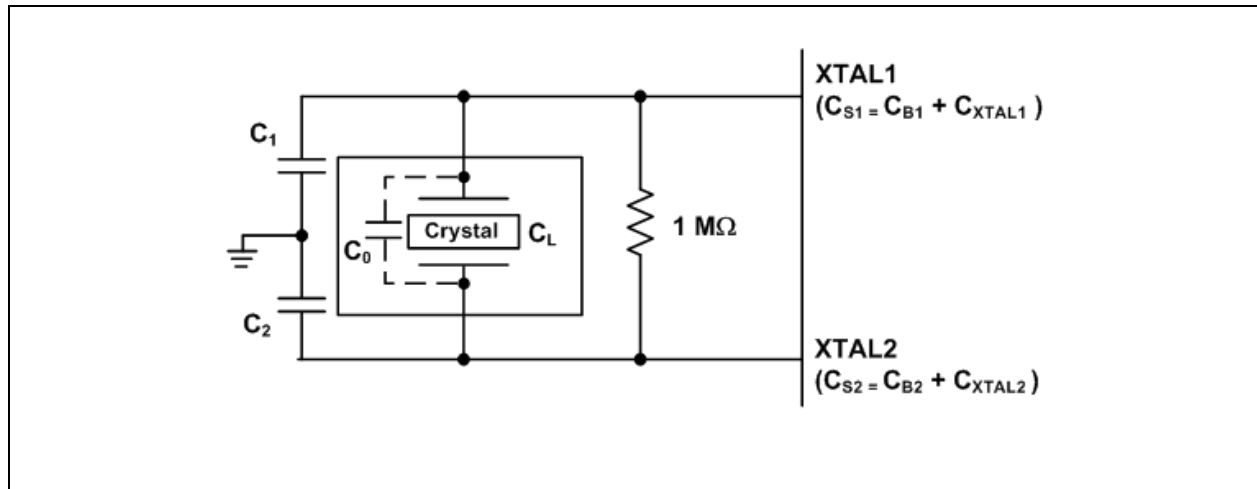


TABLE 9-1: CRYSTAL CIRCUIT LEGEND

| Symbol | Description | In Accordance with |
|------------|--|---|
| C_0 | Crystal shunt capacitance | Crystal manufacturer's specification (see Note 9-1) |
| C_L | Crystal load capacitance | |
| C_B | Total board or trace capacitance | OEM board design |
| C_S | Stray capacitance | Microchip IC and OEM board design |
| C_{XTAL} | XTAL pin input capacitance | Microchip IC |
| C_1 | Load capacitors installed on OEM board | Calculated values based on Figure 9-2 (see Note 9-2) |
| C_2 | | |

FIGURE 9-2: CAPACITANCE FORMULAS

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Note 9-1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to '0' for use in the calculation of the capacitance formulas in [Figure 9-2](#). However, the OEM PCB itself may present a parasitic capacitance between XTAL1 and XTAL2. For an accurate calculation of C_1 and C_2 , take the parasitic capacitance between traces XTAL1 and XTAL2 into account.

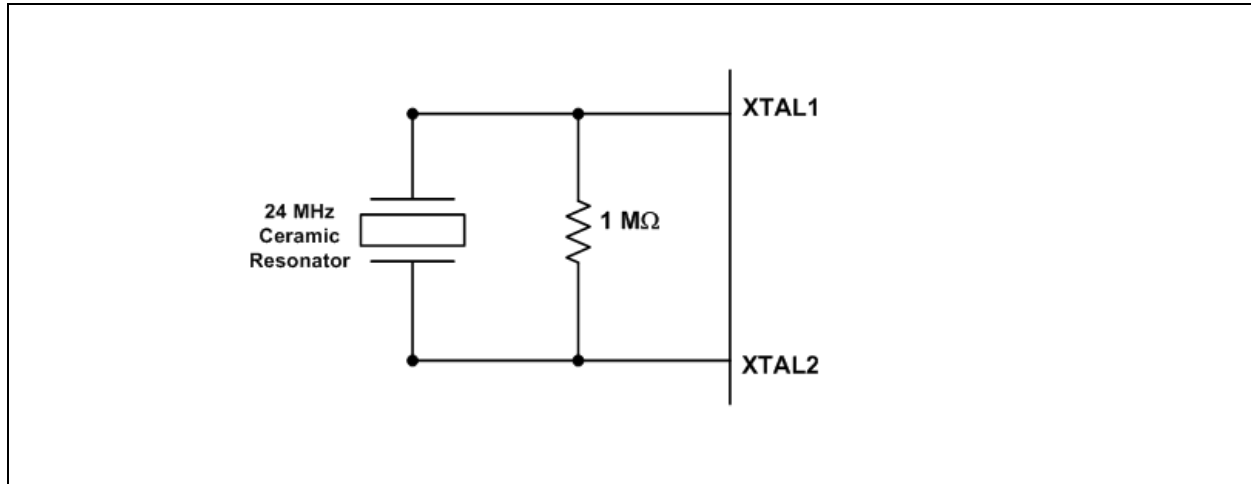
Note 9-2 Each of these capacitance values is typically approximately 18 pF.

USB2642

9.2 Ceramic Resonator

24 MHz \pm 350 ppm

FIGURE 9-3: CERAMIC RESONATOR USAGE WITH MICROCHIP IC



9.3 External Clock

50% Duty cycle \pm 10%, 24 MHz \pm 350 ppm, Jitter < 100 ps rms

The external clock is recommended to conform to the signaling level designated in the *JESD76-2 Specification* ([References](#)) on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect.

9.3.1 I²C EEPROM

Frequency is fixed at 58.6 kHz \pm 20%.

9.3.2 USB 2.0

The Microchip device conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* ([References](#)).

10.0 PACKAGE OUTLINES

FIGURE 10-1: USB2642 48-PIN QFN

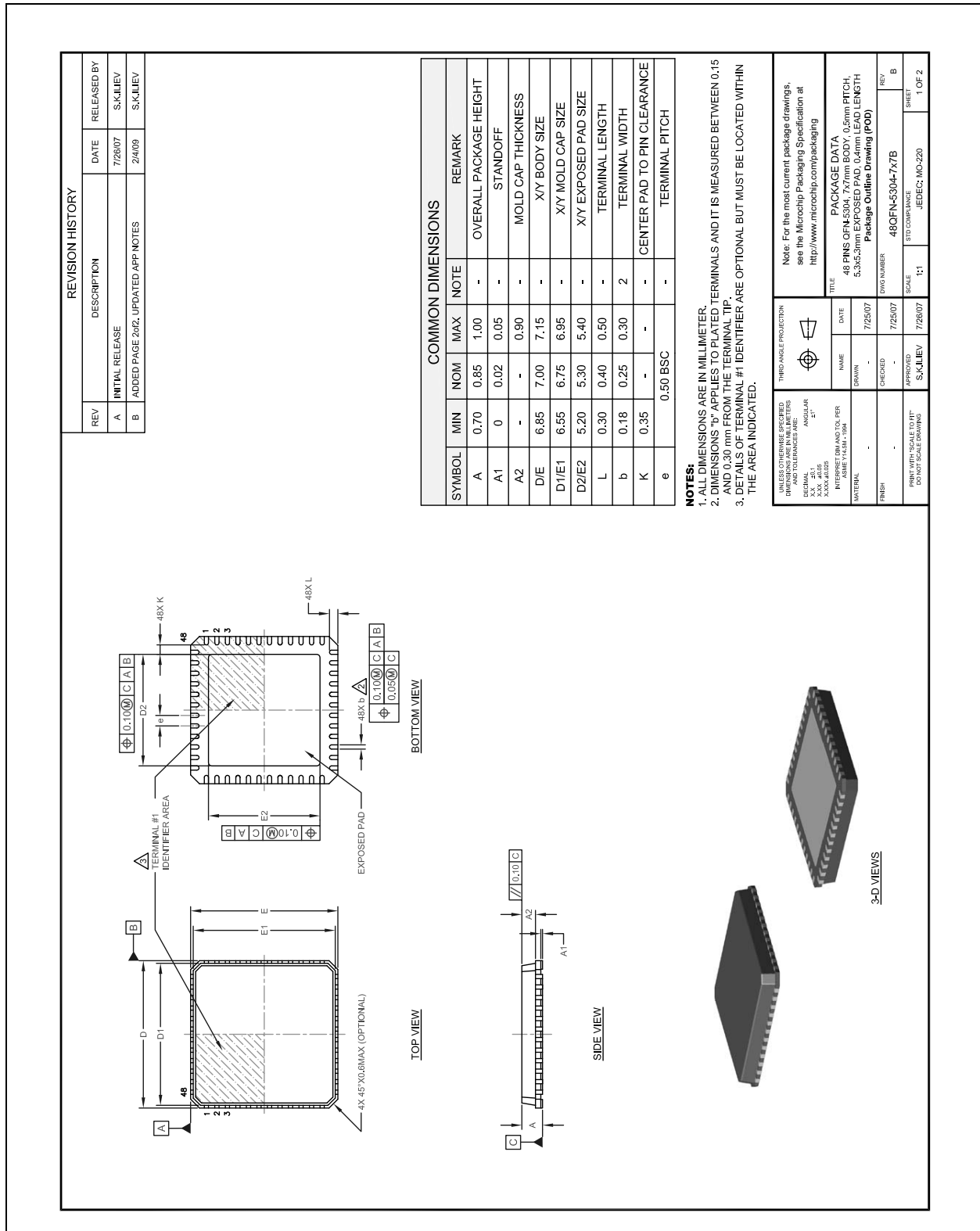
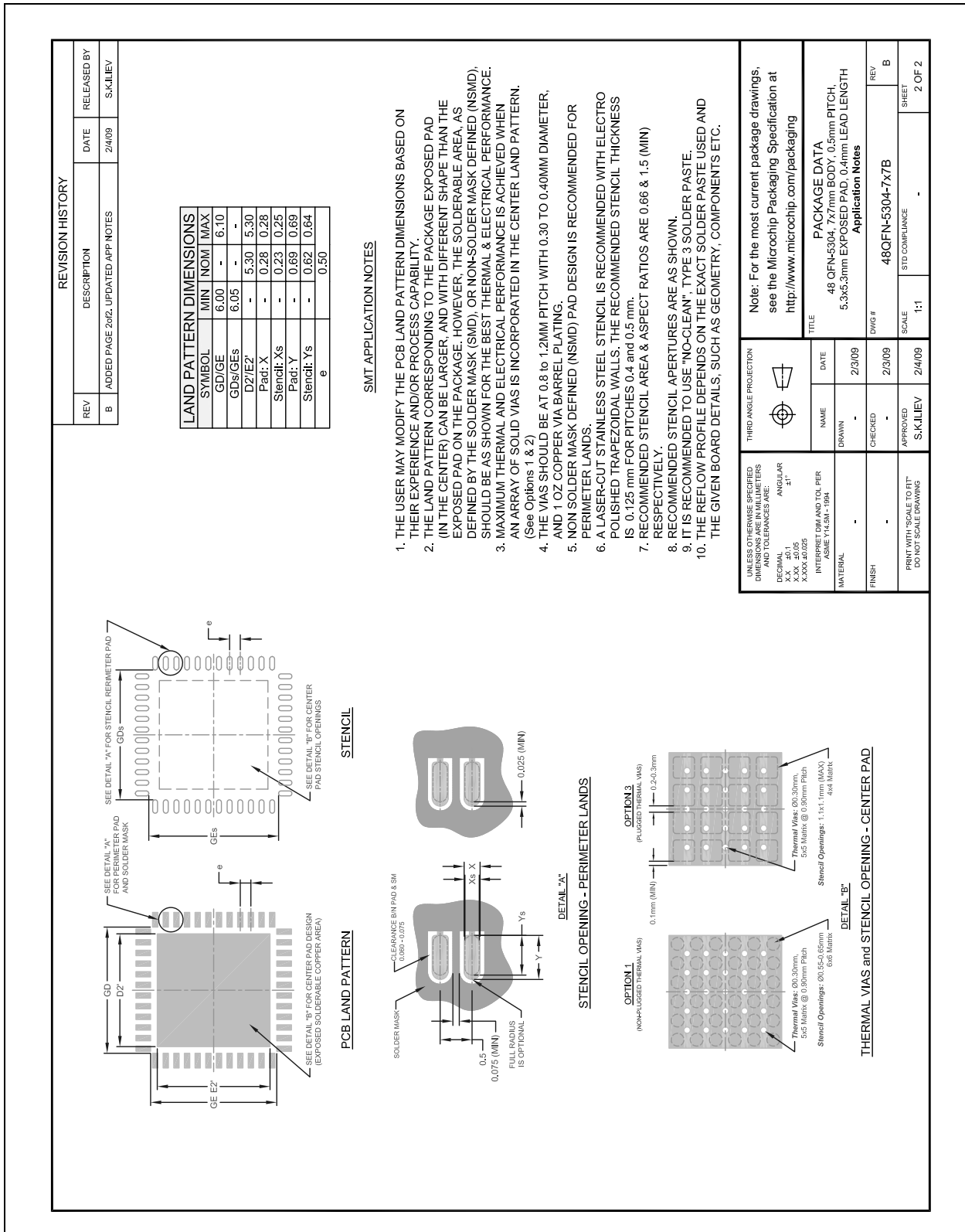


FIGURE 10-2: USB2642 LANDING PATTERN



11.0 REVISION HISTORY

TABLE 11-1: REVISION HISTORY

| Revision | Section/Figure/Entry | Correction |
|---------------------------|--|--|
| DS00001578C (03-19-15) | All | Removed misleading reference to SDIO support |
| | Section 8.4, DC Electrical Characteristics | Added Note 11 regarding I Buffer |
| DS00001578C (03-13-15) | Table 5-1, "USB2642 Pin Descriptions" | Changed Buffer type from "IS" to "I" for RESET_N |
| | Product Identification System | Changed ordering code example "d" from: USB2642T-I/ML, Tape & reel, Industrial temp., 48-pin QFN to: USB2642T-I/ML-SEU, Tape & reel, Industrial temp., 48-pin QFN, Low Alpha Emissions package |
| | Worldwide Sales and Service | Updated Worldwide Sales Listing page |
| DS00001578B | Conversion to MCHP template | |
| DS00001578A | DS00001578A replaces the previous SMSC version, Revision 1.1 | |

APPENDIX A: ACRONYMS

| Acronym | Description |
|-------------------|---------------------------|
| EOF | End of (micro) Frame |
| EOP | End of Packet |
| FMC | Flash Media Controller |
| FS | USB Full-Speed |
| HS | USB Hi-Speed |
| I ² C™ | Inter-Integrated Circuit |
| LS | USB Low-Speed |
| LUN | Logical Unit Number |
| MMC | MultiMediaCard |
| OCS | Over-current Sense |
| PHY | Physical Layer |
| PLL | Phase-Locked Loop |
| SDC | Secure Digital Controller |

I²C is a trademark of Philips Corporation.

APPENDIX B: REFERENCES

- [1] Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)
USB Implementers Forum, Inc. <http://www.usb.org>
- [2] USB Mass Storage Class Specification Overview Rev 1.2
<http://www.usb.org>
- [3] USB Mass Storage Class Bulk-Only Transport Rev 1.0
<http://www.usb.org>
- [4] SCSI Architecture Model - 2 (SAM-2) and (SPC-2)
<http://www.t10.org>
- [5] SD Specifications Part 1 Physical Layer Specification Version 2.00
<http://www.sdcard.org>
- [6] SD Specifications Part A2 SD Host Controller Standard Specification Version 2.00
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- [7] I²C-Bus Specification Version 1.1
NXP (formerly a division of Philips). <http://www.nxp.com>
- [8] System Management Bus Specification, version 1.0
SMBus. <http://smbus.org/specs/>
- [9] MicroChip 24AA02/24LC02B (Revision C)
Microchip Technology Inc. <http://www.microchip.com/>
- [10] JEDEC Specifications: JESD76-2 (June 2001) and J-STD-020D.1 (March 2008)
JEDEC Global Standards for the Microelectronics Industry. <http://www.jedec.org/standards-documents>

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| <u>PART NO.</u> | <u>[XI]⁽¹⁾</u> | - | <u>XX</u> | / | <u>[XX]</u> | - | <u>XXX</u> |
|---|---------------------------|---|--|---|--------------|---|--------------------|
| Device | Tape and Reel Option | | Temperature Range | | Package | | Special (Optional) |
| Device: | USB2642 | | | | | | |
| Tape and Reel Option: | Blank | = | Standard packaging (tray) | | | | |
| | T | = | Tape and Reel ⁽¹⁾ | | | | |
| Temperature Range: | Blank | = | 0°C to +70°C | | (Commercial) | | |
| | I | = | -40°C to +85°C | | (Industrial) | | |
| Package: | ML | = | 48-pin QFN | | | | |
| Special: | SEU | = | Single Event Upset (Low Alpha Emissions Package) | | | | |
| Examples: | | | | | | | |
| a) USB2642/ML Tray, Commercial temp., 48-pin QFN | | | | | | | |
| b) USB2642-I/ML Tray, Industrial temp., 48-pin QFN | | | | | | | |
| c) USB2642T/ML Tape & reel, Commercial temp., 48-pin QFN | | | | | | | |
| d) USB2642T-I/ML-SEU Tape & reel, Industrial temp., 48-pin QFN, Low Alpha Emissions Package | | | | | | | |
| Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. | | | | | | | |

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