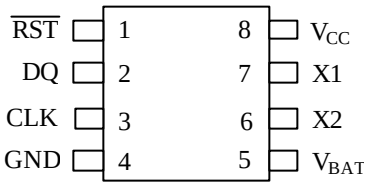
DS1602
Elapsed Time Counter

www.maxim-ic.com

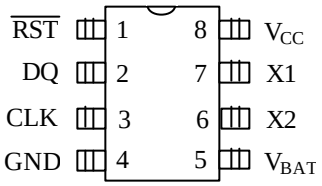
FEATURES

- Two 32-bit counters keep track of real-time and elapsed time
- Counters keep track of seconds for over 125 years
- Battery powered counter counts seconds from the time battery is attached until V_{BAT} is less than 2.5V
- V_{CC} powered counter counts seconds while V_{CC} is above V_{TP} and retains the count in the absence of V_{CC} under battery backup power
- Clear function resets selected counter to 0
- Read/write serial port affords low pin count
- Maximum current drain of less than 1 µA from V_{BAT} pin when serial port is disabled
- One byte protocol defines read/write, counter address and software clear function
- 8-pin DIP or optional 8-pin SOIC
- Operating temperature range of -40°C to +85°C
- Reduced performance operation down to V_{CC} = 2.5V
- Underwriters Laboratory (UL) recognized

PIN ASSIGNMENT



DS1602
8-Pin DIP (300mil)



DS1602
8-Pin SOIC (208mil)

Package Dimension Information

www.maxim-ic.com/TechSupport/DallasPackInfo.htm

PIN DESCRIPTION

$\overline{RST}$	- Reset
CLK	- Clock
DQ	- Data Input/Output
GND	- Ground
X1, X2	- Crystal Inputs
V_{BAT}	- + Battery Input
V_{CC}	- +5V

DESCRIPTION

The DS1602 is a real-time clock/elapsed time counter designed to count seconds when V_{CC} power is applied and continually count seconds under battery backup power with an additional counter regardless of the condition of V_{CC}. The continuous counter can be used to derive time of day, week, month, and year by using a software algorithm. The V_{CC} powered counter will automatically record the amount of time that V_{CC} power is applied. This function is particularly useful in determining the operational time of equipment in which the DS1602 is used. Alternatively, this counter can also be used under software control to record real-time events. Communication to and from the DS1602 takes place via a 3-wire serial port. A 1-byte protocol selects read/ write functions, counter clear functions and oscillator trim. A low cost 32.768kHz crystal attaches directly to the X1 and X2 pins. If battery powered-only operation is desired, the V_{BAT} pin must be grounded and the V_{CC} pin must be connected to the battery.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

OPERATION

The main elements of the DS1602 are shown in Figure 1. As shown, communications to and from the elapsed time counter occur over a 3-wire serial port. The port is activated by driving $\overline{RST}$ to a high state. With $\overline{RST}$ at high level, 8 bits are loaded into the protocol shift register providing read/write, register select, register clear, and oscillator trim information. Each bit is serially input on the rising edge of the clock input. After the first eight clock cycles have loaded the protocol register with a valid protocol, additional clocks will output data for a read or input data for a write. V_{CC} must be present to access the DS1602. If $V_{CC} < V_{TP}$, the DS1602 goes into a battery backup mode which disables the serial port to conserve battery capacity. For battery only operations, the V_{BAT} pin must be grounded and the V_{CC} pin must be connected to the battery. This will keep the DS1602 out of battery backup mode. Battery powered operation down to 2.5V is possible with reduced speed performance on the serial port. The 32-bit continuous counter always runs provided that a valid supply is present and the oscillator is enabled. The 32-bit V_{CC} active counter is gated by V_{CC} and the internal 1Hz signal.

PROTOCOL REGISTER

The protocol bit definition is shown in Figure 2. Valid protocols and the resulting actions are shown in Table 1. Each data transfer to the protocol register designates what action is to occur. As defined, the MSB (bit 7 which is designated ACC) selects the 32-bit continuous counter for access. If ACC is a logical 1 the continuous counter is selected and the 32 clock cycles that follow the protocol will either read or write this counter. If the counter is being read, the contents will be latched into a different register at the end of protocol and the latched contents will be read out on the next 32 clock cycles. This avoids reading garbled data if the counter is clocked by the oscillator during a read. Similarly, if the counter is to be written, the data is buffered in a register and all 32 bits are jammed into the counter simultaneously on the rising edge of the 32nd clock. The next bit (bit 6 which is designated AVC) selects the 32-bit V_{CC} active counter for access. If AVC is a logical 1 this counter is selected and the 32 clock cycles that follow will either read or write this counter. If both bit 7 and bit 6 are written to a logic high, all clock cycles beyond the protocol are ignored and bits 5, 4, and 3 are loaded into the oscillator trim register. A value of binary 3 (011) will give a clock accuracy of ±120 seconds per month at +25°C. Increasing the binary number towards 7 will cause the real-time clock to run faster. Conversely, lowering the binary number towards 0 will cause the clock to run slower. Binary 000 will stop the oscillator completely. This feature can be used to conserve battery life during storage. In this mode the I_{BAT} current is reduced to 100nA maximum. In applications where oscillator trimming is not practical or not needed, a default setting of 011 is recommended. Bit 2 of protocol (designated CCC) is used to clear the continuous counter. When set to logic 1, the continuous counter will reset to 0 when $\overline{RST}$ is taken low. Bit 1 of protocol (designated CVC) is used to clear the V_{CC} active counter. When set to logical 1, the V_{CC} active counter will reset to 0 when $\overline{RST}$ is taken low. Both counters can be reset simultaneously by setting CCC and CVC both to a logical 1. Bit 0 of the protocol (designated RD) determines whether the 32 clocks to follow will write a counter or read a counter. When RD is set to a logical 0 a write action will follow when RD is set to a logical 1 a read action will follow. When sending the protocol, 8 bits should always be sent. Sending less than 8 bits can produce erroneous results. If clearing the counters or trimming the oscillator, the data transfer can be terminated after the 8-bit protocol is sent. However, when reading or writing the counters, 32 clock cycles should always follow the protocol.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input has two functions. First, $\overline{RST}$ turns on the serial port logic, which allows access to the protocol register for the protocol data entry. Second, the $\overline{RST}$ signal provides a method of terminating the protocol transfer or the 32-bit counter

transfer. A clock cycle is a sequence of a rising edge followed by a falling edge. For write inputs, data must be valid during the rising edge of the clock. Data bits are output on the falling edge of the clock when data is being read. All data transfers terminate if the $\overline{RST}$ input is transitioned low and the DQ pin goes to a high-impedance state. $\overline{RST}$ should only be transitioned low while the clock is high to avoid disturbing the last bit of data. All data transfers must consist of 8 bits when transferring protocol only or 8 + 32 bits when reading or writing either counter. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 8-bit protocol that inputs write mode, 32 bits of data are written to the selected counter on the rising edge of the next 32 CLK cycles. After 32 bits have been entered any additional CLK cycles will be ignored until $\overline{RST}$ is transitioned low to end data transfer, and then high again to begin new data transfer.

DATA OUTPUT

Following the eight CLK cycles that input read mode protocol, 32 bits of data will be output from the selected counter on the next 32 CLK cycles. The first data bit to be transmitted from the selected 32-bit counter occurs on the falling edge after the last bit of protocol is written. When transmitting data from the selected 32-bit counter, $\overline{RST}$ must remain at high level as a transition to low level will terminate data transfer. Data is driven out the DQ pin as long as CLK is low. When CLK is high the DQ pin is tristated.

CRYSTAL SELECTION

A standard 32.768kHz quartz crystal can be directly connected to the DS1602 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6pF. For more information on crystal selection and crystal layout considerations, please consult *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks.*

BATTERY SELECTION

The battery selected for use with the DS1602 should have an output voltage between 2.5V and 3.5V. A lithium battery of 35mAh or greater will run the elapsed time counter for over 10 years in the absence of power. Small lithium coin cell batteries produce both the proper output voltage and have the capacity to supply the DS1602 for the useable lifetime of the equipment where they are installed.

PIN DESCRIPTIONS

Vcc, GND – DC power is provided to the device on these pins. V_{CC} is the +5V input. When 5V is applied within normal limits, the device is fully accessible and data can be written and read. When a 3V battery is connected to the device and V_{CC} is below 1.25 x V_{BAT}, reads and writes are inhibited. As V_{CC} falls below V_{BAT} the continuous counter is switched over to the external power supply (nominal 3.0V DC) at V_{BAT}.

CLK (Serial Clock Input) – CLK is used to synchronize data movement on the serial interface.

DQ (Data Input/Output) – The DQ pin is the bidirectional data pin for the 3-wire interface.

$\overline{RST}$ (Reset) – The reset signal must be asserted high during a read or a write.

X1, X2 – Connections for a standard 32.768kHz quartz crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with*

Dallas Real-Time Clocks. The DS1602 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

V_{BAT} – Battery input for any standard 3V lithium cell or other energy source. Battery voltage must be held between 2.5V and 3.5V for proper operation. The nominal write-protect trip-point voltage at which access to the DS1602 is denied is set by the internal circuitry as 1.25 x V_{BAT} nominal. UL recognized to ensure against reverse charging current when used in conjunction with a lithium battery. See "Conditions of Acceptability" at www.maxim-ic.com/TechSupport/QA/ntrl.htm.

Figure 1. ELAPSED TIME COUNTER BLOCK DIAGRAM

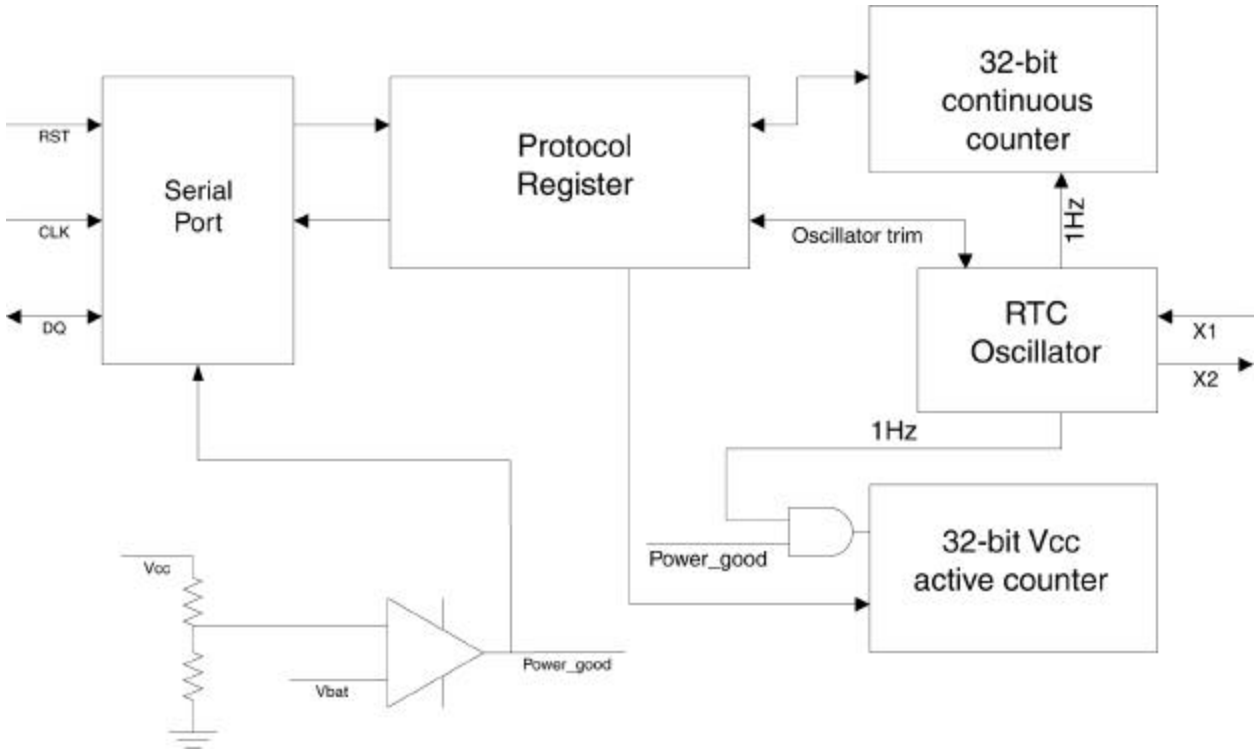


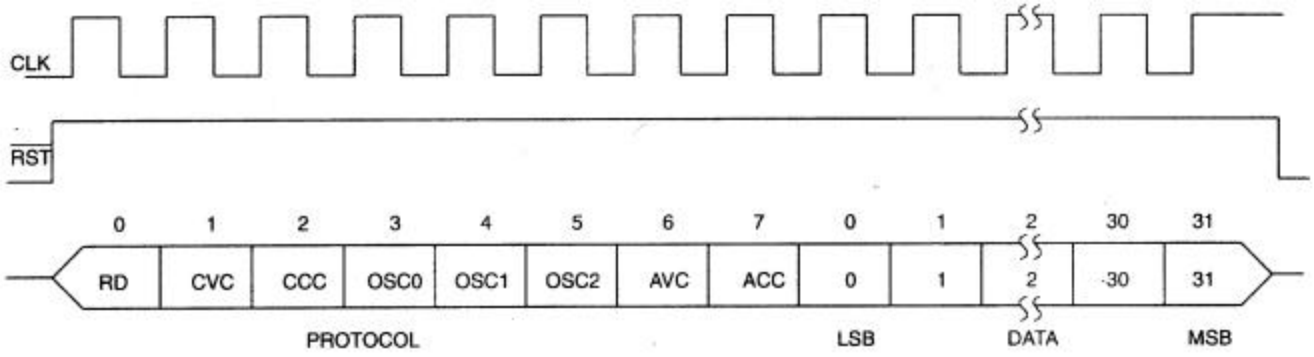
Figure 2. PROTOCOL BIT MAP

7	6	5	4	3	2	1	0
ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD

Table 1. VALID PROTOCOLS

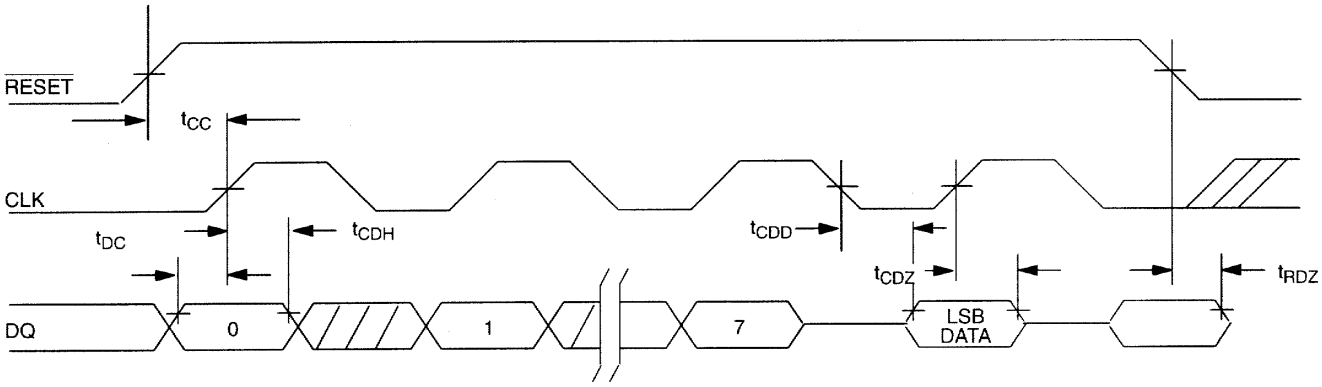
ACTION	PROTOCOL								FUNCTION
	ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD	
Read Continuous Counter	1	0	X	X	X	X	X	1	Output continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Write Continuous Counter	1	0	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Read V_{CC} Active Counter	0	1	X	X	X	X	X	1	Output V_{CC} active counter on the 32 clocks following protocol, oscillator trim register is not updated. Counters are not reset.
Write V_{CC} Active Counter	0	1	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Clear Continuous Counter	0	0	X	X	X	1	X	X	Resets the continuous counter to all zeros at the end of protocol. Oscillator trim register is not updated.
Clear V_{CC} Active Counter	0	0	X	X	X	X	1	X	Resets the V_{CC} active counter to all zeros at the end of protocol. Oscillator trim register is not updated.
Set Oscillator Trim Bits	1	1	A	B	C	X	X	0	Sets the oscillator trim register to a value of ABC. Counters are unaffected.
X = Don't Care									

Figure 3. DATA TRANSFER

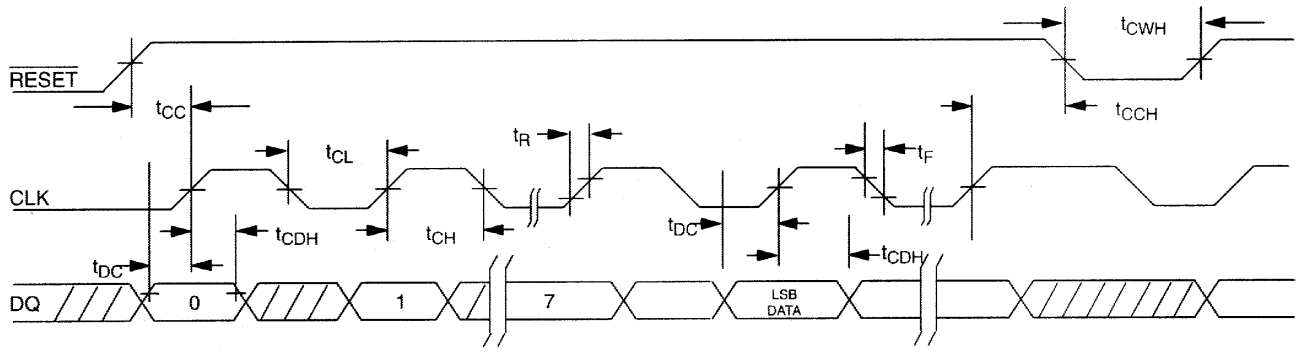


TIMING DIAGRAM: READ/WRITE DATA TRANSFER

READ DATA TRANSFER



WRITE DATA TRANSFER



Note: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature Range	See IPC/JEDEC J-STD-020A

This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Battery Supply Voltage	V_{BAT}	2.5	3.0	3.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
I/O Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current	I_{CC}			1	mA	4
Timekeeping Current	I_{CC1}			50	µA	5, 12
Timekeeping Current	I_{BAT}			400	nA	6, 12
Leakage Current	I_{BATL}			100	nA	11
Battery Trip Point	V_{TP}	1.216 x V_{BAT}	1.26 x V_{BAT}	1.285 x V_{BAT}	V	

CAPACITANCE (t_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	10

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5V ±10%; -40°C to 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	7
CLK to Data Hold	t_{CDH}	60			ns	7
CLK to Data Delay	t_{CDD}			200	ns	7, 8, 9
CLK Low Time	t_{CL}	250			ns	7
CLK High Time	t_{CH}	250			ns	7
CLK Frequency	f_{CLK}	DC		2.0	MHz	7
CLK Rise and Fall	t_F, t_R			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	7
CLK to $\overline{RST}$ Hold	t_{CCH}	60			ns	7
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	7
$\overline{RST}$ Low to I/O High-Z	t_{RDZ}			70	ns	7
CLK High to I/O High-Z	t_{CDZ}			20	ns	7

NOTES:

1) All voltages are referenced to ground.
2) Logic 1 voltages are specified at a source current of 1mA.
3) Logic 0 voltages are specified at a sink current of 4mA.
4) I_{CC} is specified with the DQ pin open.
5) I_{CC1} is specified with V_{CC} at 5.0V and $\overline{RST}$ = GND.
6) I_{BAT} is specified with $V_{CC} < V_{BAT}$ and V_{BAT} within DC recommended operating conditions.
7) Measured at V_{IH} = 2.0V or V_{IL} = 0.8V.
8) Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
9) Load capacitance = 50pF.
10) Specified as the load capacitance for which the crystal frequency is guaranteed (see crystal manufacturer's data sheet).
11) Leakage current is the amount of current consumed from the battery when V_{CC} is not present and the oscillator is turned off.
12) Using a crystal on X1 and X2.

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