

# HITFET

Smart Low Side Power Switch

## HITFET - BTS3104SDL

104 mOhm single channel smart low side power switch for 12V & 24V Application

## Datasheet

Rev. 1.0, 2009-12-06

|          |  |           |
|----------|--|-----------|
| <b>1</b> | <b>Overview</b>                        | <b>3</b>  |
| <b>2</b> | <b>Block Diagram</b>                   | <b>5</b>  |
| 2.1      | Terms                                  | 5         |
| <b>3</b> | <b>Pin Configuration</b>               | <b>6</b>  |
| 3.1      | Pin Assignment BTS3104SDL              | 6         |
| 3.2      | Pin Definitions and Functions          | 6         |
| <b>4</b> | <b>General Product Characteristics</b> | <b>7</b>  |
| 4.1      | Absolute Maximum Ratings               | 7         |
| 4.2      | Functional Range                       | 7         |
| 4.3      | Thermal Resistance                     | 8         |
| 4.3.1    | Transient Thermal Impedance            | 9         |
| <b>5</b> | <b>Input and Power Stage</b>           | <b>10</b> |
| 5.1      | Input Circuit                          | 10        |
| 5.1.1    | Failure Feedback                       | 11        |
| 5.2      | Power stage                            | 11        |
| 5.2.1    | Output On-state Resistance             | 11        |
| 5.2.2    | Output Timing                          | 13        |
| 5.3      | Characteristics                        | 14        |
| <b>6</b> | <b>Protection Functions</b>            | <b>16</b> |
| 6.1      | Thermal Protection                     | 16        |
| 6.2      | Overvoltage Protection                 | 17        |
| 6.3      | Short Circuit Protection               | 18        |
| 6.4      | Characteristics                        | 19        |
| <b>7</b> | <b>Package Outlines BTS3104SDL</b>     | <b>20</b> |
| <b>8</b> | <b>Revision History</b>                | <b>21</b> |



## 1 Overview

### Features

- Short circuit and over load protection
- Thermal shutdown with latch behavior
- ESD protection
- Over voltage protection
- Logic level input suitable for 5V and 3.3V
- Analog driving possible
- 12V and 24V usability
- Green Product (RoHS compliant)
- AEC Qualified



**PG-TO252-3-11**

### Description

The BTS3104SDL is a single channel low-side MOSFET power switch in PG-TO252-3-11 package providing embedded protective functions.

The device is monolithically integrated with a N channel vertical power FET and embedded protection functions. The BTS3104SDL is automotive qualified and can be used in 12V and 24V automotive and industrial applications.

**Table 1 Product Summary**

|   |              |        |
|---|--------------|--------|
| Drain voltage <sup>1)</sup>                               | $V_D$        | 60 V   |
| Maximum Input Voltage                                     | $V_{IN}$     | 10 V   |
| Maximum On-State resistance at 150°C at 5V input voltage  | $R_{DS(ON)}$ | 323 mΩ |
| Typical On-State resistance at 25°C and 10V input voltage | $R_{DS(ON)}$ | 104 mΩ |
| Nominal load current                                      | $I_{D(nom)}$ | 2.0 A  |
| Minimum current limitation level                          | $I_{D(lim)}$ | 6 A    |

1) Active clamped

| Type       | Package       | Marking |
|------------|---------------|---------|
| BTS3104SDL | PG-TO252-3-11 |         |

**Protective Functions**

- Electrostatic discharge protection (ESD)
- Active clamp over voltage protection
- Thermal shutdown with latch behavior
- Over load and Short circuit protection
- Current limitation

**Analog Fault Information**

- Thermal shutdown
- Short to Battery
- Overload

**Applications**

- Designed for inductive and lamp loads in automotive and industrial applications.
- 12V and 24V applications
- All types of resistive, inductive and capacitive loads
- Replaces discrete circuits

**Detailed Description**

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by  $E_{AS}$  and maximum current capabilities.

The BTS3104SDL offers ESD protection on the IN Pin which refers to the Source pin (Ground).

The overtemperature protection prevents the device from overheating due to overload and/or bad cooling conditions. The temperature information is given by a temperature sensor in the power MOSFET. During thermal shutdown the device sinks an increased input current at the IN pin to feedback the fault condition.

The BTS3104SDL has a thermal-latch function. The device will turn off and stay off, even after the measured temperature has dropped below the thermal hysteresis. After cooling down the device can be switched on again by toggling the IN pin.

The over voltage protection gets activated during load dump or inductive turn off conditions. The power MOSFET is limiting the drain-source voltage, if it rises above the  $V_{DS(\text{clamp})}$ .

## 2 Block Diagram



Figure 1 Block Diagram

### 2.1 Terms

Figure 2 shows all external terms used in this data sheet.

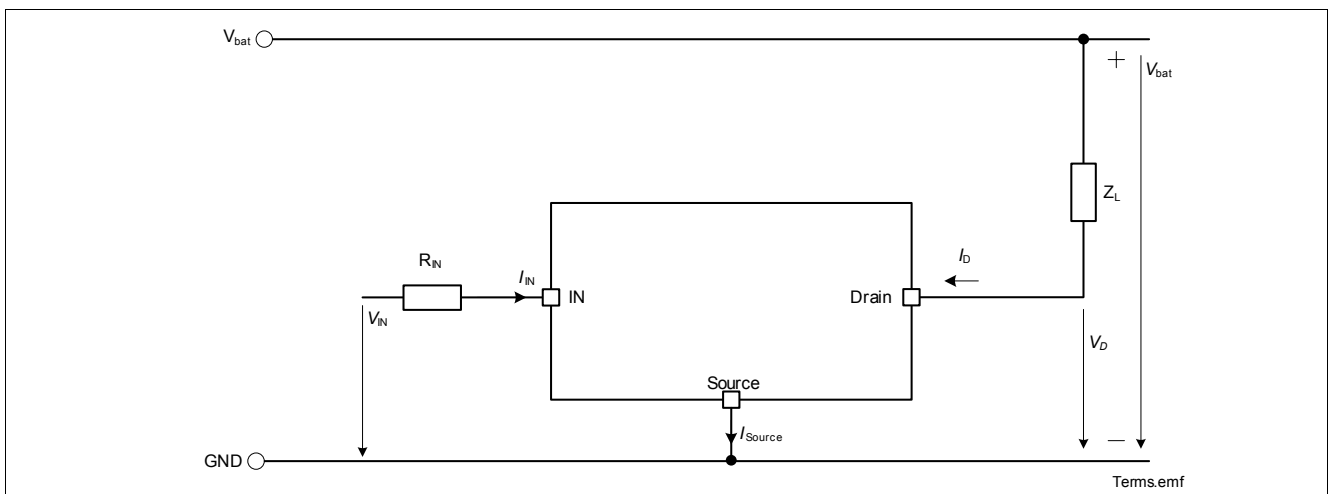


Figure 2 Naming of electrical parameters

### 3 Pin Configuration

#### 3.1 Pin Assignment BTS3104SDL



Figure 3 Pin Configuration PG-TO252-3-11

#### 3.2 Pin Definitions and Functions

| Pin | Symbol | Function                       |
|-----|--------|--------------------------------|
| 1   | IN     | Input and fault feedback       |
| 2,4 | Drain  | Load connection for power DMOS |
| 3   | Source | Ground, Source of power DMOS   |

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings<sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

| Pos.                      | Parameter  | Symbol      | Limit Values |      | Unit | Test Conditions  |
|---------------------------|--|-------------|--------------|------|------|--|
|                           |  |             | Min.         | Max. |      |  |
| <b>Voltages</b>           |  |             |              |      |      |  |
| 4.1.1                     | Drain voltage  | $V_D$       | –            | 60   | V    | <sup>2)</sup> $V_{IN} = 0\text{ V}$ , $I_D = 10\text{ mA}$                                   |
| 4.1.2                     | Drain voltage for short circuit protection           | $V_{D(SC)}$ | –            | 36   | V    | $V_{IN} = 5\text{ V}$<br>$R_{SC} = 200\text{ m}\Omega$<br>$L_{SC} = 5\text{ }\mu\text{H}$    |
| 4.1.3                     | Input Current  | $I_{IN}$    | self limited |      | mA   | $-0.2\text{ V} < V_{IN} < 10\text{ V}$   |
|                           |  |             | -2           | 2    | mA   | $V_{IN} < -0.2\text{ V}$<br>or $V_{IN} > 10\text{ V}$  |
| 4.1.4                     | Drain Current  | $I_D$       | –            | 6    | A    | <sup>3)</sup>  |
| <b>Energies</b>           |  |             |              |      |      |  |
| 4.1.5                     | Unclamped single pulse inductive energy single pulse | $E_{AS}$    | –            | 50   | mJ   | $I_{D(start)} = 4.5\text{ A}$<br>$V_{bat} = 24\text{ V}$ ;<br>$T_{J(start)} = 150\text{ °C}$ |
| <b>Temperatures</b>       |  |             |              |      |      |  |
| 4.1.6                     | Operating temperature                                | $T_J$       | -40          | +150 | °C   | –  |
| 4.1.7                     | Storage temperature                                  | $T_{STG}$   | -55          | +150 | °C   | –  |
| <b>ESD Susceptibility</b> |  |             |              |      |      |  |
| 4.1.8                     | ESD Resistivity                                      | $V_{ESD}$   | -2           | 2    | kV   | HBM <sup>4)</sup>  |

1) Not subject to production test, specified by design.

2) Active clamped.

3) Active limited

4) ESD susceptibility, HBM according to EIA/JESD 22-A114, Pin Source connected to Ground

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation*

### 4.2 Functional Range

| Pos.  | Parameter                     | Symbol   | Limit Values |      | Unit | Conditions |
|-------|-------------------------------|----------|--------------|------|------|------------|
|       |                               |          | Min.         | Max. |      |            |
| 4.2.1 | Input pin voltage (device ON) | $V_{IN}$ | 2            | 10   | V    | –          |
| 4.2.2 | Drain voltage                 | $V_D$    | 2.5          | 36   | V    | –          |

| Pos.  | Parameter                     | Symbol        | Limit Values |      | Unit | Conditions       |
|-------|-------------------------------|---------------|--------------|------|------|------------------|
|       |                               |               | Min.         | Max. |      |                  |
| 4.2.3 | Input pin current consumption | $I_{IN(ON)}$  | –            | 30   | μA   | normal operation |
| 4.2.4 | Input pin feedback current    | $I_{IN(lim)}$ | –            | 300  | μA   | fault indication |

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

### 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards.

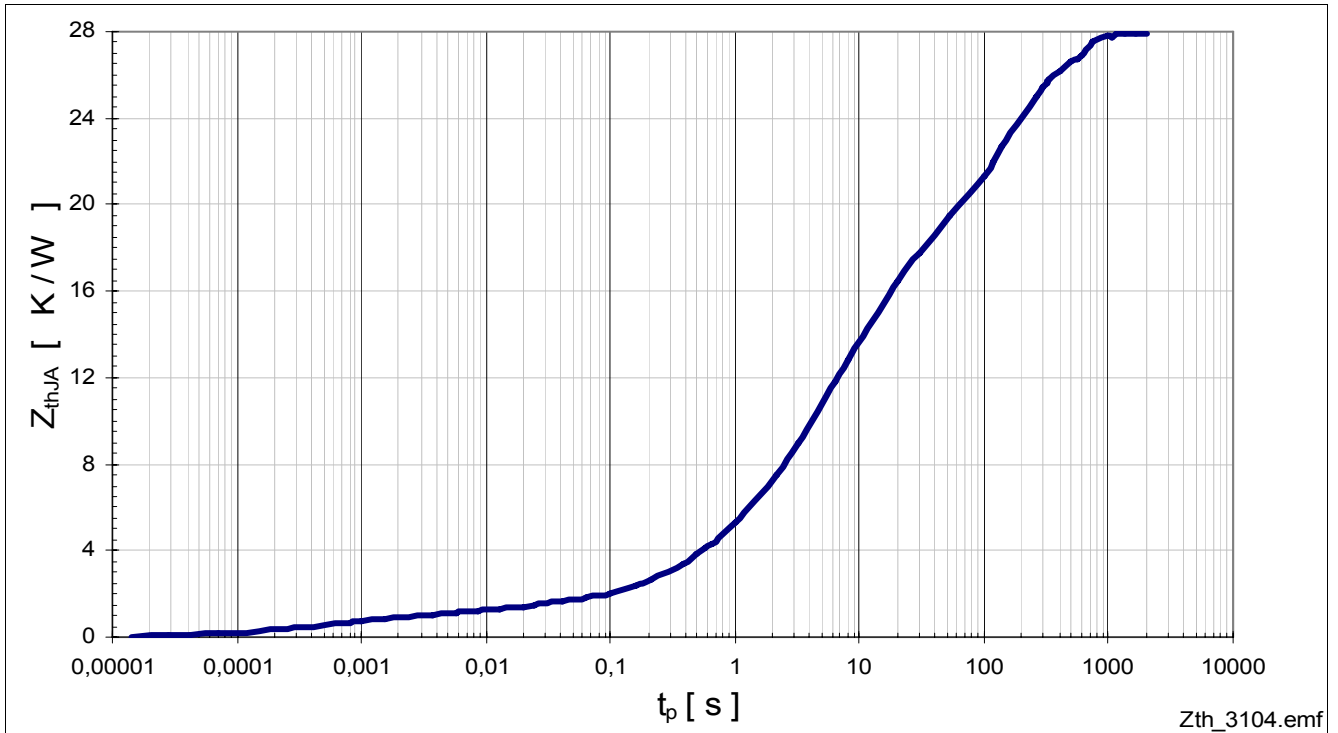
For more information, go to [www.jedec.org](http://www.jedec.org).

| Pos.  | Parameter   | Symbol           | Limit Values |      |      | Unit | Conditions |
|-------|---|------------------|--------------|------|------|------|------------|
|       |   |                  | Min.         | Typ. | Max. |      |            |
| 4.3.5 | Junction to Case                                    | $R_{thJC}$       | –            | –    | 1.3  | K/W  | 1) 2)      |
| 4.3.6 | Junction to Ambient (2s2p)                          | $R_{thJA(2s2p)}$ | –            | 28   | –    | K/W  | 1) 3)      |
| 4.3.7 | Junction to Ambient<br>(1s0p+600mm <sup>2</sup> Cu) | $R_{thJA(1s0p)}$ | –            | 48   | –    | K/W  | 1) 4)      |

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature).  $T_a = 25\text{ °C}$ . Device is loaded with 1W power.
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μm Cu, 2 x 35 μm Cu).  $T_a = 25\text{ °C}$ , Device is loaded with 1W power.
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm<sup>2</sup> and 70 μm thickness.  $T_a = 25\text{ °C}$ , Device is loaded with 1W power.



### 4.3.1 Transient Thermal Impedance



**Figure 4** Typical transient thermal impedance

$$Z_{thJA} = f(t_p), T_a = 25\text{ }^\circ\text{C}$$

Value is according to Jeduc JESD51-2,-7 at natural convection on FR4 2s2p board;

The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70 μm Cu, 2 x 35 μm Cu). Device is dissipating 1 W power.

## 5 Input and Power Stage

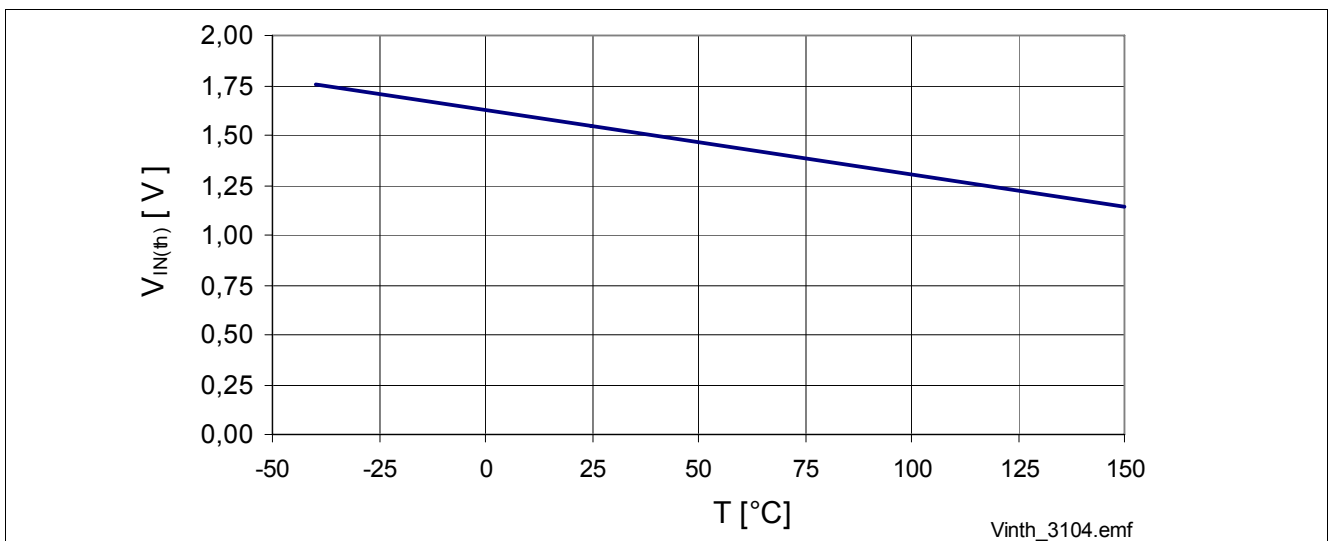
### 5.1 Input Circuit

**Figure 5** shows the input circuit of the BTS3104SDL. The Zener Diode  $Z_D$  protects the input circuit against ESD pulses. The internal circuitry is powered via the input pin. During normal operation the Input is connected to the Gate of the power MOSFET. During fault condition the device sinks the current  $I_{IN(fault)}$  to give the fault information back to the driving circuit. The current handling capability of the driving circuit does not influence the device behavior as long as the supply current  $I_{IN}$  is supplied.



**Figure 5** Input Circuit

The following Figure shows the typical input threshold voltage of BTS3104SDL.



**Figure 6** Typical Input Threshold Voltage  $V_{in\text{th}} = f(T_J)$ ;  $I_D = 1.2\text{mA}$ ,  $V_D = V_{IN}$

The following Figure shows the typical transfer characteristic of BTS3104SDL.

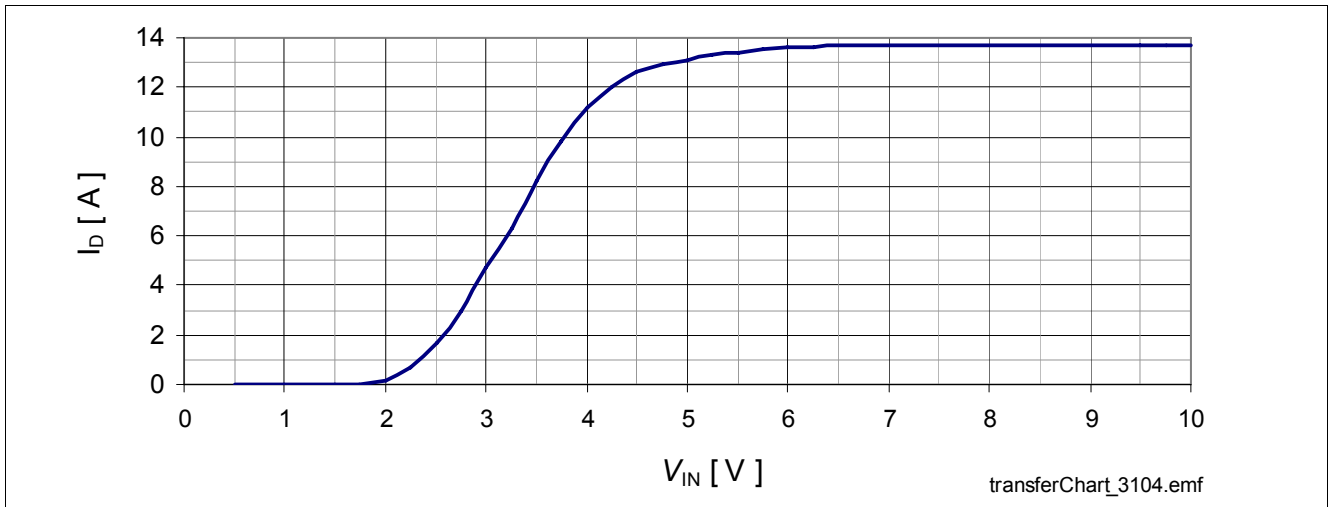


Figure 7 Typical Transfer Characteristic  $I_D = f(V_{IN})$ ;  $V_D = 13.5 \text{ V}$ ,  $T_{J(\text{start})} = 25 \text{ }^\circ\text{C}$

### 5.1.1 Failure Feedback

During failure condition the BTS3104SDL sinks the increased current  $I_{IN(\text{fault})}$ .

## 5.2 Power stage

### 5.2.1 Output On-state Resistance

The on-state resistance depends on the junction temperature  $T_J$  and on the applied input voltage. The following Figures show this dependencies for the typical on-state resistance  $R_{DS(\text{on})}$ .

Temperature dependency of  $R_{DS(\text{on})}$  at 3 different input voltage conditions:

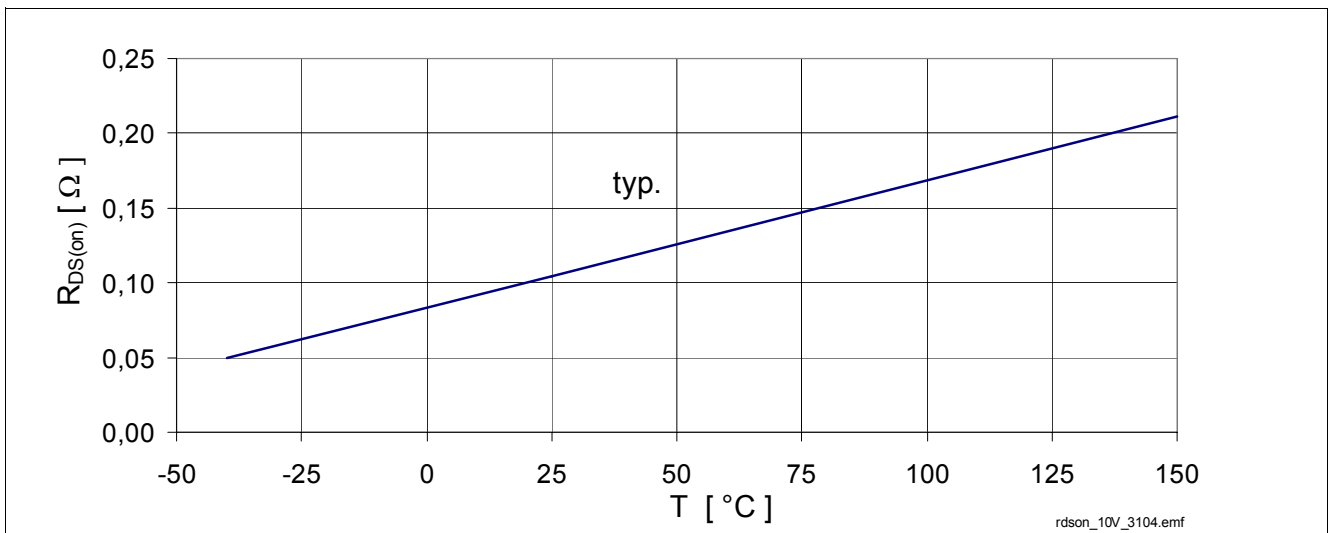


Figure 8 Typical On-State Resistance,  $R_{DS(\text{on})} = f(T_J)$ ,  $V_{IN} = 10 \text{ V}$

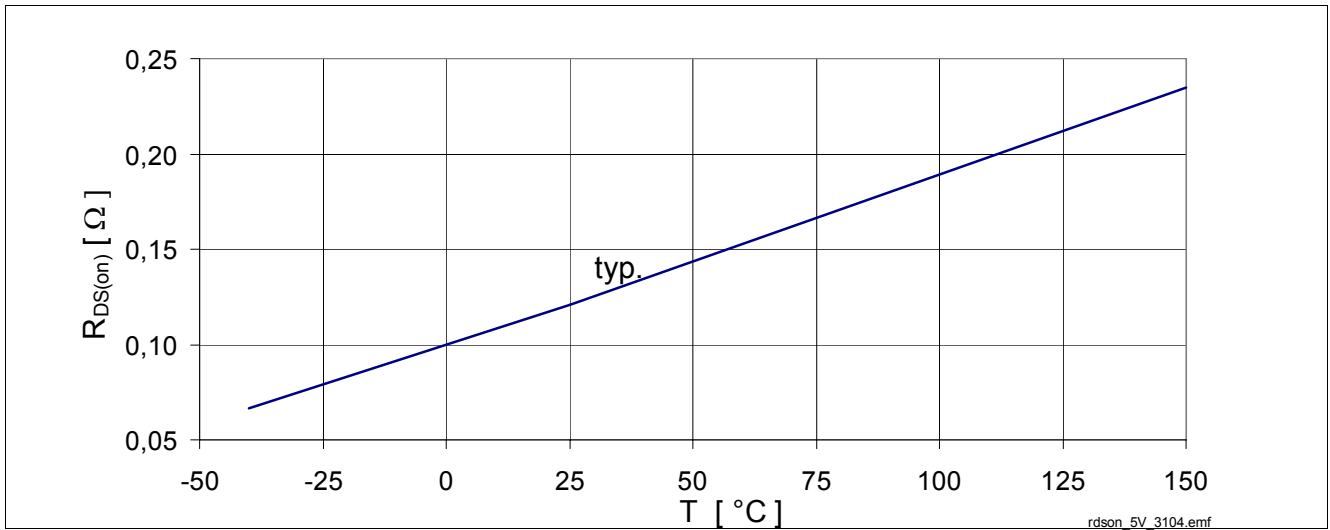


Figure 9 Typical On-State Resistance,  $R_{DS(on)} = f(T_J)$ ,  $V_{IN} = 5\text{V}$

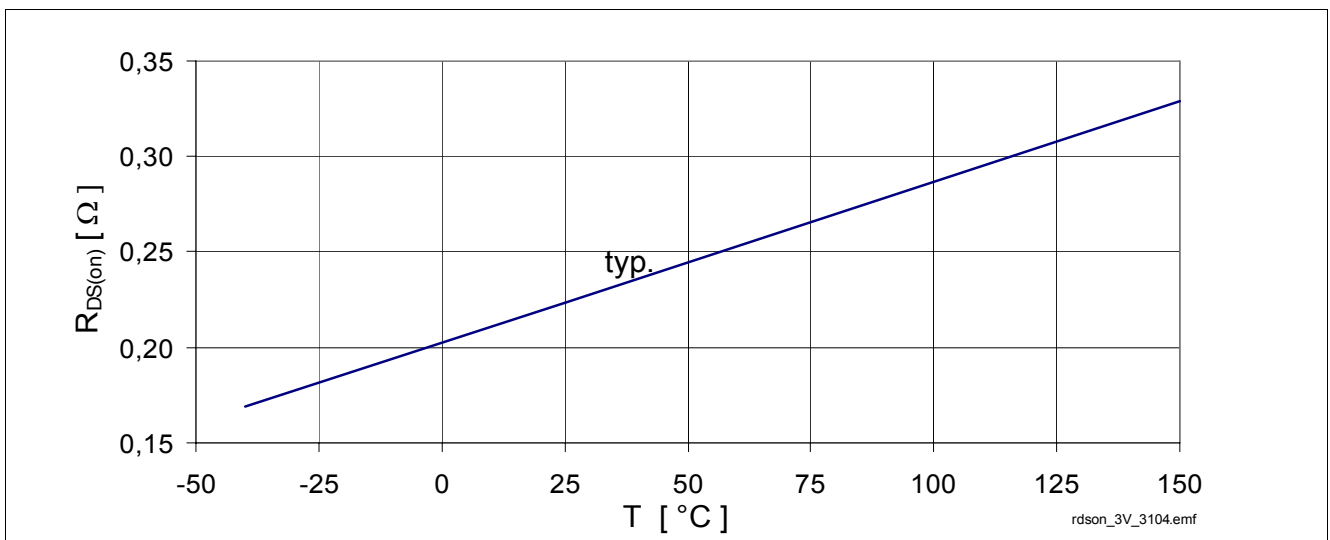


Figure 10 Typical On-State Resistance,  $R_{DS(on)} = f(T_J)$ ,  $V_{IN} = 3\text{V}$

### 5.2.2 Output Timing

A voltage signal at the input pin above the threshold voltage causes the power MOSFET to switch on.

Figure 11 shows the timing definition.

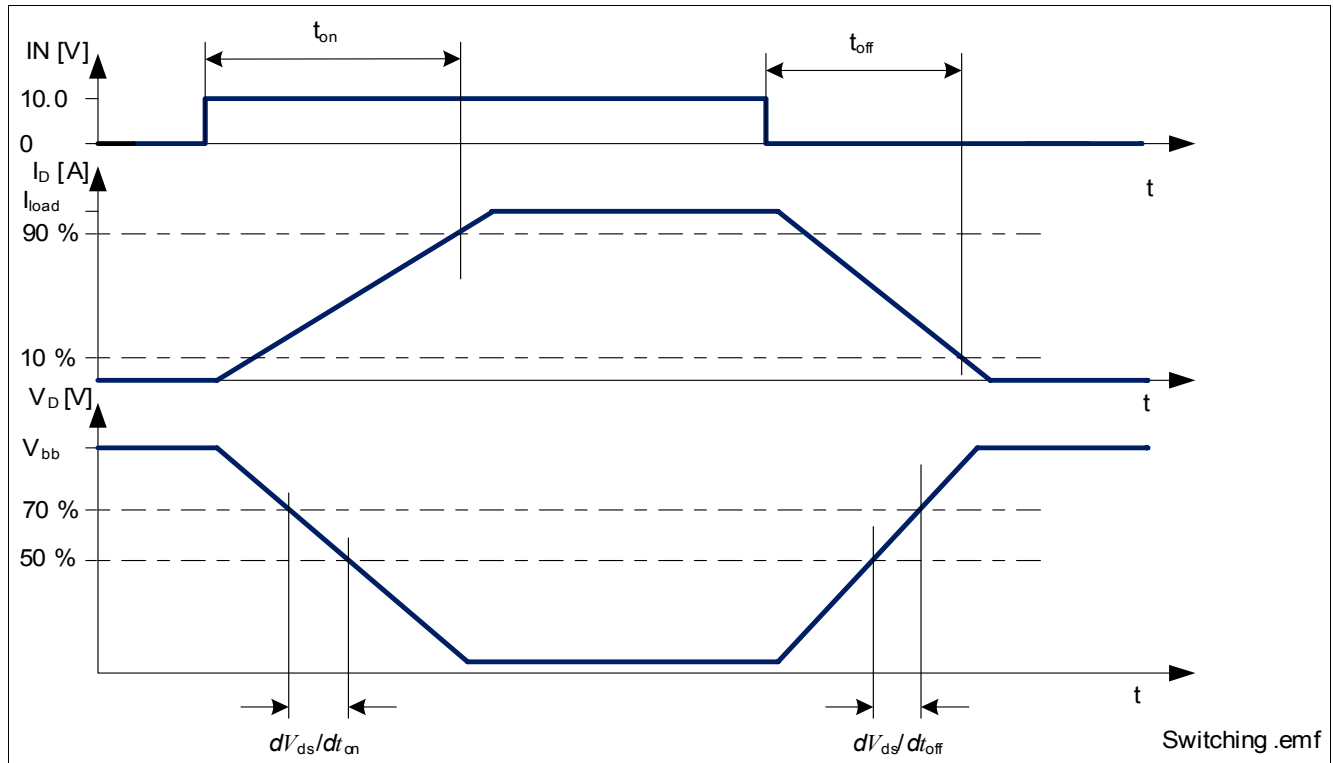


Figure 11 Definition of Power Output Timing for Resistive Load

### 5.3 Characteristics

Note: Characteristics show the deviation of parameter at given input voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

All voltages with respect to Source Pin unless otherwise stated.

#### Electrical Characteristics: Input and Power Stage

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ,  $V_{\text{bat}} = 8.0\text{ V}$  to  $36\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.               | Parameter                        | Symbol               | Limit Values |      |      | Unit             | Test Conditions   |
|--------------------|----------------------------------|----------------------|--------------|------|------|------------------|---|
|                    |                                  |                      | Min.         | Typ. | Max. |                  |   |
| <b>Input</b>       |                                  |                      |              |      |      |                  |   |
| 5.3.1              | Supply current from Input Pin    | $I_{\text{IN(nom)}}$ | –            | 10   | 30   | $\mu\text{A}$    | $V_{\text{D}} = 0\text{ V};$<br>$V_{\text{IN}} = 10\text{ V}$   |
| 5.3.2              | Input current protection mode    | $I_{\text{IN(lim)}}$ | –            | 100  | 300  | $\mu\text{A}$    | $V_{\text{IN}} = 10\text{ V};$<br>$T_j = 150\text{ °C}$   |
| 5.3.3              | Input threshold voltage          | $V_{\text{IN(th)}}$  | 0.8          | 1.6  | 2    | V                | $V_{\text{D}} = V_{\text{IN}};$<br>$I_{\text{D}} = 1.2\text{ mA}$   |
| <b>Power Stage</b> |                                  |                      |              |      |      |                  |   |
| 5.3.4              | On-State Resistance              | $R_{\text{DS(on)}}$  | –            | 104  | –    | $\text{m}\Omega$ | $T_j = 25\text{ °C};$<br>$V_{\text{IN}} = 10\text{ V};$<br>$I_{\text{D}} = 3\text{ A}$  |
|                    |                                  |                      | –            | 208  | 270  | $\text{m}\Omega$ | $T_j = 150\text{ °C};$<br>$V_{\text{IN}} = 10\text{ V};$<br>$I_{\text{D}} = 3\text{ A}$   |
|                    |                                  |                      | –            | 121  | –    | $\text{m}\Omega$ | $T_j = 25\text{ °C};$<br>$V_{\text{IN}} = 5\text{ V};$<br>$I_{\text{D}} = 3\text{ A}$   |
|                    |                                  |                      | –            | 235  | 323  | $\text{m}\Omega$ | $T_j = 150\text{ °C};$<br>$V_{\text{IN}} = 5\text{ V};$<br>$I_{\text{D}} = 3\text{ A}$  |
|                    |                                  |                      | –            | 220  | –    | $\text{m}\Omega$ | <sup>1)</sup> $T_j = 25\text{ °C};$<br>$V_{\text{IN}} = 3\text{ V};$<br>$I_{\text{D}} = 3\text{ A}$   |
|                    |                                  |                      | –            | 325  | 450  | $\text{m}\Omega$ | <sup>1)</sup> $T_j = 150\text{ °C};$<br>$V_{\text{IN}} = 3\text{ V};$<br>$I_{\text{D}} = 3\text{ A}$  |
| 5.3.5              | Nominal load current             | $I_{\text{D(nom)}}$  | 2.0          | 2.5  | –    | A                | <sup>1)</sup> $T_j < 150\text{ °C};$<br>$T_{\text{A}} = 105\text{ °C};$<br>$V_{\text{IN}} = 10\text{ V};$<br>$V_{\text{DS}} = 0.5\text{ V}$ |
| 5.3.6              | Zero input voltage drain current | $I_{\text{DSS}}$     | –            | 2.5  | 6    | $\mu\text{A}$    | $V_{\text{D}} = 36\text{ V};$<br>$V_{\text{IN}} = 0\text{ V};$<br>$T_j = -40\text{ °C}$ to $85\text{ °C}$                                   |
|                    |                                  |                      | –            | 6    | 12   | $\mu\text{A}$    | $V_{\text{D}} = 36\text{ V};$<br>$V_{\text{IN}} = 0\text{ V};$<br>$T_j = 150\text{ °C}$   |

**Electrical Characteristics: Input and Power Stage (cont'd)**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ,  $V_{bat} = 8.0\text{ V}$  to  $36\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.  | Parameter                     | Symbol             | Limit Values |      |      | Unit                   | Test Conditions   |                       |
|---|-------------------------------|--------------------|--------------|------|------|------------------------|---|-----------------------|
|   |                               |                    | Min.         | Typ. | Max. |                        |   |                       |
| <b>Switching</b> (see <a href="#">Figure 11</a> for definition details) |                               |                    |              |      |      |                        |   |                       |
| 5.3.7   | Turn-on time                  | $t_{on}$           | –            | 50   | 100  | $\mu\text{s}$          | $V_{bb}=13.5\text{ V}$ , $R_L=4.7\ \Omega$<br>$T_j = -40\text{ °C}$ to $85\text{ °C}$ |                       |
|   |                               |                    |              | 60   | 120  |                        |   | $T_j = 150\text{ °C}$ |
| 5.3.8   | Turn-off time                 | $t_{off}$          | –            | 80   | 120  | $\mu\text{s}$          | $V_{bb}=13.5\text{ V}$ , $R_L=4.7\ \Omega$<br>$T_j = -40\text{ °C}$ to $85\text{ °C}$ |                       |
|   |                               |                    |              | 120  | 200  |                        |   | $T_j = 150\text{ °C}$ |
|   |                               |                    |              | 80   | 200  |                        |   | $\mu\text{s}$         |
| 5.3.9   | Slew rate on                  | $-dV_{ds}/dt_{on}$ | –            | 0.7  | 1.5  | $\text{V}/\mu\text{s}$ | $V_{bb}=13.5\text{ V}$ , $R_L=4.7\ \Omega$  |                       |
|   |                               |                    |              | 0.7  | 1.5  |                        |   | $\mu\text{s}$         |
| 5.3.10  | Slew rate off                 | $dV_{ds}/dt_{off}$ | –            | 0.7  | 1.5  | $\text{V}/\mu\text{s}$ | $V_{bb}=13.5\text{ V}$ , $R_L=4.7\ \Omega$  |                       |
|   |                               |                    |              | 0.7  | 1.5  |                        |   | $\mu\text{s}$         |
| <b>Inverse Diode</b>  |                               |                    |              |      |      |                        |   |                       |
| 5.3.11  | Inverse Diode forward voltage | $V_{D,inverted}$   | –            | -1.0 | -1.5 | V                      | $I_D = -11\text{ A}$<br>$V_{IN} = 0\text{ V}$   |                       |

1) Not subject to production test, calculated by  $R_{thJA}$  and  $R_{DS(on)}$ .

## 6 Protection Functions

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operation.

### 6.1 Thermal Protection

The device is protected against over temperature due to overload and / or bad cooling conditions. To ensure this a temperature sensor located in the Power MOSFET is used.

The BTS3104SDL has a thermal-latch function. The device will turn off and stay off, even after the measured temperature has dropped below the thermal hysteresis. After cooling down the device can be switched on again by toggling the IN pin.

The protective switch off can be reset by setting the input pin voltage to low. Then the internal logic is not supplied anymore and the next time the voltage on the IN pin rises above the input threshold voltage, the device will switch on, if the temperature is not above the over temperature threshold.

see [Figure 12](#).

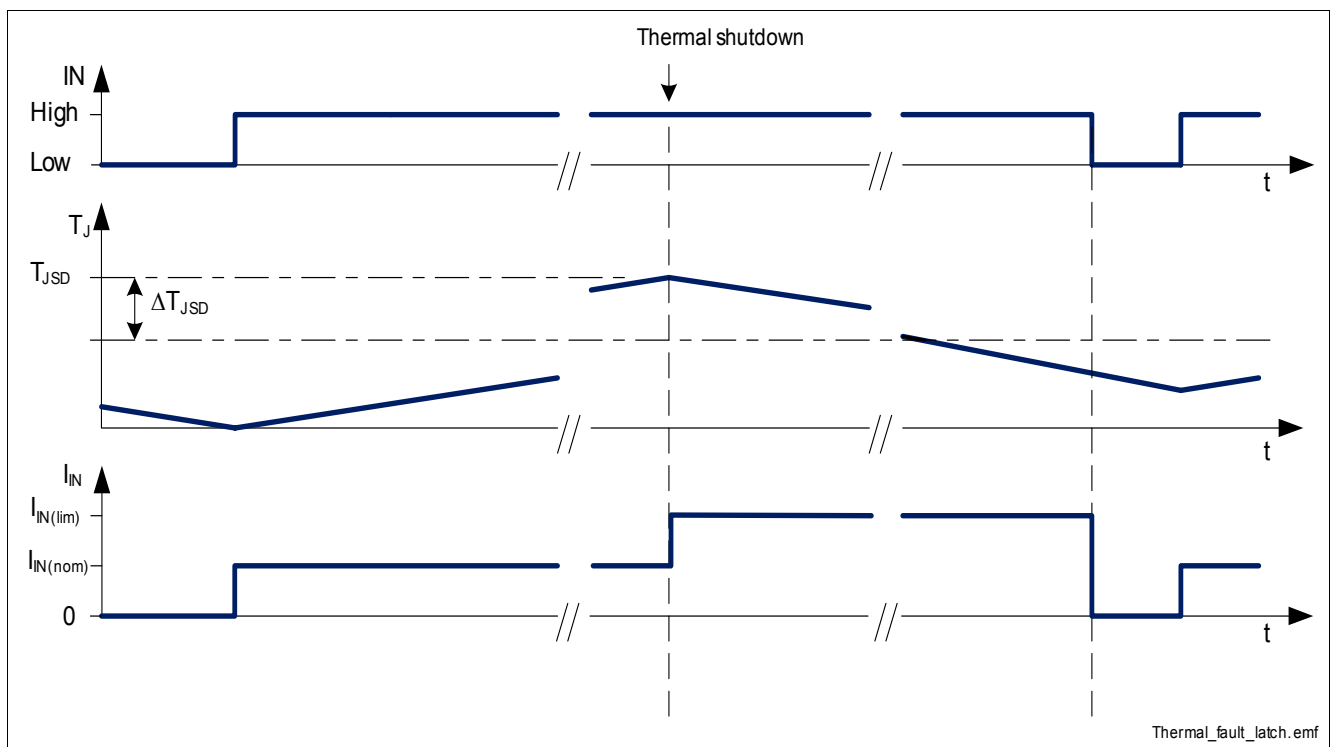
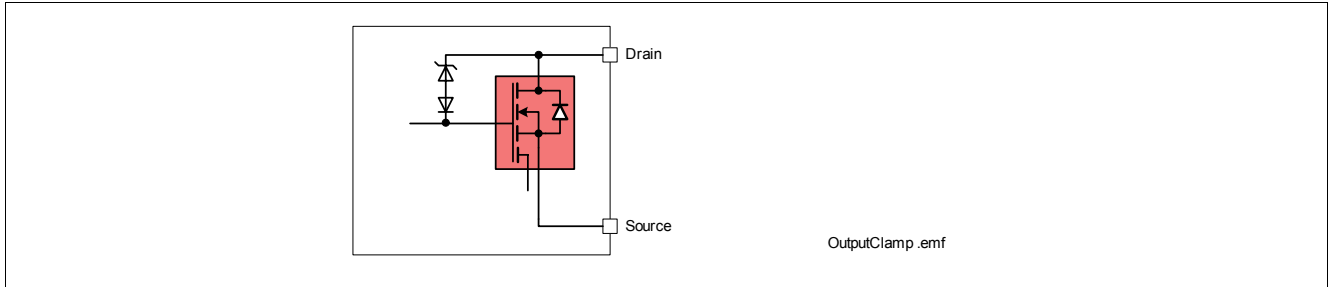


Figure 12 Error Signal via Input Current at Thermal Shutdown



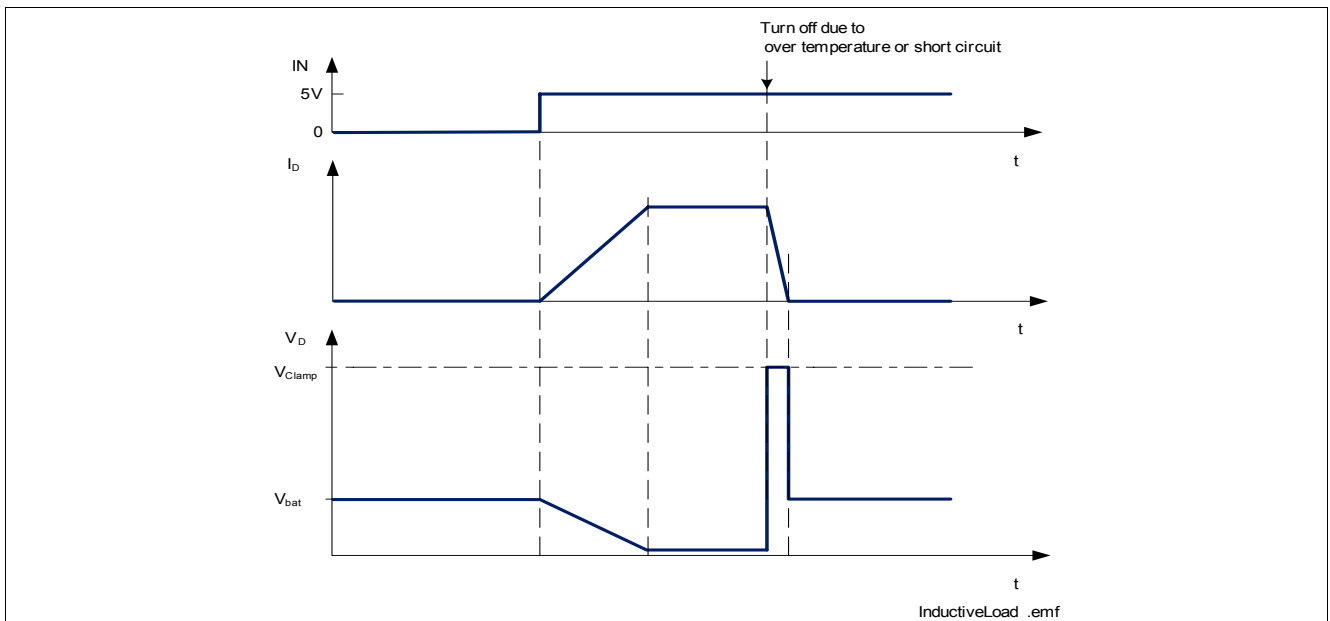
## 6.2 Overvoltage Protection

When switching off inductive loads with low-side switches, the Drain-Source voltage  $V_D$  rises above battery potential, because the inductance intends to continue driving the current.



**Figure 13 Output Clamp**

The BTS3104SDL is equipped with a voltage clamp mechanism that prevents the Drain-Source voltage to rise above  $V_{D(Clamp)}$ . See [Figure 13](#) and [Figure 14](#) for more details.



**Figure 14 Switching an Inductance**

While demagnetization of inductive loads, energy has to be dissipated in the BTS3104SDL. This energy can be calculated by the following equation:

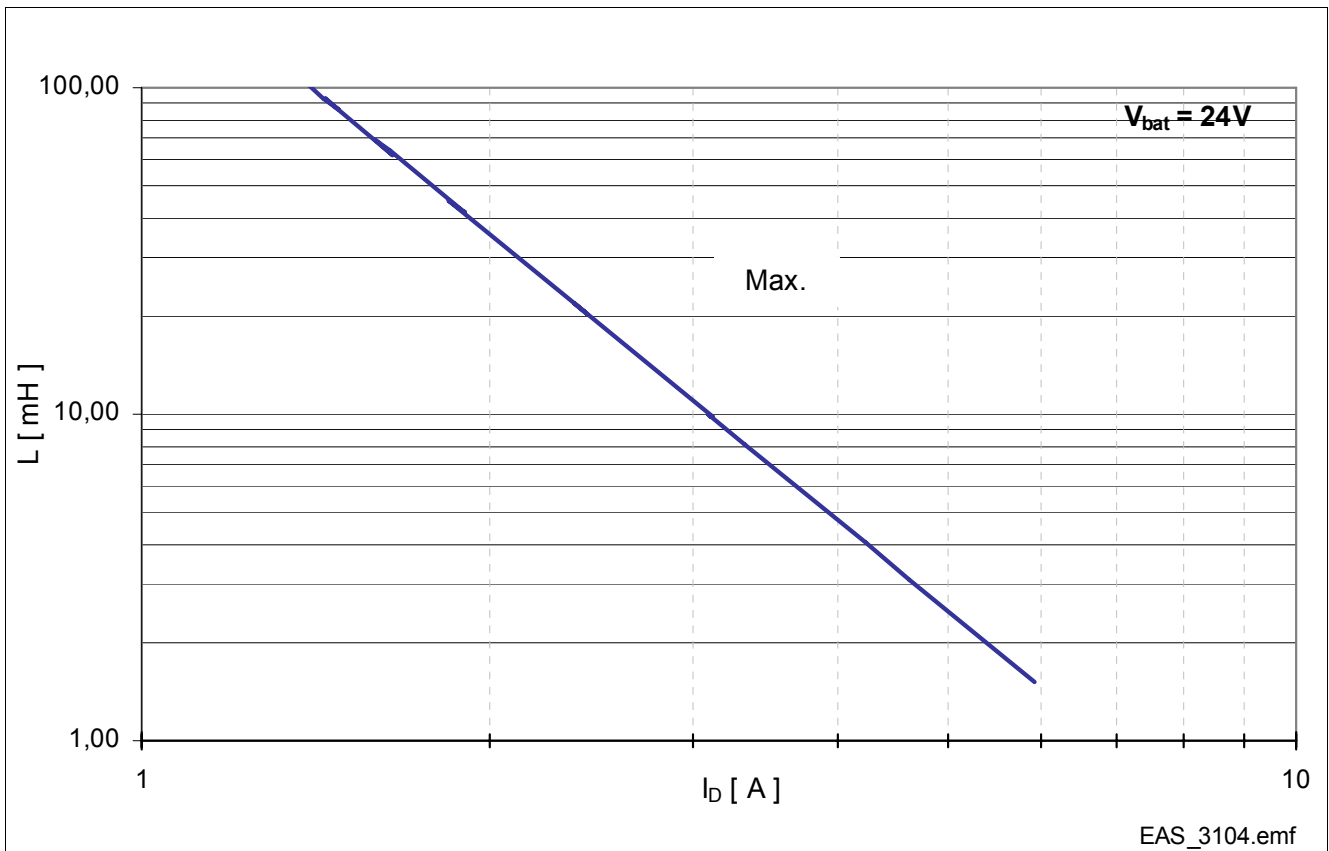
$$E = V_{D(Clamp)} \cdot \left[ \frac{V_{bat} - V_{D(Clamp)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_{bat} - V_{D(Clamp)}} \right) + I_L \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under assumption of  $R_L = 0$

$$E = \frac{1}{2} L I_L^2 \cdot \left( 1 - \frac{V_{bat}}{V_{D(Clamp)}} \right)$$

[Figure 16](#) shows the inductance / current combination the BTS3104SDL can handle.

For maximum single avalanche energy please also refer to  $E_{AS}$  value in **“Energies”** on Page 7



**Figure 15** Maximum load inductance for single pulse  
 $L = f(I_L)$ ,  $T_{j(start)} = 150\text{ °C}$ ,  $V_{bat} = 24V$

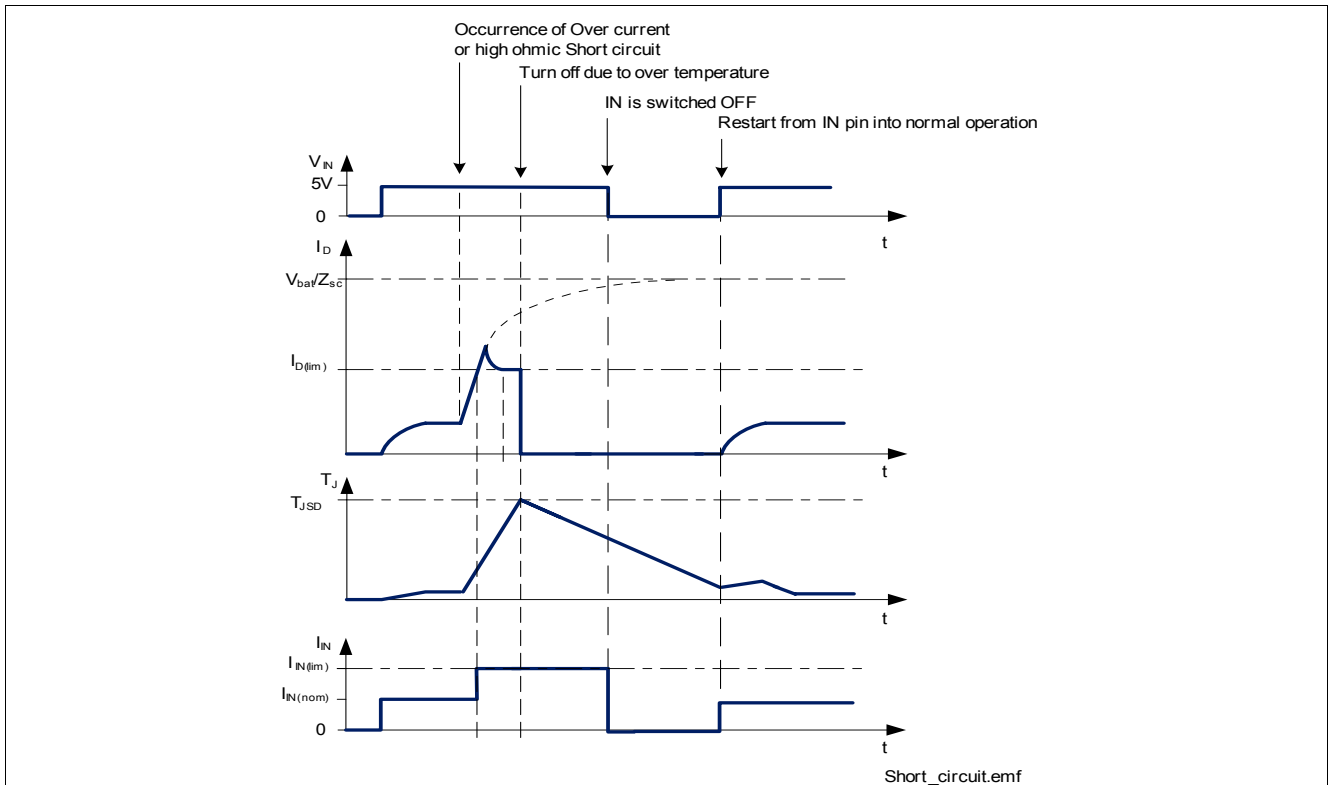
### 6.3 Short Circuit Protection

The condition short circuit is an overload condition of the device. If the current reaches the limitation value of  $I_{D(lim)}$  the device limits the current and starts heating up. When the thermal shutdown temperature is reached, the device turns off.

The time from the beginning of current limitation until the over temperature switch off depends strongly on the cooling conditions.

The device sinks higher current on IN pin during the protective switch off and switches back ON after the IN toggles.

**Figure 16** shows this behavior.


**Figure 16 Short circuit protection via current limitation and over temperature switch off**

## 6.4 Characteristics

Note: Characteristics show the deviation of parameter at given input voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

### Electrical Characteristics: Protection Functions

Unless otherwise specified:  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $V_{bat} = 8.0\text{ V to }36\text{ V}$

| Pos.                          | Parameter                              | Symbol           | Limit Values |                   |      | Unit | Test Conditions   |
|-------------------------------|--|------------------|--------------|-------------------|------|------|---|
|                               |  |                  | Min.         | Typ.              | Max. |      |   |
| <b>Thermal Protection</b>     |  |                  |              |                   |      |      |   |
| 6.4.1                         | Thermal shut down junction temperature | $T_{JSD}$        | 150          | 175 <sup>1)</sup> | –    | °C   | –   |
| 6.4.2                         | Thermal hysteresis                     | $\Delta T_{JSD}$ | –            | 10                | –    | K    | <sup>1)</sup>   |
| <b>Overvoltage Protection</b> |  |                  |              |                   |      |      |   |
| 6.4.3                         | Drain clamp voltage                    | $V_{D(Clamp)}$   | 60           | –                 | 75   | V    | $V_{IN} = 0\text{ V}; I_D = 10\text{ mA}$   |
| <b>Current limitation</b>     |  |                  |              |                   |      |      |   |
| 6.4.4                         | Current limitation                     | $I_{D(lim)}$     | 6            | 13                | 20   | A    | $V_{IN} = 10\text{ V};$<br>$V_D = 13.5\text{ V};$<br><br>$t_{measure} = 200\mu\text{s}$ |

1) Not subject to production test, specified by design.

## 7 Package Outlines BTS3104SDL



Figure 17 PG-T0252-3-11 (Plastic Dual Small Outline Package)

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## **8 Revision History**

| <b>Version</b> | <b>Date</b> | <b>Changes</b>              |
|----------------|-------------|-----------------------------|
| Rev. 1.0       | 2009-12-06  | initial released data sheet |

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