



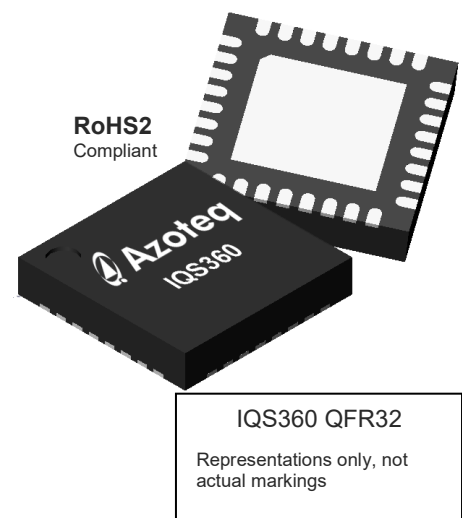
## ProxSense® IQS360 Datasheet

### 12 Channel Projected Capacitive Touch & Proximity Controller with Trackpad and Keypad Capability

The **IQS360** ProxSense® IC is 12-channel mutual capacitive touch and proximity controller with market leading sensitivity and automatic tuning. The **IQS360** provides a cost effective implementation in a small outline package for **key pads** and **trackpads** up to 4 rows and 3 columns. Keypads can offer second level touch activation (snap) when used with metal snap domes.

#### Main Features

- 12 Mutual Channel Capacitive Controller
- Trackpad with on chip XY coordinate calculation
- Configurable up to 4x3 elements
- 768 x 512 resolution
- Up to 50Hz report rate
- Absolute and Relative Tracking Data
- 1MHz or 2MHz Charge Transfer Frequency
- Advanced on-chip digital signal processing
- Automatic adjustment for optimal performance (ATI)
- User selectable Proximity and Touch thresholds
- Long proximity range
- Automatic drift compensation
  
- Fast I2C Interface
- Event mode or Streaming modes
  
- 8 PWM LED/Output drivers (5mA source/10mA sink)
  - Hardware PWM set through I<sup>2</sup>C memory map – no overhead from host
  - Dimming modes available, up and down
  - Minimum, maximum & adjustable limit levels for dimming modes
  - Adjustable dimming speed
  
- Low Power, suitable for battery applications
- Supply voltage: 1.8V to 3.6V
- <3µA Active Sensing LP Mode



#### Applications

- Trackpads
- Remote Controls & Smart Remotes
- Electronic Keypads or Pin pads

#### Available options

|                |             |
|----------------|-------------|
| T <sub>A</sub> | QFR(5x5)-32 |
| -20°C to 85°C  | IQS360      |



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## Functional Overview

### 1 Introduction

The **IQS360** is a 12 channel mutual capacitive proximity and touch sensor capable of 4x3 Trackpad calculations, featuring an internal voltage regulator and reference capacitor ( $C_s$ ).

The **IQS360** implements a trackpad using 4 receivers, and 3 transmitters. Three pins are used for serial data communication through the I<sup>2</sup>C™ compatible protocol, including an optional RDY pin. Up to 4 configurable outputs provide 4 PWM or general purpose I/O's.

The device automatically tracks slow varying environmental changes via various filters, detects noise and is equipped with an Automatic Tuning Implementation (ATI) to adjust the device for optimal sensitivity.

#### 1.1 Applicability

All specifications, except where specifically mentioned otherwise, provided by this datasheet are applicable to the following ranges:

- Temperature -20°C to +85°C
- Supply voltage ( $V_{DDHI}$ ) 1.8V to 3.6V

### 2 Analogue Functionality

CRX and CTX electrodes are arranged in a suitable configuration that results in a mutual capacitance ( $C_m$ ) between the two electrodes. CTX is charged up to a set positive potential during a charge cycle which results in a negative charge buildup at CRX.

The resulting charge displacement is then measured within the **IQS360** device through a charge transfer process that is periodically initiated by the digital circuitry. The capacitance measurement circuitry

makes use of an internal reference capacitor  $C_s$  and voltage reference ( $V_{REF}$ ).

The measuring process is referred to as a conversion and consists of the discharging of  $C_s$  and  $C_x$  capacitors, the charging of  $C_x$  and then a series of charge transfers from  $C_x$  to  $C_s$  until a trip voltage is reached. The number of charge transfers required to reach the trip voltage is referred to as the Counts (CS) value.

The analogue circuitry further provides functionality for:

- Power On Reset (POR) detection.
- Brown Out Detection (BOD).
- Internal regulation provides for accurate sampling.

### 3 Digital Functionality

The digital processing functionality is responsible for:

- Managing BOD and WDT events.
- Initiation of conversions at the selected rate.
- Processing of counts values and execution of algorithms.
- Monitoring and execution of the ATI algorithm.
- Signal processing and digital filtering.
- Detection of PROX and TOUCH events.
- Managing outputs of the device.
- Managing serial communications.



## 4 Hardware Configuration

### 4.1 IQS360 Pin Out – QFN32

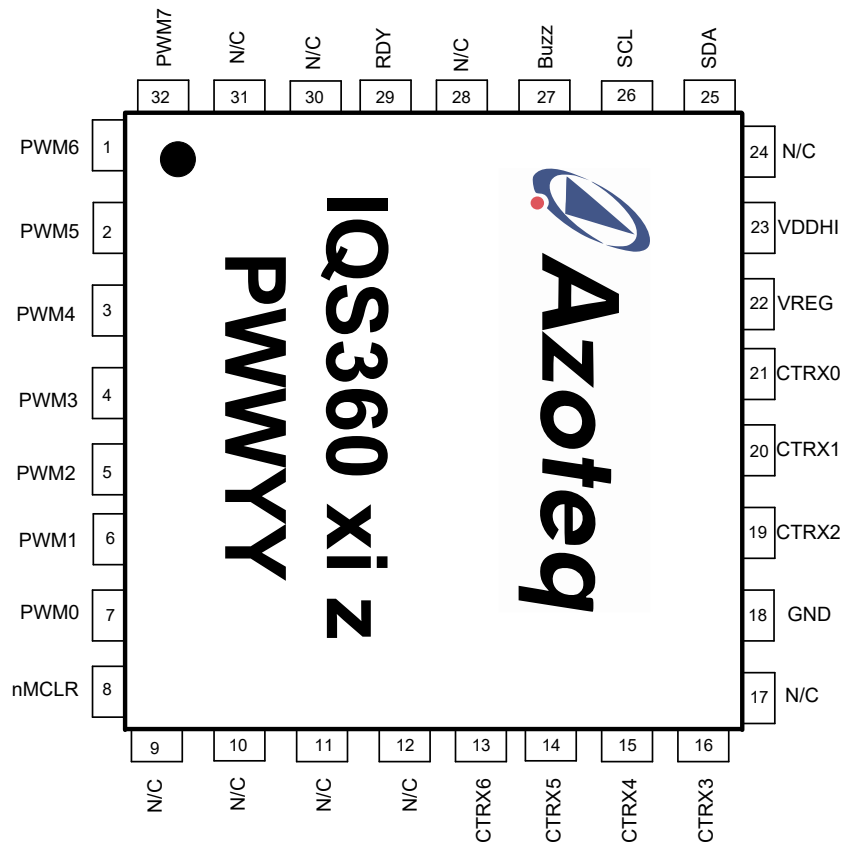


Figure 4.1 IQS360 Pin out in QFN-32.



Table 4.1 IQS360 QFN-32 Pin-outs.

| Pin | Pin Description           | Function               |
|-----|---------------------------|------------------------|
| 1   | PWM6                      | Output                 |
| 2   | PWM5                      | Output                 |
| 3   | PWM4                      | Output                 |
| 4   | PWM3                      | Output                 |
| 5   | PWM2                      | Output                 |
| 6   | PWM1                      | Output                 |
| 7   | PWM0                      | Output                 |
| 8   | NMCLR                     | Master Clear           |
| 9   | N/C                       | No Connect             |
| 10  | Internal use <sup>1</sup> | No Connect             |
| 11  | Internal use              | Connect to GND         |
| 12  | Internal use              | Connect to GND         |
| 13  | Tx2                       | Sense Electrode        |
| 14  | TX1                       | Sense Electrode        |
| 15  | TX0                       | Sense Electrode        |
| 16  | RX3                       | Sense Electrode        |
| 17  | N/C                       | No Connect             |
| 18  | GND                       | Supply Ground          |
| 19  | RX2                       | Sense Electrode        |
| 20  | RX1                       | Sense Electrode        |
| 21  | RX0                       | Sense Electrode        |
| 22  | VREG                      | Regulator Output       |
| 23  | VDDHI                     | Supply Input           |
| 24  | Internal use              | No Connect             |
| 25  | SDA                       | I <sup>2</sup> C Data  |
| 26  | SCL                       | I <sup>2</sup> C Clock |
| 27  | BUZ                       | Buzzer                 |
| 28  | N/C                       | Connect to GND         |
| 29  | RDY                       | Ready                  |
| 30  | N/C                       | No Connect             |
| 31  | N/C                       | No Connect             |
| 32  | PWM7                      | Output                 |

<sup>1</sup> Do not connect to GND



## 4.2 Reference Design

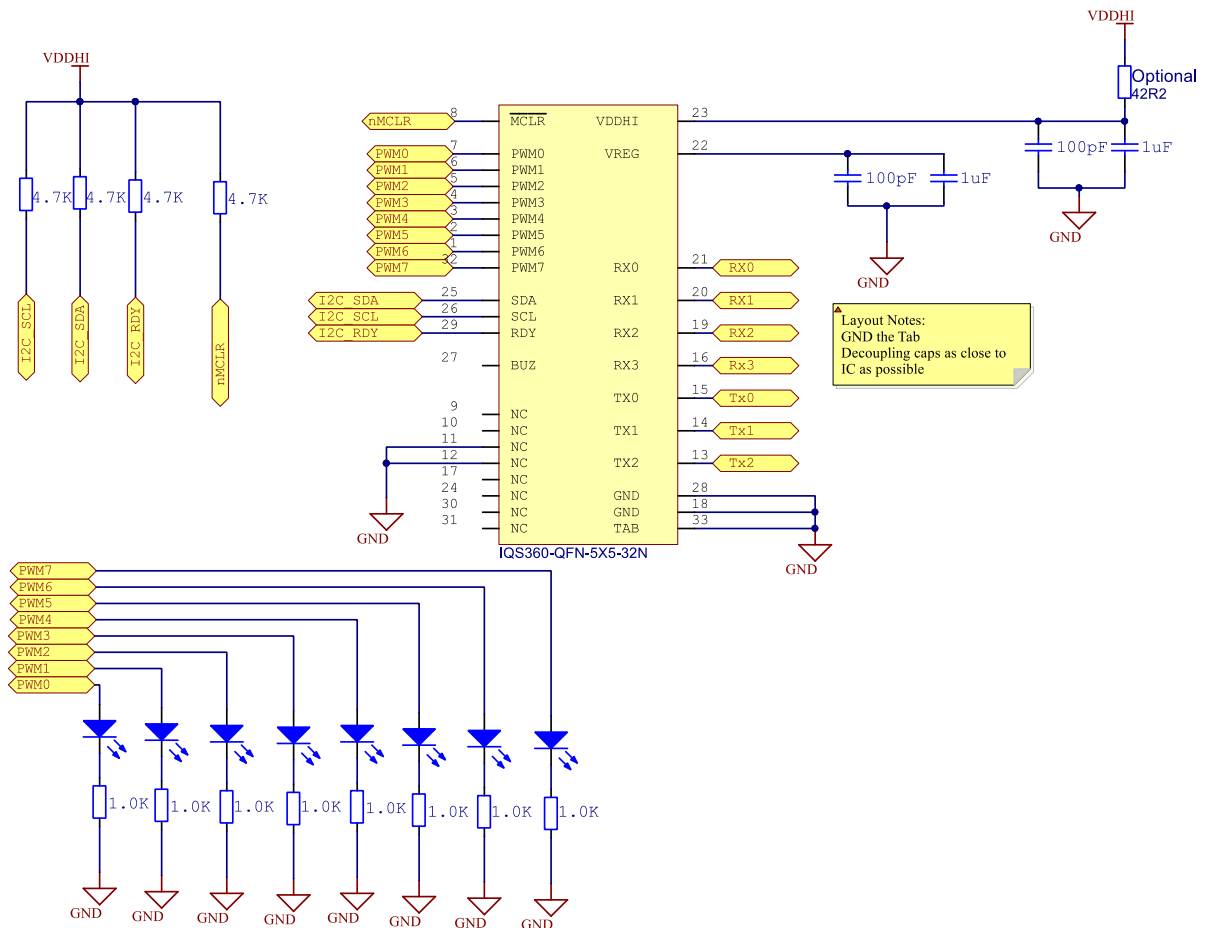


Figure 4.2 IQS360 Reference Design.

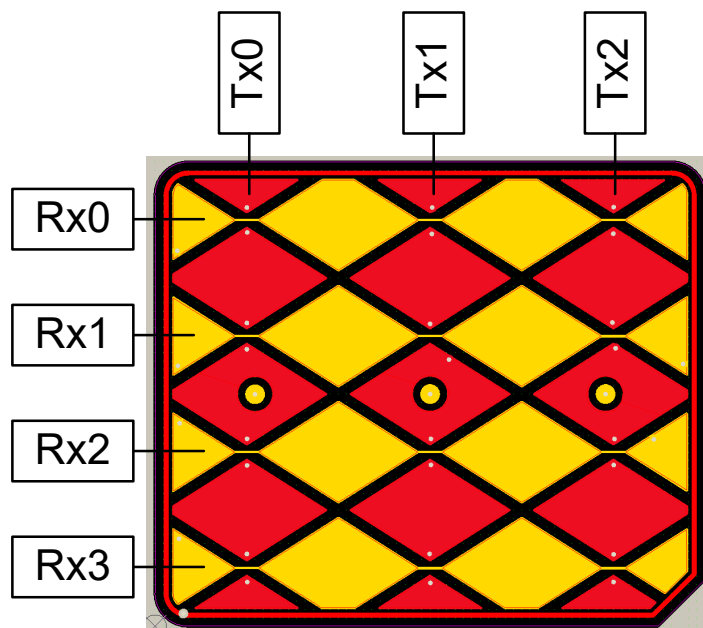


Figure 4.3 Trackpad Layout Reference. Refer to the Trackpad Design Guide, application note AZD068.

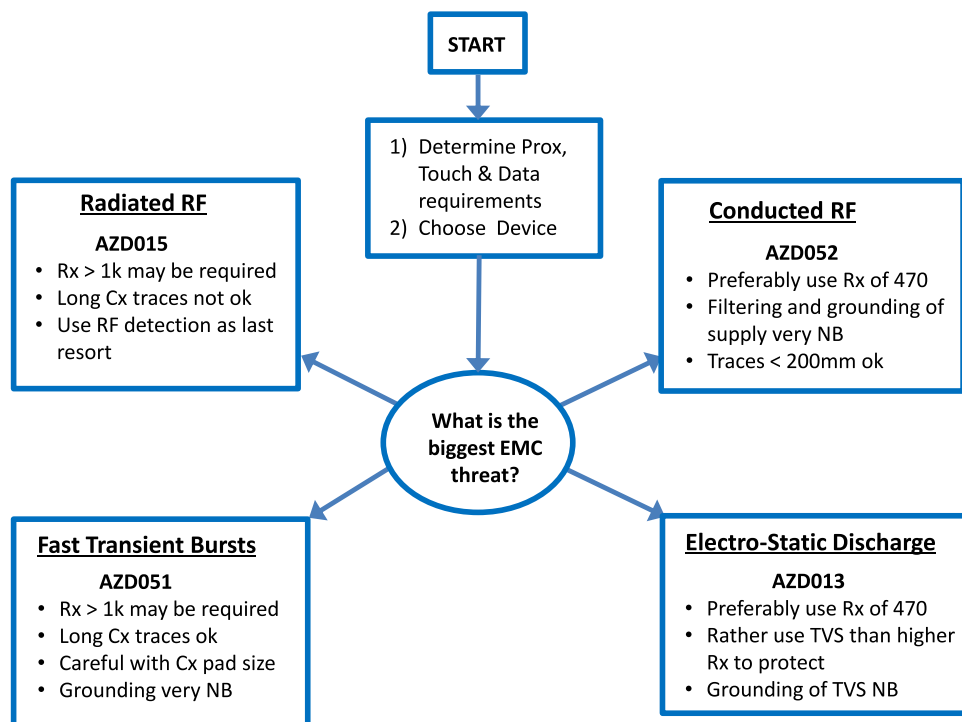


### 4.3 Power Supply and PCB Layout

Azoteq IC's provide a high level of on-chip hardware and software noise filtering and ESD protection (refer to application note “AZD013 – ESD Overview”). Designing PCB's with better noise immunity against EMI, FTB and ESD in mind, it is always advisable to keep the critical noise suppression components like the de-coupling capacitors and series resistors in **Figure 4.2** as close as possible to the IC. Always maintain a good ground connection and ground pour underneath the IC. For more guidelines please refer to the relevant application notes as mentioned in **Section 4.4**.

Where a system level ESD strike is found to cause the IC to go into ESD induced latch-up, it is suggested that the supply current to the IQS360 IC is limited by means of a series resistor that could limit the maximum supply current to the IC to <80mA.

### 4.4 Design Rules for Harsh EMC Environments



➤ **Applicable application notes: AZD013, AZD015, AZD051, AZD052.**

### 4.5 High Sensitivity

Through patented design and advanced signal processing, the device is able to provide extremely high sensitivity to detect proximity. This enables designs to detect proximity at distances that cannot be equaled by most other products. When the device is used in environments where high levels of noise or floating metal objects exist, a reduced proximity threshold is proposed to ensure reliable functioning of the sensor. The high sensitivity also allows the device to sense through overlay materials with low dielectric constants, such as wood or porous plastics.



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For more guidelines on the layout of capacitive sense electrodes, please refer to application note **AZD008**, available on the Azoteq web page: [www.azoteq.com](http://www.azoteq.com).





## 5 User Configurable Options

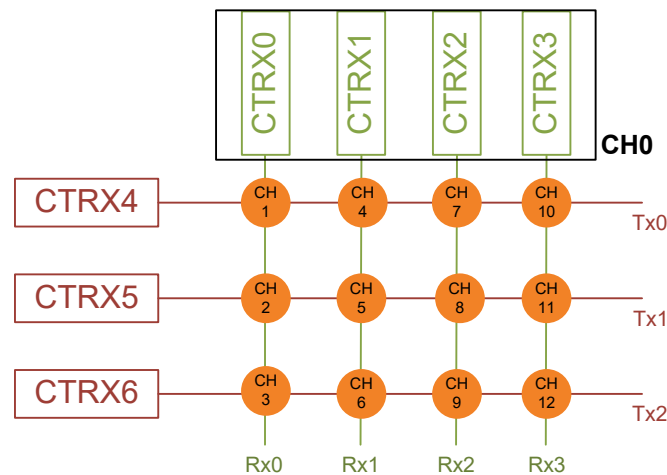
The **IQS360** requires configuration by a master/host controller or MCU. The user needs to select the number of channels, Trackpad size and corresponding touch and proximity thresholds.

### 5.1 Active Channels

The **IQS360** can be configured to have up to 12 active touch channels (CH1-CH12) with one additional proximity channel (CH0). By default CH0 is a distributed proximity channel, comprised of charging all electrodes together as self-capacitive electrodes.

The desired number of channels and the number of Trackpad channels can be selected in [Register 0x0EH](#). The active channels will be from 0 up to n, where channel n is the last channel (maximum 12 channels).

**Figure 5.1** illustrates the **IQS360** channels mapped to the respective transmit (CTX) and receive (CRX) sense electrodes.



**Figure 5.1** IQS360 Channel Mapping. In projected mode, CH0 can be selected as all the Rx electrodes or only Rx3 together will all the Tx electrodes.



## 5.2 Operational mode

As indicated on the reference schematic in Figure 4.2, the IQS360 is designed to function as a high speed Trackpad when connected to a diamond grid pattern. Several selections are available to increase the speed of available data, including disabling the LTA filters. The user has the option to read raw count values or XY-coordinates. XY data can be set to be absolute or relative values in [Register 0x08H](#) settings byte 3.

## 5.3 Proximity Threshold

A proximity threshold for channel 0 can be selected by the designer in [Register 0x09](#), byte 0, to obtain the desired proximity sensitivity. The proximity threshold is selectable between 1 (most sensitive) and 254 (least sensitive) counts. These threshold values (i.e. 1-255) are specified in Counts (CS). Note: The **IQS360** has a default proximity thresholds of  $P_{TH} = 16$ .

## 5.4 Touch Thresholds

A touch threshold for each channel can be selected by the designer to obtain the desired touch sensitivity and is selectable between 1/256 (most sensitive) to 255/256 (least sensitive). The touch threshold is calculated as a fraction of the Long-Term Average (LTA) given by,

$$T_{THR} = \frac{x}{256} \times LTA$$

With lower target values (therefore lower LTA's) the touch threshold will be lower and vice versa.

Individual touch thresholds can be set for each channel (excl. CH0) in [Register 0x09](#), byte 1 to 12, for channels 1 to 12.

Note: The **IQS360** has a default touch threshold of  $16/256 \times LTA$  for all active channels.

## 5.5 Halt times

The Halt Timer is started when a proximity or touch event occurs and is restarted when that event is removed or reoccurs. When a proximity condition occurs, the LTA value for channel 0 will be "halted", thus its value will be kept fixed, until the proximity event is cleared, or the halt timer reaches the halt time. The halt timer will count to the selected halt time ( $t_{HALT}$ ), which can be configured in [Register 0x0A](#), byte 0. When the timer expires, the output will be cleared, and a reseed or re-ATI event will occur (depending on whether the counts are within the ATI band).

It is possible that the CS (Count Value) could be outside the ATI boundary (ATI Target  $\pm 12.5\%$ ) when the timer expires, which will cause the device to perform a re-ATI event on that channel and not just a reseed event.

The designer needs to select a halt timer value ( $t_{HALT}$ ) to best accommodate the required application. The value of  $t_{HALT}$  is selectable between 1 and 255 (times 250ms). The default value is 0x50H (80 decimal times 250ms = 20 seconds).

There is also the option to set  $t_{HALT}$  timer to never halt, or always halt in [Register 0x08](#), Setting byte 2.

## 5.6 AC Filter

The AC filter can be implemented to provide better stability of Counts (CS) in electrically noisy environments.

The AC filter also enforces a longer minimum sample time for detecting proximity events on CH0, which will result in a slower response rate when the device enters low power modes. The AC filter is enabled by default, and can be disabled in [Register 0x08](#), Settings byte 2.

The AC filter is automatically switched off when Touch Events are made, to increase



the report rate for faster tracking. In some applications the count values may appear more noisy.

## 5.7 Power Modes

### 5.7.1 LP Modes

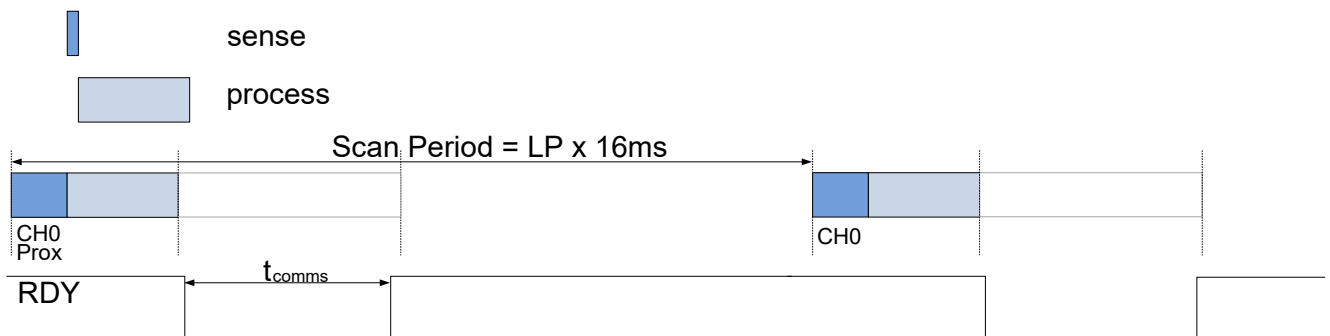
The IQS360 IC has a wide range of configurable low power modes, specifically designed to reduce current consumption for low power and battery applications.

The power modes are implemented around the occurrence of a charge cycle every  $t_{SAMPLE}$  seconds. The value of  $t_{SAMPLE}$  is determined by the custom ( $LP_{value}$ ) value between 1 and 255 in [Register 0x0A](#), byte 2, multiplied by 16ms.

Lower sampling frequencies typically yield significant lower power consumption (but also decreases the response time).

NOTE: While in any power mode the device will zoom to Boost Power (BP) mode whenever the condition  $(CS - LTA)^1 > PROX\_TH$  or  $TOUCH\_TH$  holds, indicating a possible proximity or touch event. This improves the response time. The device will remain in BP for  $t_{ZOOM}$  (4 seconds) after the last proximity event on CH0 is cleared and then return to the selected power mode. The Zoom function allows reliable detection of events with current samples being produced at the BP rate. The LP charge cycle timing is illustrated in **Figure 5.2**. The bit3 in [Register 0x10](#), byte 0, will indicate if low power is active, or the device is zoomed in.

When designing for low power operation, the  $V_{REG}$  capacitors should ensure that  $V_{REG}$  does not drop more than 50mV during low power operations.



**Figure 5.2 IQS360 Charge Cycle Timing in Low Power Mode.**

Typical timings of the charge sequence shown above are listed in Table 5.1. These timings are only as reference, as they will differ with each application, depending on the setup of the IQS360. For example, the sense (or charge time) is affected by the target counts and charge transfer frequency, while process time is dependent on the turbo mode activation, ATI checking for counts within the pre-set band, filter settings and XY-coordinate calculations. Communication time is affected by the MCU clock speed and the amount of data read (as well as the sequence thereof). Communication can be bypassed by using Event Mode.

<sup>1</sup> CS-LTA in Projected mode. LTA-CS in Self capacitive sensing mode.



**Table 5.1 Typical Timings in LP mode**

| Typical timings of IQS360 |                          |    |
|---------------------------|--------------------------|----|
| t <sub>sense</sub>        | 900                      | μs |
| t <sub>process</sub>      | 1.4                      | ms |
| t <sub>comms</sub>        | 6                        | ms |
| Scan Period               | LP register setting x 16 | ms |



### 5.7.2 Turbo Mode

Setting the Turbo Mode bit in [Register 0x08](#), Settings byte 1 will enable the **IQS360** device to perform conversions (charge transfers) as fast as processing and communication allows. Enabling Turbo Mode will maximize detection speeds, but also increase current consumption. Disabling Turbo Mode will yield in a fixed sampling period  $t_{\text{Sample}}$ .

## 5.8 Base Value

The **IQS360** has the option to individually change the base value of each channel during the ATI algorithm. Depending on the application, this provides the user with another option to select the sensitivity of the **IQS360** without changes in the hardware (CRX/CTX sizes and routing, etc).

The base values are set in [Register 0x06](#), byte 0 to 12 (for channels 0 to 12). The base values can be selected to be **100(default), 75, 150 or 200**.

The base value influences the overall sensitivity of the channel and establishes a base count from where the ATI algorithm starts executing. A lower base value will typically result in a higher sensitivity of the respective channel.

## 5.9 Target Value

The default target value of the **IQS360** is 512 for the proximity channel and the touch channels.

The target value is calculated by multiplying the value in [Register 0x0B](#), byte 0 (for channel 0) & 1 (for channels 1 to 12) by 8.

**Example:** CH0 target = [Register Value](#) x 8  
= 64(default) x 8 = 512.

## 5.10 Charge Transfer Speed

The frequency at which charge cycles are performed can be adjusted by the Charge Xfer Speed bits in the [Register 0x08](#), Settings byte 1.

Adjusting the charge transfer speed will change the charge cycle duration ( $t_{\text{CHARGE}}$ ) as shown in **Figure 5.2**.

The charge transfer frequency is a fraction of the main oscillator (FOSC = 8MHz or 4MHz) and can be set at **2MHz** (default) or **1MHz** (1MHz or 500kHz with FOSC set to 4MHz).

## 5.11 Snap (Dome click)

The **IQS360** has the option to enable snap detection on all active channels by setting the Snap\_Enable bit in [Register 0x08](#), Settings byte 0. The user can read the snap status in [Register 0x03](#), bytes 2 and 3.

When adding a metal snap-dome or carbon contact dome as the overlay to the trackpad pattern, an additional “Snap” function is available. The device is able to distinguish between a normal “touch” on the overlay and an actual button “snap”, which depresses the metal dome onto the Rx/Tx pattern. This output is referred to as a snap. The design must be configured so that a snap on the metal dome will result in a channels’ sample value falling well below the Long-Term Average value for that channel. A few suggestions are:

- Place the snap-dome directly above a channel (thus exactly on the Rx-Tx junction)
- Alternatively place the snap-dome in the centre of the diamond pattern, and add a round pad of the second sensor inside the diamond.
- The snap-dome must consist of the standard metal dome or carbon circle pattern (or similar conductive material) on the inside of the dome.
- This conductive dome must be of adequate size to provide good count



value deviation below the Long-Term Average of the channel on a snap.

- The conductive dome must however not be too big relative to the pitch of the Rx/Tx sensors, so as to not block the field lines for the trackpad sensing.
- No electrical connection between the snap-dome and the Rx-Tx must be made. Usually PCB solder-mask is adequate. Optimally the sensors are covered by solder-mask, with the snap-dome directly above.
- The snap-dome overlay must not have varying air-gaps between itself and the sensors. Thus having the overlay securely fastened to the PCB is ideal. A variable air-gap causes sporadic sensing, and gives unreliable data.

### 5.12 Block 7/5

When using the Reject Touches option (see Section 5.13), the **IQS360** has the option to set the Block Event on 7 and more touches instead of 5 or more touches, by setting the Block 7/5 bit in [Register 0x08](#), Settings byte 3. This feature is typically used in 4x3 applications, where the trackpad area is small.

### 5.13 Reject Touches

When Reject Touches is activated in Register 0x08, Settings byte 3, the **IQS360** will set the block event flag in Register 0x01, byte1 if more than 5 (or 7 depending on the Block setup) touches is detected at one time. This allows the user to decide if XY-data will be used, as 5 or more touches will be present on the grid, which is often the result of a flat user finger.

### 5.14 RX on Multiple

The **IQS360** Trackpad charges in Projected Capacitive mode. The proximity channel (CH0 will, however, charge in Self capacitive mode. By default, the **IQS360** will only charge CTRX3 (Rx3) for CH0. It is possible to set the **IQS360** to charge all 4 Rx lines as one distributed Self Capacitive Electrode. This is achieved by setting the Rx Multiple bit in [Register 0x08](#), Settings byte 3.

### 5.15 Prox Projected

The proximity channel on the **IQS360** CH0 can be changed to charge in projected capacitive mode<sup>1</sup>. This is achieved by setting the “Prox Proj” bit in [Register 0x08](#), Settings byte 1 (Prox\_Settings1). Projected proximity sensing can be used with a single Rx or all Rx electrodes. Single Rx is recommended for 3x3 trackpads, with proximity ring around the trackpad. For improved distance, a GND ring can be placed between the Rx ring and trackpad diamonds on the PCB layout. Rx on Multiple is recommended for 3x4 trackpads.

### 5.16 Force Sleep

The **IQS360** can be set to hibernate<sup>2</sup>, or go back to low power mode at any time, even if touches are still present, by setting the Force Sleep bit in [Register 0x08](#), Settings byte 1 (Prox\_Settings1). This will reseed CH0, and the **IQS360** will go into low power, and wake up with movement in the counts larger than the proximity threshold in any direction.

This mode allows the master to put the device into a low power state even if a user finger is still on the trackpad. If a stationary XY point is sensed by the master, such as a user resting his finger on the trackpad for a certain length of time a command is then sent by the master to the device to enter hibernation.

If for any reason the master wants to cancel the Touch Hibernate mode, then it must perform a ‘force comms’ similar to the way it does it in EVENT\_MODE, by performing a RDY handshake.

### 5.17 Relative Data

By default the **IQS360** will output Trackpad data as absolute XY-coordinates. It is possible to change this output to Relative Coordinates, but setting the Relative Coord bit in [Register 0x08](#), Settings byte 3.

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<sup>1</sup> QFN32 devices only

<sup>2</sup> QFN32 devices only



The relative data are also buffered, allowing the host controller to skip communication windows, but still read the total amount of travel of the user finger on the Trackpad.

## 5.18 Coordinate Filter

The XY data coordinate filter can be switched off to increase the report rate, but will influence the accuracy of the tracking data. To switch off the coordinate filter, set the Coord Filter bit in [Register 0x08](#), Settings byte 3. The filtering speed can also be set in [Register 0x10](#).

## 5.19 Additional Features

### 5.19.1 Halt Charge

Setting the Halt Charge bit in [Register 0x08](#), Settings byte 1, will stop all conversions.

This function is typically useful for ultra-low power requirements, where the **IQS360** can be controlled by a host MCU and does not require wake-up on proximity or touch events.

During Halt Charge, a 512ms wake up timer is used. The VREG capacitor needs to ensure VREG does not drop more than 100mV during Halt Charge. A capacitor of 4.7uA or bigger is suggested. For applications using Halt Charge, pin 11 and pin 12 needs to be connected to GND.

### 5.19.2 Force Halt

The Force Halt bit in [Register 0x08](#), Settings byte 2 can be set to halt all current LTA values and prevent them from being adjusted towards the CS values.

Setting this bit overrides all filter halt settings and prevents the device from performing re-ATI events in cases where the CS values persist outside the ATI boundaries for extended periods of time. Reseed will also not be possible.

### 5.19.3 CTX / CRX Float

During the charge transfer process, the channels that are not being processed during the current cycle, are effectively grounded to decrease the effects of noise-coupling between the sense electrodes.

In [Register 0x08](#), Settings byte 5, there is the option to specify which channels' transmit and/or receive electrodes to float when they are not charged.

### 5.19.4 Proj Bias

The **IQS360** has the option to change the bias current of the transmitter during projected sensing mode. A larger bias current is required to use larger electrodes, but will also increase the IC power consumption. The bias current is default on 10μA, and can be changed in [Register 0x08](#), Settings byte 0.

### 5.19.5 Cs Size

Another method to adjust the sensitivity of the **IQS360** is to change the size of the internal C<sub>s</sub> capacitor. The size on default is 60pF, but can be changed to 30pF by setting the Cs\_Size bit in [Register 0x08](#), Settings byte 0. Choosing the smaller C<sub>s</sub> size will effectively half the counts for the same multiplier and compensation values. Redo ATI will be required to reach the ATI target.

### 5.19.6 Soft Reset

The user has the option to do a soft reset on the **IQS360**. The soft reset will clear all the registers (the device will restart as with POR) except the PWM register will keep their state.

A soft reset is initiated by setting the bit in [Register 0x08](#), Settings byte 2. The bit Soft Reset bit will automatically clear after the command is sent.

### 5.19.7 LTA Beta

The beta value of all channels LTA filters can be adjusted by setting the Beta bits in [Register 0x08](#), Settings byte 3.



### 5.19.8 Projected Up and Pass time

The up and pass times for the charge transfer can be set in [Register 0x08](#), Settings byte 4. It is suggested to use the longest past time (0x07) for most applications. Note the default value for Settings byte 4 is 0x00.

## 6 ProxSense® Module

The **IQS360** contains a ProxSense® module that uses patented technology to provide detection of proximity and touch conditions on numerous sensing lines.

The ProxSense® module is a combination of hardware and software, based on the principles of charge transfer measurements.

### 6.1 Charge Transfer Concept

On ProxSense® devices like the **IQS360**, capacitance measurements are taken with a charge transfer process that is periodically initiated.

For mutual capacitive sensing, the device measures the capacitance between 2 electrodes referred to as the transmitter (CTX) and receiver (CRX).

The measuring process is referred to as a charge transfer cycle and consists of the following:

- Discharging of an internal sampling capacitor ( $C_s$ ) and the electrode capacitors (mutual: CTX & CRX) on a channel.
- charging of CTX's connected to the channel
- and then a series of charge transfers from the CRX's to the internal sampling capacitors ( $C_s$ ), until the trip voltage is reached.

The number of charge transfers required to reach the trip voltage on a channel is referred to as the Current Sample (**CS**) or Count value.

The device continuously repeats charge transfers on the sense electrodes connected to the CRX pins. For each channel a Long Term Average (**LTA**) is calculated (12 bit unsigned integer values). The count (CS) values (12 bit unsigned integer values) are processed and compared to the LTA to detect Touch and Proximity events.

For more information regarding capacitive sensing, refer to the application note: "**AZD004 – Azoteq Capacitive Sensing**".

**Please note: Attaching scope probes to the CTX/CRX pins will influence the capacitance of the sense electrodes and therefore the related CS values of those channels. This will have an instant effect on the CS measurements.**

### 6.2 Rate of Charge Cycles

The **IQS360** samples all its active channels (up to 12 + channel 0 for proximity) in 13 timeslots. The charge sequence (as measured on the receive electrodes) is shown in Figure 6.1, where CH0 is the Proximity channel, charges first, followed by all other active channels. There is only a communication window after all active channels have been charged, and processing is completed during the next charge transfer (therefore after channel 0).

By default channel 0 charges on CTRX3 only, but can be configured to be a distributed electrode in [Register 0x08](#), Settings byte 3.

Then charging of CH0 comprises the simultaneous charging of the 4 receive electrodes (CRX0, CRX1, CRX2 and CRX3) in Self-Capacitive mode, thus realising a distributed load. Refer to **Figure 5.1** for **IQS360** channel numbering.

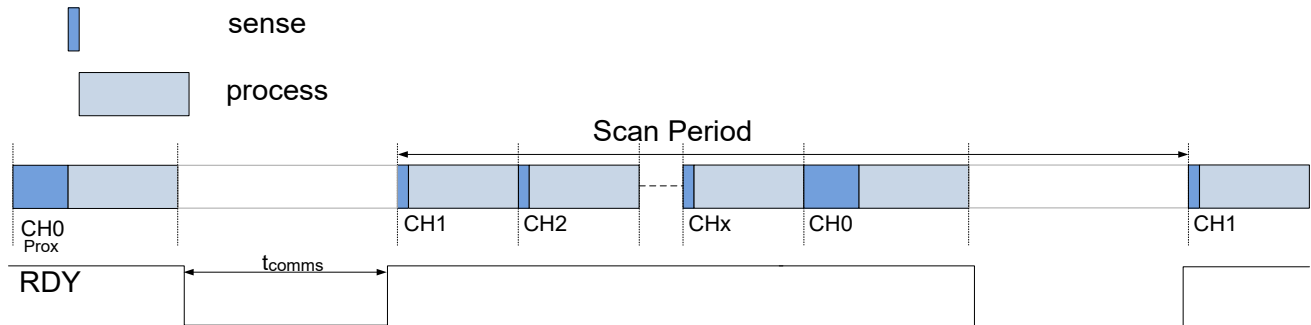




### 6.2.1 Boost Power rate

With the **IQS360** zoomed to Boost Power (BP) mode, the sense channels are charged at a fixed sampling period ( $t_{SAMPLE}$ ) per channel. This is done to ensure regular samples for processing of results.

It is calculated as each channel having a time ( $t_{SAMPLE} = \text{charge period } (t_{CHARGE}) + \text{computation time}$ ) of approximately  $t_{SAMPLE} = 1.6\text{ms}$ . Thus the time between consecutive samples on a specific channel ( $t_{CH}$ ) will depend on the number of enabled channels, the charge transfer speed and the length of communication between the **IQS360** and the host MCU.



**Figure 6.1 IQS360 charge cycle timing diagram in Boost Power mode.**

Typical timings of the charge sequence shown above are listed in Table 6.1. These timings are only as reference, as they will differ with each application, depending on the setup of the IQS360. For example, the sense (or charge time) is affected by the target counts and charge transfer frequency, while process time is dependent on the turbo mode activation, ATI checking for counts within the pre-set band, filter settings and XY-coordinate calculations. Communication time is affected by the MCU clock speed and the amount of data read (as well as the sequence thereof).

**Table 6.1 Typical Timings**

| Typical timings of IQS360 |        |                 |               |
|---------------------------|--------|-----------------|---------------|
| $t_{sense}$               |        | 200             | $\mu\text{s}$ |
| $t_{process}$             |        | 1.4             | ms            |
| $t_{comms}$               |        | 6               | ms            |
| Scan Period <sup>1</sup>  | Turbo  | 27.5            | ms            |
|                           | Normal | 35 <sup>2</sup> | ms            |

<sup>1</sup> All channels active, with all data being read during communication window. All settings default.

<sup>2</sup> Includes sleep time to force constant sample period.



### 6.2.2 Low Power rate

A wide range of low current consumption charging modes is available on the **IQS360**.

In any Low Power (LP) mode, there will be an applicable low power time ( $t_{LP}$ ). This is determined by [Register 0x0A](#), byte 1. The value written into this register multiplied by 16ms will yield the LP time ( $t_{LP}$ ).

With the detection of an undebounced proximity event the IC will zoom to BP mode, allowing a very fast reaction time for further possible touch events.

During any LP mode, only CH0 is charged every  $T_{LP}$ . The LP charge timing is illustrated in **Figure 5.2**.

If a low power rate is selected and charging is not in the zoomed state (BP mode), the low power active bit (Register 0x01) will be set.

Please refer to **Section 1.1**.

### 6.3 Touch report Rate

During Boost Power (BP) mode, the touch report rate of the **IQS360** device depends on the charge transfer frequency, the number of channels enabled and the length of communications performed by the host MCU or master device (influenced by the I<sup>2</sup>C clock frequency and the number of data bytes read).

Several factors may influence the touch report rate (and essential the XY data report rate from the Trackpad):

- **Enabled channels:** Disabling channels that are not used will not only increase the touch report rate, but will also reduce the device's current consumption.
- **Turbo Mode:** See Section 5.7.2
- **Target Values:** Lower target values requires shorter charge transfer periods ( $t_{CHARGE}$ ), thus reducing the overall sampling period ( $t_{SAMPLE}$ ) of each channel and increasing the touch report

rate.

- **Charge Transfer Speed:** Increasing the charge transfer frequency will reduce the conversion period ( $t_{CHARGE}$ ) and increase the touch report rate.
- **Internal Clock.** The **IQS360** has the ability to reduce the internal oscillator frequency from 8MHz to 4MHz in [Register 0x01H](#), byte 1. This will reduce power consumption, but will also slow down the report rate.

### 6.4 Long Term Average

The Long-term Average (LTA) filter can be seen as the baseline or reference value. The LTA is calculated to continuously adapt to any environmental drift. The LTA filter is calculated from the CS value for each channel. The LTA filter allows the device to adapt to environmental (slow moving) changes/drift. Actuation (Touch or Prox) decisions are made by comparing the CS value with the LTA reference value.

The 12bit LTA value for the indicated active channel ([ACT\\_CHAN](#) register [0x3D]) is contained in the [LTA\\_HI](#) and [LTA\\_LO](#) registers (0x83 and 0x84).

Please refer to **Section 5.5** for LTA Halt Times.

### 6.5 Determine Touch or Prox

An event is determined by comparing the CS value with the LTA. Since the CS reacts differently when comparing the self- with the mutual capacitance technology, the user should consider only the conditions for the technology used.

An event is recorded if:

- Self:  $CS < LTA - \text{Threshold}$
- Mutual:  $CS > LTA + \text{Threshold}$

**Threshold** can be either a Proximity or Touch threshold, depending on the current channel being processed.

Note that a proximity condition will be forced enabled on a certain channel if a



touch condition exists on that channel, even if the  $P_{TH}$  is greater than the  $T_{TH}$ .

Please refer to **Section 5.3** and **5.4** for proximity and touch threshold selections.

## 6.6 ATI

The **Automatic Tuning Implementation (ATI)** is a sophisticated technology implemented on the new ProxSense® series devices. It allows for optimal performance of the devices for a wide range of sense electrode capacitances, without modification or addition of external components.

The ATI allows the tuning of two parameters, an ATI Multiplier and an ATI Compensation, to adjust the sample value for an attached sense electrode.

ATI allows the designer to optimize a specific design by adjusting the sensitivity and stability of each channel through the adjustment of the ATI parameters.

The **IQS360** has a full ATI function. The full-ATI function is default enabled, but can be disabled by setting the `ATI_OFF` and `ATI_Partial` bits in [Register 0x08](#), Settings byte 0.

The `ATI_Busy` bit in [Register 0x01H](#), byte 1 will be set while an ATI event is busy.

For more information regarding the ATI algorithm, please contact Azoteq at: [ProxSenseSupport@azoteq.com](mailto:ProxSenseSupport@azoteq.com)

### 6.6.1 ATI Method

The **IQS360** can be set up to perform sensor calibration in two ways: Full ATI and Partial ATI. The ATI method is selected in [Register 0x08](#), Settings byte 0.

In Full ATI mode, the device automatically selects the multipliers through the ATI algorithm to setup the **IQS360** as close as possible to its default sensitivity for the environment where it was placed.

The user can however, select Partial ATI, and set the multipliers to a pre-configured value. This will cause the **IQS360** to only calculate the compensation (not the compensation and multipliers as in Full ATI), which allows the freedom to make the **IQS360** more or less sensitive for its intended environment of use. The Partial ATI also reduces start-up and re-ATI times.

### 6.6.2 ATI Sensitivity

On the **IQS360** device, the user can specify the `BASE` value (**Section 5.8**) for each channel individually and the `TARGET` values (**Section 5.9**) for the proximity (`CH0`) and touch (`CH1-CH9`) channels.

Sensitivity is a function of the base and target values as follows:

$$\text{Sensitivity} \propto \frac{\text{TARGET}}{\text{BASE}}$$

As can be seen from this equation, the sensitivity can be increased by either increasing the Target value or decreasing the Base value. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility.

### 6.6.3 ATI Target

The target value is reached by adjusting the `COMPENSATION` bits for each channel (ATI target limited to 2096 counts).

The target value is written into the respective channel's `TARGET` registers. The value written into these registers multiplied by 8 will yield the new target value. (Please refer to **Section 5.9**)

### 6.6.4 ATI Base (Multiplier)

The base value is calculated with the compensation set to zero. The following parameters will influence the base value:

- `CS_SIZE1`: Size of sampling capacitor.
- `PROJ_BIAS` bits: Adjusts the biasing of some analogue parameters in the

---

<sup>1</sup> Changing `CS_SIZE` if `ATI_OFF` = 0 will change CS



mutual capacitive operated IC. (Only applicable in mutual capacitance mode.)

- MULTIPLIER bits.

The base value used for the ATI function can be implemented in 2 ways:

1. ATI\_PARTIAL = 0. ATI automatically adjusts MULTIPLIER bits to reach a selected base value<sup>1</sup>. Please refer to **Section 5.8** for available base values.
2. ATI\_PARTIAL = 1. The designer can specify the multiplier settings. These settings will give a custom base value from where the compensation bits will be automatically implemented to reach the required target value. The base value is determined by two sets of multiplier bits. Sensitivity Multipliers which will also scale the compensation to normalise the sensitivity and Compensation Multipliers to adjust the gain.

### 6.6.5 Re-ATI

An automatic re-ATI event will occur if the CS is outside its re-ATI limits and no event is present on the applicable channel. The re-ATI limit or ATI boundary is calculated as the target value divided by 8. For example:

- Target = 512, Re-ATI will occur if CS is outside 512±64.

A re-ATI event can also be issued by the host MCU by setting the REDO\_ATI bit in [Register 0x08](#), Settings byte 0. The REDO\_ATI bit will clear automatically after the ATI event was started.

Note: Re-ATI will automatically clear all proximity, touch, snap and halt status bits.

### 6.6.6 Reseed

Setting the Reseed bit in [Register 0x08](#), Settings byte 0, will reseed all LTA filters to a value of  $LTA_{new} = CS + 8$ . The LTA will then track the CS value until they are even.

Performing a reseed action on the LTA filters, will effectively clear any proximity and/or touch conditions that may have been established prior to the reseed call.

### 6.6.7 ATI Band

The user has the option to select the re-ATI band as 1/8 of the ATI target (default) or 1/4 of the ATI target counts by setting the ATI BAND bit in [Register 0x08](#), byte 1 (Prox\_Settings1).

### 6.6.8 ATI ERROR

The ATI error bit (read only) in [Register 0x01](#), byte 1 (Sysflags) indicates to the user that the ATI targets were not reached. Adjustments of the base values or ATI BANDs are required.

<sup>1</sup> ATI function will use user selected CS\_SIZE and PROJ\_BIAS (if applicable) and will only adjust the MULTIPLIER bits to reach the base values.

## 7 Communication

The **IQS360** device interfaces to a master controller via a 3-wire (SDA, SCL and RDY) serial interface bus that is I<sup>2</sup>C™ compatible, with a maximum communication speed of 400kbit/s.

### 7.1 I<sup>2</sup>C Sub-address

The **IQS360** has four available sub addresses, 64H (default) to 67H, which allows up to four devices on a single I<sup>2</sup>C bus.

#### 7.1.1 Internal sub-address selection

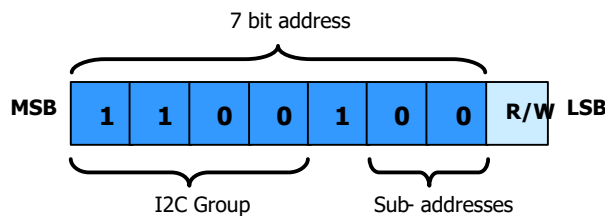
Selecting the sub-address via OTP bits allows the user 4 different options:

**Table 7.1 I<sup>2</sup>C sub-address selection**

| FG25 | FG26 | Device Address |
|------|------|----------------|
| 0    | 0    | 0x64           |
| 0    | 1    | 0x65           |
| 1    | 0    | 0x66           |
| 1    | 1    | 0x67           |

### 7.2 Control Byte

The Control byte indicates the 7-bit device address (64H default) and the Read/Write indicator bit. The structure of the control byte is shown in Figure 7.1.

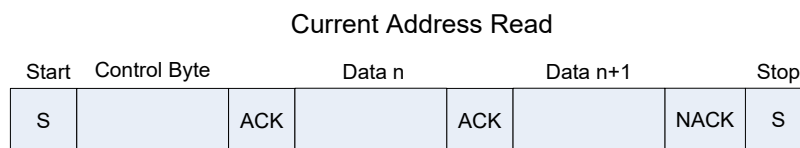


**Figure 7.1 IQS360 Control Byte.**

The I<sup>2</sup>C device has a 7 bit Slave Address (default 0x64H) in the control byte as shown in Figure 7.1. To confirm the address, the software compares the received address with the device address. Sub-address values can be set by OTP programming options.

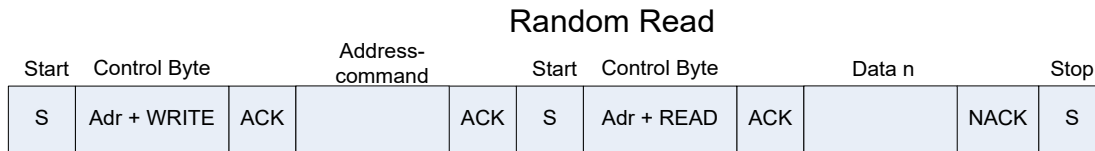
### 7.3 I<sup>2</sup>C Read

To read from the device a *current address read* can be performed. This assumes that the address-command is already setup as desired.



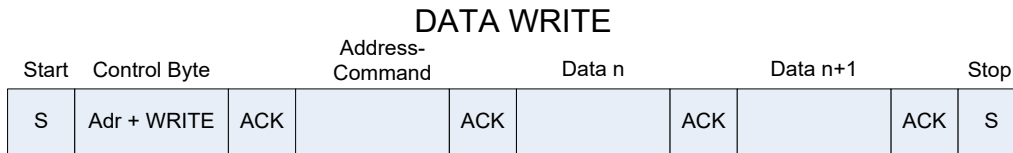
**Figure 7.2 Current Address Read.**

If the address-command must first be specified, then a *random read* must be performed. In this case a WRITE is initially performed to setup the address-command, and then a repeated start is used to initiate the READ section.



### 7.4 Random Read.I<sup>2</sup>C Write

To write settings to the device a *Data Write* is performed. Here the Address-Command is always required, followed by the relevant data bytes to write to the device.



**Figure 7.3 I<sup>2</sup>C Write.**

### 7.5 End of Communication Session / Window

Similar to other Azoteq I<sup>2</sup>C devices, to end the I<sup>2</sup>C communication session, a STOP command is given. When sending numerous read and write commands in one communication cycle, a repeated start command must be used to stack them together (since a STOP will jump out of the communication window, which is not desired).

The STOP will then end the communication, and the **IQS360** will return to process a new set of data. Once this is obtained, the communication window will again become available (RDY set LOW).

### 7.6 Event Mode

The **IQS360** device can operate in an event-driven I<sup>2</sup>C communication mode (also called “Event Mode”), with the RDY pin ONLY indicating a communication window after a prescribed event has occurred (except for the Setup Window after POR).

These events include:

- Proximity events
- Touch events
- ATI events
- Tracking events
- Snap events
- Block events

Event Mode can be enabled by setting the Event Mode bit in [Register 0x08](#), Settings byte 2.

Note: The device is also capable of functioning **without** a RDY line on a polling basis.

### 7.7 RDY Hand-Shake Routine

The master or host MCU has the capability to force a communication window at any time, by pulling the RDY line low. The communication window will open directly following the current conversion.

### 7.8 I<sup>2</sup>C Specific Commands

#### 7.8.1 Show Reset

The SHOW\_RESET bit can be read in [Register 0x01](#), byte 0, to determine whether a reset has occurred on the device. This bit will be set '1' after a reset.

The SHOW\_RESET bit will be cleared (set to '0') by writing a '1' into the ACK\_RESET bit in [Register 0x08](#), Settings byte 1. A reset will typically take place of a timeout during communication occurs.

#### 7.8.2 WDT disable

The WDT (watchdog timer) is used to reset the IC if a problem (for example a voltage spike) occurs during communication. The WDT will time-out (and thus reset the



device) after  $t_{WDT}$  if no valid communication occurred during this time.

The WDT can be disabled by setting the WDT Off bit in [Register 0x08](#), Settings byte 2.

### 7.8.3 Timeout Disable

If no communication is initiated from the master/host MCU within the first  $t_{COMMS}$  ( $t_{COMMS} = 20ms$ ) of the RDY line indicating that data is available (i.e. RDY = low), the device will resume with the next charge transfer cycle and the data from the previous conversion cycle will be lost. The **IQS360** does, however, have the ability to buffer relative XY-data for use in application where a read is possible less frequently on the master controller.

This time-out function can be disabled by setting the TIME\_OUT\_DISABLE bit in [Register 0X08](#), Settings byte 2.

## 7.9 I<sup>2</sup>C I/O Characteristics

The **IQS360** requires the input voltages given in **Table 7.2**, for detecting high (“1”) and low (“0”) input conditions on the I<sup>2</sup>C communication lines (SDA, SCL and RDY).

**Table 7.2 IQS360 I<sup>2</sup>C Input voltage**

|                     | Input Voltage (V) |
|---------------------|-------------------|
| V <sub>inLOW</sub>  | 0.3*VDDHI         |
| V <sub>inHIGH</sub> | 0.7*VDDHI         |

Table 7.3 provides the output voltage levels of the **IQS360** device during I<sup>2</sup>C communication.

**Table 7.3 IQS360 I<sup>2</sup>C Output voltage**

|                      | Output Voltage (V) |
|----------------------|--------------------|
| V <sub>outLOW</sub>  | VSS +0.2 (max.)    |
| V <sub>outHIGH</sub> | VDDHI – 0.2 (min.) |



## 8 PWM Controller

The **IQS360** incorporates a highly configurable PWM controller to implement user configurable LED lighting displays. The various PWM control modes can be easily configured with an I<sup>2</sup>C interface by writing directly to the control bytes in the memory map. There are 8 identical PWM modules with 15.625kHz PWM carrier frequency which can be controlled independently to allow for a wide range of user configurable options

### 8.1 PWM Dimming modes

The hardware PWM channels can be controlled through the memory map various dimming modes. These include:

- Incrementing to 100%
- Incrementing to a set level
- Decrementing to 0%
- Decrementing to a set level

The speed of the dimming modes is also configurable.

### 8.2 Dimming During LP

Because the **IQS360** PWM lines requires the use of FOSC to output correctly, the PWM lines cannot be used if low power modes are required in the application. During low power the main oscillator on the **IQS360** goes to sleep which results in dimming changes on all PWM lines.

### 8.3 PWM Duty Cycle Mapping

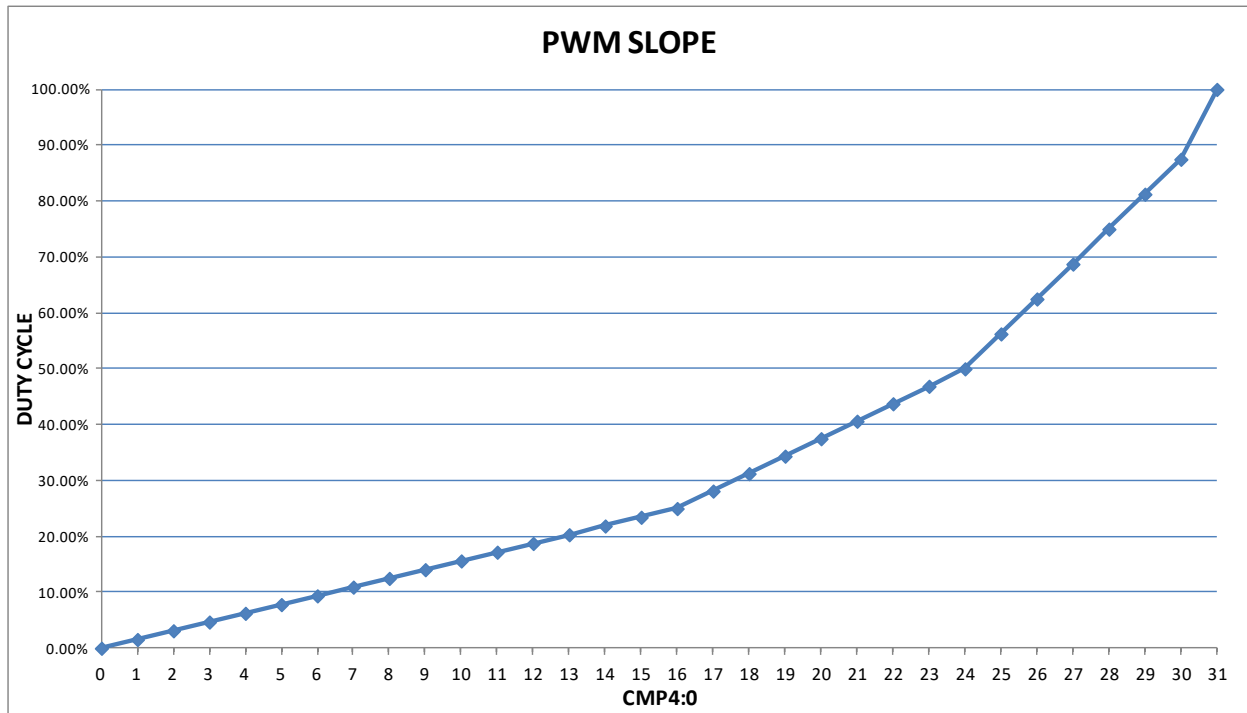
Although there are only 5 PWM bits in the MM, the resolution of the PWM engine is effectively 6 bits to ensure a more linear increase in LED brightness. A 6 bit internal timer is compared to a PWM value

comprised of CMP4:0 in [Register 0x0C](#), bytes 0 to 3.

**Table 8.1 PWM Duty Cycle Mapping**

| CMP4:0 | PWM Timer Count | PWM DUTY |
|--------|-----------------|----------|
| 0      | 0               | 0.00%    |
| 1      | 1               | 1.56%    |
| 2      | 2               | 3.13%    |
| 3      | 3               | 4.69%    |
| 4      | 4               | 6.25%    |
| 5      | 5               | 7.81%    |
| 6      | 6               | 9.38%    |
| 7      | 7               | 10.94%   |
| 8      | 8               | 12.50%   |
| 9      | 9               | 14.06%   |
| 10     | 10              | 15.63%   |
| 11     | 11              | 17.19%   |
| 12     | 12              | 18.75%   |
| 13     | 13              | 20.31%   |
| 14     | 14              | 21.88%   |
| 15     | 15              | 23.44%   |
| 16     | 16              | 25.00%   |
| 17     | 18              | 28.13%   |
| 18     | 20              | 31.25%   |
| 19     | 22              | 34.38%   |
| 20     | 24              | 37.50%   |
| 21     | 26              | 40.63%   |
| 22     | 28              | 43.75%   |
| 23     | 30              | 46.88%   |
| 24     | 32              | 50.00%   |
| 25     | 36              | 56.25%   |
| 26     | 40              | 62.50%   |
| 27     | 44              | 68.75%   |
| 28     | 48              | 75.00%   |
| 29     | 52              | 81.25%   |
| 30     | 56              | 87.50%   |
| 31     | 64              | 100.00%  |





**Figure 8.1 PWM Slope.**



## 9 RF Noise

### 9.1 RF Noise Immunity

The **IQS360** has advanced immunity to RF noise sources such as GSM cellular telephones, DECT, Bluetooth and WIFI devices. Design guidelines should however be followed to ensure the best noise immunity on a hardware level.

In general, the design of capacitive sensing applications may encompass a large range of configurations; however, following the guidelines in **Section 9.1.1** may improve a capacitive sensing design.

#### 9.1.1 Notes for layout:

- A ground plane should be placed under the IC, except under the CRX lines.
- Place the sensor IC as close as possible to the sense electrodes.
- All the tracks on the PCB must be kept as short as possible.
- The capacitor between VDDHI and GND as well as between VREG and GND must be placed as close as possible to the IC.
- A 100 pF capacitor can be placed in parallel with the 1uF capacitor between VDDHI and GND. Another 100 pF capacitor can be placed in parallel with the 1uF capacitor between VREG and GND.
- When the device is too sensitive for a specific application a parasitic capacitor (max 5pF) can be added between the CX line and ground.
- Proper sense electrode and button design principles must be followed.
- Unintentional coupling of sense electrodes to ground and other circuitry must be limited by increasing the distance to these sources.
- In some instances a ground plane some distance from the device and sense electrode may provide significant shielding from undesirable interference.

- \* However, if after proper layout, interference from an RF noise source persists, please refer to application note: “**AZD015: RF Immunity and detection in ProxSense devices**”.



## 10 Communication Command/Address Structure

### 10.1 Registers

Table 10.1 IQS360 Registers

| Address | Description                | Access | Section |
|---------|----------------------------|--------|---------|
| 0x00H   | <b>Device Information</b>  | R      | 10.2.1  |
| 0x01H   | <b>System Flags</b>        | R      | 10.2.2  |
| 0x02H   | <b>XY-Data</b>             | R      | 10.2.3  |
| 0x03H   | <b>Status</b>              | R      | 10.2.4  |
| 0x04H   | <b>Counts</b>              | R      | 10.2.5  |
| 0x05H   | <b>LTA</b>                 | R      | 10.2.6  |
| 0x06H   | <b>Multipliers</b>         | R/W    | 10.2.7  |
| 0x07H   | <b>Compensation</b>        | R/W    | 10.2.8  |
| 0x08H   | <b>Settings</b>            | R/W    | 10.2.9  |
| 0x09H   | <b>Thresholds</b>          | R/W    | 10.2.10 |
| 0x0AH   | <b>Timings</b>             | R/W    | 10.2.11 |
| 0x0BH   | <b>ATI Targets</b>         | R/W    | 10.2.12 |
| 0x0CH   | <b>PWM</b>                 | R/W    | 10.2.13 |
| 0x0DH   | <b>PWM LIM &amp; SPEED</b> | R/W    | 10.2.14 |
| 0x0EH   | <b>Active Channels</b>     | R/W    | 10.2.15 |
| 0x0FH   | <b>Snap Thresholds</b>     | R/W    | 10.2.16 |
| 0x10H   | <b>Correction Constant</b> | R/W    | 10.2.17 |
| 0x11H   | <b>Buzzer</b>              | R/W    | 10.2.18 |



## 10.2 Registers Descriptions

### 10.2.1 Device Information 0x00H

Information regarding the device type and version is recorded here. Any other information specific to the device version can be stored here. Each Azoteq ROM has a unique Product- and Version number.

|        |       | Product Number (PROD_NUM) |   |   |   |   |   |   |   |
|--------|-------|---------------------------|---|---|---|---|---|---|---|
| Access | Bit   | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R      | Value | 55 (Decimal) <sup>1</sup> |   |   |   |   |   |   |   |

|        |       | Version Number (VERSION_NUM) |   |   |   |   |   |   |   |
|--------|-------|------------------------------|---|---|---|---|---|---|---|
| Access | Bit   | 7                            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R      | Value | 01 (Decimal)                 |   |   |   |   |   |   |   |

### 10.2.2 System Flags 0x01H

|        |      | System Flags (SYSFLAGS) |               |       |        |           |          |                |      |
|--------|------|-------------------------|---------------|-------|--------|-----------|----------|----------------|------|
| Access | Bit  | 7                       | 6             | 5     | 4      | 3         | 2        | 1              | 0    |
| R      | Name | Show reset              | Filter Halted | 8M 4M | Is Ch0 | LP Active | ATI Busy | Noise detected | Zoom |

|        |      | Events    |             |            |   |             |             |            |           |
|--------|------|-----------|-------------|------------|---|-------------|-------------|------------|-----------|
| Access | Bit  | 7         | 6           | 5          | 4 | 3           | 2           | 1          | 0         |
| R      | Name | ATI ERROR | Block Event | Snap Event | ~ | Track Event | Touch Event | Prox Event | ATI Event |

<sup>1</sup> Product and Version number will be 32 13 for QFN20 – for alpha customers only



### 10.2.3 XY-Data 0x02H

|        |      | X Low                 |   |   |   |   |   |   |   |
|--------|------|-----------------------|---|---|---|---|---|---|---|
| Access | Bit  | 7                     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R      | Name | X Coordinate Low Byte |   |   |   |   |   |   |   |
| Byte 0 |      |                       |   |   |   |   |   |   |   |

|        |      | X High                 |   |   |   |   |   |   |   |
|--------|------|------------------------|---|---|---|---|---|---|---|
| Access | Bit  | 7                      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R      | Name | X Coordinate High Byte |   |   |   |   |   |   |   |

|        |      | Y Low                 |   |   |   |   |   |   |   |
|--------|------|-----------------------|---|---|---|---|---|---|---|
| Access | Bit  | 7                     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R      | Name | Y Coordinate Low Byte |   |   |   |   |   |   |   |

|        |      | Y High                 |   |   |   |   |   |   |   |
|--------|------|------------------------|---|---|---|---|---|---|---|
| Access | Bit  | 7                      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R      | Name | Y Coordinate High Byte |   |   |   |   |   |   |   |
| Byte 3 |      |                        |   |   |   |   |   |   |   |

### 10.2.4 Status 0x03H

|        |      | Touch Channels 0 |     |     |     |     |     |     |              |
|--------|------|------------------|-----|-----|-----|-----|-----|-----|--------------|
| Access | Bit  | 7                | 6   | 5   | 4   | 3   | 2   | 1   | 0            |
| R      | Name | CH7              | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0/<br>Prox |
| Byte 0 |      |                  |     |     |     |     |     |     |              |



|               |             | Touch Channels 1 |          |          |          |          |          |          |          |
|---------------|-------------|------------------|----------|----------|----------|----------|----------|----------|----------|
| <b>Access</b> | <b>Bit</b>  | <b>7</b>         | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>R</b>      | <b>Name</b> |                  |          |          | CH12     | CH11     | CH10     | CH9      | CH8      |

|               |             | Snap Channels 0 |          |          |          |          |          |          |          |
|---------------|-------------|-----------------|----------|----------|----------|----------|----------|----------|----------|
| <b>Access</b> | <b>Bit</b>  | <b>7</b>        | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>R</b>      | <b>Name</b> | CH7             | CH6      | CH5      | CH4      | CH3      | CH2      | CH1      |          |

|               |             | Snap Channels 1 |          |          |          |          |          |          |          |
|---------------|-------------|-----------------|----------|----------|----------|----------|----------|----------|----------|
| <b>Access</b> | <b>Bit</b>  | <b>7</b>        | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>R</b>      | <b>Name</b> |                 |          |          | CH12     | CH11     | CH10     | CH9      | CH8      |
| <b>Byte 3</b> |             |                 |          |          |          |          |          |          |          |

### 10.2.5 Counts 0x04H

|               |             | CH0 Low                              |          |          |          |          |          |          |          |
|---------------|-------------|--------------------------------------|----------|----------|----------|----------|----------|----------|----------|
| <b>Access</b> | <b>Bit</b>  | <b>7</b>                             | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>R</b>      | <b>Name</b> | Channel 0 CS (Counts) Low byte first |          |          |          |          |          |          |          |

|               |             | CH n High   |          |          |          |          |          |          |          |
|---------------|-------------|---|----------|----------|----------|----------|----------|----------|----------|
| <b>Access</b> | <b>Bit</b>  | <b>7</b>  | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>R</b>      | <b>Name</b> | Last active channel, Count value (High byte last) |          |          |          |          |          |          |          |

### 10.2.6 LTA 0x05H

|               |             | CH0 LTA Low byte             |          |          |          |          |          |          |          |
|---------------|-------------|------------------------------|----------|----------|----------|----------|----------|----------|----------|
| <b>Access</b> | <b>Bit</b>  | <b>7</b>                     | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>R</b>      | <b>Name</b> | Channel 0 LTA Low byte first |          |          |          |          |          |          |          |



|        |      | CH n LTA High byte                              |   |   |   |   |   |   |   |
|--------|------|---|---|---|---|---|---|---|---|
| Access | Bit  | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R      | Name | Last active channel, LTA value (High byte last) |   |   |   |   |   |   |   |

### 10.2.7 Multipliers 0x06H

|        |      | CH0 Multipliers |   |             |   |   |   |   |   |
|--------|------|-----------------|---|-------------|---|---|---|---|---|
| Access | Bit  | 7               | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
| R      | Name | Base            |   | Multipliers |   |   |   |   |   |

**Bit 7:6:** 00 = 100 (default)  
01 = 75  
10 = 150  
11 = 200

|        |      | CH n Multipliers |   |             |   |   |   |   |   |
|--------|------|------------------|---|-------------|---|---|---|---|---|
| Access | Bit  | 7                | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
| R      | Name | Base             |   | Multipliers |   |   |   |   |   |

### 10.2.8 Compensation 0x07H

|        |      | CH0 Compensation value           |   |   |   |   |   |   |   |
|--------|------|----------------------------------|---|---|---|---|---|---|---|
| Access | Bit  | 7                                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name | Compensation value for Channel 0 |   |   |   |   |   |   |   |
| Byte 0 |      |                                  |   |   |   |   |   |   |   |

|        |      | CH n Compensation Value                    |   |   |   |   |   |   |   |
|--------|------|--|---|---|---|---|---|---|---|
| Access | Bit  | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name | Compensation value for last Active Channel |   |   |   |   |   |   |   |
| Byte n |      |  |   |   |   |   |   |   |   |



### 10.2.9 Settings 0x08H

|        |         | Settings 0                  |                                 |                                 |                              |                        |                                    |                           |   |
|--------|---------|-----------------------------|---------------------------------|---------------------------------|------------------------------|------------------------|------------------------------------|---------------------------|---|
| Access | Bit     | 7                           | 6                               | 5                               | 4                            | 3                      | 2                                  | 1                         | 0 |
| R/W    | Name    | <a href="#">ATI<br/>OFF</a> | <a href="#">ATI<br/>Partial</a> | <a href="#">Snap<br/>Enable</a> | <a href="#">Redo<br/>ATI</a> | <a href="#">Reseed</a> | <a href="#">C<sub>s</sub> Size</a> | <a href="#">Proj Bias</a> |   |
| Byte 0 | Default | 0x06                        |                                 |                                 |                              |                        |                                    |                           |   |

- Bit 7:** 0 = Automatic Retuning is On  
1 = Automatic Retuning is OFF (counts can drift outside the ATI band)
- Bit 6:** 0 = Full ATI  
1 = Partial ATI (Multipliers needs to be se manually for base value)
- Bit 5:** 0 = Disabled  
1 = Snap detection Enabled
- Bit 4:** 0 = No action  
1 = ATI retunes (bit clears automatically)
- Bit 3:** 0 = No action  
1 = Reseeds LTA values (bit clears automatically)
- Bit 2:** 0 = Small  
1 = Large (default)
- Bit 1:0:** 00 = 2.5µA  
01 = 5µA  
10 = 10µA (default)  
11 = 20µA





|        |         | Settings 1                |                      |                            |                             |   |                           |                             |                          |
|--------|---------|---------------------------|----------------------|----------------------------|-----------------------------|---|---------------------------|-----------------------------|--------------------------|
| Access | Bit     | 7                         | 6                    | 5                          | 4                           | 3 | 2                         | 1                           | 0                        |
| R/W    | Name    | <a href="#">ACK Reset</a> | <a href="#">XFER</a> | <a href="#">Turbo Mode</a> | <a href="#">Halt Charge</a> | ~ | <a href="#">Prox Proj</a> | <a href="#">Force Sleep</a> | <a href="#">ATI Band</a> |
| Byte 1 | Default | 0x00H                     |                      |                            |                             |   |                           |                             |                          |

- Bit 7:** 0 = No Action  
1 = Clears the Reset Flag (bit will clear automatically)
- Bit 6:** 0 = 2MHz  
1 = 1MHz
- Bit 5:** 0 = Disabled  
1 = Turbo Mode Enabled
- Bit 4:** 0 = No action  
1 = Halts Conversions
- Bit 3:** Internal Use
- Bit 2:** 0 = Self Proximity Sensing  
1 = Projected Proximity Sensing
- Bit 1:** 0 = No Action  
1 = Force Low Power Mode (bit will clear upon Low Power Exit)
- Bit 0:** 0 = 1/8 x LTA  
1 = 1/4 x LTA



|        |         | Settings 2                 |                         |                            |                             |                          |                            |                      |   |
|--------|---------|----------------------------|-------------------------|----------------------------|-----------------------------|--------------------------|----------------------------|----------------------|---|
| Access | Bit     | 7                          | 6                       | 5                          | 4                           | 3                        | 2                          | 1                    | 0 |
| R/W    | Name    | <a href="#">Soft Reset</a> | <a href="#">WDT Off</a> | <a href="#">Force Halt</a> | <a href="#">ACF Disable</a> | <a href="#">Time Out</a> | <a href="#">Event Mode</a> | <a href="#">Halt</a> |   |
| Byte 2 | Default | 0x00H                      |                         |                            |                             |                          |                            |                      |   |

- Bit 7:** 0 = No Action  
1 = Software Reset (all settings default except PWM)
- Bit 6:** 0 = WDT ON  
1 = WDT OFF
- Bit 5:** 0 = No Action  
1 = All LTA values halted at current level (no ATI possible)
- Bit 4:** 0 = No action  
1 = Counts Filtering disabled
- Bit 3:** 0 = No action  
1 = Communication Timeout Disabled
- Bit 2:** 0 = Full Streaming  
1 = Event Mode Streaming
- Bit 1-0:** 00 = Filter Halt Period (set in 0x0A)  
01 = Filter Halt Period (set in 0x0A)  
10 = Never Halt  
11 = Always Halt (not applicable on Snap Events)



|        |         | Settings 3                |   |                      |   |                              |                                |                                |                              |
|--------|---------|---------------------------|---|----------------------|---|------------------------------|--------------------------------|--------------------------------|------------------------------|
| Access | Bit     | 7                         | 6 | 5                    | 4 | 3                            | 2                              | 1                              | 0                            |
| R/W    | Name    | <a href="#">Block 7/5</a> |   | <a href="#">Beta</a> |   | <a href="#">Reject Touch</a> | <a href="#">RX on Multiple</a> | <a href="#">Relative Coord</a> | <a href="#">Coord Filter</a> |
| Byte 3 | Default | 0x06H                     |   |                      |   |                              |                                |                                |                              |

**Bit 7:** 0 = Reject Touches on 5 or more touches  
1 = Reject Touches on 7 or more touches

**Bit 6:** Internal Use

**Bit 5:4:** 00 = 2<sup>5</sup>  
01 = 2<sup>6</sup>  
10 = 2<sup>7</sup>  
11 = 2<sup>8</sup>

**Bit 3:** 0 = No action  
1 = Reject Touches Active

**Bit 2:** 0 = Proximity Sensing with CTRX3  
1 = Proximity Sensing with all Rx or Cx electrodes

**Bit 1:** 0 = Absolute Coordinates  
1 = Relative Coordinates

**Bit 0:** 0 = Filtered XY Data  
1 = Unfiltered XY Data

|        |         | Settings 4 |    |    |    |       |      |      |      |
|--------|---------|------------|----|----|----|-------|------|------|------|
| Access | Bit     | 7          | 6  | 5  | 4  | 3     | 2    | 1    | 0    |
| R/W    | Name    |            | UP | UP | UP | UP_EN | PASS | PASS | PASS |
| Byte 5 | Default | 0x07H      |    |    |    |       |      |      |      |

|        |         | Setting 5                 |   |   |   |   |   |   |   |
|--------|---------|---------------------------|---|---|---|---|---|---|---|
| Access | Bit     | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | <a href="#">CTR_X_VSS</a> |   |   |   |   |   |   |   |
| Byte 6 | Default | 0x7FH                     |   |   |   |   |   |   |   |



### 10.2.10 Thresholds 0x09H

|        |         | CH0 Threshold       |   |   |   |   |   |   |   |
|--------|---------|---------------------|---|---|---|---|---|---|---|
| Access | Bit     | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Proximity Threshold |   |   |   |   |   |   |   |
| Byte 0 | Default | 04H                 |   |   |   |   |   |   |   |

|        |         | Channel 1 Threshold       |   |   |   |   |   |   |   |
|--------|---------|---------------------------|---|---|---|---|---|---|---|
| Access | Bit     | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Channel 1 Touch Threshold |   |   |   |   |   |   |   |
| Byte 1 | Default | 10H                       |   |   |   |   |   |   |   |

|         |         | Channel 12 Threshold       |   |   |   |   |   |   |   |
|---------|---------|----------------------------|---|---|---|---|---|---|---|
| Access  | Bit     | 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W     | Name    | Channel 12 Touch Threshold |   |   |   |   |   |   |   |
| Byte 12 | Default | 10H                        |   |   |   |   |   |   |   |

### 10.2.11 Timings 0x0AH

|        |         | Filter Halt (t <sub>HALT</sub> ) <sup>1</sup> |   |   |   |   |   |   |   |
|--------|---------|---|---|---|---|---|---|---|---|
| Access | Bit     | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Steps of 250ms                                |   |   |   |   |   |   |   |
| Byte 0 | Default | 0x4FH   |   |   |   |   |   |   |   |

|        |         | Power Mode (LP) |   |   |   |   |   |   |   |
|--------|---------|-----------------|---|---|---|---|---|---|---|
| Access | Bit     | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Steps of 16ms   |   |   |   |   |   |   |   |
| Byte 1 | Default | 0x00H           |   |   |   |   |   |   |   |

<sup>1</sup> See errata for t<sub>HALT</sub> > 0x10H.



|        |         | Timeout Period  |   |   |   |   |   |   |   |
|--------|---------|-----------------|---|---|---|---|---|---|---|
| Access | Bit     | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Steps of 1.28ms |   |   |   |   |   |   |   |
| Byte 2 | Default | 0x02H           |   |   |   |   |   |   |   |

### 10.2.12 ATI Targets 0x0BH

|        |         | ATI Target CH0 |   |   |   |   |   |   |   |
|--------|---------|----------------|---|---|---|---|---|---|---|
| Access | Bit     | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Steps of 8     |   |   |   |   |   |   |   |
| Byte 0 | Default | 0x40H          |   |   |   |   |   |   |   |

|        |         | ATI Targets CH1 to CH 12 |   |   |   |   |   |   |   |
|--------|---------|--------------------------|---|---|---|---|---|---|---|
| Access | Bit     | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Steps of 8               |   |   |   |   |   |   |   |
| Byte 1 | Default | 0x20H                    |   |   |   |   |   |   |   |

### 10.2.13 PWM 0x0CH

|        |         | PWM 0 |   |   |         |   |   |   |   |
|--------|---------|-------|---|---|---------|---|---|---|---|
| Access | Bit     | 7     | 6 | 5 | 4       | 3 | 2 | 1 | 0 |
| R/W    | Name    | Mode  |   |   | Compare |   |   |   |   |
| Byte 0 | Default |       |   |   |         |   |   |   |   |

|        |         | PWM 7 |   |   |         |   |   |   |   |
|--------|---------|-------|---|---|---------|---|---|---|---|
| Access | Bit     | 7     | 6 | 5 | 4       | 3 | 2 | 1 | 0 |
| R/W    | Name    | Mode  |   |   | Compare |   |   |   |   |
| Byte 3 | Default |       |   |   |         |   |   |   |   |

Bit 7-5: **MODE2:MODE0**: Selects PWM mode.



- 000 = PWM Off
- 001 / 010 / 011 = PWM Constant
- 100 = PWM CMP4:0 decremented and stops at 0%
- 101 = PWM CMP4:0 decremented and stops at value in PWM\_LIM
- 110 = PWM CMP4:0 incremented and stops at 100%
- 111 = PWM CMP4:0 incremented and stops at value in PWM\_LIM

Bit 4-0: **CMP4:0**: LED Duty Cycle Value

### 10.2.14 PWM LIM 0x0DH

|        |         | PWM Lim |   |   |         |   |   |   |   |
|--------|---------|---------|---|---|---------|---|---|---|---|
| Access | Bit     | 7       | 6 | 5 | 4       | 3 | 2 | 1 | 0 |
| R/W    | Name    |         |   |   | PWM LIM |   |   |   |   |
| Byte 0 | Default |         |   |   |         |   |   |   |   |

Bit 7-5: **System Use**

Bit 4-0: **LIM4:LIM0**: CMP 4:0 is compared against this value if MODE 2:0 is configured 101 or 111

|        |         | PWM SPEED |   |   |   |           |   |   |   |
|--------|---------|-----------|---|---|---|-----------|---|---|---|
| Access | Bit     | 7         | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
| R/W    | Name    |           |   |   |   | PWM SPEED |   |   |   |
| Byte 1 | Default |           |   |   |   |           |   |   |   |

Bit 7-4: **System Use**

Bit 3-0: **SPD3:SPD0**: PWM slope adjustment speed control

$$PWM\ Timing = SPD3:0 \times [CMP4:0 + 1] \times 8.192ms$$

**Example:**

SPD3:0 = 0100

CMP4:0 = 11111 (PWM Duty = 100%)

$$Ton = 4 \times [31 + 1] \times 8.192ms = 1.0486s$$



### 10.2.15 Active Channels 0x0EH

|        |      | Active Channels 0 |     |     |     |     |     |     |     |
|--------|------|-------------------|-----|-----|-----|-----|-----|-----|-----|
| Access | Bit  | 7                 | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| R      | Name | CH7               | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
| Byte 0 |      |                   |     |     |     |     |     |     |     |

|        |      | Active Channels 1 |   |   |      |      |      |     |     |
|--------|------|-------------------|---|---|------|------|------|-----|-----|
| Access | Bit  | 7                 | 6 | 5 | 4    | 3    | 2    | 1   | 0   |
| R      | Name |                   |   |   | CH12 | CH11 | CH10 | CH9 | CH8 |

|        |      | Trackpad Active Channels 0 |     |     |     |     |     |     |     |
|--------|------|----------------------------|-----|-----|-----|-----|-----|-----|-----|
| Access | Bit  | 7                          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| R      | Name | CH7                        | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |

|        |      | Trackpad Active Channels 1 |   |   |      |      |      |     |     |
|--------|------|----------------------------|---|---|------|------|------|-----|-----|
| Access | Bit  | 7                          | 6 | 5 | 4    | 3    | 2    | 1   | 0   |
| R      | Name |                            |   |   | CH12 | CH11 | CH10 | CH9 | CH8 |
| Byte 3 |      |                            |   |   |      |      |      |     |     |

### 10.2.16 Snap Thresholds 0x0FH

|        |         | Channel 1 Snap Threshold |   |   |   |   |   |   |   |
|--------|---------|--------------------------|---|---|---|---|---|---|---|
| Access | Bit     | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Channel 1 Snap Threshold |   |   |   |   |   |   |   |
| Byte 0 | Default | 0x18H                    |   |   |   |   |   |   |   |



|         |         | Channel 12 Threshold      |   |   |   |   |   |   |   |
|---------|---------|---------------------------|---|---|---|---|---|---|---|
| Access  | Bit     | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W     | Name    | Channel 12 Snap Threshold |   |   |   |   |   |   |   |
| Byte 11 | Default | 0x18H                     |   |   |   |   |   |   |   |

### 10.2.17 Trackpad Filters 0x10H

|        |         | Count Filter              |   |   |   |   |   |   |   |
|--------|---------|---------------------------|---|---|---|---|---|---|---|
| Access | Bit     | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Counts Filtering Constant |   |   |   |   |   |   |   |
| Byte 0 | Default | 0x01H                     |   |   |   |   |   |   |   |

|        |         | XY BETA (Slow)   |   |   |   |   |   |   |   |
|--------|---------|--|---|---|---|---|---|---|---|
| Access | Bit     | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Trackpad Coordinate Filter Constant for Slow Filtering |   |   |   |   |   |   |   |
| Byte 0 | Default | 0x03H  |   |   |   |   |   |   |   |

|        |         | XY BETA (Fast)   |   |   |   |   |   |   |   |
|--------|---------|--|---|---|---|---|---|---|---|
| Access | Bit     | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | Trackpad Coordinate Filter Constant for Fast Filtering |   |   |   |   |   |   |   |
| Byte 0 | Default | 0x00H  |   |   |   |   |   |   |   |

|        |         | DYNAMIC_XY_THRESHOLD |   |   |   |   |   |   |   |
|--------|---------|----------------------|---|---|---|---|---|---|---|
| Access | Bit     | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R/W    | Name    | XY                   |   |   |   |   |   |   |   |
| Byte 0 | Default | 0x0AH                |   |   |   |   |   |   |   |

Changes in the XY coordinates will be filter with the slow Beta if it is smaller than the Dynamic\_XY\_Threshold. If changes in XY coordinates are larger than the Dynamic\_XY\_Threshold, the coordinates will be filtered with the fast Beta.





### 10.2.18 Buzzer Output 0x11H

|        |         | Buzzer 0 |   |   |   |   |    |      |       |
|--------|---------|----------|---|---|---|---|----|------|-------|
| Access | Bit     | 7        | 6 | 5 | 4 | 3 | 2  | 1    | 0     |
| R/W    | Name    | Enable   |   |   |   |   | DC | PERM | Burst |
| Byte 0 | Default | 0x00H    |   |   |   |   |    |      |       |

This Byte sets up the Buzzer as shown below:

**Bit 7:**            **Enable:** This bit enables or Disables the Buzzer output

0 = Disabled

1 = Enabled

**Bit 6-3:**       **Not Used**

**Bit 2:**           **DC:** Makes a DC output

0 = Low

1 = High

**Bit 1:**           **Perm:** Permanently sounding the buzzer

0 = Disabled

1 = Enabled

**Bit 0:**           **Burst:** Burst mode to make a “click” sound

0 = Disabled

1 = Enabled



## 11 IQS360 OTP Options

The **IQS360** only provide OTP (**O**ne-**T**ime **P**rogrammable) options for configuration of the device I<sup>2</sup>C sub-address.

Configuration of the OTP settings can be done on packaged devices or in-circuit. In-circuit configuration may be limited by values of external components chosen.

Azoteq offers a Configuration Tool (CT210 or later) and associated software that can be used to program the OTP user options for prototyping purposes. For further information regarding this subject, please contact your local distributor or submit enquiries to Azoteq at: [ProxSenseSupport@azoteq.com](mailto:ProxSenseSupport@azoteq.com)

### 11.1 User Selectable OTP options

**Table 11.1 User Selectable OTP options : Bank3**

| bit7       | Bank 3     |            |            |            |                           |                           | bit0       |
|------------|------------|------------|------------|------------|---------------------------|---------------------------|------------|
| System use | System use | System use | System use | System use | I <sup>2</sup> C SubAddr1 | I <sup>2</sup> C SubAddr0 | System use |

|                       |  |
|-----------------------|--|
| <b>Bank3: bit7</b>    | <b>System Use</b>  |
| <b>Bank3: bit6</b>    | <b>System Use</b>  |
| <b>Bank3: bit5</b>    | <b>System Use</b>  |
| <b>Bank3: bit4</b>    | <b>System Use</b>  |
| <b>Bank3: bit 3</b>   | <b>System Use</b>  |
| <b>Bank3: bit 2:1</b> | <b>I<sup>2</sup>C SubAddr1: I<sup>2</sup>C SubAddr0 : I<sup>2</sup>C Sub-Address selection</b> |
|                       | 00 = 0x64<br>01 = 0x65<br>10 = 0x66<br>11 = 0x67   |
| <b>Bank3: bit 0</b>   | <b>System Use</b>  |



## 12 Specifications

### 12.1 Absolute Maximum Specifications

The following absolute maximum parameters are specified for the device:

*Exceeding these maximum specifications may cause damage to the device.*

- Operating temperature -20°C to 85°C
- Supply Voltage (VDDHI – VSS) 3.6V
- Maximum pin voltage VDDHI + 0.5V (may not exceed VDDHI max)
- Maximum continuous current (for specific Pins) 10mA
- Minimum pin voltage VSS - 0.5V
- Minimum power-on slope 100V/s
- ESD protection ±8kV (Human body model)
- Package Moisture Sensitivity Level (MSL) 3

**Table 12.1 IQS360 General Operating Conditions<sup>1</sup>**

| DESCRIPTION               | Conditions                    | PARAMETER           | MIN  | TYP  | MAX  | UNIT |
|---------------------------|-------------------------------|---------------------|------|------|------|------|
| Supply voltage            |                               | V <sub>DDHI</sub>   | 1.8  | 3.3V | 3.6  | V    |
| Internal regulator output | 1.8 ≤ V <sub>DDHI</sub> ≤ 3.6 | V <sub>REG</sub>    | 1.62 | 1.7  | 1.79 | V    |
| Default Operating Current | 3.3V                          | I <sub>IQS360</sub> | -    | 530  |      | µA   |
| Low Power Setting 8*      | 3.3V, LP=8                    | 128ms               | -    | 14   |      | µA   |
| Low Power Setting 16*     | 3.3V, LP=16                   | 256ms               | -    | 8    |      | µA   |
| Low Power Setting 32*     | 3.3V, LP=32                   | 512ms               | -    | <6   |      | µA   |

\*LP interval period = Low power value x 16ms

**Table 12.2 Start-up and shut-down slope Characteristics**

| DESCRIPTION      | Conditions                                | PARAMETER | MIN | MAX | UNIT |
|------------------|---|-----------|-----|-----|------|
| Power On Reset   | V <sub>DDHI</sub> Slope ≥ 100V/s<br>@25°C | POR       |     | 1.6 | V    |
| Brown Out Detect | V <sub>DDHI</sub> Slope ≥ 100V/s<br>@25°C | BOD       | 1   |     | V    |

<sup>1</sup>Operating current shown in this datasheet, does not include power dissipation through I<sup>2</sup>C pull up resistors.



## 12.2 Moisture Sensitivity Level

**Moisture Sensitivity Level (MSL)** relates to the packaging and handling precautions for some semiconductors. The MSL is an electronic standard for the time period in which a moisture sensitive device is allowed to be exposed to ambient room conditions (approximately 30°C/60%RH) before reflow must occur.

**Table 12.3 MSL**

| Package   | Level (duration)  |
|-----------|-------------------|
| QFN5x5-32 | MSL 3 (168 hours) |
| QFR5x5-32 | MSL 3 (168 hours) |

## 12.3 Recommended storage environment

This storage environment assumes that the IC's are packed properly inside a humidity barrier bag:

| Parameter        | Description          | Min | Typ | Max | Unit | Notes  |
|------------------|----------------------|-----|-----|-----|------|--|
| T <sub>STG</sub> | Storage Temperature  | -55 | 25  | 150 | °C   | Recommended storage temperature is 25 °C ± 25 °C. Extended duration storage at temperatures above 85 °C degrades reliability as well as reduces data retention performance |
| T <sub>j</sub>   | Junction Temperature |     |     | 150 |      |  |

### 12.3.1 Supplementary notes according to Jedec recommendations:

- Optimal Storage Temperature Range: 5 °C to 30 °C
- Humidity: between 40 to 70% RH - Avoid condensation
- Air should be clean - Avoid harmful gasses and dust
- Avoid outdoor exposure or storage in areas subject to rain or water spraying
- Avoid storage in areas subject to corrosive gas or dust. Products shall not be stored in areas exposed to direct sunlight
- Avoid rapid changes of temperature
- Mechanical stress such as vibration and impact shall be avoided
- The products shall not be placed directly on the floor
- The products shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall

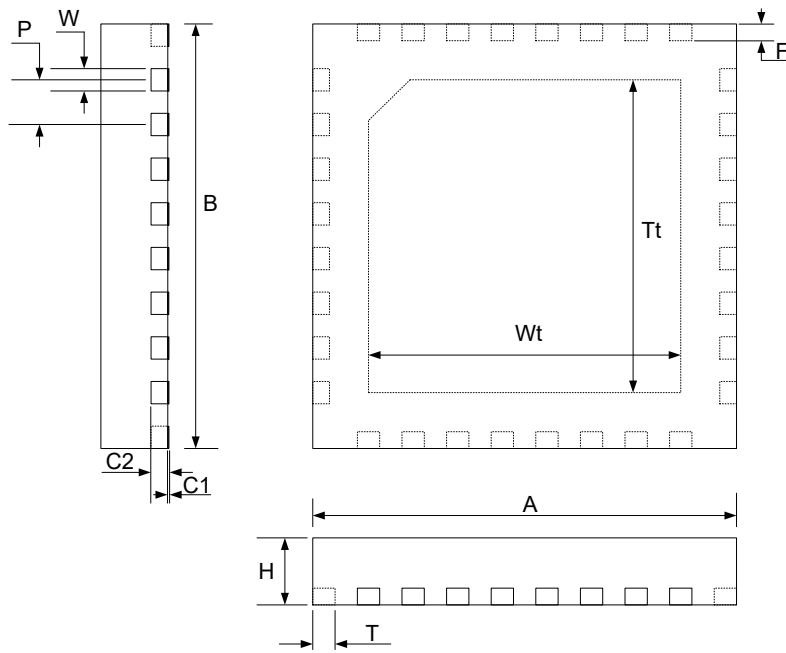
**Table 12.4 Typical Timings**

| Typical timings of IQS360 |     |    |
|---------------------------|-----|----|
| t <sub>sense</sub>        | 200 | µs |
| t <sub>process</sub>      | 1.4 | ms |
| t <sub>comms</sub>        | 6   | ms |
| Scan Period <sup>1</sup>  | 35  | ms |

<sup>1</sup> All channels active, with all data being read during communication window. All settings default.

## 13 Package information

### 13.1 IQS360 Package dimensions



**Figure 13.1 IQS360 Package. Drawings not too scale - illustration only.**

**Table 13.1 Packaging Dimensions.**

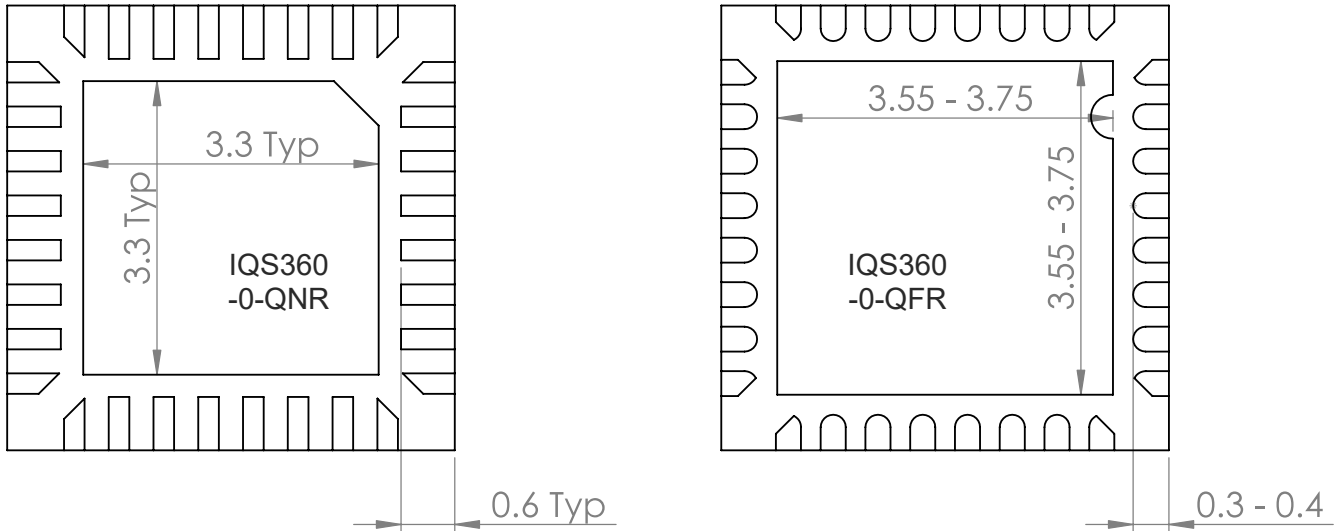
| DESCRIPTION    | QNR      |      | QFR      |      | Unit |
|----------------|----------|------|----------|------|------|
|                | MIN      | MAX  |          |      |      |
| A              | 4.90     | 5.10 | 4.90     | 5.10 | mm   |
| B              | 4.90     | 5.10 | 4.90     | 5.10 | mm   |
| C1             | 0        | 0.05 | 0        | 0.05 | mm   |
| C2             | 0.203TYP |      | 0.203TYP |      | mm   |
| F              | 0.600TYP |      | 0.3      | 0.4  | mm   |
| H              | 0.85     | 0.95 | 0.85     | 0.95 | mm   |
| P              | 0.5TYP   |      | 0.5TYP   |      | mm   |
| T              | 0.3      | 0.5  | 0.3      | 0.5  | mm   |
| T <sub>t</sub> | 3.3 TYP  |      | 3.55     | 3.75 | mm   |
| W              | 0.25TYP  |      | 0.25TYP  |      | mm   |
| W <sub>t</sub> | 3.3 TYP  |      | 3.55     | 3.75 | mm   |



### 13.1.2 QFR package differences to QNR package

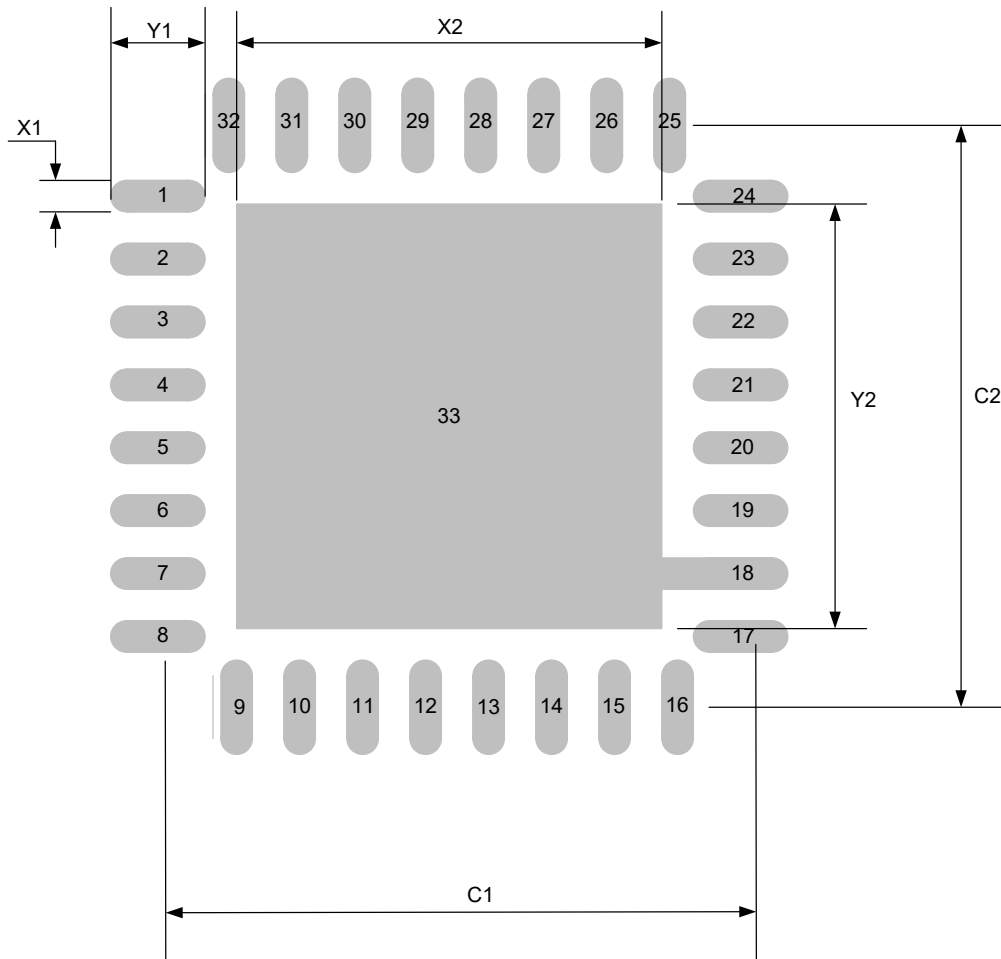
The overall physical size of the part ( $l \times w \times h$ ) and pitch of the pins did not change.

The mechanical dimensions of the saddle ( $T_t$  &  $W_t$ ) and length of the pins ( $F$ ) have changed from the old part (IQS360-0-QNR) to the new part (IQS360-0-QFR). The new dimensions are given below:



**Figure 13.2 Changes in Package Dimensions. Drawing for illustration only, not too scale.**

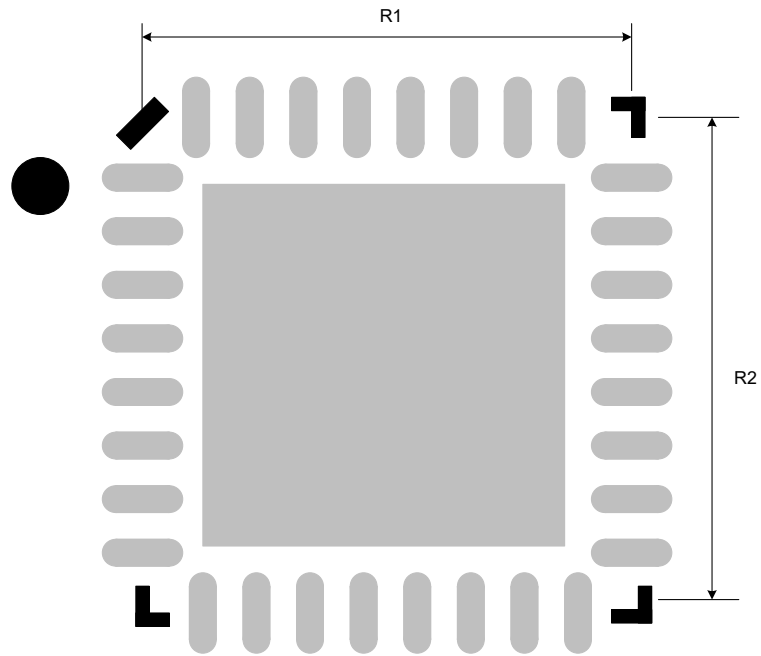
### 13.2 IQS360 Footprints



**Figure 13.3** IQS360 Recommended Footprint. Illustration is not too scale.

**Table 13.2** IQS360 Footprint Recommended Dimensions.

| DESCRIPTION | QFN       | QFR       | Unit |
|-------------|-----------|-----------|------|
|             | Dimension | Dimension |      |
| C1          | 4.90      | 4.85      | mm   |
| C2          | 4.90      | 4.85      | mm   |
| X1          | 0.30      | 0.25      | mm   |
| X2          | 3.25      | 3.65      | mm   |
| Y1          | 0.90      | 0.8       | mm   |
| Y2          | 3.25      | 3.65      | mm   |



**Figure 13.4 Silk Screen - optional.**

**Table 13.3 Silk Screen Dimensions.**

| DESCRIPTION | Dimension | Unit |
|-------------|-----------|------|
| R1          | 5.00      | mm   |
| R2          | 5.00      | mm   |





### 13.3 Tape and Reel Information

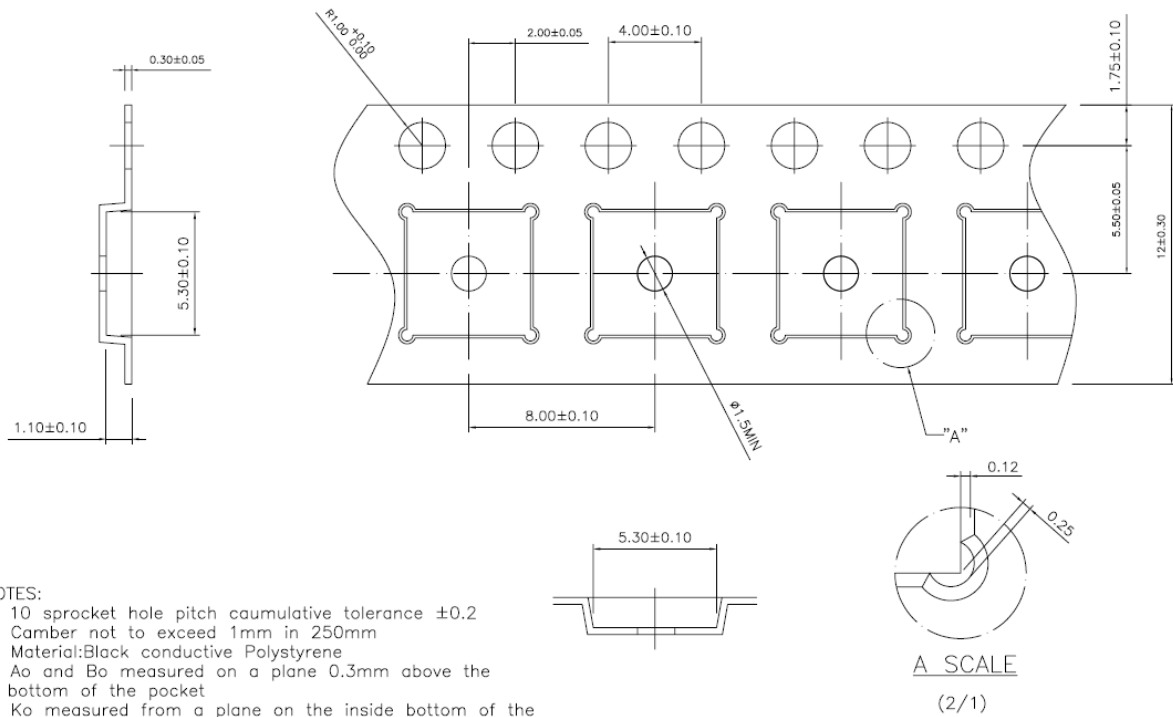
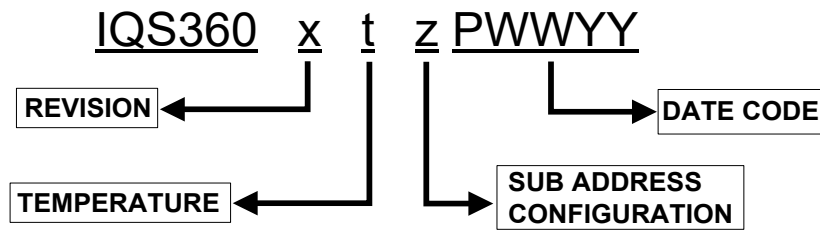


Figure 13.5 12mm Carrier Tape. Pin 1 – Left Bottom.



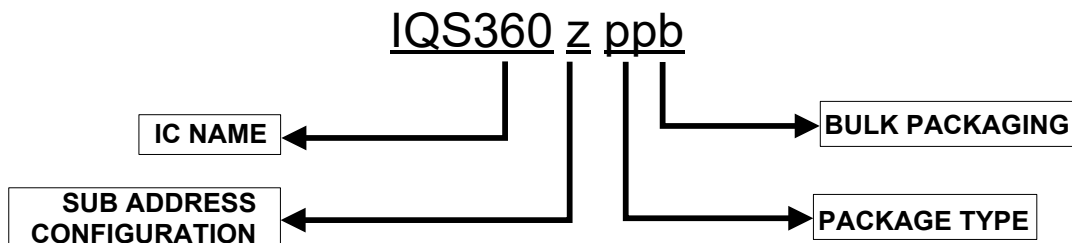
## 14 Device Marking



|                          |           |   |   |
|--------------------------|-----------|---|---|
| <b>REVISION</b>          | <b>x</b>  | = | IC Revision Number  |
| <b>TEMPERATURE RANGE</b> | <b>t</b>  | = | I    -20°C to 85°C (Industrial)<br>C    0°C to 70°C (Commercial)                    |
| <b>IC CONFIGURATION</b>  | <b>z</b>  | = | Sub Address Configuration (Hexadecimal)<br>0 = 64H<br>1 = 65H<br>2 = 66H<br>3 = 67H |
| <b>DATE CODE</b>         | <b>P</b>  | = | Package House   |
|                          | <b>WW</b> | = | Week  |
|                          | <b>YY</b> | = | Year  |

## 15 Ordering Information

Order quantities will be subject to multiples of a full reel. Contact the official distributor for sample quantities. A list of the distributors can be found under the “Distributors” section of [www.azoteq.com](http://www.azoteq.com).



|                       |               |   |                     |
|-----------------------|---------------|---|---------------------|
| <b>IC NAME</b>        | <b>IQS360</b> | = | IQS360              |
|                       | <b>0</b>      | = | 64H                 |
|                       | <b>1</b>      | = | 65H                 |
|                       | <b>2</b>      | = | 66H                 |
|                       | <b>3</b>      | = | 67H                 |
| <b>PACKAGE TYPE</b>   | <b>QN</b>     | = | QFN(5x5)-32         |
|                       | <b>QF</b>     | = | QFR(5x5)-32         |
| <b>BULK PACKAGING</b> | <b>R</b>      | = | Reel (3000pcs/reel) |



## **16 Errata**

### **16.1 Filter halt times**

During streaming mode (Event Mode Disabled) the filter halt times, as specified in Timings register (0x0A, byte0) will only work for values of 1 to 16 (decimal) if there is not a value written in the low power register. Therefore, if lower power is not set, the MCU needs to control halt times for values larger than 4 seconds.

The halt times work correctly if the low power register is not zero; Timings register (0x0A, byte1 set to 1 or more).

When used in Event Mode, the halt times work as specified in the Timings register (0x0A, byte0) regardless of the low power settings.

### **16.2 Last Active Channels**

The IQS360 only accepts settings for active channels. Therefore, to update any settings for channels that are not enabled by default (channels 10, 11 and 12), these channels need to be activated first (followed by a STOP command), before settings can be written to the IQS360 in the next communication window. Settings here include everything specific to an individual channel, such as base values and touch thresholds.



## 17 Datasheet Revision History

Table 17.1 Document Revisions

| Revision | Description  | Date           |
|----------|--|----------------|
| 1.00     | Preliminary Release  | January 2013   |
| 1.01     | Add QFN32 information,   | July 2013      |
| 1.02     | Update Table 6.1   | August 2013    |
| 1.03     | Update Settings Registers Default Values   | February 2014  |
| 1.04     | Add Errata   | March 2014     |
| 1.05     | Update patent list, PWM description and Figure 13.1                                      | August 2014    |
| 1.06     | Update Errata for Filter halt times during Event Mode, add description of Always Halt    | September 2014 |
| 1.07     | Update Errata for last active channel Remove Alpha version information                   | October 2014   |
| 1.08     | Add QFR32 Information  | November 2014  |
| 1.09     | Update Contact and Patent Information, add Trackpad Filtering Details in Register 0x10H. | March 2015     |
| 1.10     | Updated Electrical Specifications  | October 2015   |
| 1.11     | ESD reference design updated   | October 2016   |
| 1.12     | Update Contact and Patent information  | February 2018  |
| 1.13     | Update Reference Schematic for Halt Charge   | May 2018       |




## Appendix A. Contact Information

|                         | <b>USA</b>  | <b>Asia</b>   | <b>South Africa</b>                                  |
|-------------------------|---|---|--|
| <b>Physical Address</b> | 6507 Jester Blvd<br>Bldg 5, suite 510G<br>Austin<br>TX 78750<br>USA | Rm1227, Glittery City<br>Shennan Rd<br>Futian District<br>Shenzhen, 518033<br>China | 109 Main Street<br>Paarl<br>7646<br>South Africa     |
| <b>Postal Address</b>   | 6507 Jester Blvd<br>Bldg 5, suite 510G<br>Austin<br>TX 78750<br>USA | Rm1227, Glittery City<br>Shennan Rd<br>Futian District<br>Shenzhen, 518033<br>China | PO Box 3534<br>Paarl<br>7620<br>South Africa         |
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| <b>Fax</b>              | +1 512 672 8442   |   | +27 21 863 1512                                      |
| <b>Email</b>            | <a href="mailto:info@azoteq.com">info@azoteq.com</a>                | <a href="mailto:info@azoteq.com">info@azoteq.com</a>                                | <a href="mailto:info@azoteq.com">info@azoteq.com</a> |

Please visit [www.azoteq.com](http://www.azoteq.com) for a list of distributors and worldwide representation.

The following patents relate to the device or usage of the device: US 6,249,089; US 6,952,084; US 6,984,900; US 8,395,395; US 8,531,120; US 8,659,306; US 9,209,803; US 9,360,510; US 9,496,793; US 9,709,614; US 9,948,297; EP 2,351,220; EP 2,559,164; EP 2,748,927; EP 2,846,465; HK 1,157,080; SA 2001/2151; SA 2006/05363; SA 2014/01541; SA 2017/02224;

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