Quad, 16-Bit DAC with 5 ppm/°C On-Chip Reference in 14-Lead TSSOP

AD5666

FEATURES

Low power quad 16-bit DAC
14-lead TSSOP
On-chip 1.25 V/2.5 V, 5 ppm/°C reference
Power down to 400 nA @ 5 V, 200 nA @ 3 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on reset to zero scale or midscale
3 power-down functions
Hardware $\overline{\text{LDAC}}$ with $\overline{\text{LDAC}}$ override function
$\overline{\text{CLR}}$ function to programmable code
SDO daisy-chaining option
Rail-to-rail operation

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

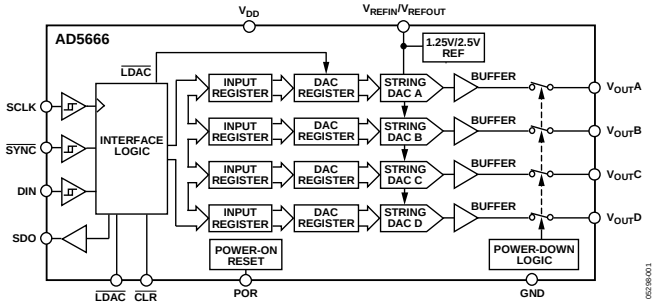

Figure 1.

GENERAL DESCRIPTION

The AD5666 is a low power, quad, 16-bit, buffered voltage-output DAC. The part operates from a single 2.7 V to 5.5 V supply and is guaranteed monotonic by design.

The AD5666 has an on-chip reference with an internal gain of 2. The AD5666-1 has a 1.25 V 5 ppm/°C reference, giving a full-scale output of 2.5 V; the AD5666-2 has a 2.5 V 5 ppm/°C reference, giving a full-scale output of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is turned on by writing to the DAC.

The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V (POR pin low) or to midscale (POR pin high) and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode for any or all DAC channels.

The outputs of all DACs can be updated simultaneously using the $\overline{\text{LDAC}}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{\text{CLR}}$ that clears all DACs to a software-selectable code—0 V, midscale, or full scale.

The AD5666 utilizes a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The on-chip precision output amplifier enables rail-to-rail output swing.

PRODUCT HIGHLIGHTS

1. Quad, 16-bit DAC.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 14-lead TSSOP.
4. Selectable power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 200 nA at 3 V and 400 nA at 5 V.

Rev. D
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REVISION HISTORY

6/10—Rev. C to Rev. D
Changes to Figure 19 and Figure 20 Captions ... 14

10/09—Rev. B to Rev. C
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2/09—Rev. A to Rev. B
Changes to Reference Current Parameter, Table 1 ... 3
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11/05—Rev. 0 to Rev. A
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10/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Grade[1]			B Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[2]								
Resolution	16			16			Bits	
Relative Accuracy			±32			±16	LSB	See Figure 6
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design (see Figure 7)
Zero-Code Error		1	9		1	9	mV	All 0s loaded to DAC register (see Figure 13)
Zero-Code Error Drift		±2			±2		µV/°C	
Full-Scale Error		−0.2	−1		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 12)
Gain Error			±1			±1	% FSR	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
Offset Error		±1	±9		±1	±9	mV	
DC Power Supply Rejection Ratio		−80			−80		dB	V_{DD} ± 10%
DC Crosstalk (External Reference)		10			10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5			5		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		2			2		nF	$R_L = \infty$
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 5 V
Power-Up Time		4			4		µs	Coming out of power-down mode V_{DD} = 5 V
REFERENCE INPUTS								
Reference Input Voltage		V_{DD}			V_{DD}		V	
Reference Current		20	55		20	55	µA	$V_{REF} = V_{DD}$ = 5.5 V
Reference Input Range	0		V_{DD}	0		V_{DD}	V	
Reference Input Impedance		14.6			14.6		kΩ	Per DAC channel
REFERENCE OUTPUT								
Output Voltage	2.495		2.505	2.495		2.505	V	At ambient
Reference TC[3]		±5	±10		±5	±10	ppm/°C	
Reference Output Impedance		7.5			7.5		kΩ	
LOGIC INPUTS[3]								
Input Current			±3			±3	µA	All digital inputs
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 5 V
Input High Voltage, V_{INH}	2			2			V	V_{DD} = 5 V
Pin Capacitance		3			3		pF	

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Conditions/Comments
LOGIC OUTPUTS (SDO)[3]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} − 1			V_{DD} − 1				I_{SOURCE} = 2 mA
High Impedance Leakage Current			±0.25			±0.25	µA	
High Impedance Output Capacitance		2			2		pF	
POWER REQUIREMENTS								
V_{DD}	4.5		5.5	4.5		5.5	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[4]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.7	0.9		0.7	0.9	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		1.3	1.6		1.3	1.6	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]								
V_{DD} = 4.5 V to 5.5 V		0.4	1		0.4	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of 512 to 65,024. Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All four DACs powered down.

V_{DD} = 2.7 V to 3.6 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	A Grade[1]			B Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[2]								
Resolution	16			16			Bits	
Relative Accuracy			±32			±16	LSB	See Figure 5
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design (see Figure 6)
Zero-Code Error		1	9		1	9	mV	All 0s loaded to DAC register (see Figure 13)
Zero-Code Error Drift		±2			±2		µV/°C	
Full-Scale Error		−0.2	−1		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 12)
Gain Error			±1			±1	% FSR	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
Offset Error		±1	±9		±1	±9	mV	
DC Power Supply Rejection Ratio		−80			−80		dB	V_{DD} ± 10%
DC Crosstalk (External Reference)		10			10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5			5		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		2			2		nF	$R_L = \infty$
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 3 V coming out of power-down mode
Power-Up Time		4			4		µs	Coming out of power-down V_{DD} = 3 V
REFERENCE INPUTS								
Reference Input Voltage		V_{DD}			V_{DD}		V	
Reference Current		40	55		40	55	µA	$V_{REF} = V_{DD}$ = 3.6 V
Reference Input Range	0		V_{DD}	0		V_{DD}		
Reference Input Impedance		14.6			14.6		kΩ	Per DAC channel
REFERENCE OUTPUT								
Output Voltage	1.247		1.253	1.247		1.253	V	At ambient
Reference TC[3]		±5	±15		±5	±15	ppm/°C	
Reference Output Impedance		7.5			7.5		kΩ	
LOGIC INPUTS[3]								
Input Current			±3			±3	µA	
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 3 V
Input High Voltage, V_{INH}	2			2			V	V_{DD} = 3 V
Pin Capacitance		3			3		pF	
LOGIC OUTPUTS (SDO)[3]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} − 0.5			V_{DD} − 0.5				I_{SOURCE} = 2 mA
High Impedance Leakage Current			±0.25			±0.25	µA	
High Impedance Leakage		2			2		pF	

Parameter	A Grade[1]			B Grade[1]			Unit	Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
Current								
POWER REQUIREMENTS								
V_{DD}	2.7		3.6	2.7		3.6	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[4]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.65	0.85		0.65	0.85	mA	Internal reference off
V_{DD} = 2.7 V to 3.6 V		1.3	1.5		1.3	1.5	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]								
V_{DD} = 2.7 V to 3.6 V		0.2	1		0.2	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of 512 to 65,024. Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All four DACs powered down.

AC CHARACTERISTICS

V_{DD} =2.7V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time		6	10	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.5		V/µs	
Digital-to-Analog Glitch Impulse		4		nV-s	1 LSB change around major carry (see Figure 29)
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 Hz to 20 MHz
SDO Feedthrough		3		nV-s	Daisy-chain mode; SDO load is 10 pF
Digital Feedthrough		0.1		nV-s	
Digital Crosstalk		0.5		nV-s	
Analog Crosstalk		2.5		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.2 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = 0x8400, 1 kHz
		100		nV/√Hz	DAC code = 0x8400, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to + 105°C, typical at 25°C.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 3 and Figure 5. V_{DD} = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX} V_{DD} = 2.7 V to 5.5 V	Unit	Conditions/Comments
t_1[1]	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	13	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge set-up time
t_5	4	ns min	Data set-up time
t_6	4	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	15	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	13	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK fall ignore
t_{10}	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ fall ignore
t_{11}	10	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{12}	15	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ rising edge
t_{13}	5	ns min	$\overline{\text{CLR}}$ pulse width low
t_{14}	0	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ falling edge
t_{15}	300	ns typ	$\overline{\text{CLR}}$ pulse activation time
t_{16}[2, 3]	22	ns max	SCLK rising edge to SDO valid
t_{17}[3]	5	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_{18}[3]	8	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK rising edge
t_{19}[3]	0	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.
[2] Measured with the load circuit of Figure 16. t_{16} determines the maximum SCLK frequency in daisy-chain mode.
[3] Daisy-chain mode only.

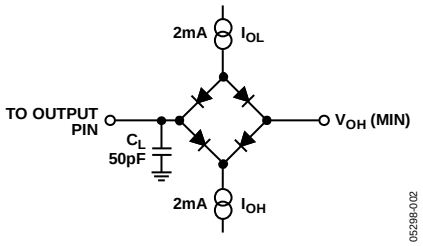

Figure 2. Load Circuit for Digital Output (SDO) Timing Specifications

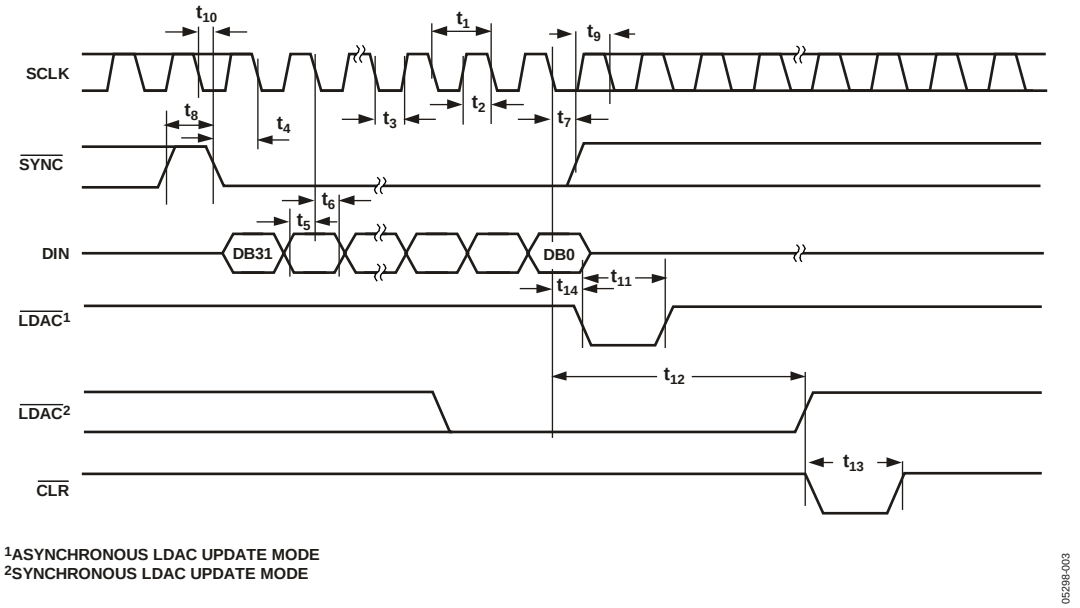

Figure 3. Serial Write Operation

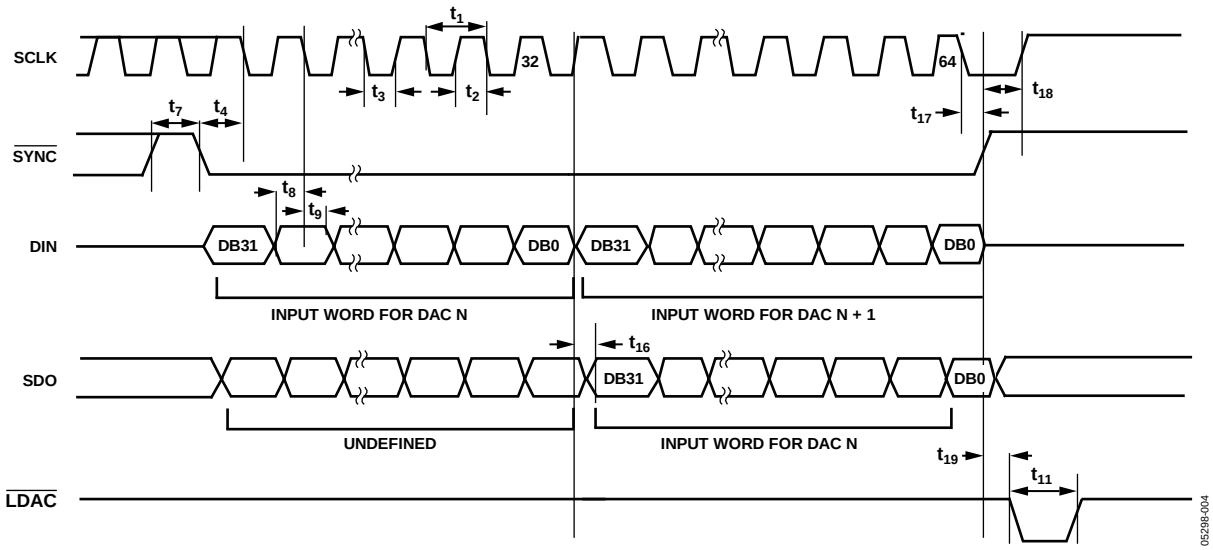

Figure 4. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	+150°C
TSSOP Package	
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb Free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

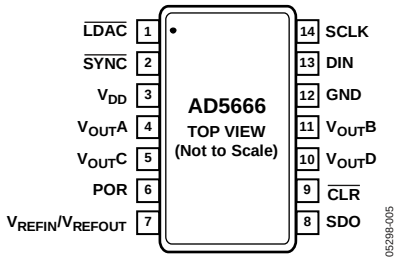

Figure 5. 14-Lead TSSOP (RU-14)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	POR	Power-on Reset Pin. Tying this pin to GND powers up the part to 0 V. Tying this pin to V_{DD} powers up the part to midscale.
7	V_{REFIN}/V_{REFOUT}	The AD5666 has a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
8	SDO	Serial Data Output. Can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
9	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
10	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	GND	Ground Reference Point for All Circuitry on the Part.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

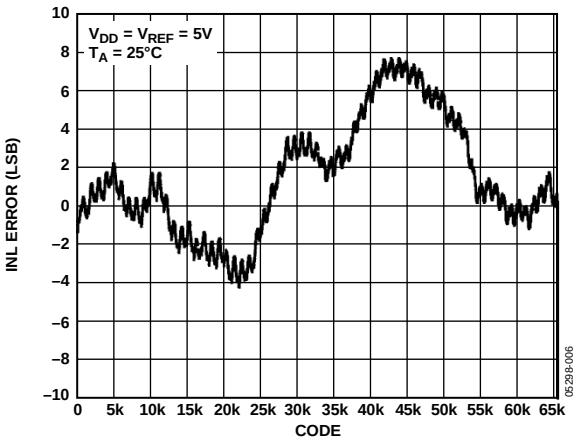

Figure 6. INL

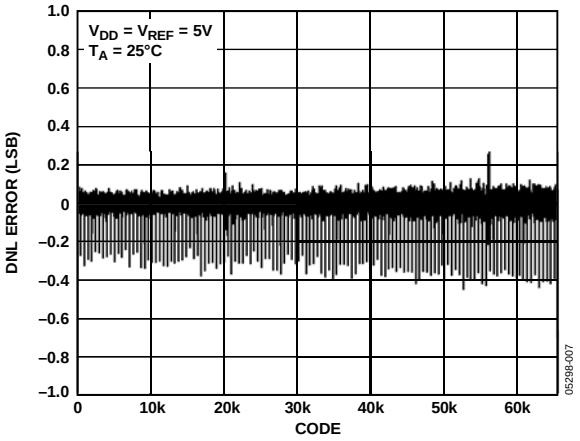

Figure 7. DNL

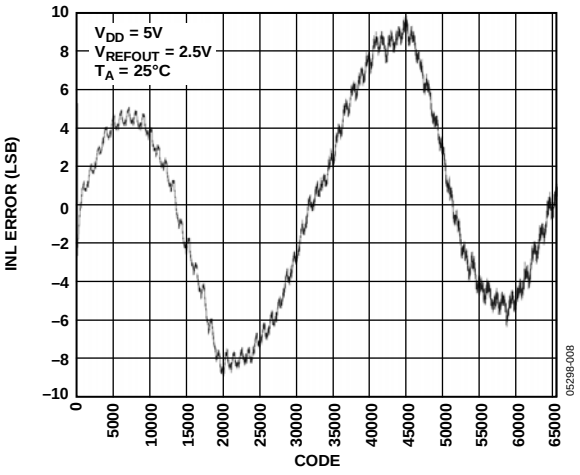

Figure 8. INL—AD5666-2

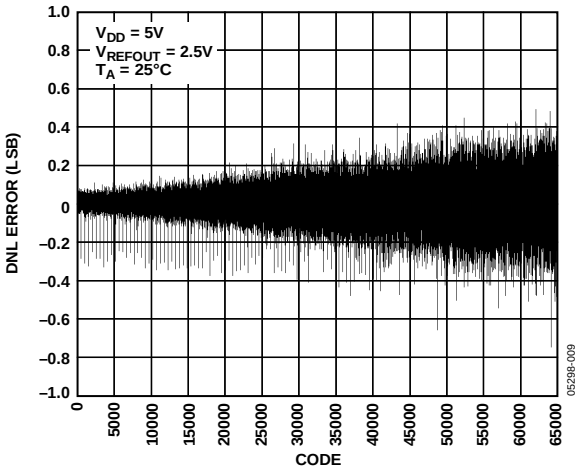

Figure 9. DNL—AD5666-2

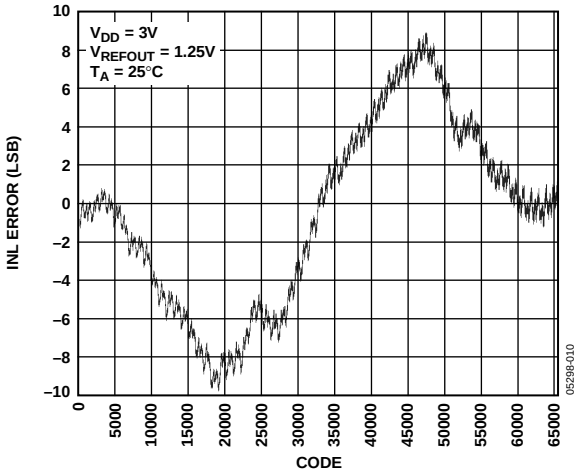

Figure 10. INL—AD5666-1

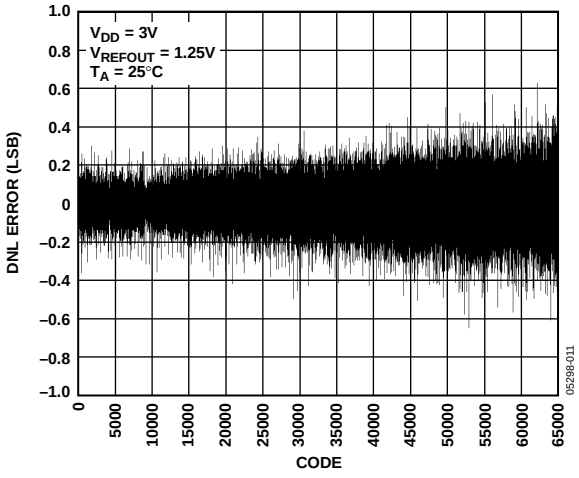

Figure 11. DNL—AD5666-1

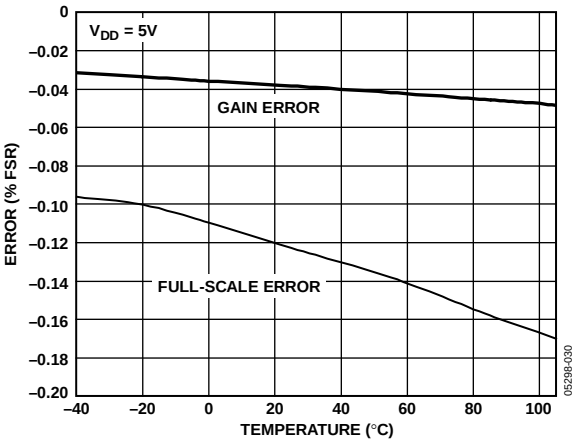

Figure 12. Gain Error and Full-Scale Error vs. Temperature

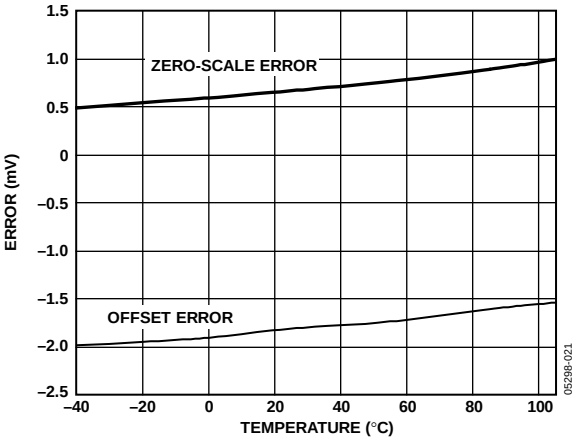

Figure 13. Zero-Scale Error and Offset Error vs. Temperature

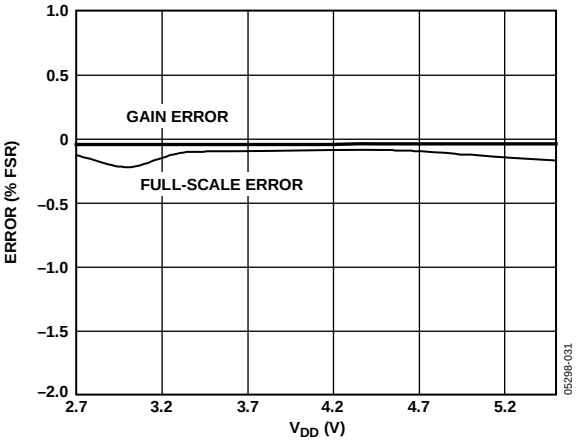

Figure 14. Gain Error and Full-Scale Error vs. Supply Voltage

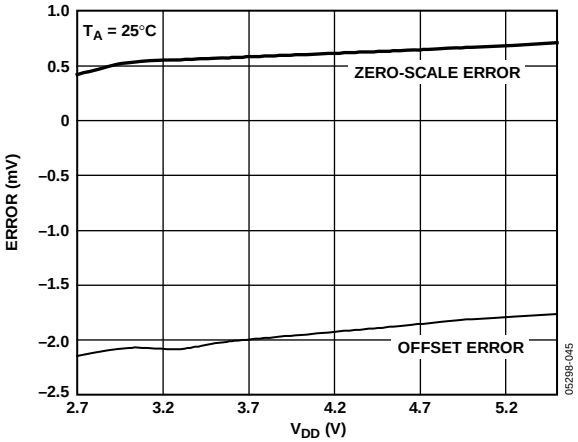

Figure 15. Zero-Scale Error and Offset Error vs. Supply Voltage

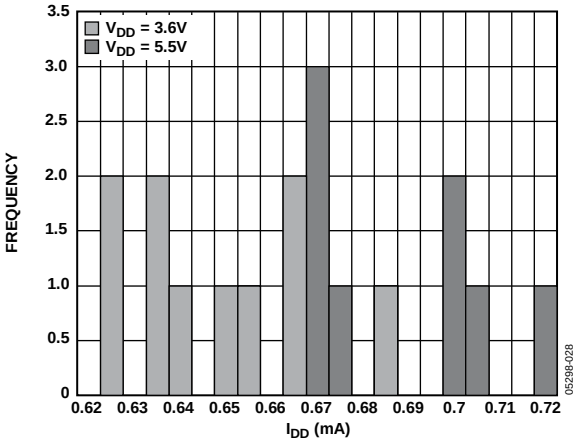

Figure 16. I_{DD} Histogram with External Reference

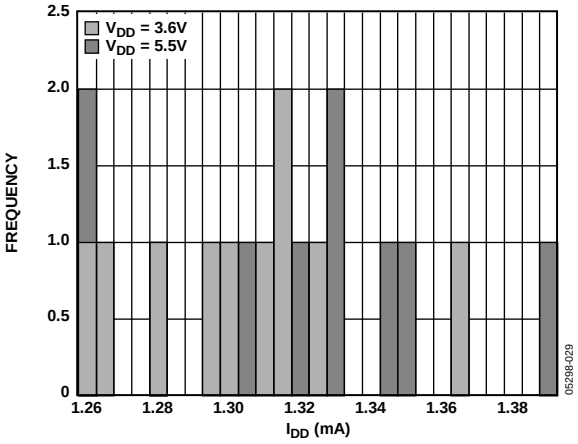

Figure 17. I_{DD} Histogram with Internal Reference

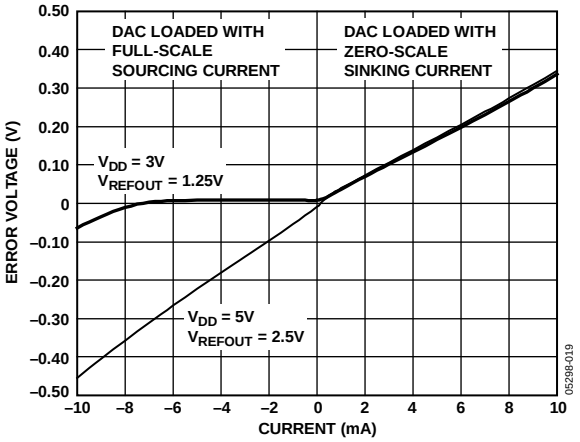

Figure 18. Headroom at Rails vs. Source and Sink

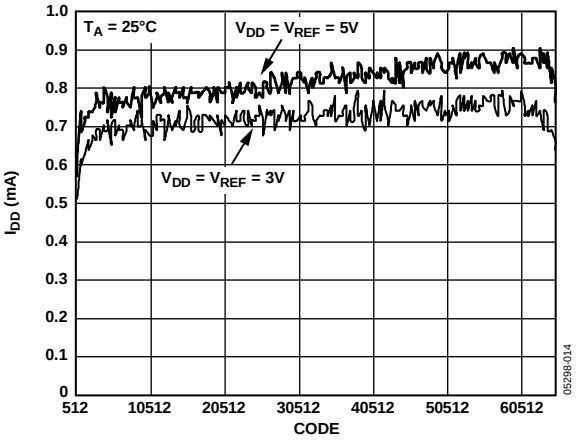

Figure 21. Supply Current vs. Code

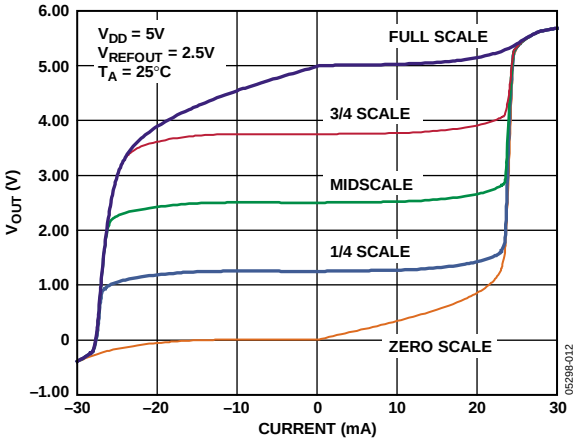

Figure 19. Source and Sink Current Capability with V_{DD} = 5 V

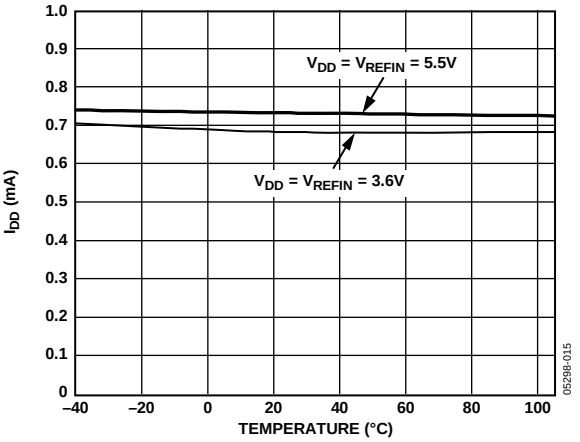

Figure 22. Supply Current vs. Temperature

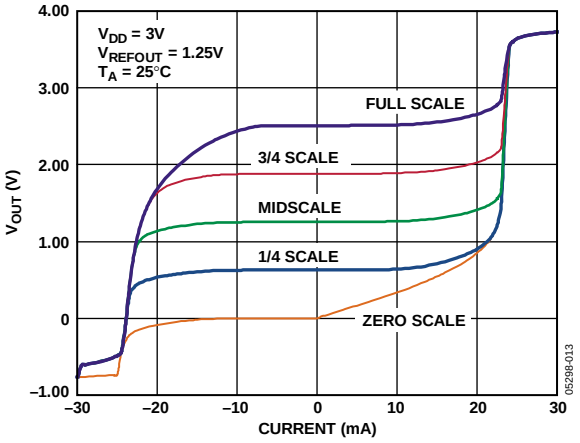

Figure 20. Source and Sink Current Capability with V_{DD} = 3 V

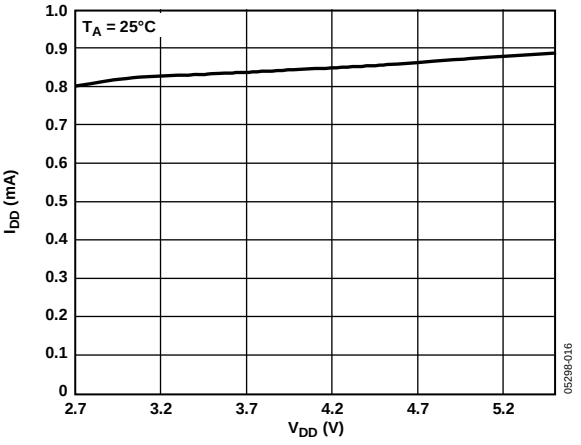

Figure 23. Supply Current vs. Supply Voltage

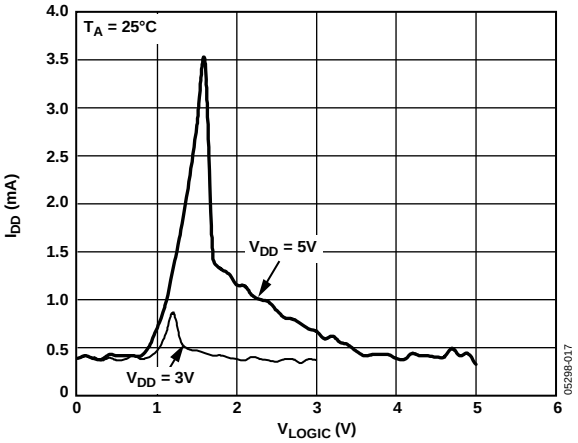

Figure 24. Supply Current vs. Logic Input Voltage

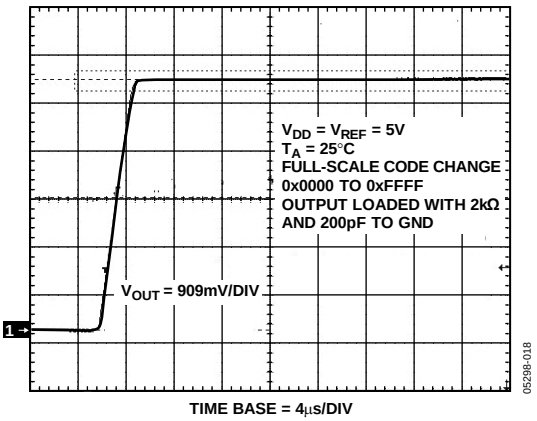

Figure 25. Full-Scale Settling Time

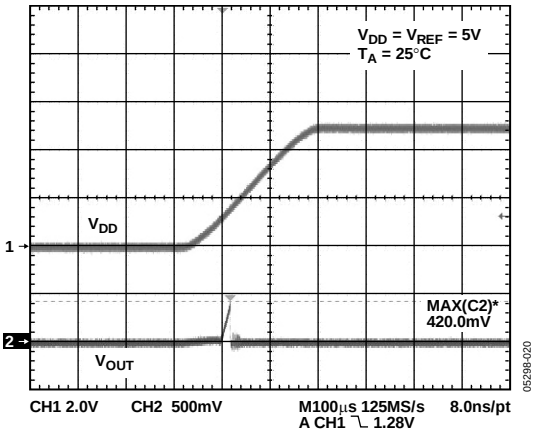

Figure 26. Power-On Reset to 0 V

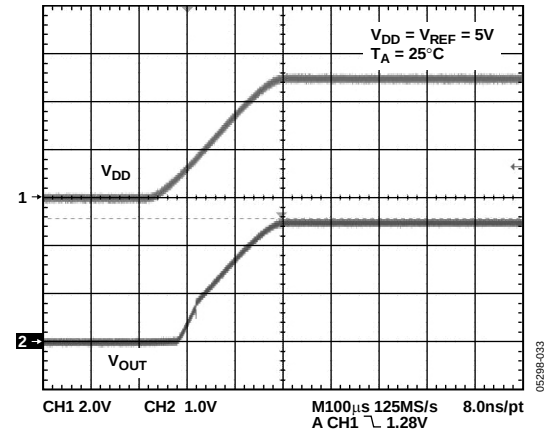

Figure 27. Power-On Reset to Midscale

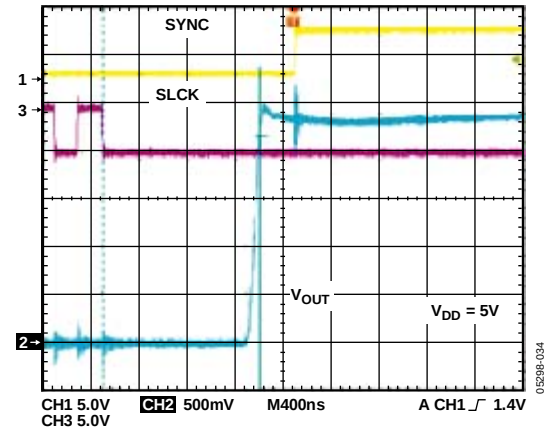

Figure 28. Exiting Power-Down to Midscale

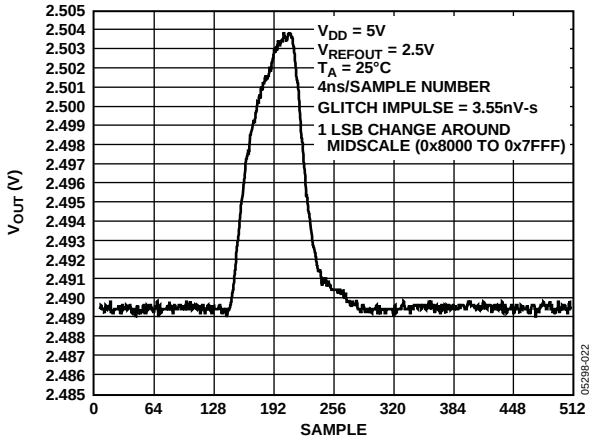

Figure 29. Digital-to-Analog Glitch Impulse

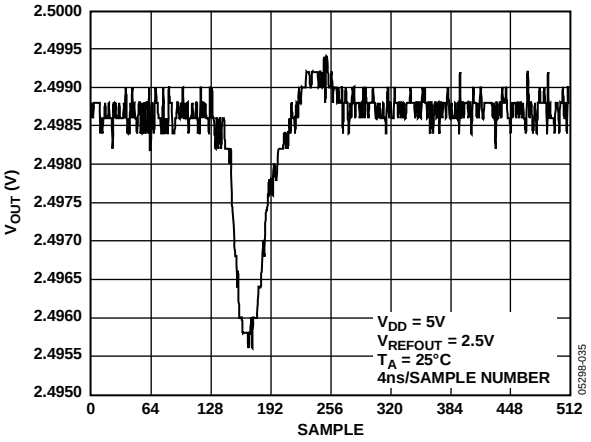

Figure 30. Analog Crosstalk

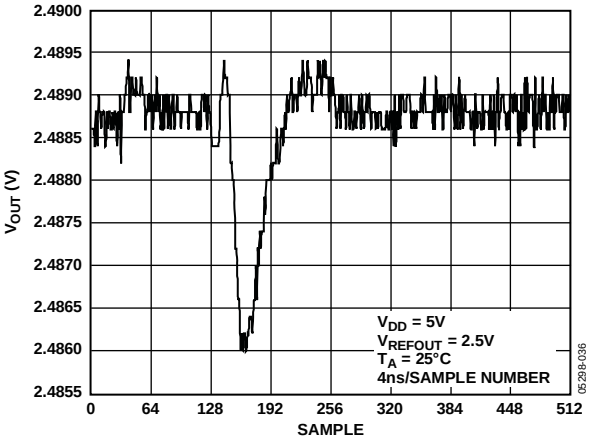

Figure 31. DAC-to-DAC Crosstalk

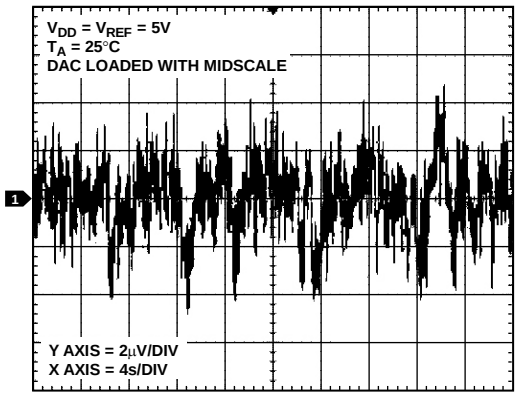

Figure 32. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

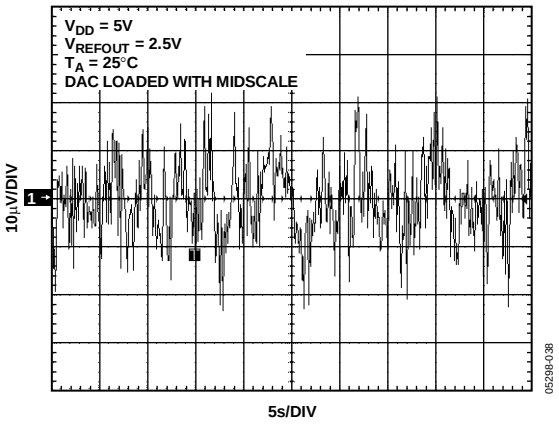

Figure 33. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

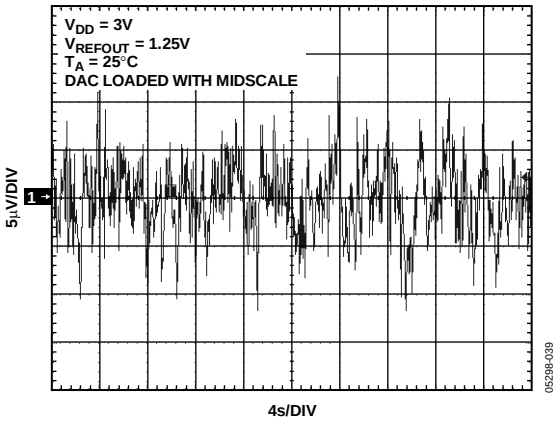

Figure 34. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

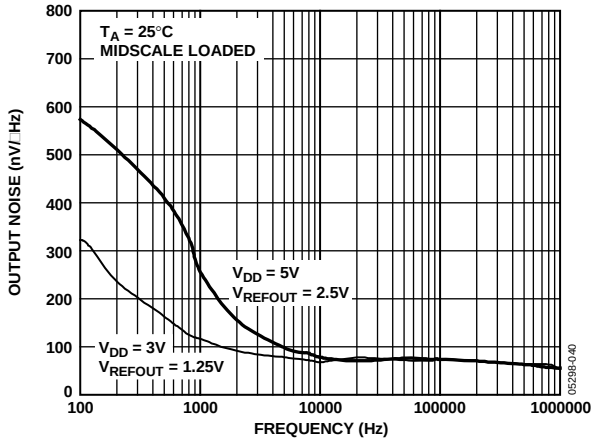

Figure 35. Noise Spectral Density, Internal Reference

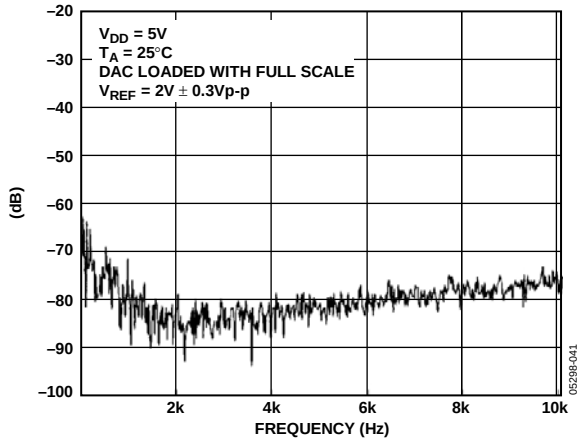

Figure 36. Total Harmonic Distortion

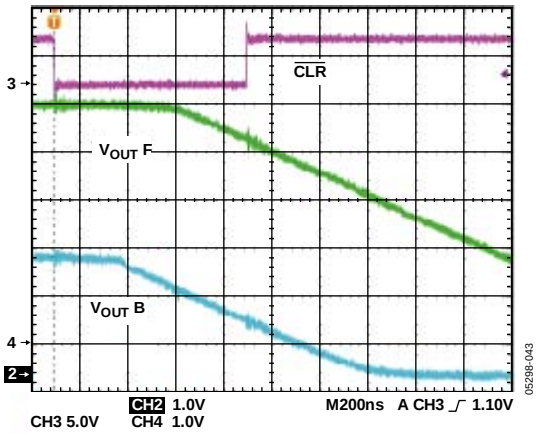

Figure 38. Hardware $\overline{CLR}$

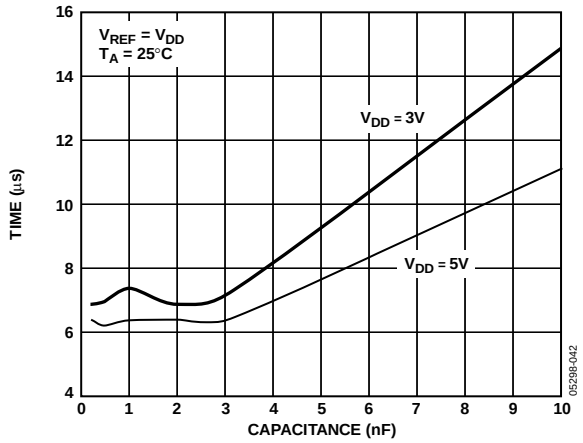

Figure 37. Settling Time vs. Capacitive Load

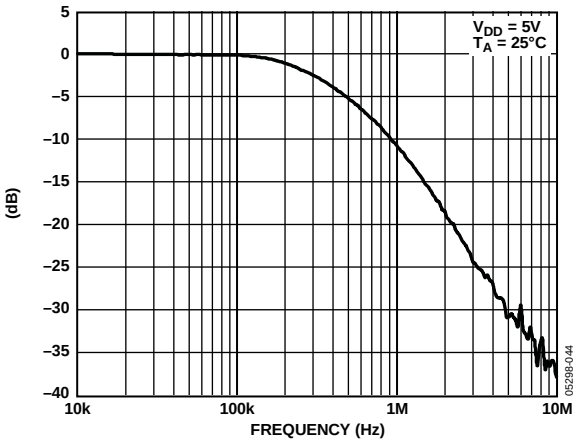

Figure 39. Multiplying Bandwidth

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. Figure 6 shows a plot of typical INL vs. code.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Figure 7 shows a plot of typical DNL vs. code.

Offset Error
Offset error is a measure of the difference between the actual V_{OUT} and the ideal V_{OUT}, expressed in millivolts in the linear region of the transfer function. Offset error is measured on the AD5666 with Code 512 loaded into the DAC register. It can be negative or positive and is expressed in millivolts.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5666, because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts. Figure 13 shows a plot of typical zero-code error vs. temperature.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Zero-Code Error Drift

Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift

Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. Figure 13 shows a plot of typical full-scale error vs. temperature.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 29.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2 V, and V_{DD} is varied ±10%.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nV-s and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high, and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

THEORY OF OPERATION

D/A SECTION

The AD5666 DAC is fabricated on a CMOS process. The architecture consists of a string of DACs followed by an output buffer amplifier. The parts include an internal 1.25 V/2.5 V, 5 ppm/°C reference with an internal gain of 2. Figure 40 shows a block diagram of the DAC architecture.

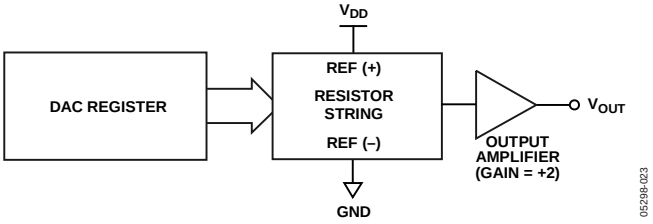

Figure 40. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

The ideal output voltage when using and internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:
D = decimal equivalent of the binary code that is loaded to the DAC register.
0 to 65,535 for AD5666 (16 bits).
N = the DAC resolution.

RESISTOR STRING

The resistor string section is shown in Figure 41. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

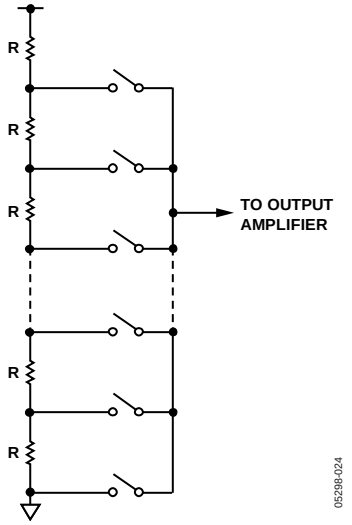

Figure 41. Resistor String

INTERNAL REFERENCE

The AD5666 has an on-chip reference with an internal gain of 2. The AD5666-1 has a 1.25 V 5 ppm/°C reference, giving a full-scale output of 2.5 V. The AD5666-2 has a 2.5 V 5 ppm/°C reference, giving a full-scale output of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a write to a control register.

The internal reference associated with each part is available at the V_{REFOUT} pin. A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor be placed between the reference output and GND for reference stability.

Individual channel power-down is not supported while using the internal reference.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The amplifier is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 19 and Figure 20. The slew rate is 1.5 V/μs with a ¼ to ¾ scale settling time of 10 μs.

SERIAL INTERFACE

The AD5666 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 3 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5666 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Because the $\overline{SYNC}$ buffer draws more current when V_{IN} = 2 V than it does when V_{IN} = 0.8 V, $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned previously, however, $\overline{SYNC}$ must be brought high again just before the next write sequence.

Table 7. Command Definitions

Command				
C3	**C2**	**C1**	**C0**	**Description**
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, update all (software $\overline{LDAC}$)
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up DCEN/REF register
1	0	0	1	No operation
–	–	–	–	Reserved
1	1	1	1	Reserved

Table 8. Address Commands

Address (n)				
A3	**A2**	**A1**	**A0**	**Selected DAC Channel**
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
1	1	1	1	All DACs

INPUT SHIFT REGISTER

The input shift register is 32 bits wide (see Figure 42). The first four bits are don't cares. The next four bits are the command bits, C3 to C0 (see Table 8), followed by the 4-bit DAC address bits, A3 to A0 (see Table 9) and finally the 16-bit data-word. The data-word comprises the 16-bit input code followed by four don't care bits for the AD5666 (see Figure 42). These data bits are transferred to the DAC register on the 32nd falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 43).

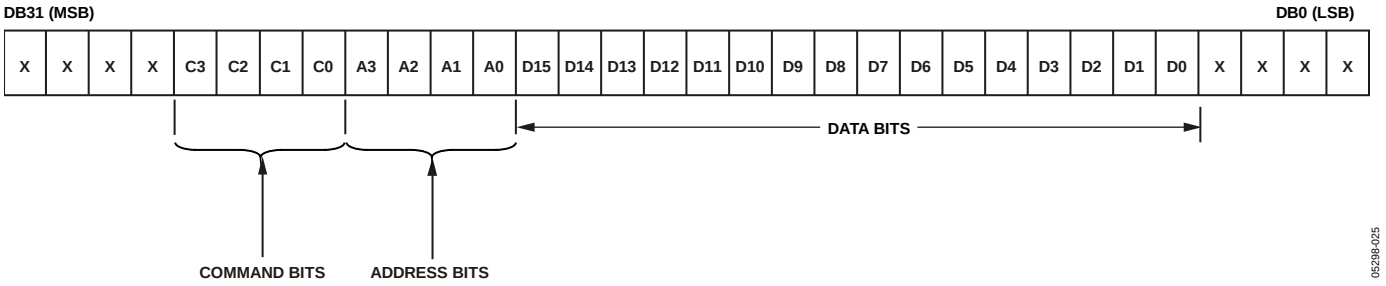

Figure 42. AD5666 Input Register Content

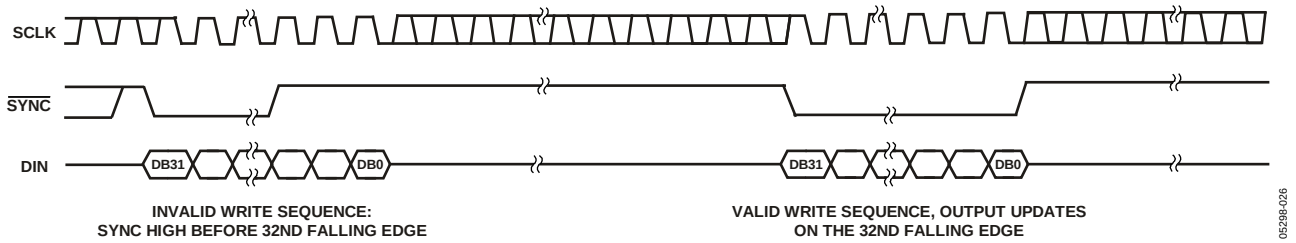

Figure 43. $\overline{\text{SYNC}}$ Interrupt Facility

DAISY-CHAINING

For systems that contain several DACs, or where the user wishes to read back the DAC contents for diagnostic purposes, the SDO pin can be used to daisy-chain several devices together and provide serial readback.

The daisy-chain mode is enabled through a software executable DCEN command. Command 1000 is reserved for this DCEN function (see Table 7). The daisy-chain mode is enabled by setting a bit (DB1) in the DCEN register. The default setting is standalone mode, where Bit DCEN = 0. Table 9 shows how the state of the bits corresponds to the mode of operation of the device.

The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 32 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next DAC in the chain, a multi-DAC interface is constructed. Each DAC in the system requires 32 clock pulses; therefore, the total number of clock cycles must equal 32N, where N is the total number of devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This prevents any further data from being clocked into the input shift register.

If $\overline{\text{SYNC}}$ is taken high before 32 clocks are clocked into the part, it is considered an invalid frame and the data is discarded.

The serial clock can be continuous or a gated clock. A continuous SCLK source can be used only if the $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

INTERNAL REFERENCE REGISTER

The on-board reference is off at power-up by default. This allows the use of an external reference if the application requires it. The on-board reference can be turned on/off by a user-programmable REF register by setting Bit DB0 high or low (see Table 9). Command 1000 is reserved for this internal REF set-up command (see Table 7). Table 11 shows how the state of the bits in the input shift register corresponds to the mode of operation of the device.

POWER-ON RESET

The AD5666 contains a power-on reset circuit that controls the output voltage during power-up. By connecting the POR pin low, the AD5666 output powers up to 0 V; by connecting the POR pin high, the AD5666 output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is reserved for this reset function (see Table 7). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

POWER-DOWN MODES

The AD5666 contains four separate modes of operation. Command 0100 is reserved for the power-down function (see Table 7). These modes are software-programmable by setting two bits, Bit DB19 and Bit DB18, in the control register. Table 11 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC D to DAC A) can be powered down to the selected mode by setting the corresponding four bits (DB7, DB6, DB1, DB0) to 1. See Table 12 for the contents of the input shift register during power-down/power-up operation. When using the internal reference, only all channel power-down to the selected modes is supported.

When both bits are set to 0, the part works normally with its normal power consumption of 700 μA at 5 V. However, for the three power-down modes, the supply current falls to 400 nA at 5 V (200 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 44.

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. The internal reference is powered down only when all channels are powered down. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 μs for V_{DD} = 5 V and for V_{DD} = 3 V (see Figure 28).

Any combination of DACs can be powered up by setting PD1 and PD0 to 0 (normal operation). The output powers up to the value in the input register ($\overline{\text{LDAC}}$ Low) or to the value in the DAC register before powering down ($\overline{\text{LDAC}}$ high).

Table 9. Daisy-Chain Enable/Internal Reference Register

DCEN (DB1)	REF (DB0)	Action
0	0	Standalone mode, reference off (default)
0	1	Standalone mode, reference on
1	0	DCEN mode, reference off
1	1	DCEN mode, reference on

Table 10. 32-Bit Input Shift Register Contents for Daisy-Chain Enable and Reference Set-Up Function

MSB											LSB
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB19 to DB2**	**DB1**	**DB0**
X	1	0	0	0	X	X	X	X	X	1/0	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	DCEN/REF register	

Table 11. Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

Table 12. 32-Bit Input Shift Register Contents for Power-Up/Power-Down Function

MSB																LSB
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB19 to DB10**	**DB9**	**DB8**	**DB7 to DB4**	**DB3**	**DB2**	**DB1**	**DB0**
X	0	1	0	0	X	X	X	X	X	PD1	PD0	X	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C2 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Power-down mode		Don't cares	Power-down/power-up channel selection—set bit to 1 to select			

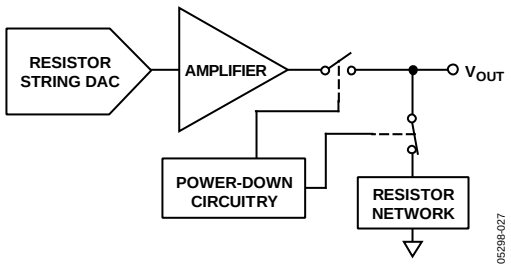

Figure 44. Output Stage During Power-Down

CLEAR CODE REGISTER

The AD5666 has a hardware $\overline{CLR}$ pin that is an asynchronous clear input. The $\overline{CLR}$ input is falling edge sensitive. Bringing the $\overline{CLR}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{CLR}$ register and sets the analog outputs accordingly. This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting two bits, Bit DB1 and Bit DB0, in the control register (see Table 13). The default setting clears the outputs to 0 V. Command 0101 is reserved for loading the clear code register (see Table 7).

The part exits clear code mode on the 32nd falling edge of the next write to the part. If $\overline{CLR}$ is activated during a write sequence, the write is aborted.

The $\overline{CLR}$ pulse activation time—the falling edge of $\overline{CLR}$ to when the output starts to change—is typically 280 ns. However, if outside the DAC linear region, it typically takes 520 ns after executing $\overline{CLR}$ for the output to start changing (see Figure 38).

See Table 14 for contents of the input shift register during the loading clear code register operation

$\overline{LDAC}$ FUNCTION

The outputs of all DACs can be updated simultaneously using the hardware $\overline{LDAC}$ pin.

Synchronous $\overline{LDAC}$: After new data is read, the DAC registers are updated on the falling edge of the 32nd SCLK pulse. $\overline{LDAC}$ can be permanently low or pulsed as in Figure 3.

Asynchronous $\overline{LDAC}$: The outputs are not updated at the same time that the input registers are written to. When $\overline{LDAC}$ goes low, the DAC registers are updated with the contents of the input register.

Alternatively, the outputs of all DACs can be updated simultaneously using the software $\overline{LDAC}$ function by writing to Input Register n and updating all DAC registers. Command 0011 is reserved for this software $\overline{LDAC}$ function.

An $\overline{LDAC}$ register gives the user extra flexibility and control over the hardware $\overline{LDAC}$ pin. This register allows the user to select which combination of channels to simultaneously update when the hardware $\overline{LDAC}$ pin is executed. Setting the $\overline{LDAC}$ bit register to 0 for a DAC channel means that this channel's update is controlled by the $\overline{LDAC}$ pin. If this bit is set to 1, this channel updates synchronously; that is, the DAC register is updated after new data is read, regardless of the state of the $\overline{LDAC}$ pin. It effectively sees the $\overline{LDAC}$ pin as being tied low. (See Table 15 for the $\overline{LDAC}$ register mode of operation.) This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using command 0110 loads the 4-bit $\overline{LDAC}$ register (DB3 to DB0). The default for each channel is 0; that is, the $\overline{LDAC}$ pin works normally. Setting the bits to 1 means the DAC channel is updated regardless of the state of the $\overline{LDAC}$ pin. See Table 16 for the contents of the input shift register during the load $\overline{LDAC}$ register mode of operation.

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5666 should have separate analog and digital sections. If the AD5666 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5666.

The power supply to the AD5666 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should physically be as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

Table 13. Clear Code Register

Clear Code Register		
DB1	**DB0**	
CR1	**CR0**	**Clears to Code**
0	0	0x0000
0	1	0x8000
1	0	0xFFFF
1	1	No operation

Table 14. 32-Bit Input Shift Register Contents for Clear Code Function

MSB											**LSB**
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB19 to DB2**	**DB1**	**DB0**
X	0	1	0	1	X	X	X	X	X	1/0	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	Clear code register (CR1 to CR0)	

Table 15. $\overline{\text{LDAC}}$ Overwrite Definition

Load DAC Register		
$\overline{\text{LDAC}}$ Bits (DB3 to DB0)	**$\overline{\text{LDAC}}$ Pin**	**$\overline{\text{LDAC}}$ Operation**
0	1/0	Determined by $\overline{\text{LDAC}}$ pin
1	X—don't care	DAC channels update, overrides the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 0.

Table 16. 32-Bit Input Shift Register Contents for $\overline{\text{LDAC}}$ Overwrite Function

MSB													**LSB**
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB19 to DB4**	**DB3**	**DB2**	**DB1**	**DB0**
X	0	1	1	0	X	X	X	X	X	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Setting $\overline{\text{LDAC}}$ bit to 1 override $\overline{\text{LDAC}}$ pin			

OUTLINE DIMENSIONS

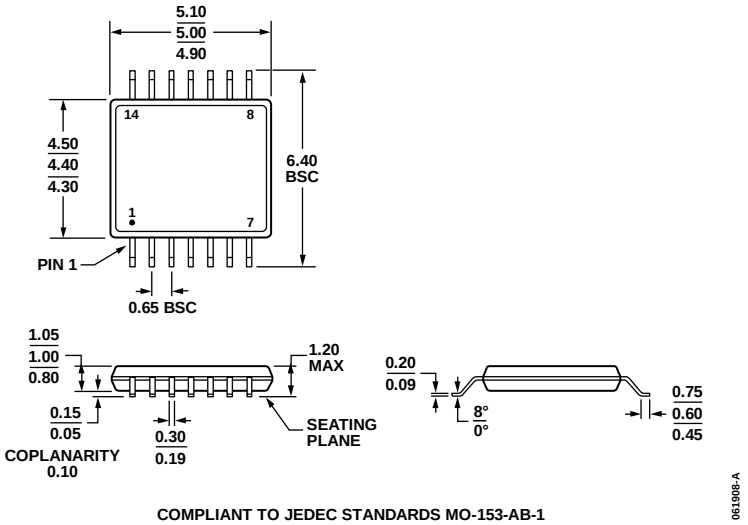

Figure 45. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Power-On Reset to Code	Accuracy	Internal Reference
AD5666BRUZ-1	−40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±16 LSB INL	1.25 V
AD5666BRUZ-1REEL7	−40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±16 LSB INL	1.25 V
AD5666BRUZ-2	−40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±16 LSB INL	2.5 V
AD5666BRUZ-2REEL7	−40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±16 LSB INL	2.5 V
AD5666ARUZ-2	−40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±32 LSB INL	2.5 V
AD5666ARUZ-2REEL7	−40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±32 LSB INL	2.5 V
EVAL-AD5666EBZ		Evaluation Board				

[1] Z = RoHS Compliant Part.

NOTES

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D05298–0–6/10(D)

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