VTM® Current Multiplier

VTM48KP020x088AA1

Sine Amplitude Converter™ (SAC™)

Features

- 43.2 Vdc to 1.8 Vdc 88 A current multiplier
  - Operating from standard 48 V or 24 V PRM® regulators
  - Up to 55 Volts DC input
  - K of 1/24 provides up to 88 A DC output current
- High efficiency (>95%) reduces system power consumption
- High density (921 A/in^3)
- Vicor's 1323 ChiP package enables low impedance interconnect to system board
- Provides enable / disable control, internal temperature monitoring, internal current monitoring
- ZVS / ZCS resonant Sine Amplitude Converter topology
- Parallel up to 10 modules

Typical Applications

- Computing and Telecom Systems
  - Optimized for the Intel VR12.5 Processor Specification
- Automated Test Equipment
- High Density Power Supplies
- Communications Systems

Product Ratings	
V_{IN} = 0 to 55 V	I_{OUT} = 88 A (nom)
V_{OUT} = 0 to 2.3 V (no load)	K = 1/24

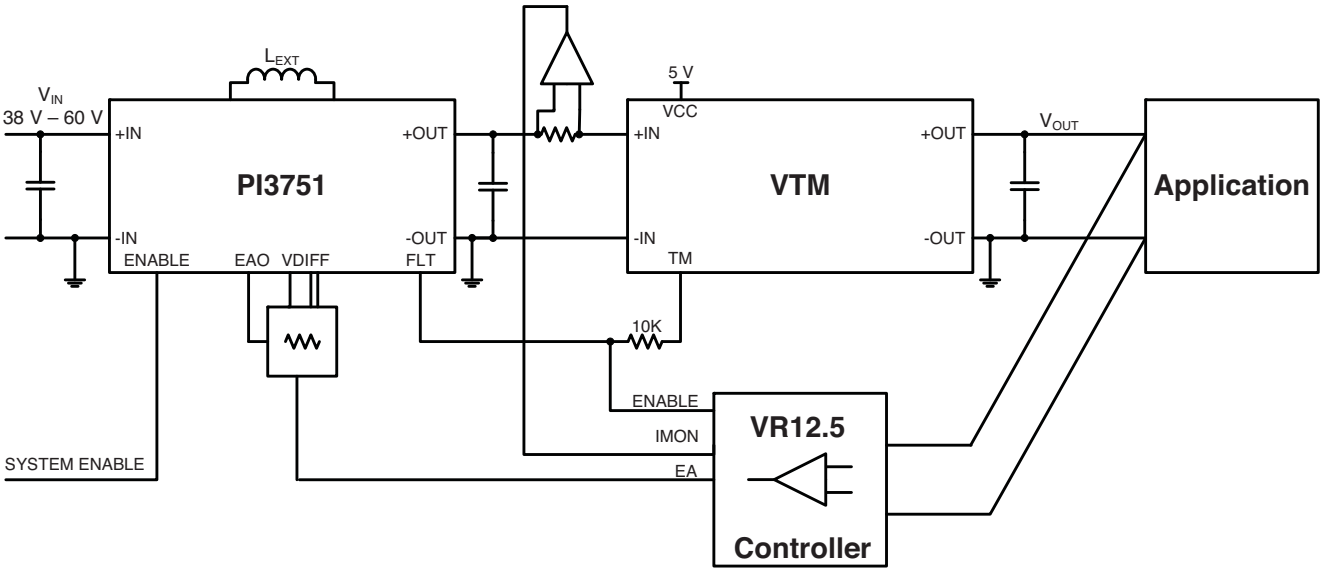
Product Description

The Vicor's 1323 ChiP VTM current multiplier is a high efficiency (>95%) Sine Amplitude Converter™ (SAC™) operating from a 0 to 55 Vdc primary bus to deliver a 0 to 2.3 Vdc low voltage output. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators; therefore capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Since the K factor of the VTM48KP020x088AA1 is 1/24, the capacitance value can be reduced by a factor of 576, resulting in savings of board area, materials and total system cost.

The VTM48KP020x088AA1 is provided in Vicor's 1323 ChiP package compatible with standard pick-and-place assembly processes. The co-molded ChiP package provides enhanced thermal management due to a large thermal interface area and superior thermal conductivity. The high conversion efficiency of the VTM48KP020x088AA1 increases overall system efficiency and lowers operating costs compared to conventional approaches.

The VTM48KP020x088AA1 enables the utilization of Factorized Power Architecture™ which provides efficiency and size benefits by lowering conversion and distribution losses and promoting high density point of load conversion.

Typical Application



Typical Application: Diagram for use within a Factorized Power, VR12.5 Design

Part Ordering Information

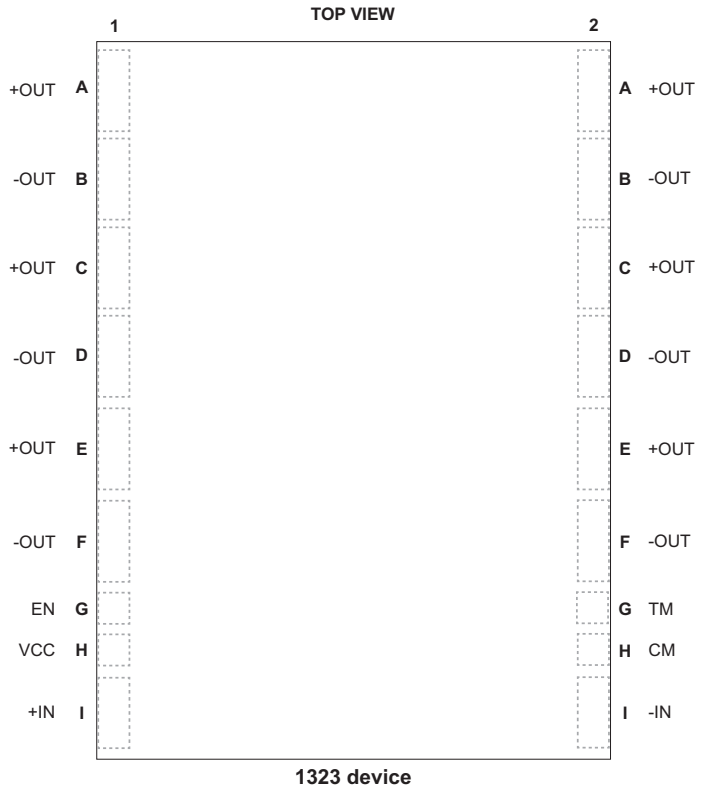
Device	Input Voltage Range	Package Type	Output Voltage	Temperature Grade	Output Current	Revision	Version
VTM	48K	P	020	x	088	A	A1
VTM = VTM	48K = 0 to 55 V	P = Through hole, 18 pin	020 = 2 V	T = -40 to 125°C	088 = 88 A	A	A1

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Standard Models

Part Number	V_{IN}	Package Type	V_{OUT}	Temperature	Current	Version
VTM48K**P**020**T**088AA1	0 to 55 V	Through hole, 18 pin	2 V (0 to 2.3 V)	-40 to 125°C	88 A	A1

Pin Configuration



Pin Numbering and Descriptions

Pin Number	Signal Name	Type	Function
A1, A2 C1, C2 E1, E2	+OUT	OUTPUT POWER	Positive output terminal
B1, B2 D1, D2 F1, F2	-OUT	OUTPUT POWER RETURN	Negative output terminal
G1	EN	INPUT	To disable VTM in system
G2	TM	OUTPUT	Temperature monitor and Power Good Flag
H1	VCC	INPUT	Power train controller supply
H2	CM	OUTPUT	Current monitor
I1	+IN	INPUT POWER	Positive input terminal
I2	-IN	INPUT POWER RETURN	Negative input terminal

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+IN to –IN		-1.0	60	V_{DC}
EN to - IN		-0.3	5.5	V_{DC}
TM to -IN		-0.3	5.5	V_{DC}
VCC to - IN		-0.3	5.5	V_{DC}
CM to - IN		0	5.5	V_{DC}
+ IN / - IN to + OUT / - OUT (hipot)	Non-isolated VTM		N/A	V_{DC}
+ IN / - IN to + OUT / - OUT (working)			0.2	V_{DC}
+ OUT to - OUT		-1.0	4	V_{DC}
Internal Operating Temperature	T Grade	-40	125	°C
Storage Temperature	T Grade	-40	125	°C

Electrical Specifications

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{INT} ≤ 125°C (T-Grade); All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Input voltage range	V_{IN}	VCC applied	**0**		**55**	Vdc
V_{IN} slew rate	dV_{IN}/dt				**1000**	V/ms
V_{IN} UV turn off	V_{IN_UV}	This protection is disabled for this product		N/A	**N/A**	V
Total No Load power dissipation	P_{NL}	V_{IN} = 43.2 V			**3.1**	W
		V_{IN} = 0 V to 55 V			**4.8**	
		V_{IN} = 43.2 V, T_C = 25°C		1.64	2.1	
		V_{IN} = 0 V to 55 V, T_C = 25°C			3.15	
Inrush current peak	I_{INRP}	VCC enable, V_{IN} = 43.2 V, C_{OUT} = 27000 µF, R_{LOAD} = 19.55 mΩ (See start up operation V_{CC} applied after input voltage)		6	**8**	A
DC input current	I_{IN_DC}	Steady state			3.73	A
Transfer ratio	K	K = V_{OUT}/V_{IN}, I_{OUT} = 0 A		**1/24**		V/V
Output voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}, I_{OUT} = 0 A	**0**		**2.36**	V
Output current (average)	I_{OUT_AVG}	Steady state **(See safe operating area)**			**88**	A
Output current (peak)	I_{OUT_PK}	T_{PEAK} ≤ 2 ms, I_{OUT_AVG} < 88 A, transient, duty cycle = 25%			**188**	A
Output power (average)	P_{OUT_AVG}	I_{OUT_AVG} ≤ 88 A			**193**	W
Efficiency (ambient)	η_{AMB}	V_{IN} = 43.2 V, I_{OUT} = 88 A	93.2	94.2		%
		V_{IN} = 26 V to 55 V, I_{OUT} = 88 A	88.0			
		V_{IN} = 43.2 V, I_{OUT} = 44 A	94.7	95.6		

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{INT} ≤ 125°C (T-Grade); All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain (Cont.)						
Efficiency (hot)	η_{HOT}	V_{IN} = 43.2 V, T_C = 100°C, I_{OUT} = 88 A	92.3	93.3		%
Efficiency (over load range)	$\eta_{20\%}$	17.6 A < I_{OUT} < 88 A	**89**			%
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 88 A	0.47	0.71	1	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 88 A	0.63	0.9	1.1	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 88 A	0.8	1.05	1.25	mΩ
Switching frequency	F_{SW}		**1.55**	1.65	**1.75**	MHz
Output ripple frequency	F_{SW_RP}		**3.1**	**3.3**	**3.5**	MHz
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 3000 µF, I_{OUT} = 88 A, V_{IN} = 43.2 V, 20 MHz BW		5	**10**	mV
Output inductance (parasitic)	L_{OUT_PAR}	Frequency up to 30 MHz, Simulated leads model		280		pH
Output capacitance (internal)	C_{OUT_INT}	Effective Value at 1.8 V_{OUT}		268		µF
Output capacitance (external)	C_{OUT}				**27000**	µF
Protection						
Overvoltage lockout	V_{IN_OVLO+}	This protection is disabled for this product	**N/A**	N/A	**N/A**	V
Overvoltage lockout response time constant	T_{OVLO}	Effective internal RC filter		N/A		µs
Output overcurrent trip	I_{OCP}	This protection is disabled for this product	**N/A**	N/A	**N/A**	A
Short circuit protection trip current	I_{SCP}	VTM latches after fault	260			A
Output overcurrent response time constant	T_{OCP}	Effective internal RC filter (Integrative).		N/A		ms
Short circuit protection response time	T_{SCP}	From detection to cessation of switching (Instantaneous)		1		µs
Thermal shutdown setpoint	T_{INT_OTP}		**125**	**130**	**135**	°C
Reverse inrush current protection		Reverse Inrush protection is enabled for this product				

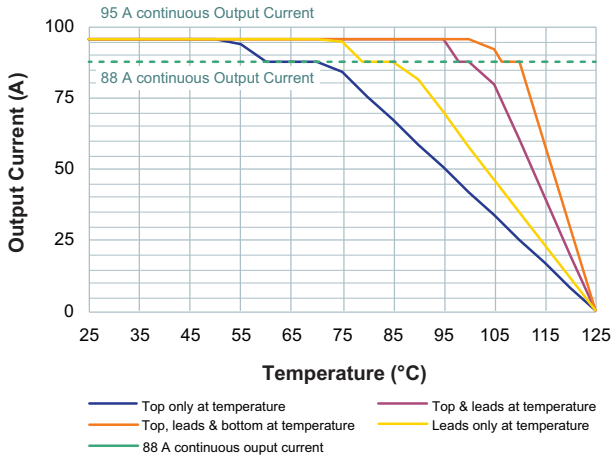


Figure 1 — *Safe thermal operating area*

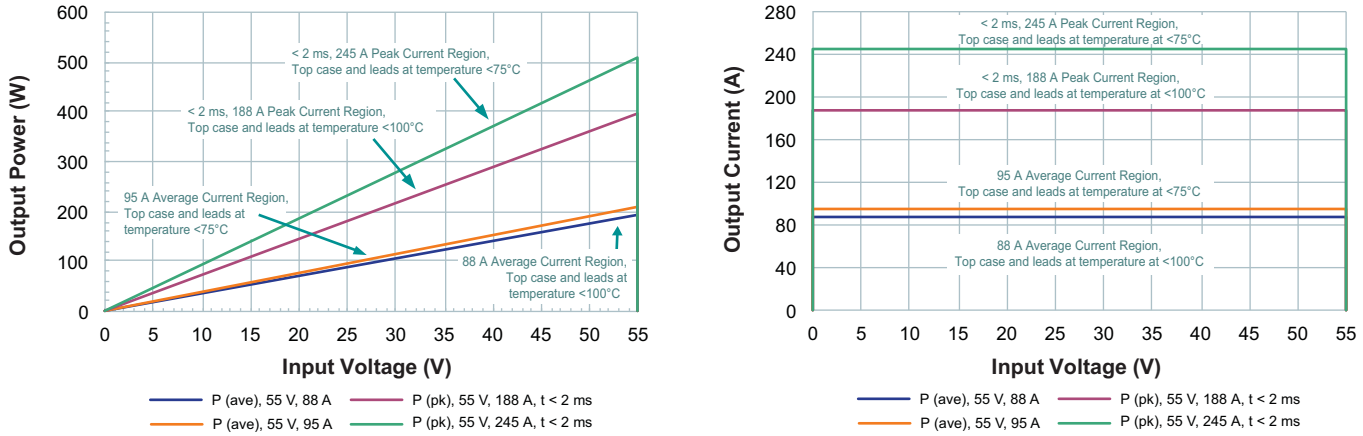


Figure 2 — *Safe electrical operating area*

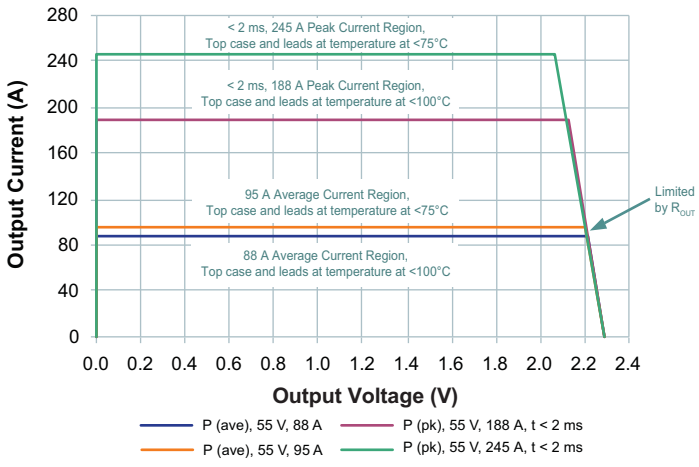


Figure 3 — *Safe electrical operating area*

Signal Characteristics

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{INT} ≤ 125°C (T-Grade); All other specifications are at T_{INT} = 25°C unless otherwise noted.

VTM VCC Supply: VCC	
• Used to wake up powertrain circuit. • A minimum of 4.85 V must be applied indefinitely for entire input voltage range to ensure normal operation.	• PRM® can be used as valid wake-up signal source. • VCC voltage must be continuously applied with the limit specified.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Steady	External VCC voltage	V_{VCC_EXT}	Required for start up, and steady state operation.	**4.85**		**5.35**	V
		VCC current draw	I_{VCC}	VCC = 4.85 V, Vin = 0 V		140	**160**	mA
				Fault mode. VCC > 4.85 V		25		
	Start Up	VCC inrush current	I_{INR_VCC}	VCC = 5.35 V, dVCC/dt = 1000 V/ms			**1**	A
	Transitional	VCC to V_{OUT} turn-on delay	T_{ON}	V_{IN} pre-applied, EN floating, VCC enable, C_{EN} = 0 µF, C_{OUT} = $C_{OUT\_EXT(MAX)}$	23	28	**34**	ms
		VCC to EN delay	T_{VCC_EN}	VCC = 4.85 V to EN high, V_{IN} = 0 V, dVCC/dt = 1000 V/ms		0.2	**0.3**	ms
		Internal VCC capacitance	C_{VCC_INT}	VCC = 0 V		1		µF

ENABLE: EN	
• The EN pin disables the VTM module. When held below 0.9 V, the VTM module will be disabled. • EN pin outputs 4.7 V minimum during normal operation. EN pin is equal to 4.7 V minimum during fault mode given VCC > 4.85 V and floating EN pin.	• Module will shutdown when pulled low with an impedance less than 400 Ω.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	EN voltage	V_{EN}		**4.7**	5	**5.3**	V
		EN source current	I_{EN_OP}			50		µA
	Start Up	EN source current	I_{EN_EN}			50		µA
DIGITAL INPUT/ OUTPUT	Enable	EN voltage	V_{EN_EN}		**0.9**	1	**1.1**	V
	Disable	EN voltage (disable)	V_{EN_DIS}				**0.9**	V
		EN resistance (external)	R_{EN_EXT}	Connected to -IN. Min value to guarantee startup (open circuit OK), EN >1.5 V	**30**			kΩ
	Transitional	EN disable time	$T_{EN\_DIS\_T}$	From EN pulled low to VTM stops switching		1.2		µs

Signal Characteristics (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{INT} ≤ 125°C (T-Grade); All other specifications are at T_{INT} = 25°C unless otherwise noted.

Current Monitor: CM

- The CM pin voltage varies between 0 V and 2.65 V representing the output current within ±20% under all operating line temperature conditions between 0% and 100% load.
- The CM pin provides a DC analog voltage proportional to the output current of the VTM module.

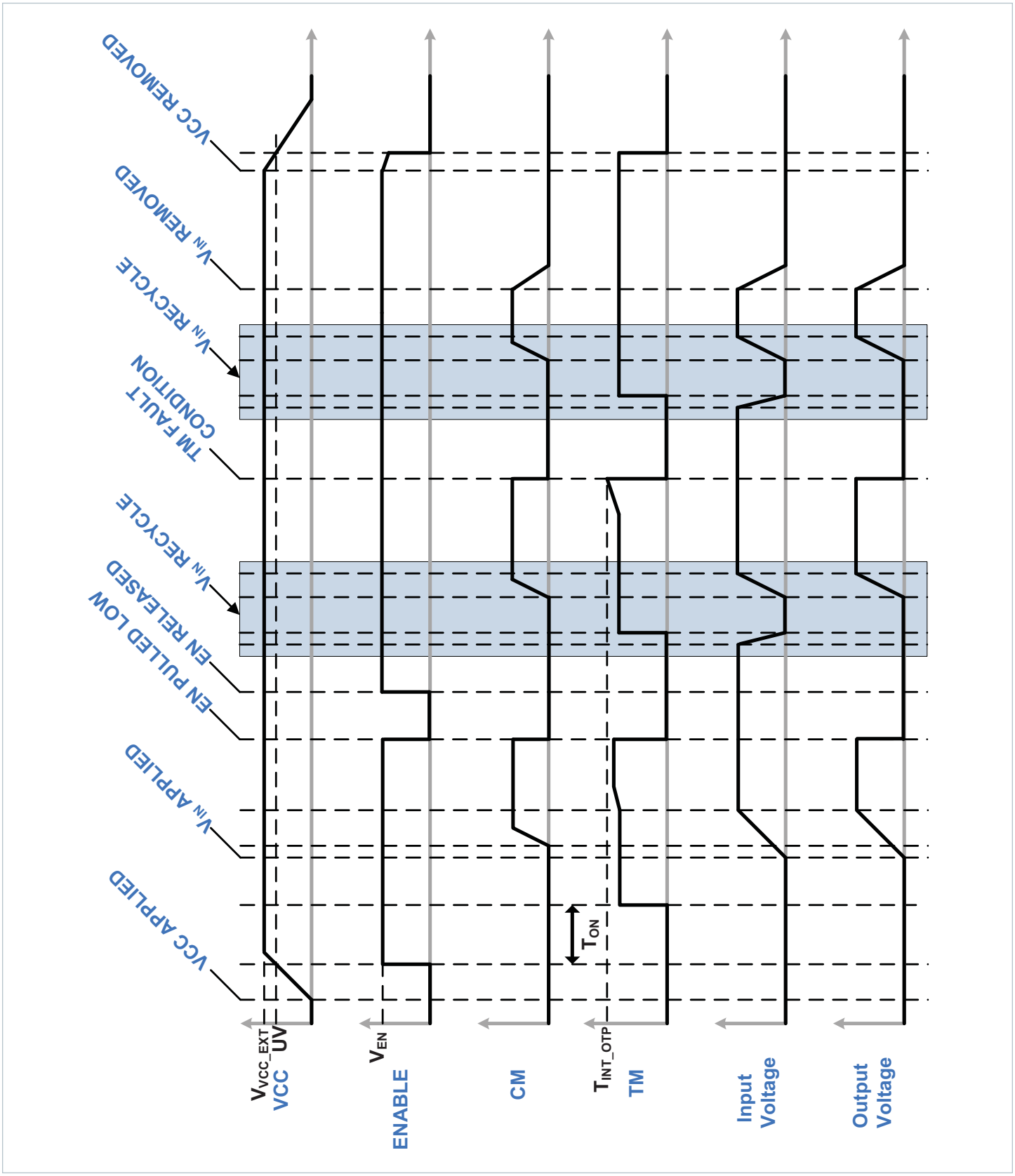
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	CM Voltage (No Load)	V_{CM_NL}	T_{INT} = 25°C, V_{IN} = 43.2 V, I_{OUT} = 0 A	0	0.03	0.05	V
		CM Voltage (50%)	$V_{CM\_50\%}$	T_{INT} = 25°C, V_{IN} = 43.2 V, I_{OUT} = 44 A		1.33		V
		CM Voltage (Full Load)	V_{CM_FL}	T_{INT} = 25°C, V_{IN} = 43.2 V, I_{OUT} = 88 A		2.65		V
		CM Gain	A_{CM}	T_{INT} = 25°C, V_{IN} = 43.2 V, 0% ≤ I_{OUT} ≤ 100%		30		mV/A
		CM Resistance (External)	R_{CM_EXT}		2.5			MΩ

Temperature Monitor: TM

- The TM pin monitors the internal temperature of the VTM controller IC within an accuracy of ±5 °C.
- Can be used as a "Power Good" flag to verify that the VTM module is operating.
- The TM pin has a room temperature setpoint of 3 V and approximate gain of 10 mV/K.
- Output drives Temperature Shutdown comparator

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	TM voltage	V_{TM_AMB}	T_{INT} controller = 27°C, I_{TM} <100 µA	2.85	3	3.15	V
		TM source current	I_{TM}				**100**	µA
		TM gain	A_{TM}			10		mV/K
		TM voltage ripple	V_{TM_PP}	C_{TM} = 0 F, V_{IN} = 43.2 V, I_{OUT} = 88 A		150	**350**	mV
DIGITAL OUTPUT (FAULT FLAG)	Steady	TM disable voltage	V_{TM_DIS}	PGOOD deasserted		0.2		V
		TM Enable Source Current	I_{TM_EN}	TM > 1 V	20			mA
		TM Fault Sink Current	I_{TM_FAULT}	TM ≤ 0.1 V, Fault state	1			mA
	Transitional	TM capacitance (external)	C_{TM_EXT}				**100**	pF
		TM fault response time	T_{FR_TM}	From fault detection to TM driven low		0.02		µs

Timing Diagram



Application Characteristics

The following values, typical of an application environment, are collected at T_C = 25 °C unless otherwise noted. See associated figures for general trend data.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	TYP	UNIT
Total No load power dissipation	P_{NL}	V_{IN} = 43.2 V, VTM enabled	1.8	W
Efficiency (ambient)	η_{AMB}	V_{IN} = 43.2 V, I_{OUT} = 88 A	93.8	%
Efficiency (hot)	η_{HOT}	V_{IN} = 43.2 V, I_{OUT} = 88 A, T_C = 100°C	92.7	%
Output resistance (cold)	R_{OUT_COLD}	V_{IN} = 43.2 V, I_{OUT} = 88 A, T_C = -40°C	0.81	mΩ
Output resistance (ambient)	R_{OUT_AMB}	V_{IN} = 43.2 V, I_{OUT} = 88 A	0.95	mΩ
Output resistance (hot)	R_{OUT_HOT}	V_{IN} = 43.2 V, I_{OUT} = 88 A, T_C = 100°C	1.16	mΩ
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 0 F, I_{OUT} = 88 A, V_{IN} = 43.2 V, 20 MHz BW	125	mV
V_{OUT} transient (positive)	V_{OUT_TRAN+}	I_{OUT_STEP} = 0 A to 88 A, V_{IN} = 43.2 V, I_{SLEW} = 24 A/µs	50	mV
V_{OUT} transient (negative)	V_{OUT_TRAN-}	I_{OUT_STEP} = 88 A to 0 A, V_{IN} = 43.2 V, I_{SLEW} = 150 A/µs	42	mV

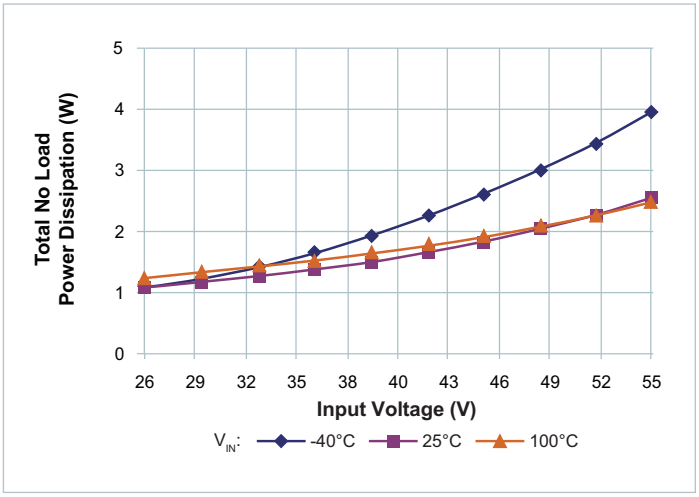


Figure 4 — *Total no load power dissipation vs. input voltage*

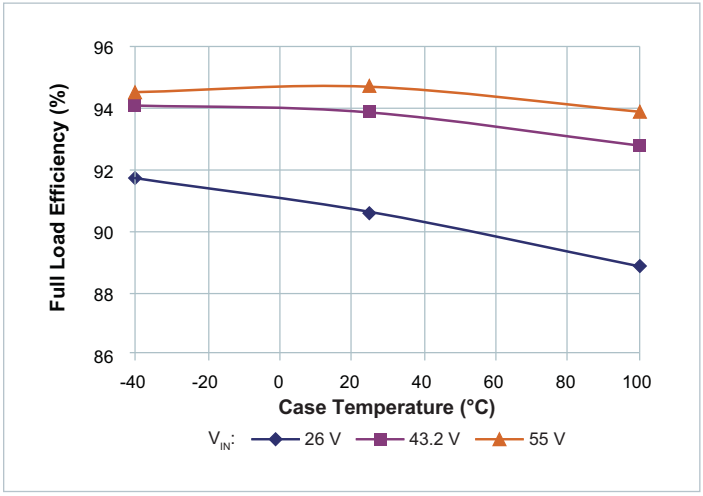


Figure 5 — *Full load efficiency vs. case temperature*

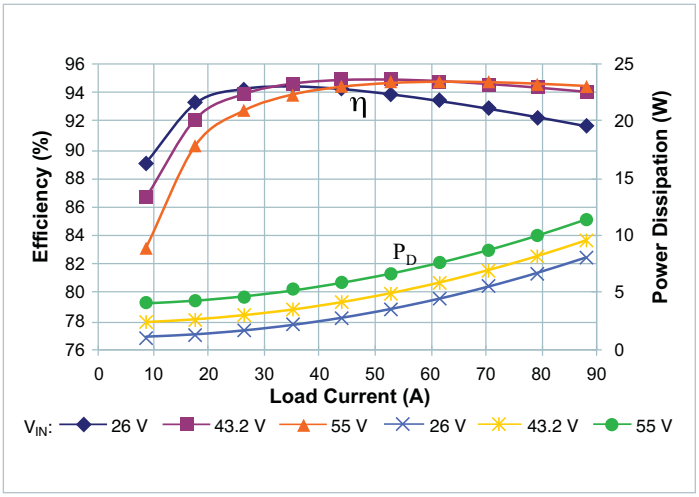


Figure 6 — *Efficiency and power dissipation at –40°C case temperature*

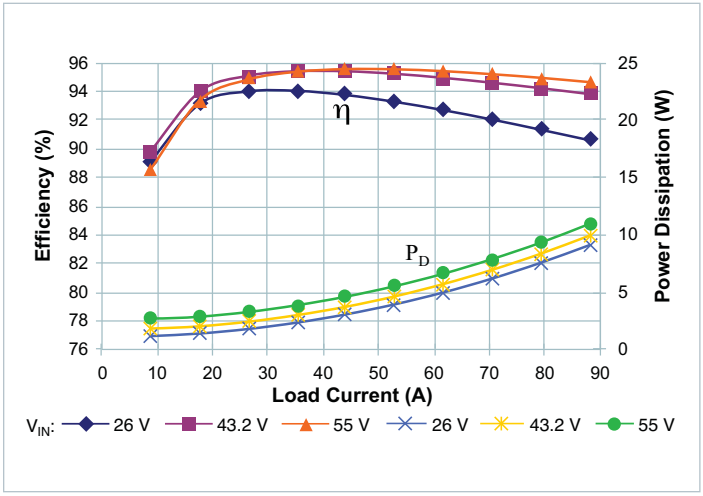


Figure 7 — *Efficiency and power dissipation at 25°C case temperature*

Application Characteristics (Cont.)

The following values, typical of an application environment, are collected at T_C = 25 °C unless otherwise noted. See associated figures for general trend data.

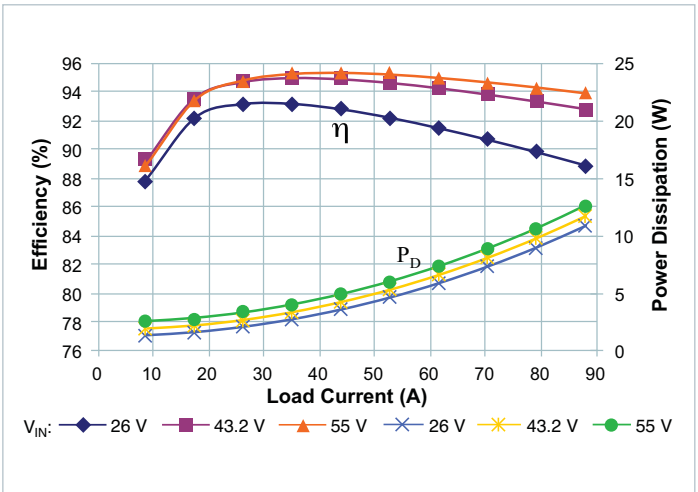


Figure 8 — *Efficiency and power dissipation at 100°C case temperature*

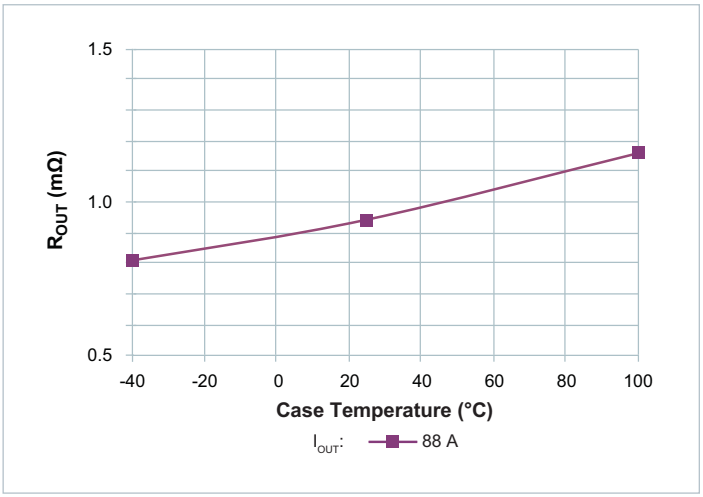


Figure 9 — *Output resistance (R_{OUT}) vs. case temperature at 43.2 V nominal input voltage*

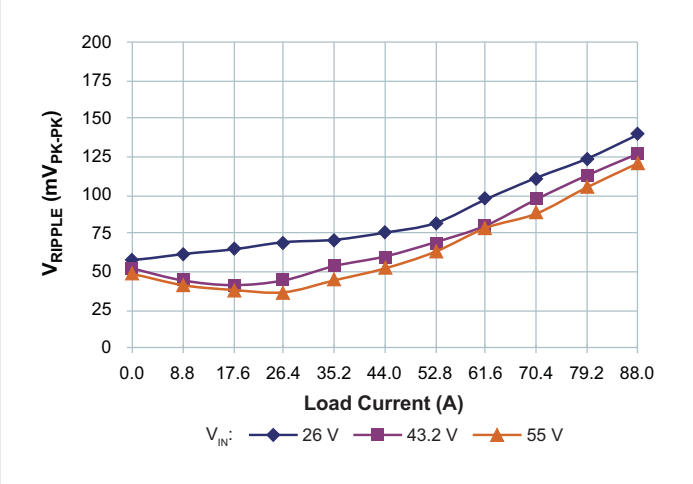


Figure 10 — *Output voltage ripple (V_{RIPPLE}) vs. Load (I_{OUT}); No external C_{OUT}.*

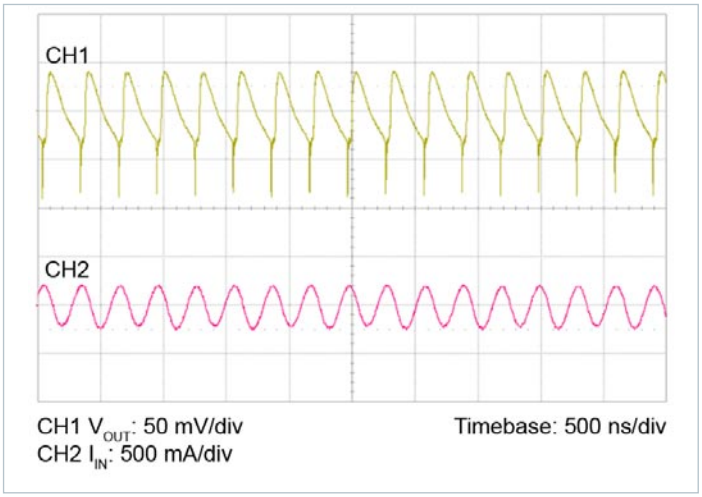


Figure 11 — *Full load ripple, 100 µF C_{IN}; No external C_{OUT}.*

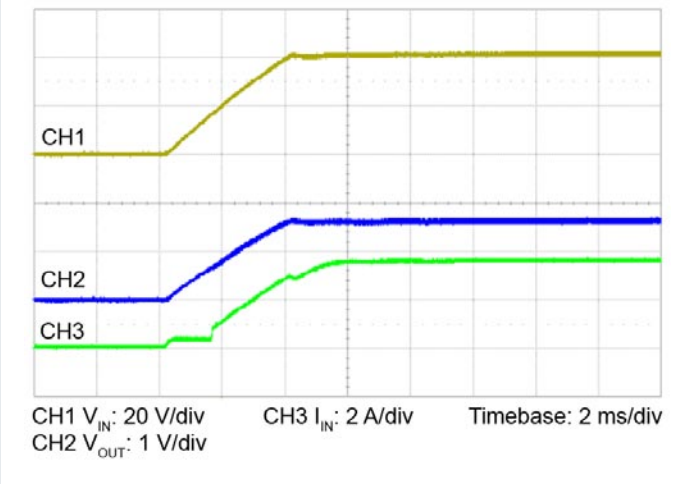


Figure 12 — *Start up from application of V_{IN}; VCC pre-applied C_{OUT} = 3000 µF*

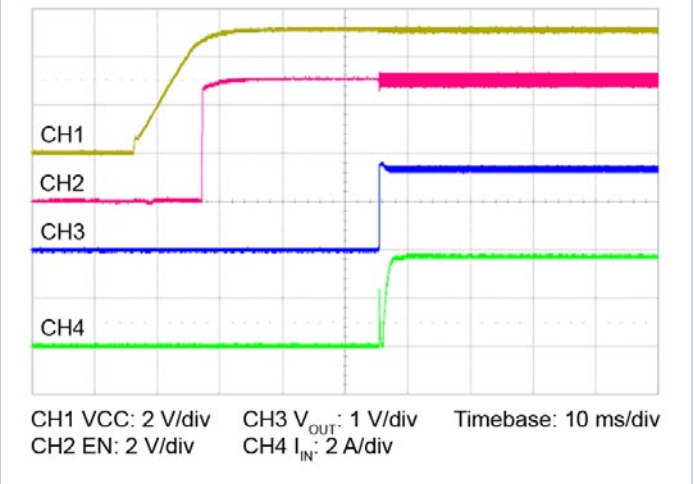


Figure 13 — *Start up from application of VCC; V_{IN} pre-applied C_{OUT} = 3000 µF*

Application Characteristics (Cont.)

The following values, typical of an application environment, are collected at T_C = 25 °C unless otherwise noted. See associated figures for general trend data.

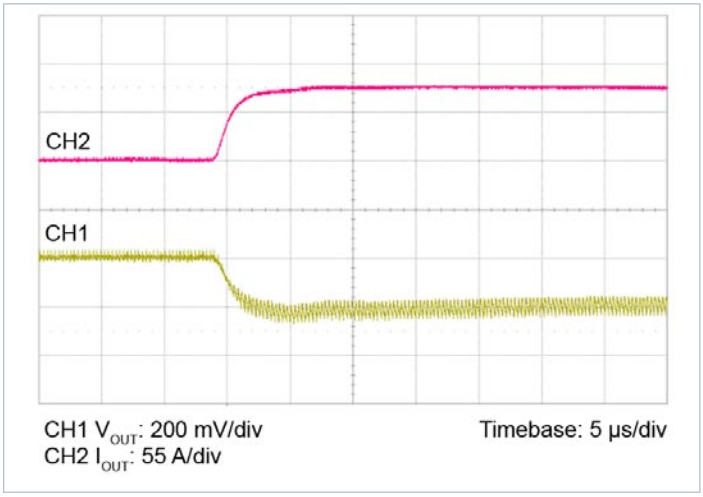


Figure 14 — *0 A – 88 A transient response: C_{IN} = 100 µF, no external C_{OUT}*

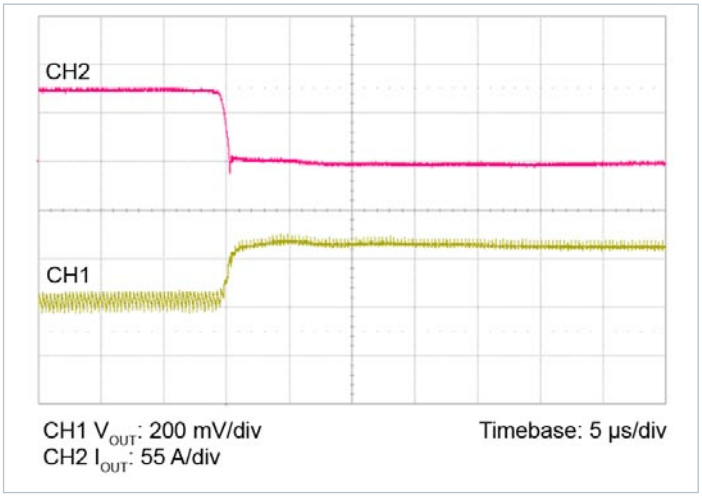


Figure 15 — *88 A – 0 A transient response: C_{IN} = 100 µF, no external C_{OUT}*

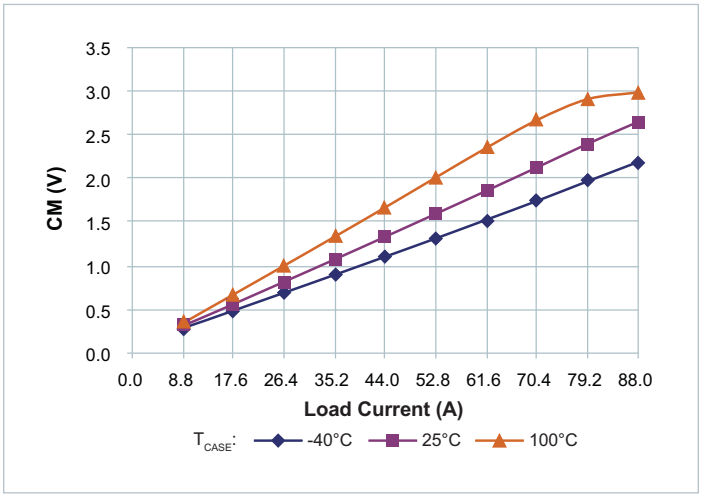


Figure 16 — *CM voltage vs. load current at 43.2 V nominal input voltage*

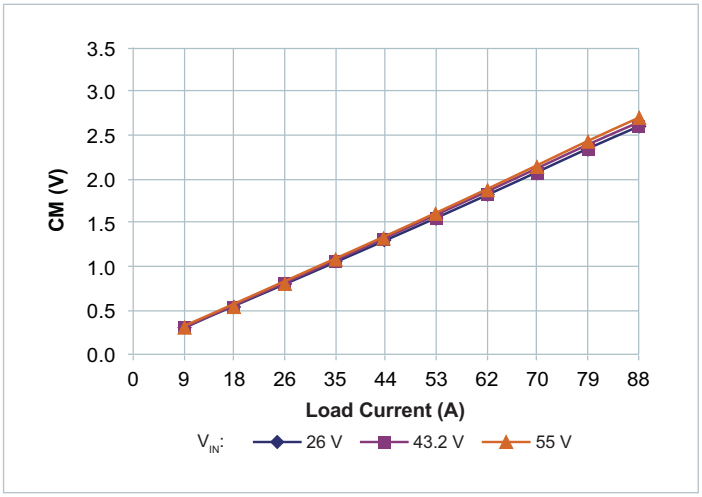


Figure 17 — *CM voltage vs. load current at 25°C case temperature*

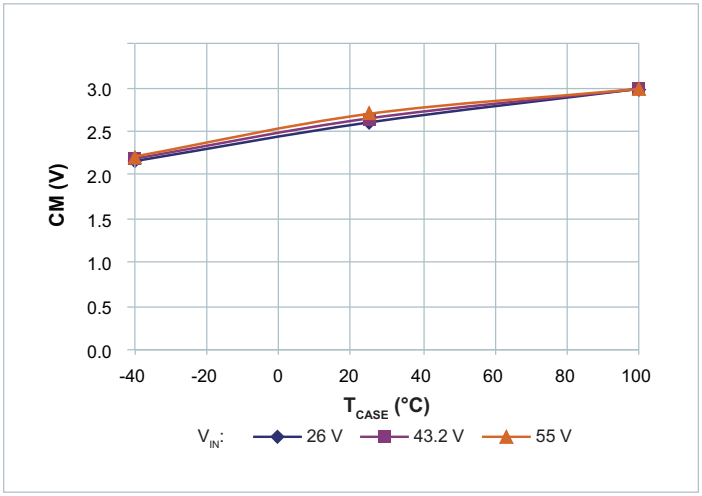


Figure 18 — *88 A Full load CM voltage vs. case temperature (T_{CASE})*

General Characteristics

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{INT} ≤ 125°C (T-Grade); All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
		Mechanical				
Length	L		22.37 / [0.881]	22.50 / [0.886]	22.63 / [0.891]	mm/[in]
Width	W		15.09 / [0.594]	15.47 / [0.609]	15.85 / [0.624]	mm/[in]
Height	H		4.45 / [0.175]	4.50 / [0.177]	4.55 / [0.179]	mm/[in]
Volume	Vol	No heat sink		1.57 / [0.096]		cm^3/[in^3]
Weight	W			5.8 / [0.205]		g/[oz]
Lead finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
		Thermal				
Operating temperature	T_{INT}	T-Grade	-40		125	°C
Thermal resistance top side	$\phi_{INT-TOP}$	Estimated thermal resistance to maximum temperature internal component from isothermal top		3.5		°C/W
Thermal resistance leads	$\phi_{INT-LEADS}$	Estimated thermal resistance to maximum temperature internal component from isothermal leads		2.6		°C/W
Thermal resistance bottom side	$\phi_{INT-BELLY}$	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		3.2		°C/W
Thermal capacity				4.25		Ws/°C
		Assembly				
Peak compressive force applied to case (Z-axis)		Supported by leads only			5	lbs
					9.27	lbs/in^2
Storage temperature	T_{ST}	T-Grade	-40		125	°C
ESD withstand	ESD_{HBM}	Human Body Model, "JEDEC JESD 22-A114C.01"	2000			Vdc
	ESD_{CDM}	Charge Device Model, "JEDEC JESD 22-C101-C"	500			

General Characteristics (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{INT} ≤ 125°C (T-Grade); All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
		Safety				
Isolation voltage (hipot)	V_{HIPOT}	Non isolated VTM	**N/A**			
Isolation capacitance	C_{IN_OUT}	Unpowered unit		0.22		µF
Isolation resistance	R_{IN_OUT}			1		Ω
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.79		MHrs
		Telcordia Issue 2 - Method I Case III; Ground Benign, Controlled		8.82		MHrs
Agency approvals / standards		cTUVus				
		cURus				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Using the Control Signals VCC, EN, TM, CM

VCC: The VTM VCC Supply

This pin is an input pin which powers the internal VCC circuit within the specified voltage range of 4.85 V to 5.35 V. This voltage is required for VTM current multiplier start up and must be applied for entire input voltage range.

Some additional notes on the using the VCC pin:

- The VCC voltage must be applied indefinitely allowing for continuous operation for entire input voltage range of VTM.
- The fault response of the VTM module is latching. Recycle of input voltage in presence of VCC is required in order to restart the unit, provided the EN pin is floating.

EN: ENABLE

This pin can be used to accomplish the following functions:

- Output disable: EN pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 400 Ω.
- EN pulled low of VTM module is latching. Recycle of input voltage in presence of VCC is required in order to restart the unit, provided the EN pin is floating.

TM: Temperature Monitor

This pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- Monitor the control IC temperature: The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27ºC). If a heat sink is applied, TM can be used to thermally protect the system.
- Fault detection flag: The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM signal.

CM: Current Monitor

This pin provides a voltage proportional to the output current of the VTM module. The nominal voltage will vary between 0.03 V and 2.65 V over the output current range of the VTM module (See Figures 16 - 18). The accuracy of the CM pin will be within (±20%) under all line and temperature conditions between 0% and 100% load.

Start Up Behavior

Depending on the sequencing of the VCC with respect to the input voltage, the behavior during start-up will vary as follows:

- **Normal start up operation (VCC applied prior to Input voltage):** In this case the controller is active prior to ramping the input voltage. In this mode of operation, EN signal and CM signal appear when VCC crosses its under-voltage point. TM signal appearance is delayed by about T_{ON} time from EN signal. CM signal goes to 0 V when TM signal appears with no input voltage applied. It is recommended to apply the input voltage after TM signal appearance. When the input voltage is applied, the VTM module output voltage will track the input (See Figure 12). The inrush current is determined by the input voltage rate of rise, input and output capacitance. If the VCC voltage is removed prior to the input reaching 0 V, the VTM may shut down. This mode of operation is recommended when this VTM operates with upstream regulator such as PRM. Timing diagram shows the power up sequence for such mode of operation.
- **Start up operation (VCC applied after Input voltage. *It is not recommended to start up the VTM in this order*):** In this case the VTM module output will begin to rise upon the application of the VCC voltage (See Figure 13). However, the Adaptive Soft Start Circuit is disabled internal to VTM and start-up current will be unlimited. When VCC applied, EN and CM signal appear after VCC crosses its under-voltage point. TM and output voltage signal appear after delay of T_{ON} time with respect to EN signal. In this mode of start-up, input voltage is applied prior to VCC. So input capacitance is already charged prior to VCC applied. When VCC applied, VTM powertrain generates the output voltage and charges the output capacitance. In this mode of operation inrush is due to the output capacitance. The following diagram shows the power up sequence for such mode of operation. This product requires an external soft start circuit to limit inrush current in this mode of operation. This product does not support the auto-restart feature in fault conditions.

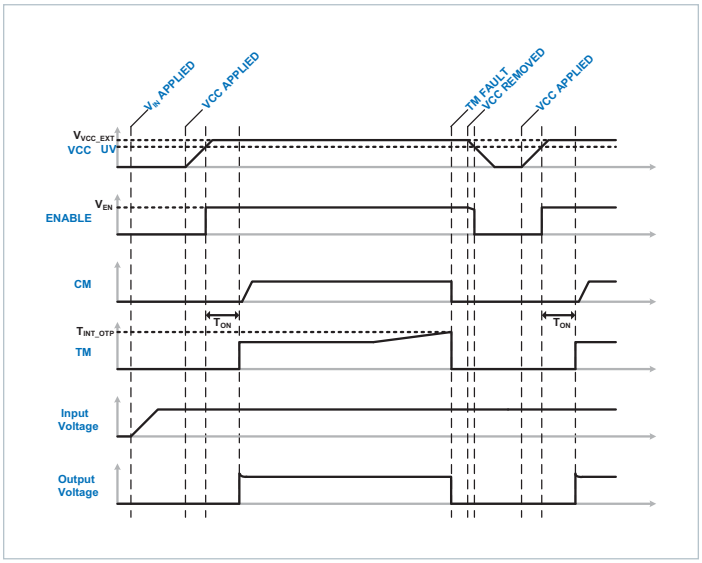
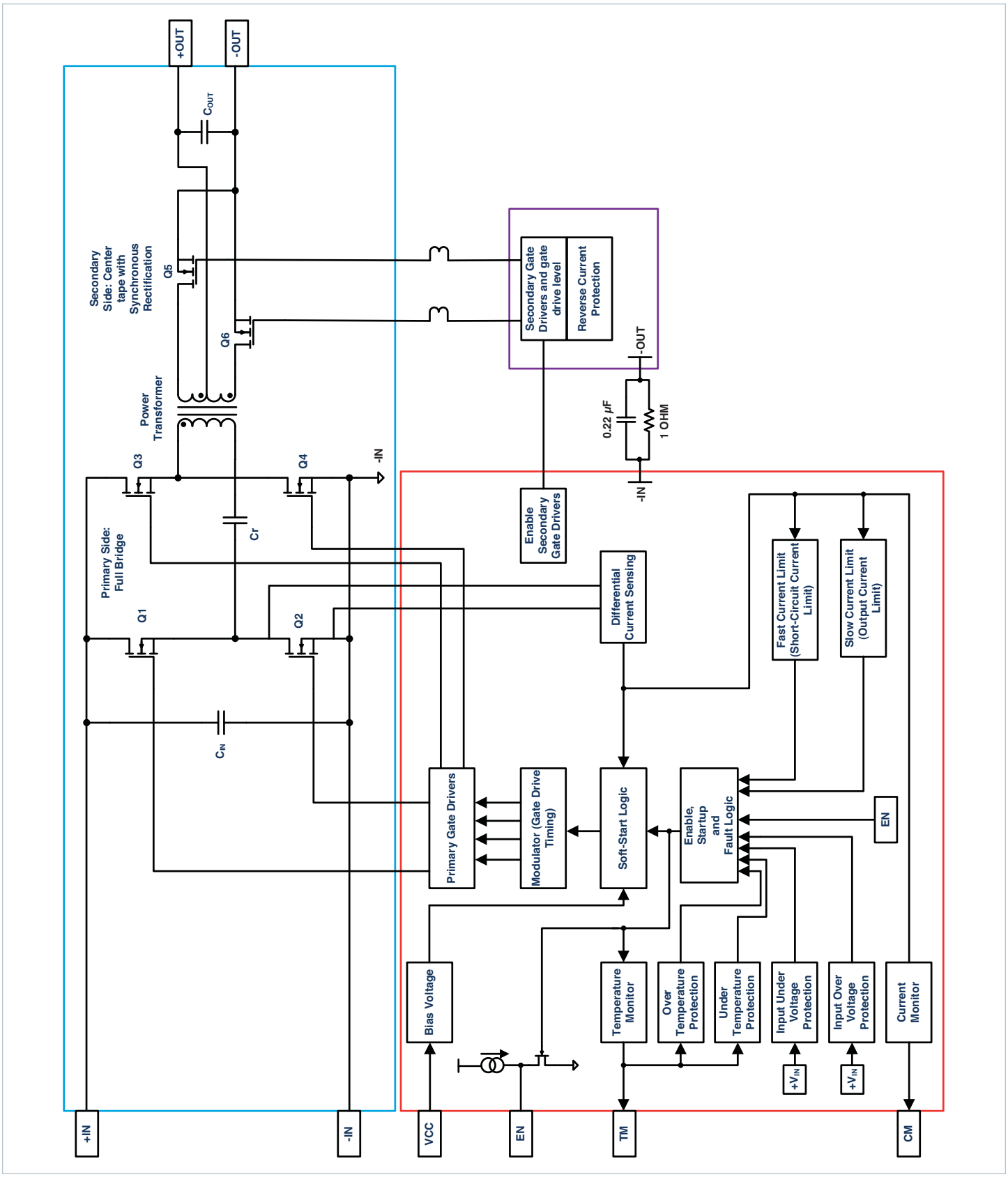


Figure 19 — *VCC applied after Input Voltage*

VTM Module Block Diagram



Sine Amplitude Converter™ Point of Load Conversion

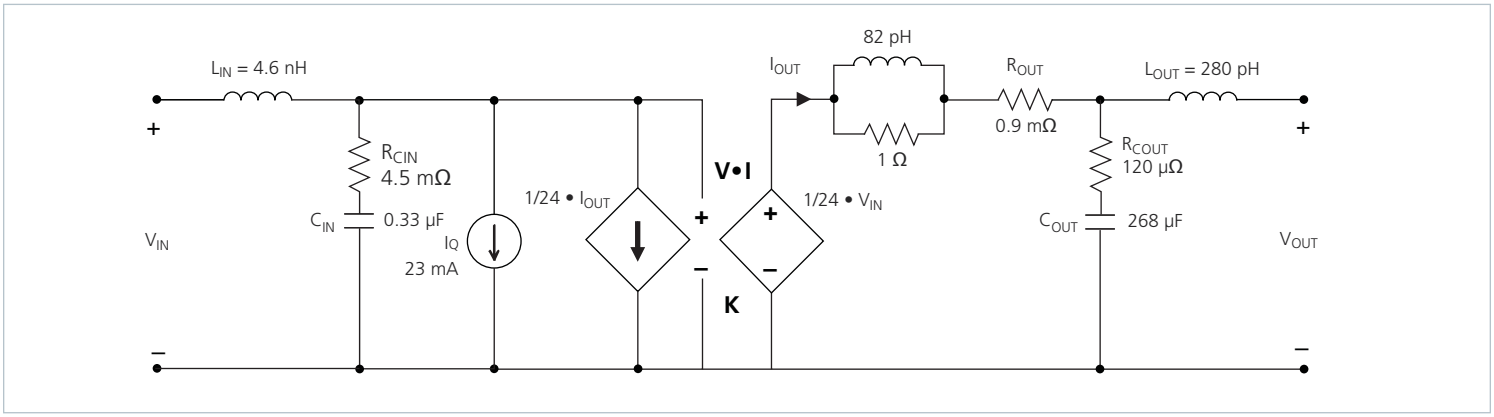


Figure 20 — *VI Chip® product AC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings as shown in the VTM Module Block Diagram). The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The VTM48KP020x088AA1 SAC can be simplified into the following model:

At no load:

$$V_{OUT} = V_{IN} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC.
Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \qquad (2)$$

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \qquad (3)$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \qquad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DSON} of the input and output MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control and gate drive circuitry.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{OUT} = 0\ \Omega$ and $I_Q = 0$ A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{IN} as shown in Figure 21.

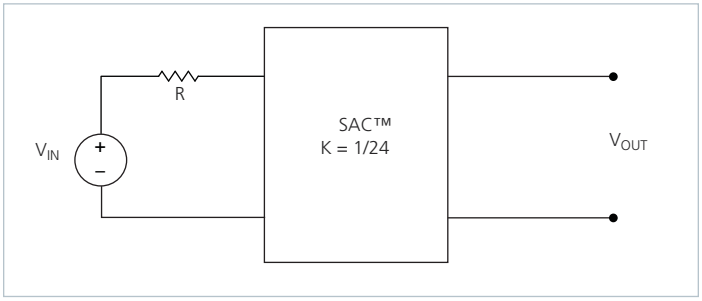


Figure 21 — *K = 1/24 Sine Amplitude Converter with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R_{IN}) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_Q is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{IN} \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{OUT} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1 Ω, the effective R as seen from the secondary side is 1.74 mΩ, with K = 1/24 as shown in Figure 21.

A similar exercise should be performed with the addition of a capacitor or shunt impedance at the input to the SAC.
A switch in series with Vin is added to the circuit. This is depicted in Figure 22.

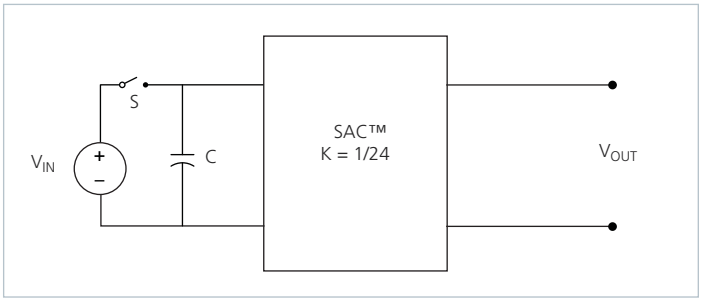


Figure 22 — *Sine Amplitude Converter™ with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{IN}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \bullet K \qquad (8)$$

Substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \qquad (9)$$

The equation in terms of the output has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity, results in an effectively larger capacitance on the output when expressed in terms of the input. With a K = 1/24 as shown in Figure 22, C = 1 µF would appear as C = 576 µF when viewed from the output.

Low impedance is a key requirement for powering a high-current, low voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the VTM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load. It includes the components due to input voltage and VCC voltage.
- Resistive loss (R_{OUT}): refers to the power loss across the VTM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \qquad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \qquad (12)$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}\right)$$

Input and Output Filter Design

A major advantage of a SAC™ system versus a conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:

  To take full advantage of the VTM current multiplier dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. Input capacitance may be added to improve transient performance or compensate for high source impedance.

- Further reduce input and/or output voltage ripple without sacrificing dynamic response:

  Given the wide bandwidth of the VTM module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the VTM module multiplied by its K factor.

- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:

  The module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.
  The VI Chip® module input/output voltage ranges must not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Capacitive Filtering Considerations for a Sine Amplitude Converter™

It is important to consider the impact of adding input and output capacitance to a Sine Amplitude Converter on the system as a whole. Both the capacitance value and the effective impedance of the capacitor must be considered.

A Sine Amplitude Converter has a DC Rout value which has already been discussed. The AC Rout of the SAC contains several terms:

- Resonant tank impedance
- Input lead inductance and internal capacitance
- Output lead inductance and internal capacitance

The values of these terms are shown in the behavioral mode. It is important to note on which side of the transformer these impedances appear and how they reflect across the transformer given the K factor.

The overall AC impedance varies from model to model. For most models it is dominated by DC Rout value from DC to beyond 500 KHz. The behavioral model should be used to approximate the AC impedance of the specific model.

Any capacitors placed at the output of the VTM reflect back to the input of the VTM module by the square of the K factor (Eq. 9) with the impedance of the VTM module appearing in series. It is very important to keep this in mind when using a PRM® regulator to power the VTM module. Most PRM modules have a limit on the maximum amount of capacitance that can be applied to the output. This capacitance includes both the PRM output capacitance and the VTM module output capacitance reflected back to the input. In PRM remote sense applications, it is important to consider the reflected value of VTM module output capacitance when designing and compensating the PRM control loop.

Capacitance placed at the input of the VTM module appear to the load reflected by the K factor with the impedance of the VTM module in series. In step-down ratios, the effective capacitance is increased by the K factor. The effective ESR of the capacitor is decreased by the square of the K factor, but the impedance of the module appears in series. Still, in most step-down VTM modules an electrolytic capacitor placed at the input of the module will have a lower effective impedance compared to an electrolytic capacitor placed at the output. This is important to consider when placing capacitors at the output of the module. Even though the capacitor may be placed at the output, the majority of the AC current will be sourced from the lower impedance, which in most cases will be the module. This should be studied carefully in any system design using a module. In most cases, it should be clear that electrolytic output capacitors are not necessary to design a stable, well-bypassed system.

Current Sharing

The SAC™ topology bases its performance on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal current multiplier with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array with the same K factor, the VTM module will inherently share the load current (typically 5%) with parallel units according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide the PCB layout as symmetric as possible.
- Apply same input / output filters (if present) to each unit.

For further details see AN:016 Using BCM® Bus Converters in High Power Arrays.

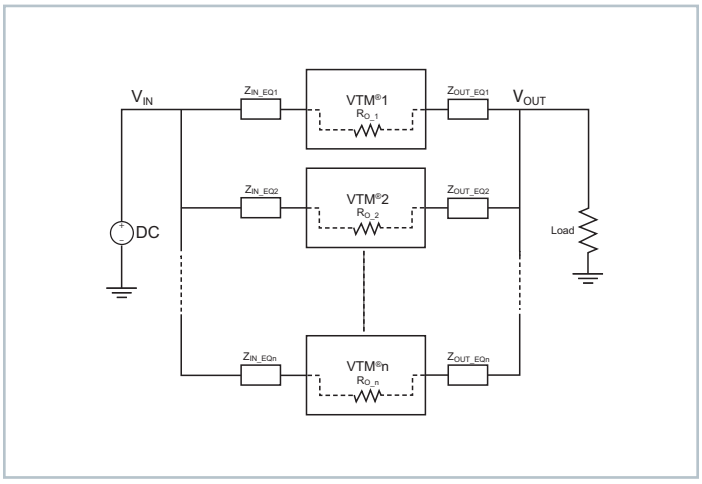


Figure 23 — *VTM current multiplier array*

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® products are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

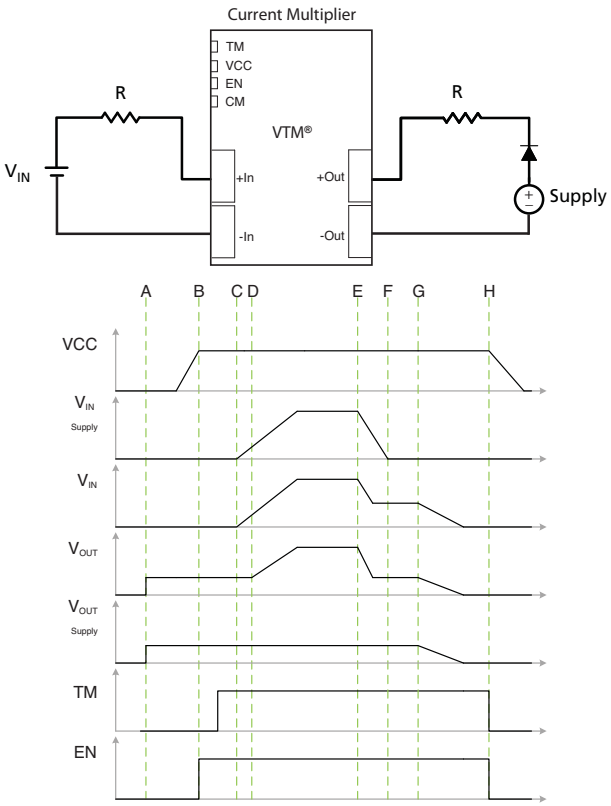
The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum current of VTM module)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t

Reverse Inrush Current Protection

The VTM48KP020x088AA1 provides reverse inrush protection which prevents reverse current flow until the input voltage is high enough to first establish current flow in the forward direction. In the event that there is a DC voltage present on the output before the VTM module is powered up, this feature protects sensitive loads from excessive dV/dT during power up as shown in Figure 24.

If a voltage is present at the output of the VTM module which satisfies the condition Vout > Vin • K after a successful power up the energy will be transferred from secondary to primary. The input to output ratio of the VTM module will be maintained. The VTM module will continue to operate in reverse as long as the input and output voltages are within the specified range. The VTM48KP020x088AA1 has not been qualified for continuous reverse operation.



A: V_{OUT} supply > 0 V

B: VCC to -IN > 4.85 V controller wakes-up, EN pulled high, reverse inrush protection blocks V_{OUT} supplying V_{IN}

C: V_{IN} supply ramps up

D: $V_{IN} > V_{OUT}/K$, powertrain starts in normal mode

E: V_{IN} supply ramps down

F: $V_{IN} > V_{OUT}/K$, powertrain transfers reverse energy

G: V_{OUT} ramps down, V_{IN} follows

H: VCC turns off

Figure 24 — *Reverse inrush protection*

Thermal Considerations

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum power that is available from a ChiP.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 25 shows the "thermal circuit" for a 1323 ChiP VTM in an application where the top, bottom, and leads are cooled. In this case, the VTM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP}, T_{CASE_BOTTOM}, and T_{LEADS}. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation would provide an estimate of heat flow through the various pathways as well as internal temperature.

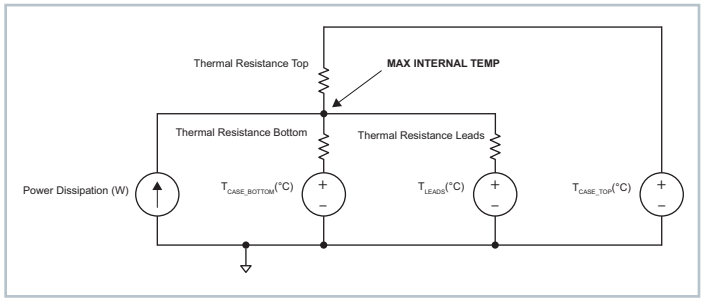


Figure 25 — *Double side cooling and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$T_{INT} - PD_1 \bullet 3.5 = T_{CASE\_TOP}$

$T_{INT} - PD_2 \bullet 3.2 = T_{CASE\_BOTTOM}$

$T_{INT} - PD_3 \bullet 2.6 = T_{LEADS}$

$PD_{TOTAL} = PD_1 + PD_2 + PD_3$

Where T_{INT} represents the internal temperature and PD_1, PD_2, and PD_3 represent the heat flow through the top side, bottom side, and leads respectively.

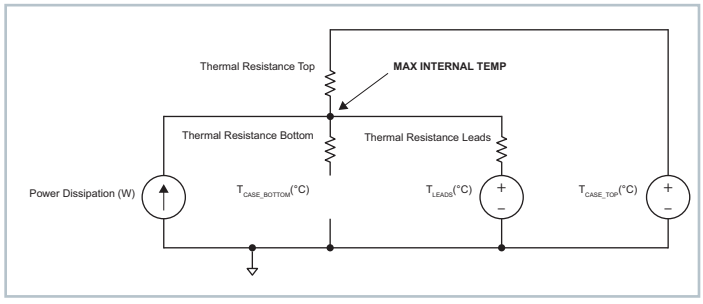


Figure 26 — *One side cooling and leads thermal model*

Figure 26 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$T_{INT} - PD_1 \bullet 3.5 = T_{CASE\_TOP}$

$T_{INT} - PD_3 \bullet 2.6 = T_{LEADS}$

$PD_{TOTAL} = PD_1 + PD_3$

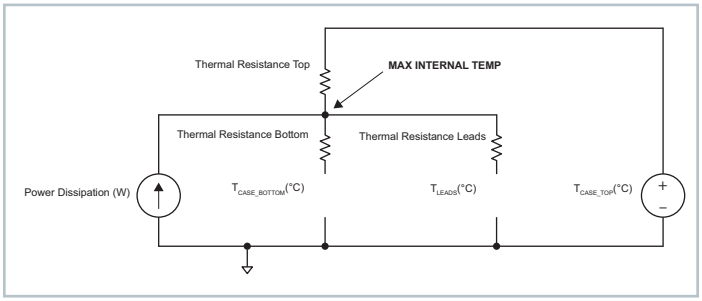


Figure 27 — *One side cooling thermal model*

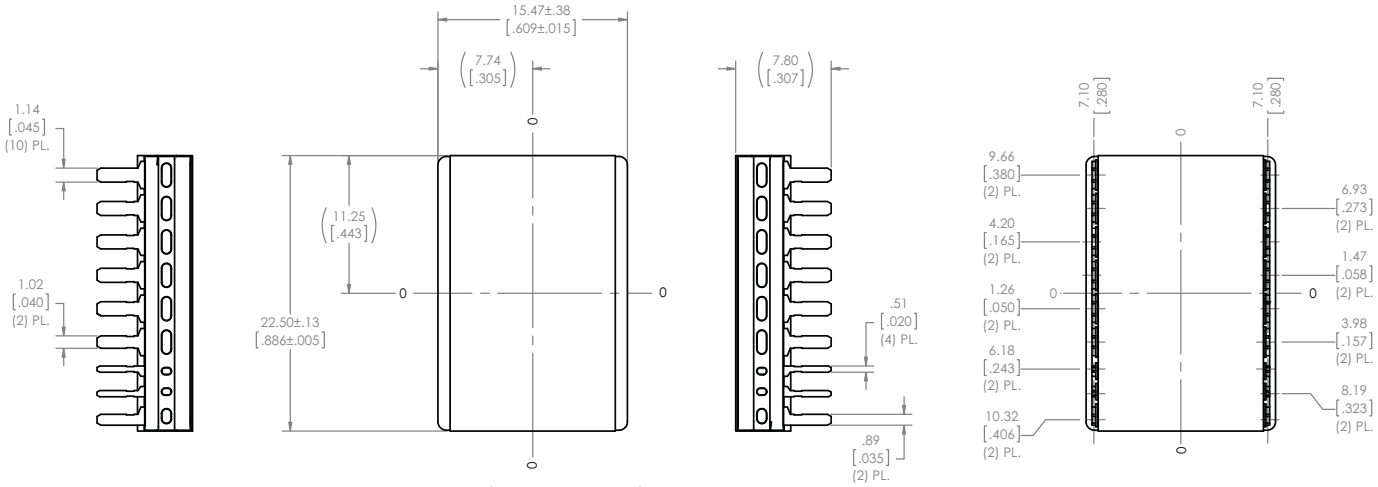
Figure 27 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$T_{INT} - PD_1 \bullet 3.5 = T_{CASE\_TOP}$

$PD_{TOTAL} = PD_1$

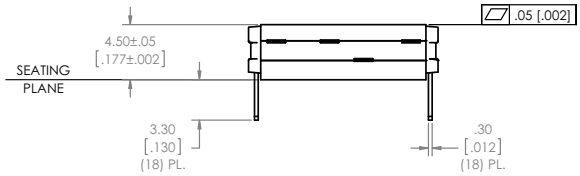
Please note that Vicor has a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a VTM thermal configuration is valid for a given condition. These tools can be found at: http://www.vicorpower.com/powerbench.

Product Outline Drawing and Recommended Land Pattern - Through Hole



TOP VIEW (COMPONENT SIDE)

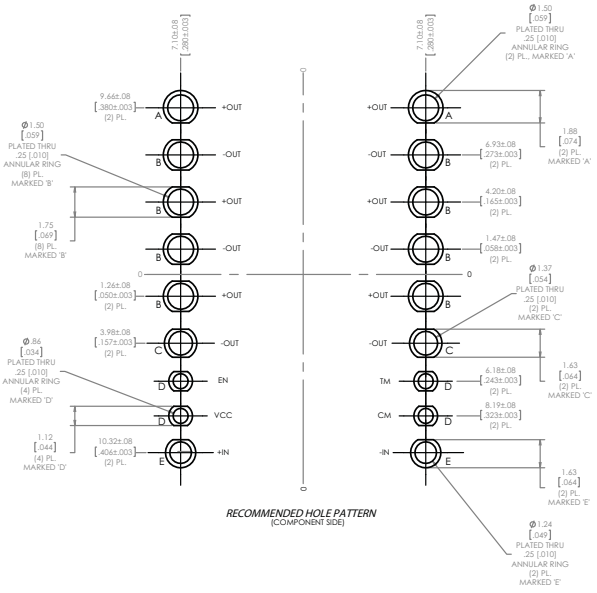
BOTTOM VIEW



NOTES:

1- RoHS COMPLIANT, LEAD FREE PER CST-0001 LATEST REVISION.

2- SEE SHEET 2 FOR RECOMMENDED HOLE PATTERN.



RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)

Revision History

Revision	Date	Description	Page Number(s)
1.0	04/14/14	Initial release	n/a
1.1	04/24/14	Updated Assembly and Soldering	13
1.2	08/29/14	Typical Application and Timing Diagram	2 & 9
1.3	10/24/14	Updated standard product model	1, 2, 3, 13, ~~23~~
1.4	02/03/15	Updated safe thermal & electrical operating area	6

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

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